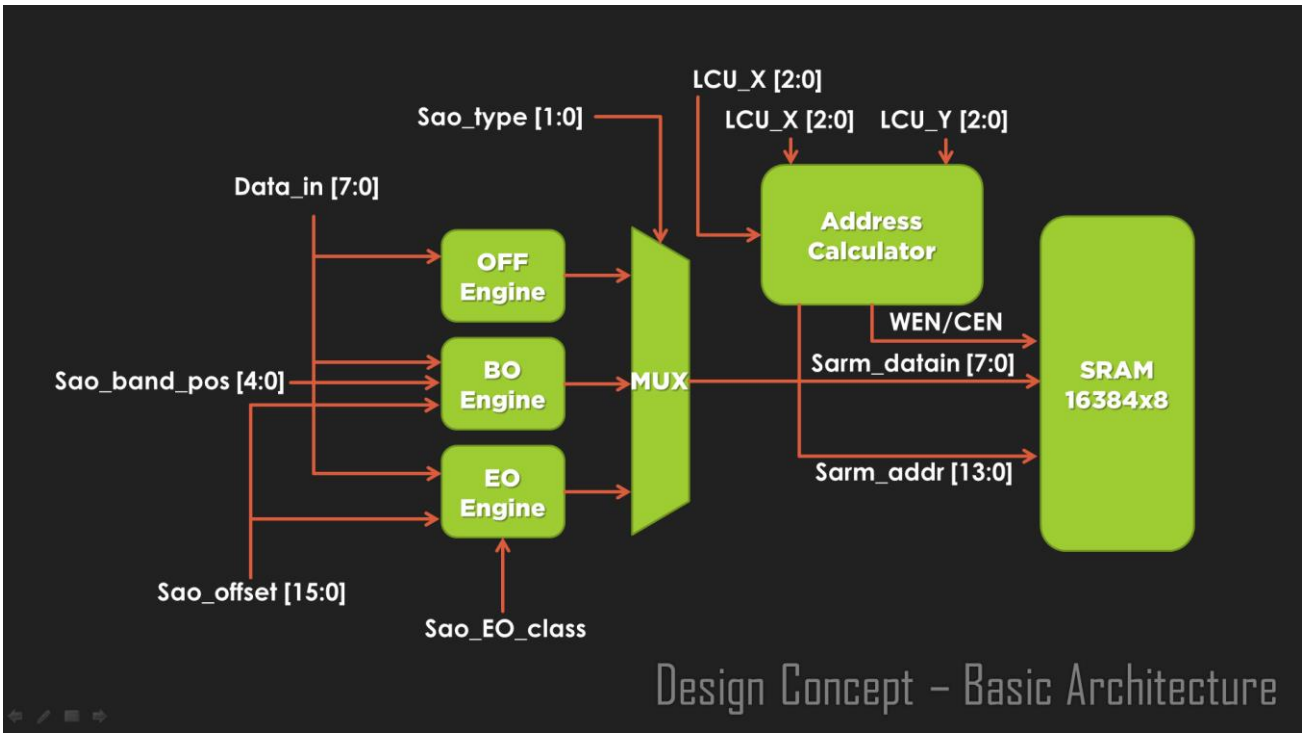
Project2: Sample Adaptive Offset Filter

14:05, January 11, 2017

Design Concepts

我的設計基本架構圖如下所示：



收到 Data in 之後便會放入 OFF/BO/EO Engine 各自做三種濾波處理，並且使用 sao type 做為 multiplexer 選出我要送入 sram 中的 data，在配合 address calculator 計算出該 data 的存放位址即可完成整個 SAO filter 的設計。

OFF Engine

對 OFF Engine 因為不做任何處理，因此直接輸出即可。

BO Engine

取送入的 data in 前五個 bit 做為判斷是否在 BO continuous band 的判斷，再去判斷是否要加上屬於該 continuous band 的 BO offset，處理後即可輸出，程式碼如下詳述。

```
assign din_shift = buffer_0[7:3];

assign BO_continuous_band_0 = (din_shift == sao_band_pos_next);
assign BO_continuous_band_1 = (din_shift == sao_band_pos_next+1);
assign BO_continuous_band_2 = (din_shift == sao_band_pos_next+2);
assign BO_continuous_band_3 = (din_shift == sao_band_pos_next+3);

assign bo_offset = BO_continuous_band_0 ? sao_offset_next[15:12] : 0 +
                   BO_continuous_band_1 ? sao_offset_next[11:8] : 0 +
                   BO_continuous_band_2 ? sao_offset_next[7:4] : 0 +
                   BO_continuous_band_3 ? sao_offset_next[3:0] : 0 ;
```

EO Engine

先設計 128 個連續的 flip-flops 去暫存每次輸入的 data，再由屬於 vertical/horizontal EO class 去計算出屬於哪個 EO category，判斷方式則由 EO class 判斷該取的 neighbor pixel，各自與 current pixel 相減後做 signed extension，取 MSB 判斷是否為負數，diff 判斷是否大於或等於 0，程式碼如下圖詳細所示：

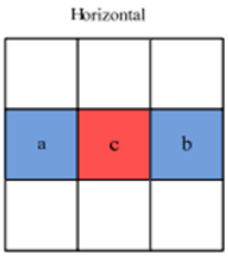
（以 horizontal EO 處理為例）

```
assign hor_diff1 = c - a;
assign hor_diff2 = c - b;

assign hor_category1 = hor_diff1[8] && hor_diff2[8];
assign hor_category2 = (hor_diff1[8] && (hor_diff2 == 0)) || (hor_diff2[8] && (hor_diff1 == 0));
assign hor_category3 = ((hor_diff1 > 0) && (hor_diff2 == 0)) || ((hor_diff2 > 0) && (hor_diff1 == 0));
assign hor_category4 = (hor_diff1 > 0) && (hor_diff2 > 0);
```

取 neighbor pixel 後做相減即可歸納出屬於何種 category，之後便計算完 EO offset 後輸出。

Table 1. Sample classification rules for edge offset.

Category	Condition
1	c<a && c<b
2	(c < a && c==b) ||(c==a&&c < b)
3	(c > a && c==b) ||(c==a&&c > b)
4	c > a && c > b
0	None of the above

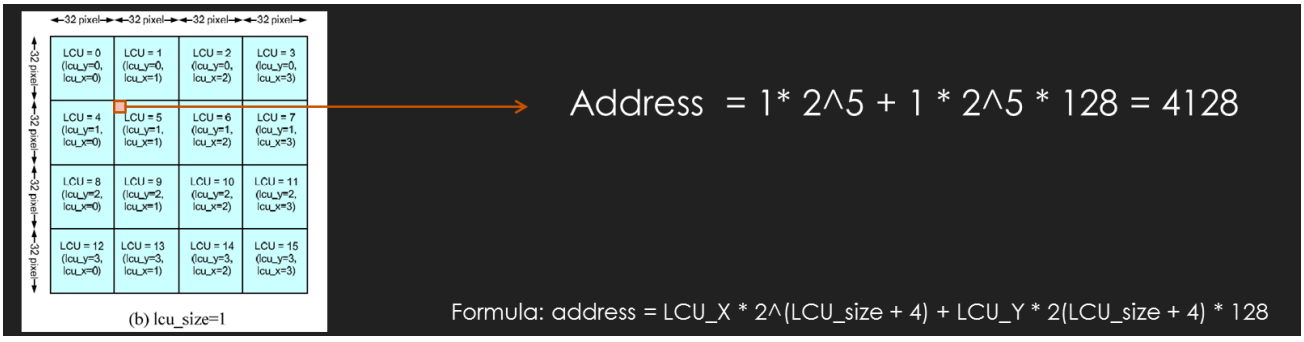


Address Calculator

開頭的判斷方式由以下公式即可求得：

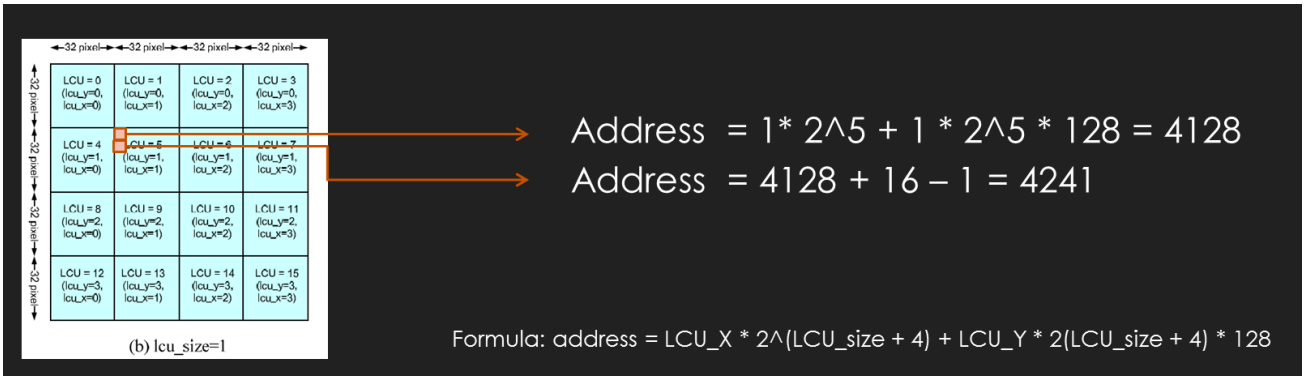
Formula: address = LCU_X * 2^(LCU_size + 4) + LCU_Y * 2(LCU_size + 4) * 128

舉例如下所示：



則可輕鬆求得 LCU=5 時的開頭位置要存放在 sram 的 4128 位置。

換行處理則只要加上 127 － LCU edge size 即可，如下圖所示：



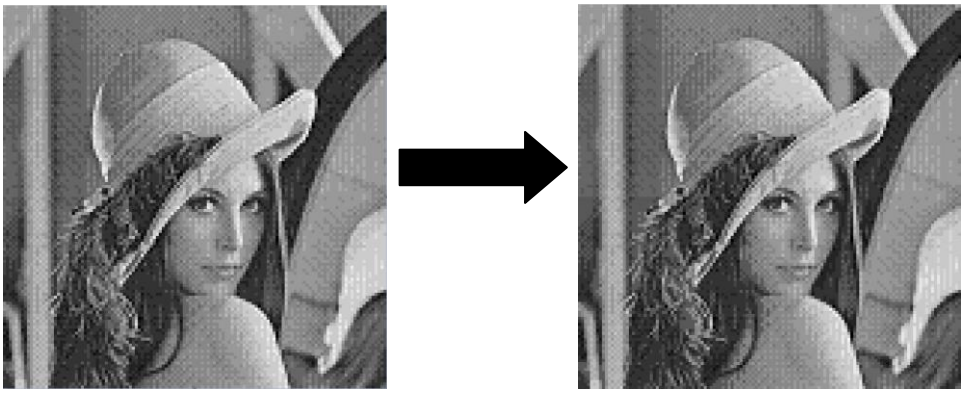
Result Display

我使用 python 的 pillow 函式庫進行影像的輸出，程式碼如下：

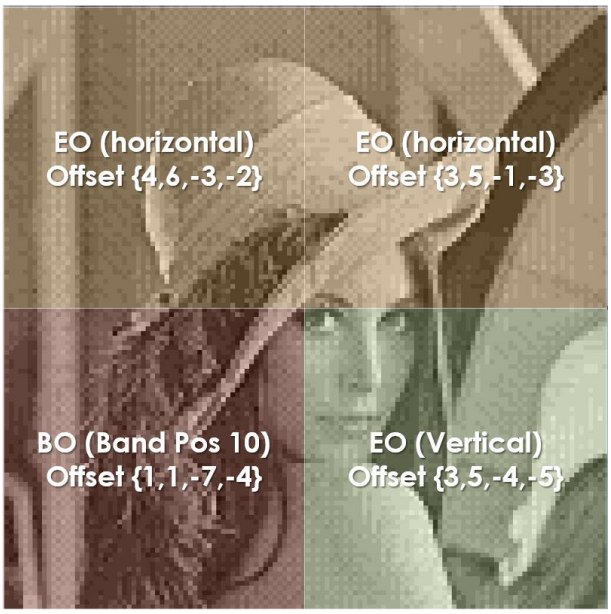
```
from PIL import Image
import sys

if len(sys.argv) < 4 :
    print 'Format'
    # print 'python image.py <input file> <output file>'
    print 'python image.py <width size> <height size> <input file> ...'
    sys.exit()

width = int(sys.argv[1])
height = int(sys.argv[2])
for everyfile in range(3,len(sys.argv)):
    input_file_name = sys.argv[everyfile]

    with open(input_file_name) as open_file:
        image_content = [int(line.strip()[:2],16) for line in open_file.readlines()]

    list_index = 0
    img = Image.new('RGBA', (width,height))
    for y in range(height):
        for x in range(width):
            rgba = (image_content[list_index], image_content[list_index] ,image_content[list_index] ,1)
            img.putpixel((x,y), rgba)
            list_index += 1

    img.show()
    img.save('output_'+input_file_name+'.png')
```

因為輸入要為 RGBA 值，因此我給定 A 值都為 1，然後因為是 pixel 為 Grayscale，因此把 pixel data 的值都都送入 R, G, B 中即可。

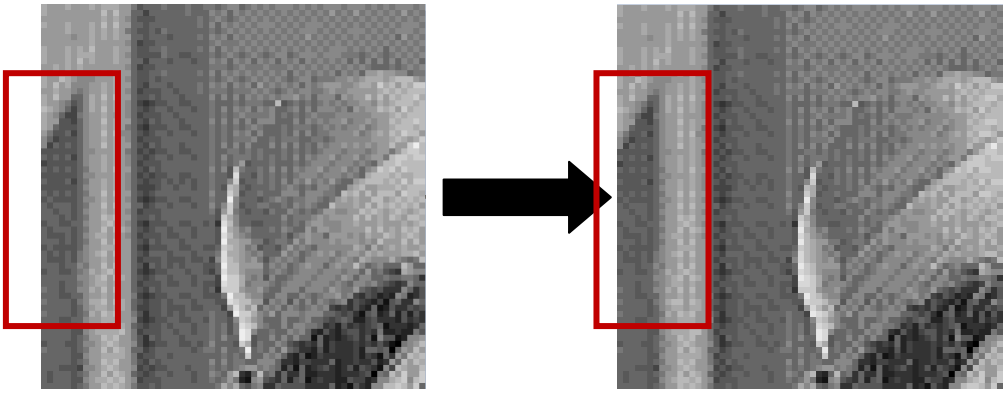
(左邊原始 pattern.dat 輸出的圖檔，右邊為使用 pattern3 經過 SAO 處理後的圖檔)



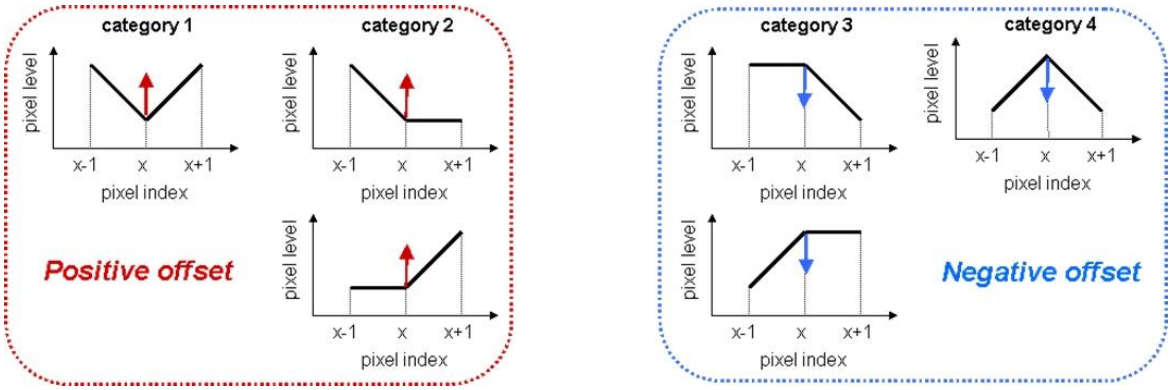
Pattern3 各 LCU block 做的處理及參數如下：



放大討論左上 LCU 細節處理如下：

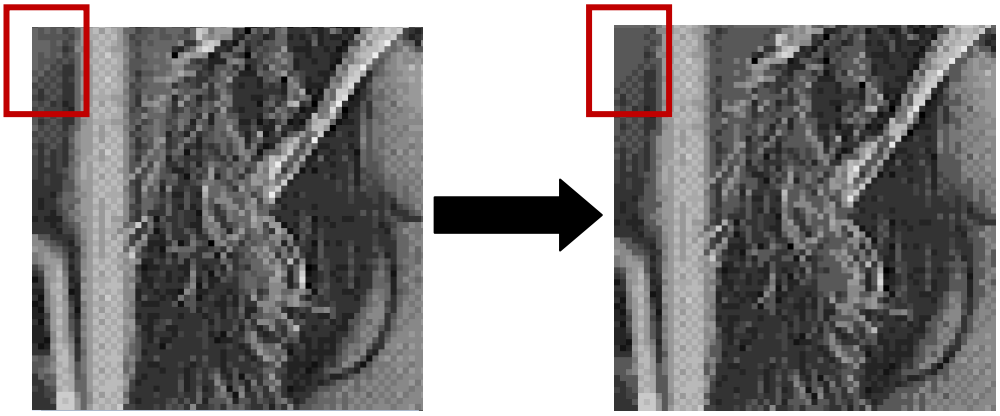


可以從上圖紅框處發現顏色有叫趨近平均，及 EO 處理後會使顏色趨近平滑，如下圖所示意：

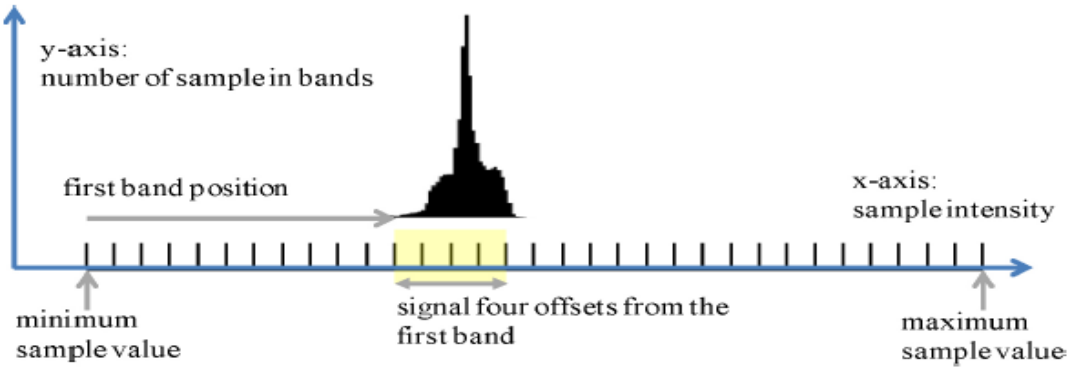


由 category 的處理便可知道，EO 處理都是協調顏色趨近同調，簡而言之極為使較黑區塊的 RGB 值往白色區塊移動，而較白區塊的 RGB 值往黑色區塊移動。

放大討論左上 LCU 細節處理如下：



BO 處理則是處理特定色帶，僅使該色帶顏色趨近同調，上圖紅框可以很清楚發現顏色被做了均勻的同調處理。



BO 處理即為根據所提供之 BO band position 作為起點，僅對一段色帶做同調處理，使該色帶顏色趨近於平滑，下圖點線為原本之 pixel level，BO 處理後的虛線可以看出 pixel level 波動較無原本點線來大的，在圖形畫面看來對比度也比較不會顯得差距大。

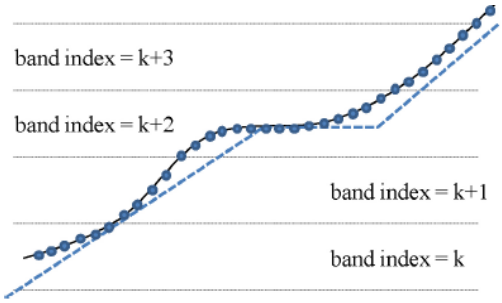
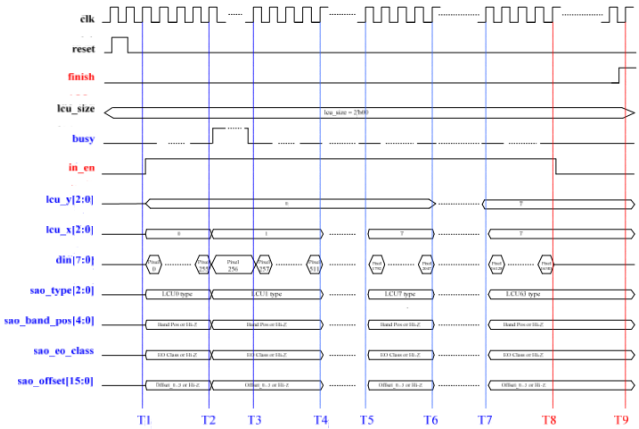


Fig. 6. Example of BO, where the dotted curve is the original samples and the solid curve is the reconstructed samples.

Stimulation

[iclab79@ic21]nWave

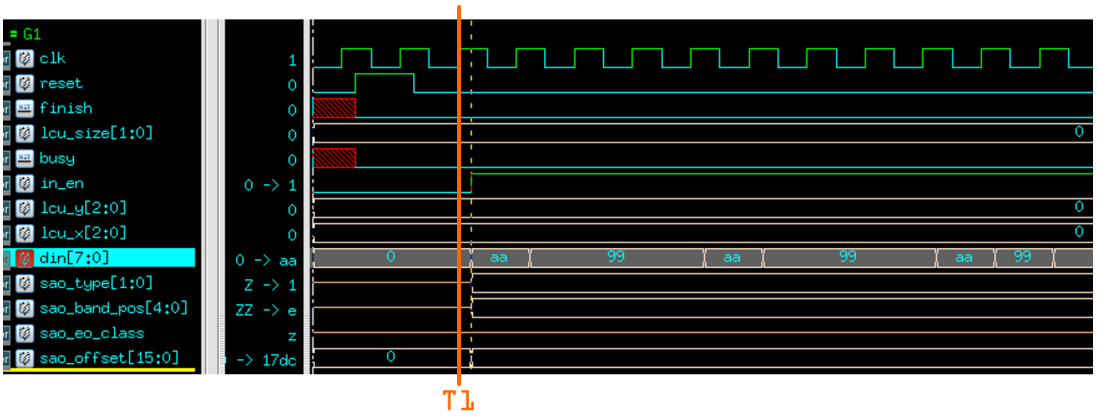
下圖為題目提供之 SAO 電路輸入之時序圖：



圖九、SAO 電路時序圖

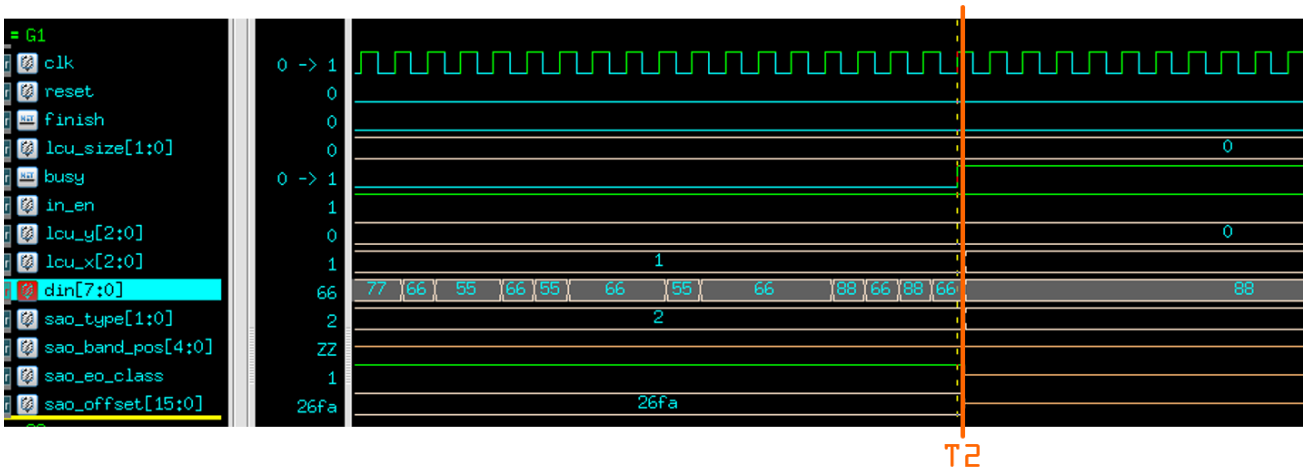
以下為使用 nWave 模擬後的實際電路時序圖：

1. T1 時間點，reset 一個 Cycle 的時間，SAO 電路初始化結束，Host 端在 T1 時間點判斷到 busy 訊號為 Low，因此開始輸入資料，in_en 拉為 High，din、lcu_y、lcu_x、din、sao_type、 sao_band_pos、sao_eo_class、sao_offset 一起送出第一筆資料，開始運算第一個

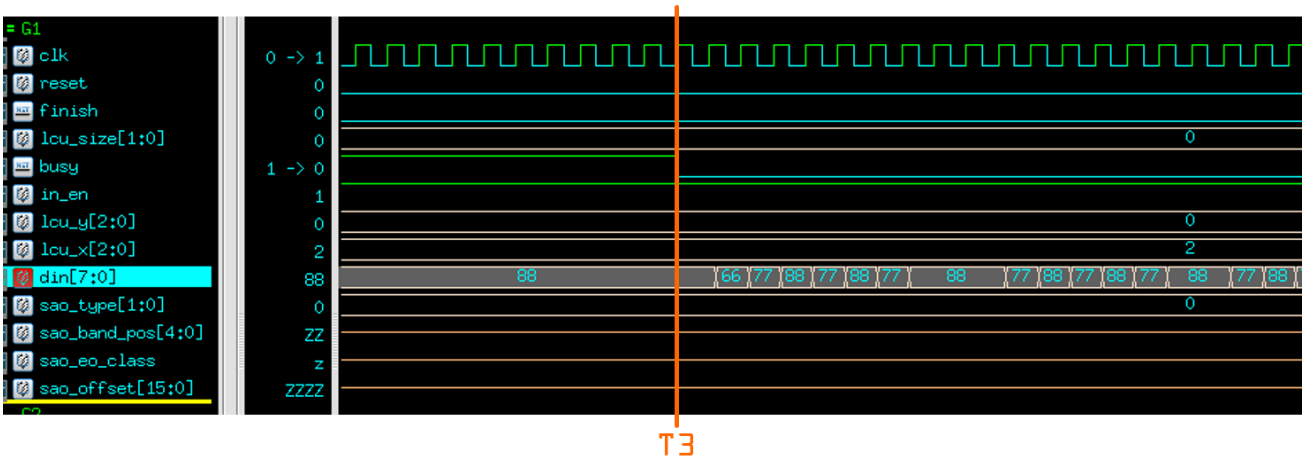


LCU 0。

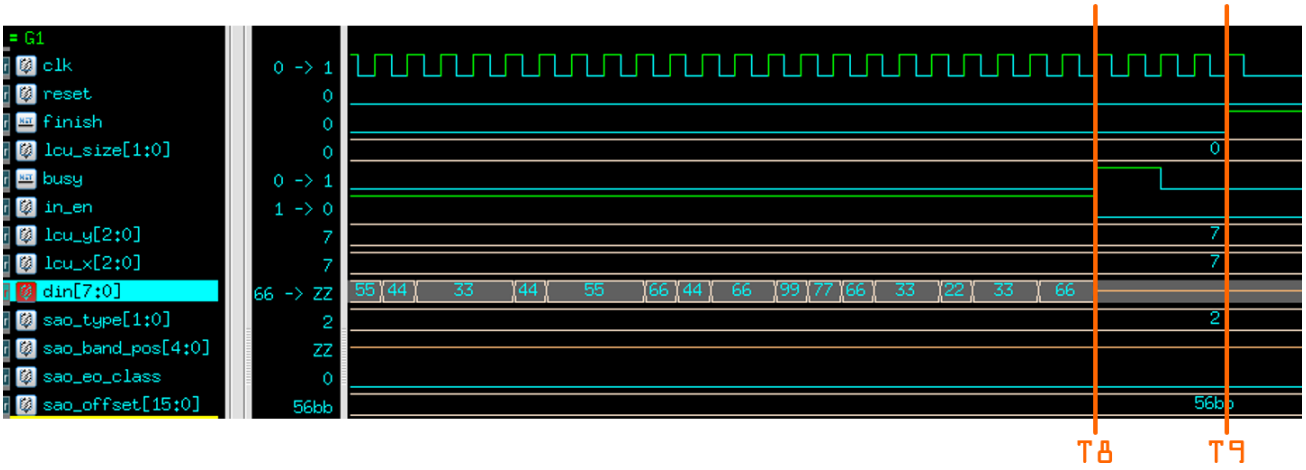
2. T2 時間點，計算過程中將 busy 訊號拉為 High，因此暫時維持 din 資料為 8'h66。



3. T3 時間點，clk 正緣發現 busy 是 Low，din 繼續輸入剩餘的影像訊號直到資料輸入完畢。



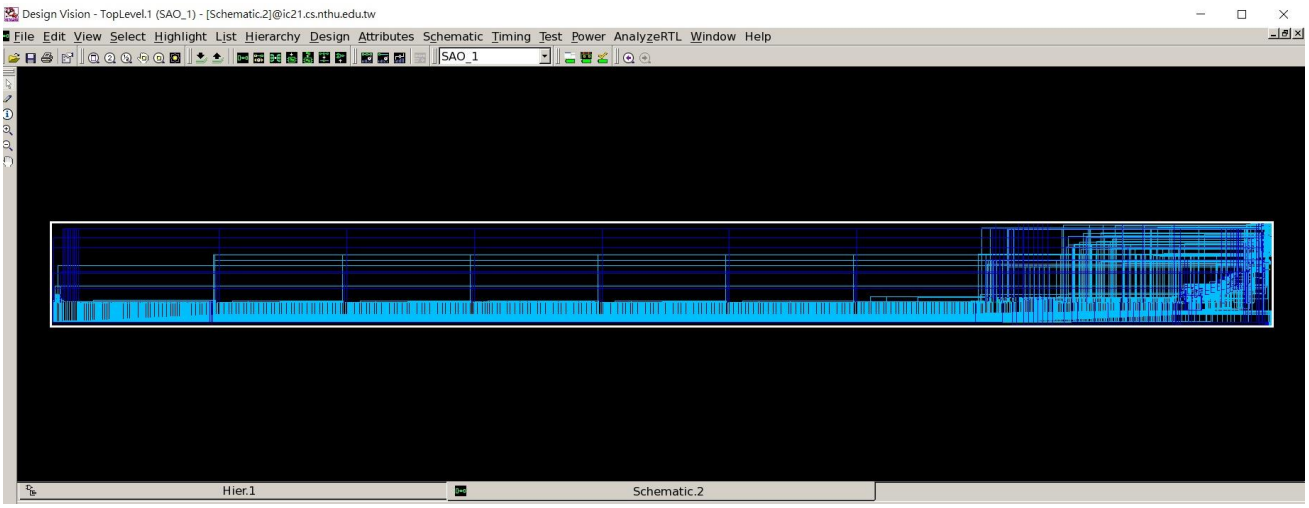
4. T8 時間點，資料全數輸入完成，in_en 拉為 Low，表示不再有新資料輸入，接下來到 SAO 運 算完 finish 之前，請趕緊把剩餘資料算完後，於 T9 時間點發出 finish 為 High 後，便告知 Host 端開始進行 SRAM 之資料比對，比對完後整個模擬立即結束。



Synthesization

[iclab79@ic21]design_vision

Schematic View



Report Area

```
Number of buf/inv:                      213
Number of references:                    55

Combinational area:              7752.025793
Buf/Inv area:                    1218.733181
Noncombinational area:          36504.283165
Macro/Black Box area:          438436.062500
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:               482692.371458
Total area:                 undefined
design_vision>
```

Log | History

design_vision>

Report Power

```
                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.6150           0.0000           9.8000e+07            0.7130  (  22.64%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register           2.3280        4.3188e-03          3.3602e+07            2.3659  (  75.12%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational  2.6016e-02        3.7533e-02          6.9936e+06         7.0543e-02  (   2.24%)
--------------------------------------------------------------------------------------------------
Total              2.9689 mW     4.1852e-02 mW     1.3860e+08 pW          3.1494 mW
design_vision>
```

Log | History

design_vision>

Report Timing Paths

```
  clock CLK (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  sram_din_reg[0]/CK (DFFRX1)              0.00      10.00 r
  library setup time                      -0.22       9.78
  data required time                                  9.78
  ----------------------------------------------------------
  data required time                                  9.78
  data arrival time                                  -8.61
  ----------------------------------------------------------
  slack (MET)                                         1.16


design_vision>
```

Log | History

design_vision>

APR Layout Flow

[[iclab79@ic21]cd ./SOCE/run
[iclab79@ic21]encounter

先進到 run 資料夾後輸入 encounter 開始進行 APR

encounter 1>setDesignMode -process 130 -addPhysicalCell hier -flowEffort none

設定設計模式參數

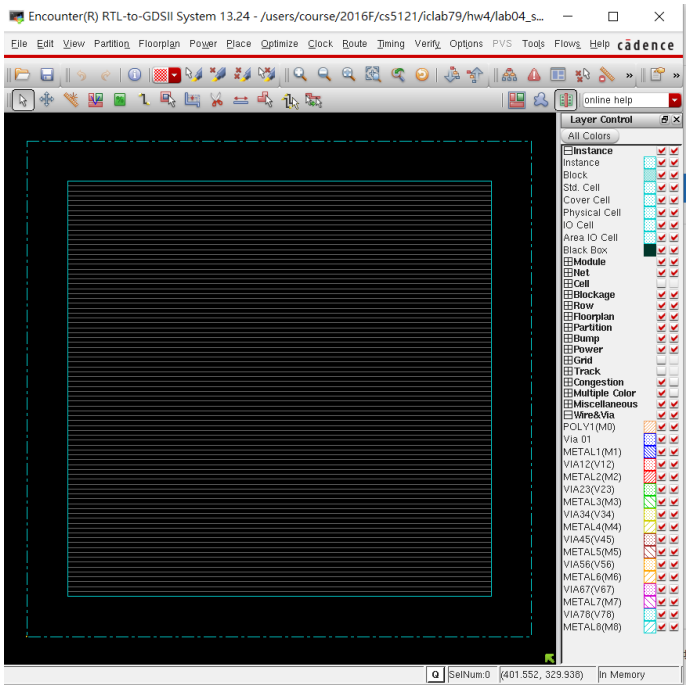
```
encounter 1> setDesignMode -process 130 -addPhysicalCell hier -flowEffort none
Applying the recommended capacitance filtering threshold values for 130nm process node: total_c_th=0, relative_c_th=1 and coupli
ng_c_th=0.4.
        These values will be used by all post-route extraction engines, including TQRC, IQRC and QRC extraction.
        Capacitance filtering mode(-capFilterMode option of the setExtractRCMode) is 'relAndCoup' for all engines.
        The accuracy mode for postRoute effortLevel low extraction will be set to 'standard'.
        Default value for EffortLevel(-effortLevel option of the setExtractRCMode) in postRoute extraction mode is 'low'.
```

File→Import Design

Power→Connect Global Nets

Floorplan→Specify Floorplan

設定好 Floorplan 參數後可以看到以下畫面，完成 Floorplan

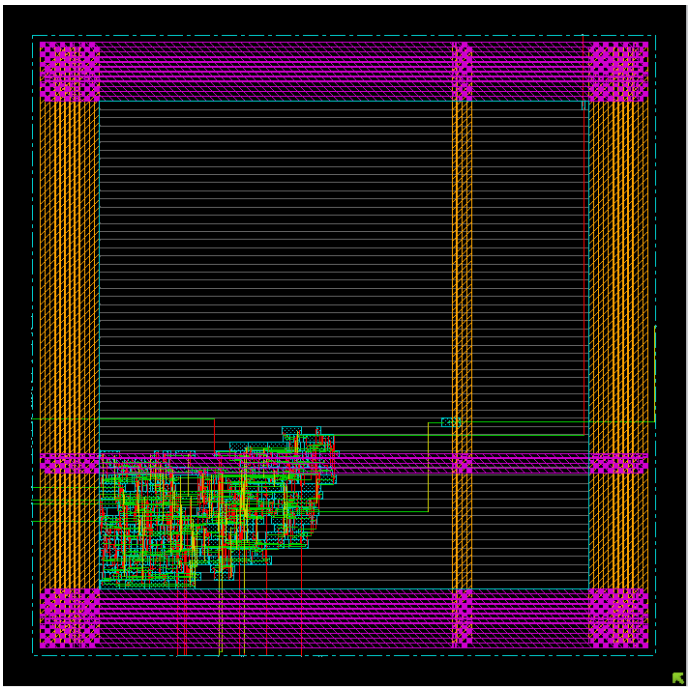


Power→Power planning→Add Rings & Add Stripes

Place→Place Standard Cell

Route→Trial Route

設定好 Placement 參數後可以看到以下畫面，完成 Placement&Route



Timing→Extract RC

Timing→Report Timing

Optimize→Optimize Design

OptDesign 報告如下，完成 Pre-CTS

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.614  |  5.657  |  5.614  |  7.634  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      1 (1)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 8.880%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
**optDesign ... cpu = 0:00:11, real = 0:00:10, mem = 780.9M, totSessionCpu=0:01:02 **
*** Finished optDesign ***
```

Place→Tie HI/LO→Add

Clock→Synthesize Clock Tree

Clock tree加入後的time report如下

```
                                (Actual)              (Required)
Rise Phase Delay              : 125.3~127.9(ps)       0~10(ps)
Fall Phase Delay              : 124.1~126.7(ps)       0~10(ps)
Trig. Edge Skew               : 2.6(ps)               100(ps)
Rise Skew                     : 2.6(ps)
Fall Skew                     : 2.6(ps)
Max. Rise Buffer Tran.        : 62.4(ps)              250(ps)
Max. Fall Buffer Tran.        : 61.9(ps)              250(ps)
Max. Rise Sink Tran.          : 52.4(ps)              250(ps)
Max. Fall Sink Tran.          : 59.8(ps)              250(ps)
Min. Rise Buffer Tran.        : 62.4(ps)              0(ps)
Min. Fall Buffer Tran.        : 61.9(ps)              0(ps)
Min. Rise Sink Tran.          : 52.2(ps)              0(ps)
Min. Fall Sink Tran.          : 59.7(ps)              0(ps)

view slow : skew = 2.6ps (required = 100ps)
view fast : skew = 3.1ps (required = 100ps)


Generating Clock Analysis Report clock_report/clock.postCTS.report ....
Clock Analysis (CPU Time 0:00:00.0)


All-RC-Corners-Per-Net-In-Memory is turned OFF...
*** End ckECO (cpu=0:00:00.2, real=0:00:00.0, mem=777.2M) ***
**clockDesign_... cpu = 0:00:04, real = 0:00:04, mem = 777.2M **
```

Route→Trial Route

Timing→Extract RC

Timing→Report Timing

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.288  |  5.656  |  5.288  |  7.948  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |              Real                 |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  |  Worst Vio     |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |   0.000        |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000        |      0 (0)       |
|   max_fanout   |      0 (0)       |     0          |      0 (0)       |
|   max_length   |      0 (0)       |     0          |      0 (0)       |
+----------------+------------------+----------------+------------------+

Density: 8.973%
Total number of glitch violations: 0
------------------------------------------------------------
```

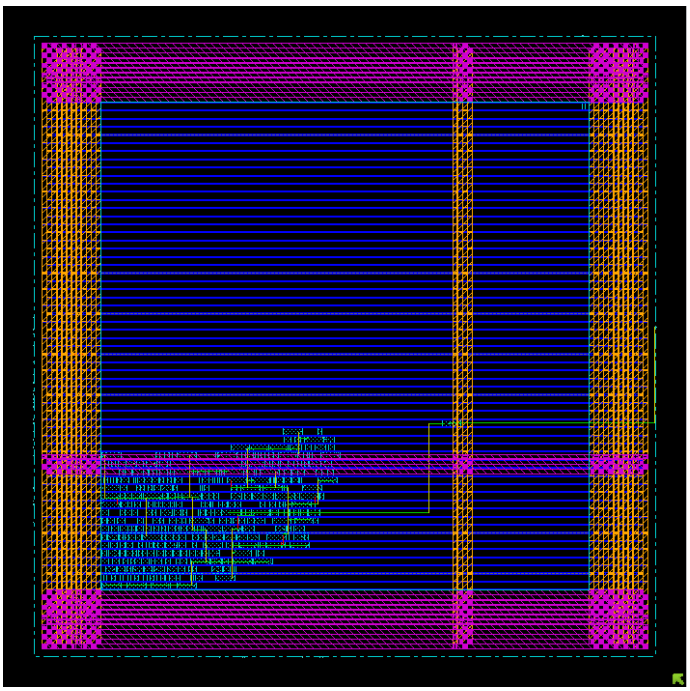
Optimize→Optimize Design

OptDesign 報告如下，完成 Post-CTS

```
------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.288  |  5.656  |  5.288  |  7.948  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.091  |  0.091  |  1.329  |  1.036  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+
```

```
+----------------+-----------------------------------+------------------+
|                |              Real                 |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  |  Worst Vio     |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |   0.000        |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000        |      0 (0)       |
|   max_fanout   |      0 (0)       |     0          |      0 (0)       |
|   max_length   |      0 (0)       |     0          |      0 (0)       |
+----------------+------------------+----------------+------------------+

Density: 8.973%
Total number of glitch violations: 0
------------------------------------------------------------
```

Route→Special Route



Route→NanoRoute→Route

Option→Set Mode→Specify RC Extraction Mode

Option→Set Mode→Specify Analysis Mode

Timing→Extract RC

Timing→Report Timing

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.288  |  5.656  |  5.288  |  7.948  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |              Real                 |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  |  Worst Vio     |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |   0.000        |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000        |      0 (0)       |
|   max_fanout   |      0 (0)       |     0          |      0 (0)       |
|   max_length   |      0 (0)       |     0          |      0 (0)       |
+----------------+------------------+----------------+------------------+

Density: 8.973%
Total number of glitch violations: 0
------------------------------------------------------------
```

Verify→Verify Connectivity

Verify→Verify Geometry→check

```
encounter 2>  *** Starting Verify Geometry (MEM: 837.6) ***

  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 8320
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.3  MEM: 15.6M)
```

encounter > analyzeFloorplan

```
encounter 2> analyzeFloorplan
Start to collect the design information.
Build netlist information for Cell SAO_1.
Finished collecting the design information.
Average module density = 0.952.
Density for the design = 0.952.
       = stdcell_area 27523 sites (46718 um^2) / alloc_area 28920 sites (49089 um^2).
Pin Density = 0.049.
            = total # of pins 1335 / total Instance area 27523.
************************** Analyze Floorplan **************************
    Die Area(um^2)             : 79581.69
    Core Area(um^2)            : 49174.05
    Chip Density (Counting Std Cells and MACROs and IOs): 58.704%
    Core Density (Counting Std Cells and MACROs): 95.004%
    Average utilization        : 95.169%
    Number of instance(s)      : 1121
    Number of Macro(s)         : 0
    Number of IO Pin(s)        : 45
    Number of Power Domain(s) : 0
************************** Estimation Results **************************
************************************************************************
```

Post-Synthesize Stimulation

RTL 模擬時的 Unix 指令

[iclab79@ic21]ncverilog +nospecify +notimingchecks SAO.v sram_1024x8_t13.v +access+r

Gate-Level Post-layout 模擬時的 Unix 指令

[iclab79@ic21]ncverilog testfixture1.v SAO_syn.v sram_1024x8_t13.v -v /theda2 \ 1_2/CBDK_IC_\Contest/cur/Verilog/tsmc13.v +define+SDF +access+r

執行完結果如下:

```
SRAM Address:16252 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=14, x=12): 33 == expect 33
SRAM Address:16253 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=14, x=13): 39 == expect 39
SRAM Address:16254 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=14, x=14): 44 == expect 44
SRAM Address:16255 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=14, x=15): 55 == expect 55
SRAM Address:16368 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 0): 55 == expect 55
SRAM Address:16369 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 1): 5b == expect 5b
SRAM Address:16370 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 2): 61 == expect 61
SRAM Address:16371 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 3): 49 == expect 49
SRAM Address:16372 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 4): 61 == expect 61
SRAM Address:16373 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 5): 6c == expect 6c
SRAM Address:16374 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 6): 94 == expect 94
SRAM Address:16375 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 7): 77 == expect 77
SRAM Address:16376 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 8): 66 == expect 66
SRAM Address:16377 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 9): 39 == expect 39
SRAM Address:16378 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=10): 2e == expect 2e
SRAM Address:16379 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=11): 27 == expect 27
SRAM Address:16380 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=12): 2e == expect 2e
SRAM Address:16381 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=13): 39 == expect 39
SRAM Address:16382 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=14): 61 == expect 61
SRAM Address:16383 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=15): 66 == expect 66
--------------------------------------------------

Congratulations! All data have been generated successfully!

-------------------------PASS-------------------------

Simulation complete via $finish(1) at time 71291100 PS + 0
```

Project Review

這次的 LAB 由於當初在操作 APR tutorial 僅按照 Flow 設定參數，因此在自己進行 APR flow 的設定時便遇到了很多問題，像是 MMMC 的 sram timing library 的引入，以及 sram 的 physical core library(.lef)的引入，因此導致做完 pre-layout 可以順利的模擬，但在 post-layout 的模擬便會產生如下圖一樣的 time violation 結果:

```
Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):74850 PS, posedge D:74150 PS,  1.000
 : 1 NS,  0.500 : 500 PS );
           File: ../apr_source/tsmc13.v, line = 18276
          Scope: test.SA0.\busy_cnt_reg[4]
           Time: 74850 PS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):79550 PS, posedge D:78850 PS,  1.000
 : 1 NS,  0.500 : 500 PS );
           File: ../apr_source/tsmc13.v, line = 18276
          Scope: test.SA0.\busy_cnt_reg[5]
           Time: 79550 PS
```

此外還有使用一維暫存器陣列是沒有辦法在 nWave 中顯示訊號的，因此最後用了十分原始的方法，也就是展開一維暫存器陣列成 128 個連接的 flip-flops 來進行 debug。

終於完成了最後一個作業了！希望真的能經過這學期大量的 lab assignment 而有所成長，最後恭喜吳助教可以擺脫我的疲勞轟炸式問問題了，有時候其實都會問的很不好意思，但因為沒有實際操作過，根據教授講義上的流程又少了點什麼，很多時候都變成問助教在講義的哪裡，說起來還真的十分抱歉! 最後就獻上在 demo 投影片中的對助教的致謝結束這門課的 report 吧!

Special Thanks

T.A. Wu

- The help to deal with tons of problems ,which I encountered on either lab assignment or design concept.