# Lab 4: APR Practice
# (Automatic Placement and Routing)

### 23:59, December 14, 2016

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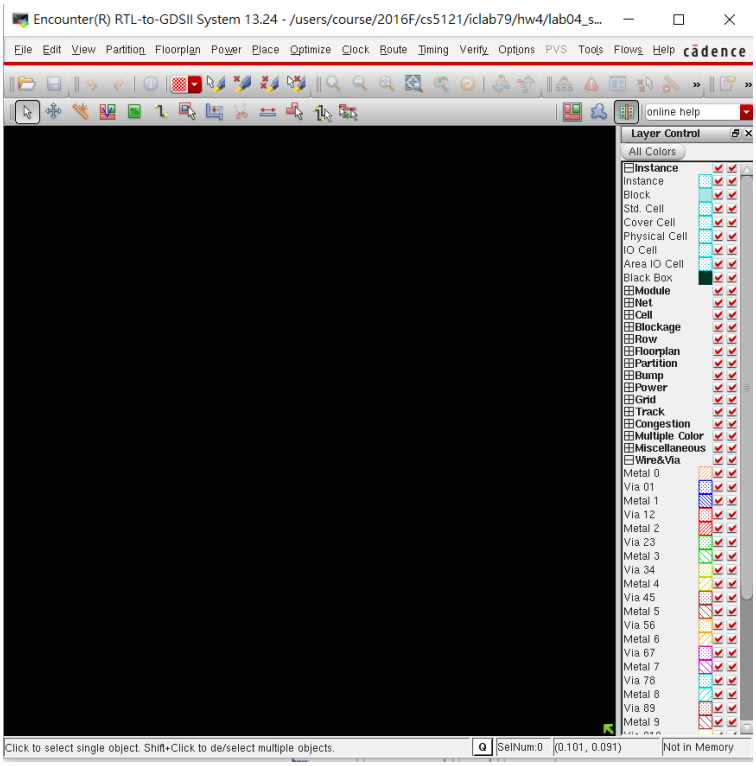
## Lab Concepts

使用 Cadence 的 SOC tool Encounter 來進行 Block Level APR 操作，藉以熟悉 APR 流程並且觀察各個階段完成後的報告差異。

## APR Flow

**[iclab79@ic21]cd ./SOCE/run**
**[iclab79@ic21]encounter**

根據 toturial 指示進入 Cadence Encounter




**encounter 1>setDesignMode -process 130 -addPhysicalCell hier -flowEffort none**

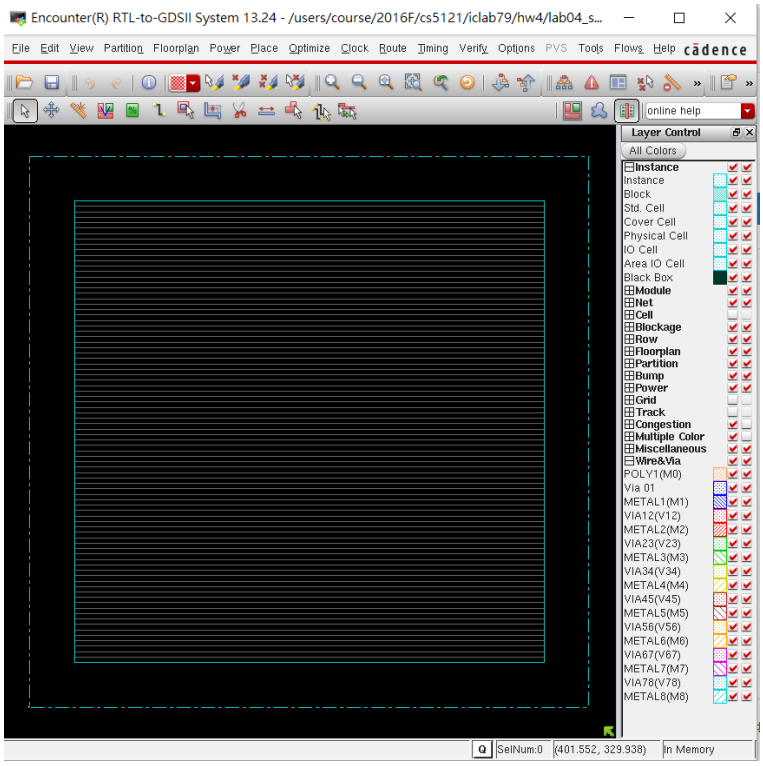
```
encounter 1> setDesignMode -process 130 -addPhysicalCell hier -flowEffort none
Applying the recommended capacitance filtering threshold values for 130nm process node: total_c_th=0, relative_c_th=1 and coupli
ng_c_th=0.4.
        These values will be used by all post-route extraction engines, including TQRC, IQRC and QRC extraction.
        Capacitance filtering mode(-capFilterMode option of the setExtractRCMode) is 'relAndCoup' for all engines.
        The accuracy mode for postRoute effortLevel low extraction will be set to 'standard'.
        Default value for EffortLevel(-effortLevel option of the setExtractRCMode) in postRoute extraction mode is 'low'.
```

**File→Import Design**

**Power→Connect Global Nets**

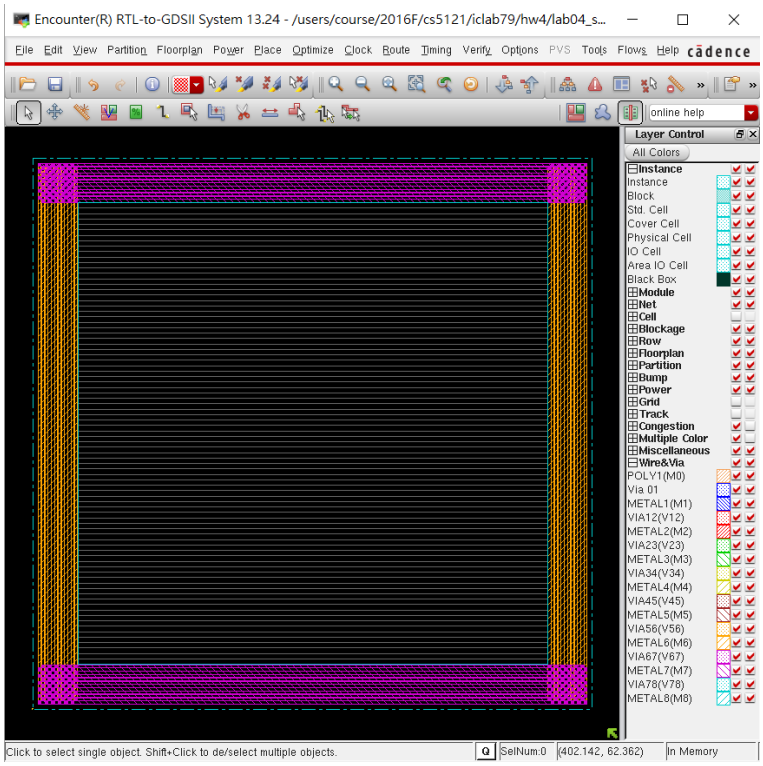
**Floorplan→Specify Floorplan**

設定好 Floorplan 參數後可以看到以下畫面，完成 Floorplan



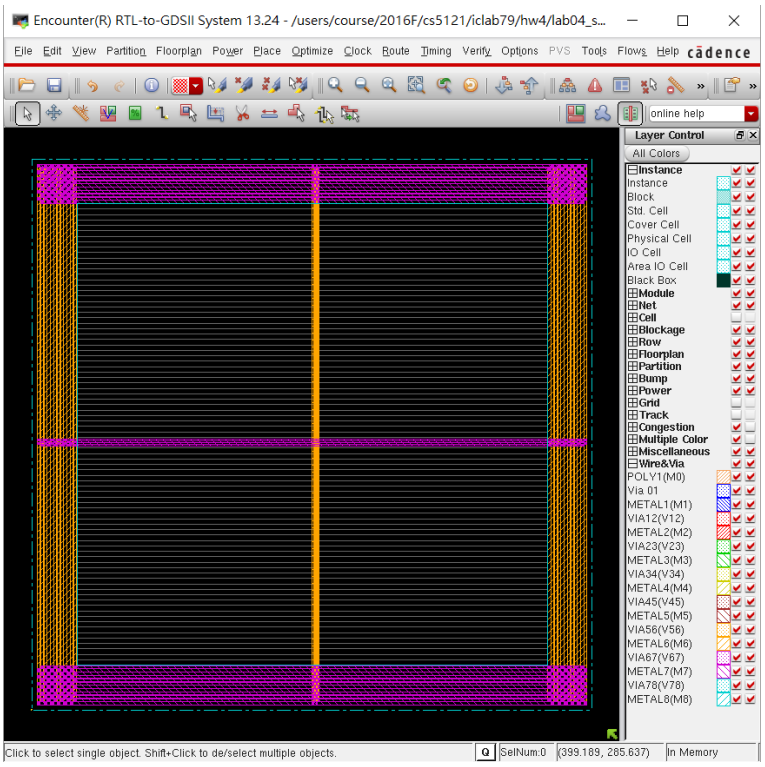

**Power→Power planning→Add Rings**

設定好 Powerplan 的 Rings 參數後可以看到以下畫面



**Power→Power planning→Add Stripes**

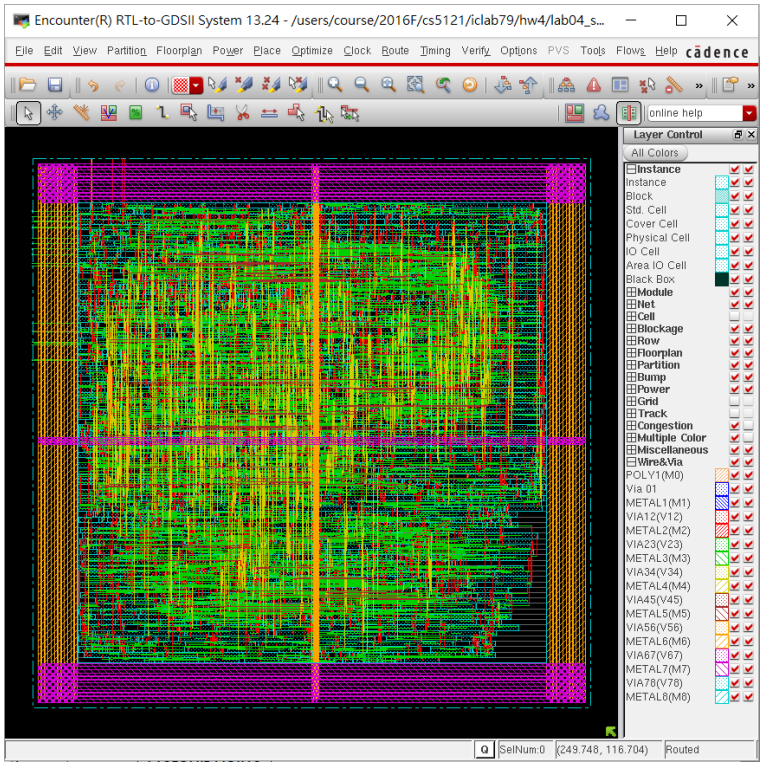
設定好 Powerplan 的 Stripes 參數後可以看到以下畫面，完成 Powerplan




**Place→Place Standard Cell**

**Route→Trial Route**

設定好 Placement 參數後可以看到以下畫面，完成 Placement&Route



**Timing→Extract RC**

**Timing→Report Timing**

**Optimize→Optimize Design**

OptDesign 報告如下，完成 Pre-CTS

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.104  |  0.104  |  2.830  |  3.254  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   827   |   394   |   426   |    9    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |     74 (74)      |    -54     |     75 (75)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 71.162%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

**encounter 2> setTieHiLoMode -maxFanout 10 -maxDistance 40**

**Place→Tie HI/LO→Add**

**Clock→Synthesize Clock Tree**

Clock tree加入後的time report如下

```
                                (Actual)              (Required)
Rise Phase Delay              : 236~253.4(ps)         0~10(ps)
Fall Phase Delay              : 240.8~258.2(ps)       0~10(ps)
Trig. Edge Skew               : 17.4(ps)              100(ps)
Rise Skew                     : 17.4(ps)
Fall Skew                     : 17.4(ps)
Max. Rise Buffer Tran.        : 103.6(ps)             200(ps)
Max. Fall Buffer Tran.        : 104.4(ps)             200(ps)
Max. Rise Sink Tran.          : 166.4(ps)             200(ps)
Max. Fall Sink Tran.          : 194(ps)               200(ps)
Min. Rise Buffer Tran.        : 103.5(ps)             0(ps)
Min. Fall Buffer Tran.        : 104.3(ps)             0(ps)
Min. Rise Sink Tran.          : 163.9(ps)             0(ps)
Min. Fall Sink Tran.          : 191.7(ps)             0(ps)

view slow : skew = 17.4ps (required = 100ps)
view fast : skew = 20.3ps (required = 100ps)
```

**Route→Trial Route**

**Timing→Extract RC**

**Timing→Report Timing**

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.098  |  0.098  |  2.658  |  3.405  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   827   |   394   |   426   |    9    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |     74 (74)      |    -54     |     76 (76)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 71.259%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

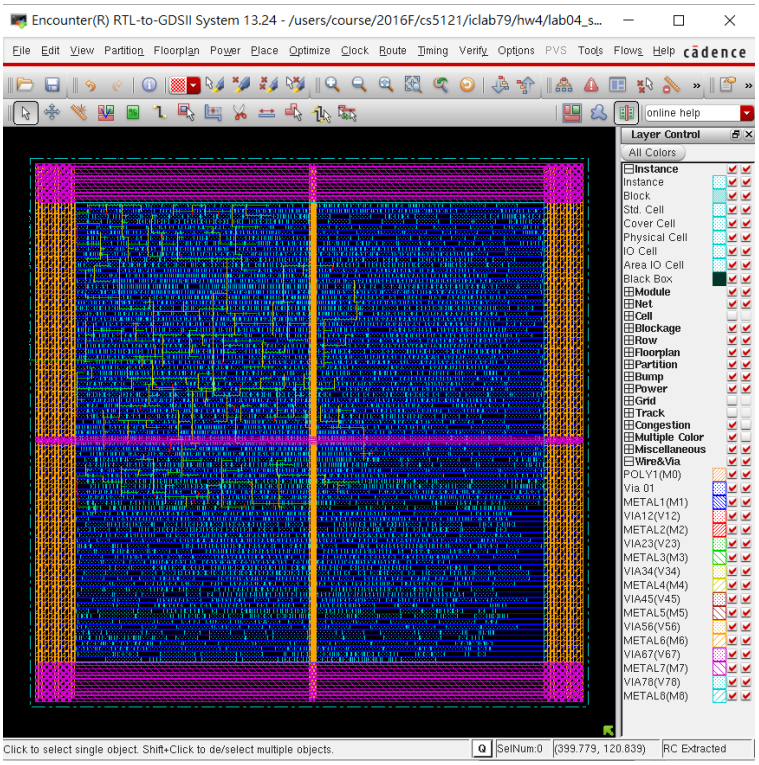
**Optimize→Optimize Design**

OptDesign 報告如下，完成 Post-CTS

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.131  |  0.131  |  1.065  |  3.408  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   827   |   394   |   426   |    9    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.060  |  0.060  |  1.164  |  0.868  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   827   |   394   |   426   |    9    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+
```

```
+----------------+---------------------------------+------------------+
|                |              Real               |       Total      |
|    DRVs        +------------------+--------------+------------------|
|                |  Nr nets(terms)  | Worst Vio    |  Nr nets(terms)  |
+----------------+------------------+--------------+------------------+
|   max_cap      |      0 (0)       |   0.000      |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000      |      0 (0)       |
|   max_fanout   |      7 (7)       |     -13      |      9 (9)       |
|   max_length   |      0 (0)       |      0       |      0 (0)       |
+----------------+------------------+--------------+------------------+

Density: 72.025%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

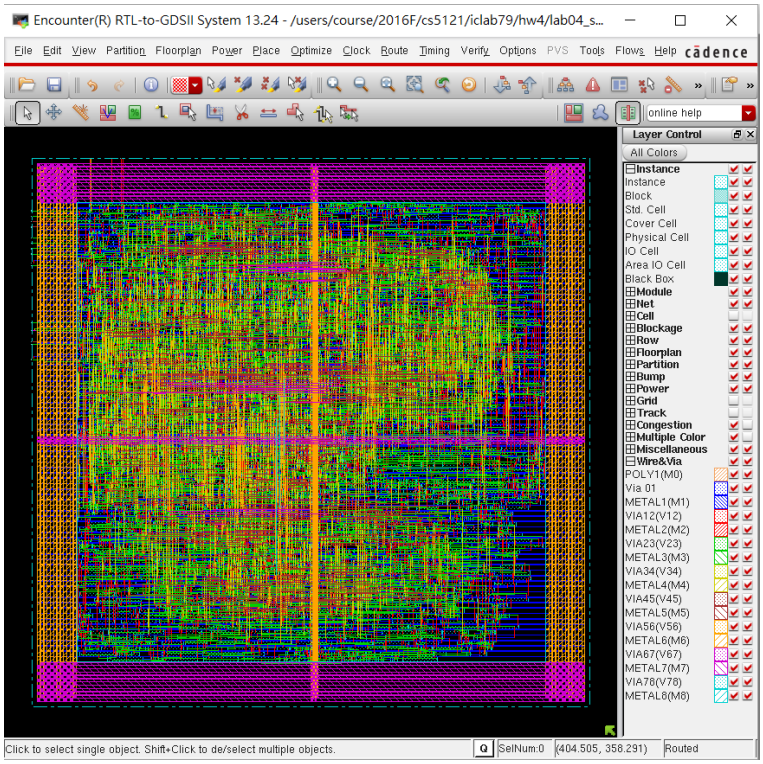
**Route→Special Route**




**Route→NanoRoute→Route**

**Route 後的 warning 如下圖所示**

```
#globalDetailRoute statistics:
#Cpu time = 00:01:00
#Elapsed time = 00:01:00
#Increased memory = 7.39 (MB)
#Total memory = 742.82 (MB)
#Peak memory = 821.16 (MB)
#Number of warnings = 7
#Total number of warnings = 53
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Wed Dec 14 01:40:28 2016
```




**Option→Set Mode→Specify RC Extraction Mode**

**Option→Set Mode→Specify Analysis Mode**

**Timing→Extract RC**

**Timing→Report Timing**

Post Routing 後報告如下

```
+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.105  |  0.105  |  1.152  |  3.386  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   827   |   394   |   426   |    9    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |              Real                 |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  |  Worst Vio     |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |    0.000       |      0 (0)       |
|   max_tran     |      0 (0)       |    0.000       |      0 (0)       |
|   max_fanout   |      7 (7)       |      -13       |      9 (9)       |
|   max_length   |      0 (0)       |        0       |      0 (0)       |
+----------------+------------------+----------------+------------------+

Density: 72.025%
Total number of glitch violations: 0
----------------------------------------------------------
```

**Optimize→Optimize Design**

Post-Routing 優化後的報告如下，完成 Post-Route

```
------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.105  |  0.105  |  1.152  |  3.386  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   827   |   394   |   426   |    9    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.059  |  0.059  |  1.156  |  0.874  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   827   |   394   |   426   |    9    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout   |      7 (7)       |    -13      |      9 (9)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 72.025%
Total number of glitch violations: 0
------------------------------------------------------------
```

**Verify→Verify Connectivity**

```
Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Dec 14 01:49:51 2016
Time Elapsed: 0:00:01.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:01.1  MEM: 3.012M)
```

**Verify→Verify Geometry→check**

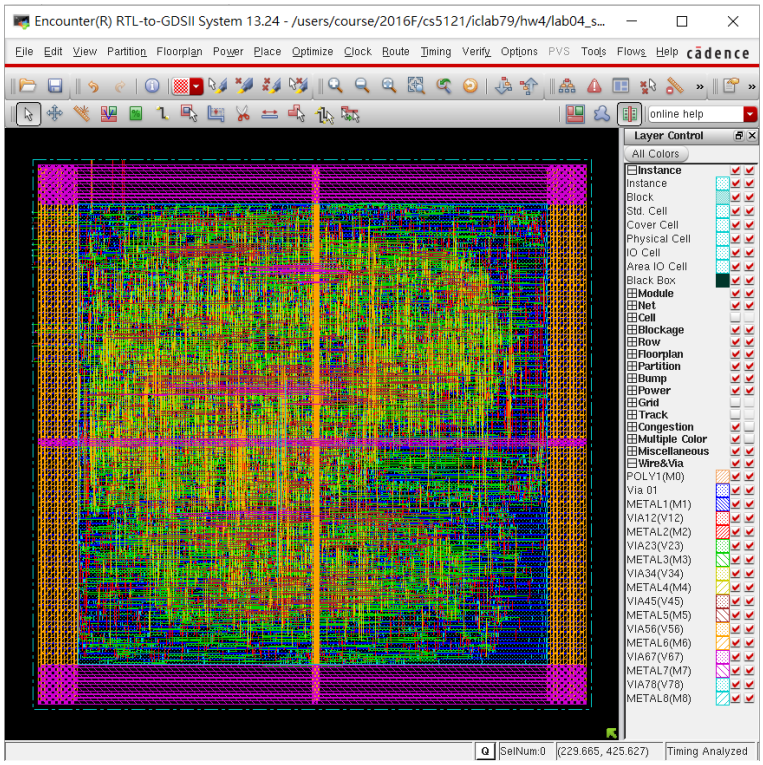
```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:01.1  MEM: 3.012M)

encounter 3>  *** Starting Verify Geometry (MEM: 952.7) ***

  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 8320
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 7.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
```

**Verify→Verify Process Antenna**

```
******* START VERIFY ANTENNA ********
Report File: TOP.antenna.rpt
LEF Macro File: TOP.antenna.lef
5000 nets processed: 0 violations
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time: 0:00:00.8  MEM: 0.812M)
```

**Tools→Violation Browser**

**Place→Physical Cell→Add Filler**




**File→Save→Netlist**

**Timing→Write SDF**

**File→Save→GDS/OASIS**

完成設計並分別儲存好 Post-Route 的設計檔，Post-Route Timing 的 sdf 檔以及 gds 檔

**Post-layout simulation**

把 Post-Route 完成後的.v 檔、.sdf 檔及.gds 檔放到 apr_source 檔，即可順利完成模擬

```
Pattern           0, correct.
Pattern           1, correct.
Pattern           2, correct.
Pattern           3, correct.
Pattern           4, correct.
Pattern           5, correct.
Pattern           6, correct.
Pattern           7, correct.
Pattern           8, correct.
Pattern           9, correct.
Pattern          10, correct.
Pattern          11, correct.
Pattern          12, correct.
Pattern          13, correct.
Pattern          14, correct.
Pattern          15, correct.
Pattern          16, correct.
Pattern          17, correct.
Pattern          18, correct.
Pattern          19, correct.
Simulation complete via $finish(1) at time 7305 NS + 0
../tbench/test.v:126       $finish;
ncsim> exit
[iclab79@ic21 run_sim]$
```

# Lab Reviews

這次的報告因為是使用教授提供的檔案來進行整個 APR flow，因此只要照著 toturial 的步驟一步一步去做其實是不會遇到問題的，此外還有最後要把完成的檔案放到 apr_source 裡面這樣根據提供的 makefile 才會找到完成 post-route 的設計檔並完成模擬。

WNS (Worst Negative Slack)和 TNS(Total Negative Slack)根據網路上查到的知識是了解用來知道整體設計的 slack 的 severity，便能知道目前階段是否有問題，若沒問題則可以繼續執行。

此外如果 WNS 是正數的時候，代表沒有任何 violation 且數值代表為最小的 positive slack 值，因為沒有任何小於 0 violation，因此總和的 Negative Slack 便會是零，即 TNS 是 0。