2016 VLSI System Design and Implementation

Block Level APR Flow with SOC Encounter (v8.1)

A. Data Prepare:

Prepare required library (for IC contest) and user data for core-level APR.

Description	File of Directory
Working directory	**./SOCE/run/**
Layout Mapping File	./SOCE/run/streamOut.map
Gate Level Netlist	./SOCE/design_data/TOP_syn.v
Timing Constraint File	./SOCE/design_data/TOP_syn.sdc
MMMC View Definition File	./SOCE/design_data/TOP.view
Antenna Rules	./SOCE/lef/antenna_8.lef
Reference Library (Core)	./SOCE/lef/tsmc13fsg_8lm_cic.lef
Timing Library (Core)	./SOCE/lib/fast.lib
	./SOCE/lib/slow.lib
	./SOCE/lib/typical.lib

B. Design Import:

1. Launch SOC Encounter in the working directory:

```
unix% cd ./SOCE/run
unix% encounter
```

2. Set design mode(command line):

```
encounter > setDesignMode -process 130 -addPhysicalCell hier -flowEffort
none
```

3. Design import:

“**File → Import Design…**”

Basic page:

Verilog Files	../design_data/TOP_syn.v
Top Cell	TOP
LEF Files	../lef/tsmc13fsg_8lm_cic.lef ../lef/antenna_8.lef
MMMC View Definition File	../design_data/TOP.view

Be careful with the sequence of files in the “LEF Files” field. “tsmc13fsg_8lm_cic.lef” must be the FIRST ONE!

Power

Power Nets	VDD
Ground Nets	VSS

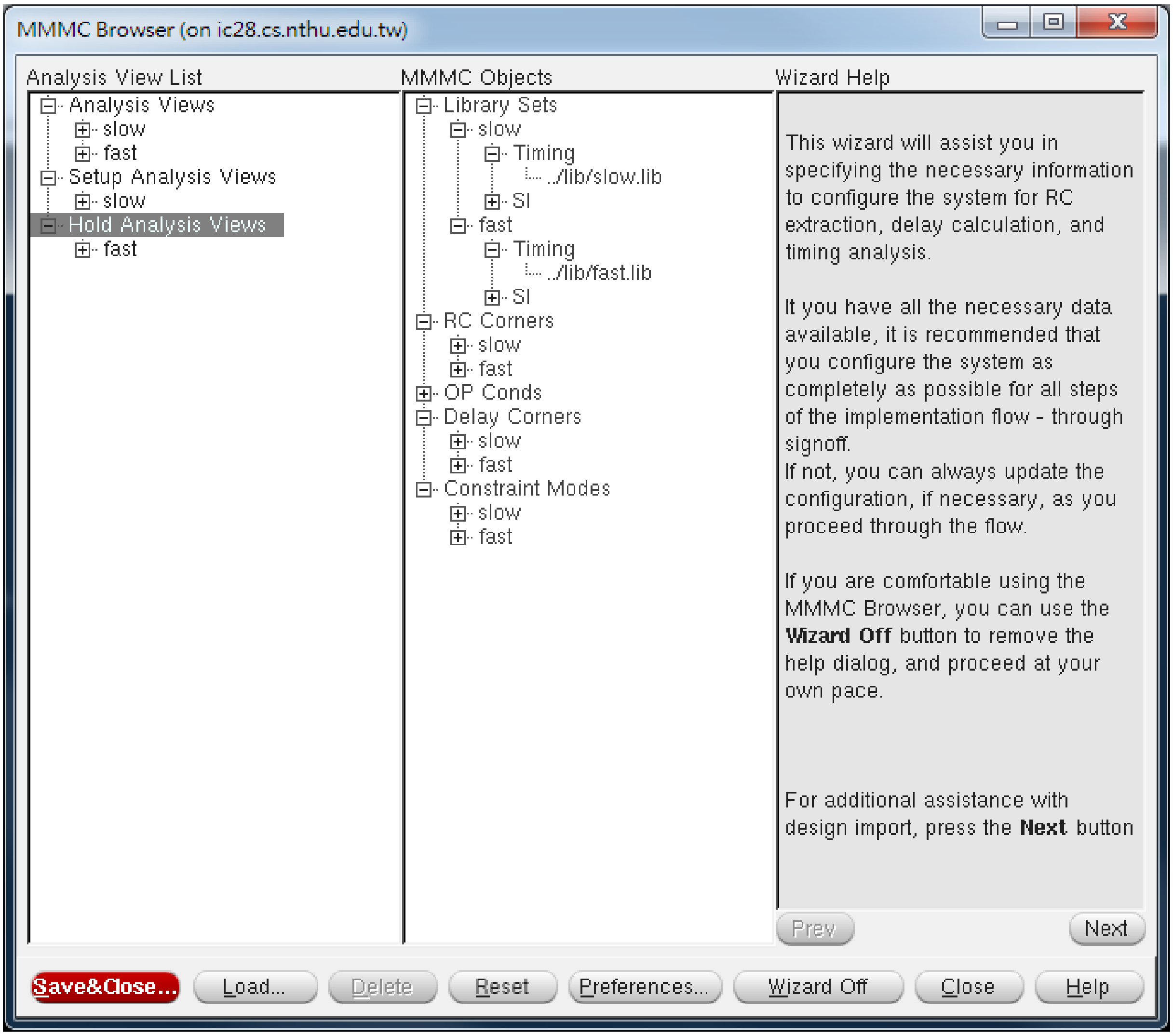
Press Save , save configuration as TOP.conf

Press OK.

Note that we provide the “MMMC View Definition File” for this lab. However,

you have to configure Multi-Mode/Multi-Corner (MMMC) environment manually by yourself when you adopt other process technology. To configure the MMMC environment, press the button "Create Analysis Configuration" to see the wizard help.

An example of MMMC configuration is shown as follows:



This wizard will assist you in specifying the necessary information to configure the system for RC extraction, delay calculation, and timing analysis.

It you have all the necessary data available, it is recommended that you configure the system as completely as possible for all steps of the implementation flow - through signoff.
If not, you can always update the configuration, if necessary, as you proceed through the flow.

If you are comfortable using the MMMC Browser, you can use the **Wizard Off** button to remove the help dialog, and proceed at your own pace.

For additional assistance with design import, press the **Next** button

C. Floor Plan:

1. Global net connection:

   "**Power → Connect Global Nets…**"

Pin	Enable
Pin Name(s)	VDD
To Global Net	VDD

Press Add to List

Tie High	Enable
Pin Name(s)	VDD
To Global Net	VDD

Press Add to List

Pin	Enable
Pins Name(s)	VSS
To Global Net	VSS

Press Add to List

Tie Low	Enable
Pins Name(s)	VSS
To Global Net	VSS

Press Add to List

There will be four entries in “Connection List”, press Apply, and then press Check, then press Cancel.

2. ~~Specify scan chain:~~ (**Skip! Do this step only if your design has scan chains**)

   ~~Type the following instructions in encounter terminal:~~

   ~~encounter> specifyScanChain scan1 –start si_1 –stop so_1~~

   ~~encounter> scantrace~~

3. Specify floor plan:

   “**Floorplan → Specify Floorplan…**”

Ratio(H/W)	1
Core Utilization	**0.9**
Core to Left	**30**
Core to Top	**30**
Core to Right	**30**
Core to Bottom	**30**
All other options	Default value

   Press OK.

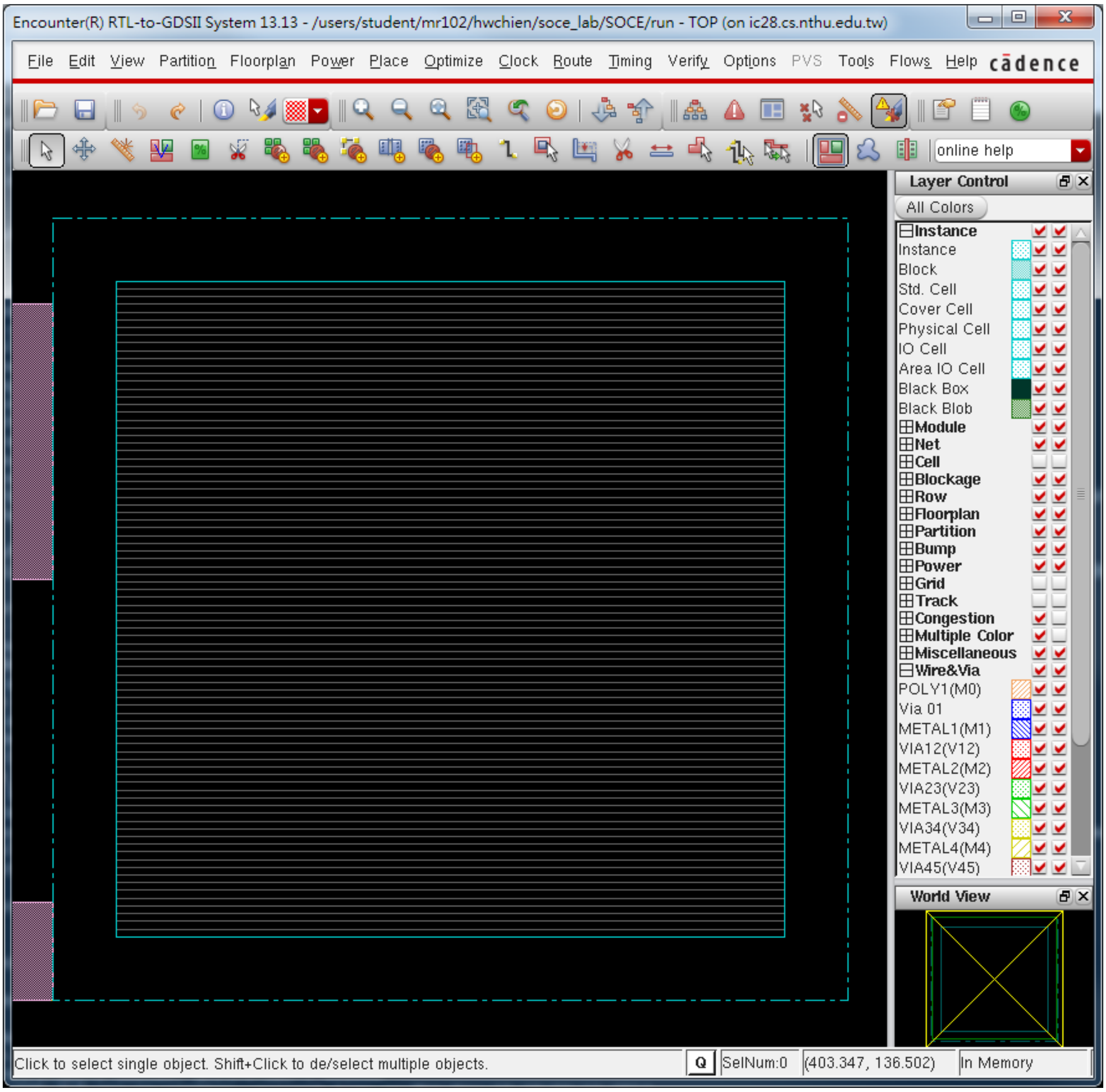
4. Save Design:

   “**File → Save Design**”

Encounter	enable
File name	Floorplan.enc

   Press ok.

   So far, you will see:


Encounter(R) RTL-to-GDSII System 13.13 - /users/student/mr102/hwchien/soce_lab/SOCE/run - TOP (on ic28.cs.nthu.edu.tw)

Click to select single object. Shift+Click to de/select multiple objects. SelNum:0 (403.347, 136.502) In Memory

D. Power Plan:

1. Create power rings for **core**:

   "**Power → Power planning → Add Rings…**"

Net(s)		VDD VSS (Press the browse button to select possible nets)
Ring Type		Core ring(s) contouring
Ring configuration →		
Top	Layer	METAL7 H
	Width	2
Bottom	Layer	METAL7 H
	Width	2
Left	Layer	METAL6 V

	Width	2
Right	Layer	METAL6 V
	Width	2
All other options		Default value

Press Update.

Switch to Advanced page:

Use wire group	Enable
Interleaving	Enable
Number of bits	6

Press OK.

2. Create power stripes:

   “**Power → Power planning → Add Stripes…**”

   Add stripes along y-coordinate.

Net(s)	VSS VDD
Layer	METAL6
Width	1

Press Update.

Set-to-set distance	160
X from left	160
X from right	0

Switch to Advanced page:

Omit stripes inside block rings	Enable
Pad/Core ring connection → Allow jogging	Enable
Block ring connection → Allow jogging	Enable
Use wire group	Enable
Interleaving	Enable
Number of bits	2
All other options	Default value

Switch to Via Generation page:

Use exact overlap area on partially intersecting wires	Enable
Split vias while encounting Obs and different net Wires/Pins	Enable
Generate same-sized stack vias while encountering macro Pins/Obs	Enable
All other options	Default value

Press Apply.

Add stripes along x-coordinate.

Net(s)	VSS VDD
Layer	METAL7
Width	1

Press Update.

Set-to-set distance	160
Start from	top
Y from top	160
Y from bottom	0

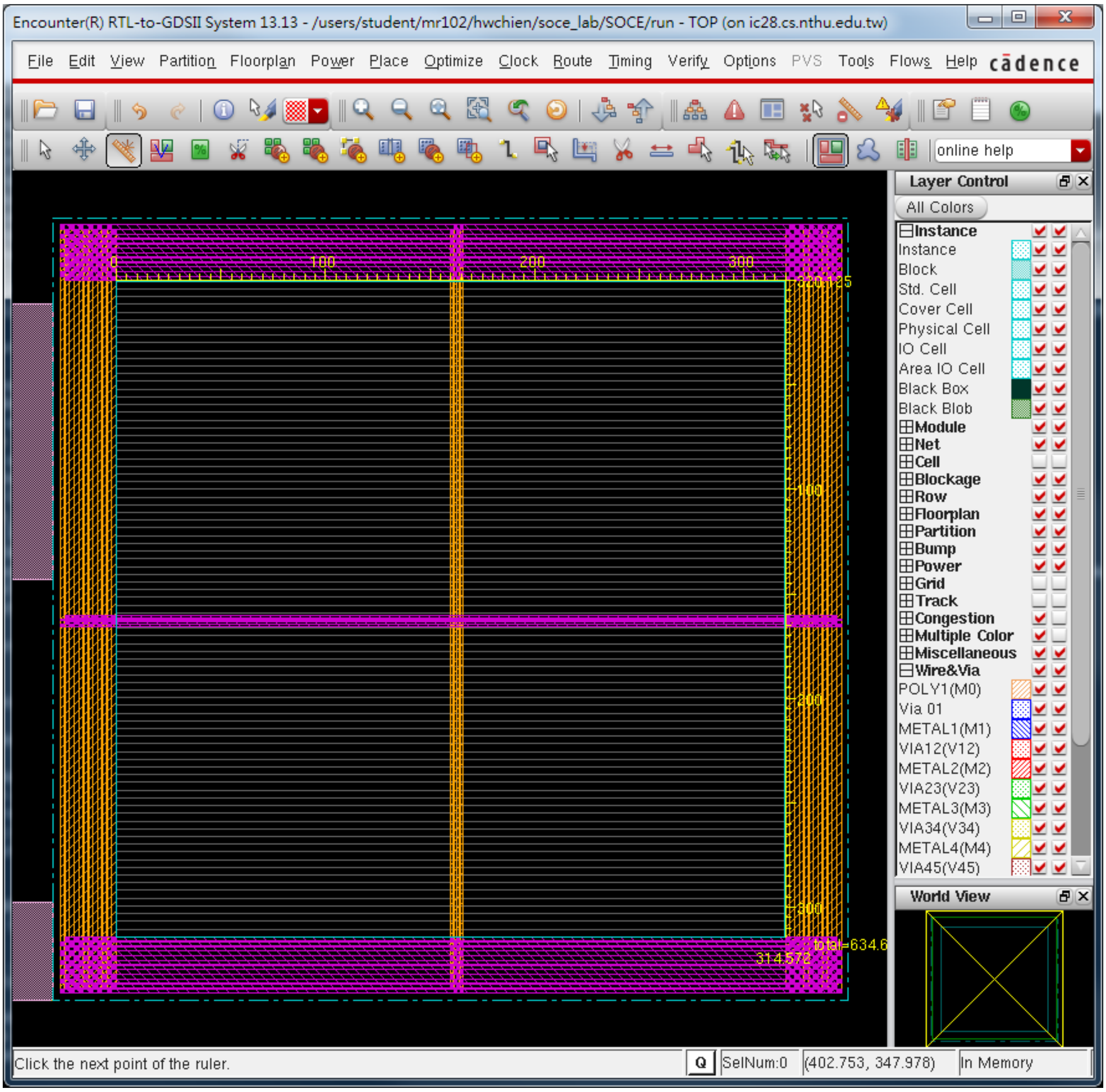
Press OK.

3. Save Design:

   "**File → Save Design…**"

File name	Powerplan.enc

So far, you will see the following floorplan:



Encounter(R) RTL-to-GDSII System 13.13 - /users/student/mr102/hwchien/soce_lab/SOCE/run - TOP (on ic28.cs.nthu.edu.tw)

Click the next point of the ruler.

E. Placement & Pre-CTS Optimization:

1. Placement:

“**Place → Place Standard Cell…**”

Default value, Press OK.

2. Trial route:

   “**Route → Trial Route…**”

Medium Effort	Enable

   Press OK.

3. Pre-CTS timing analysis:

   “**Timing → Extract RC…**”

RC Corner to Output	slow

   Press OK.

   “**Timing →Report Timing…**”

Design stage	Pre-CTS
All other options	Default value

   Press OK.

4. Pre-CTS timing optimization:

   “**Optimize → Optimize Design…**”

Design stage	Pre-CTS
All other options	Default value

   Press OK.

   Observe congestion distribution and optDesign summary.

   WNS = ?

   TNS = ?

   Density = ?

5. Save Design:

   “**File → Save Design…**”

File name	PreCTS.enc

   Press Save.

F. Clock Tree Synthesis & Post-CTS Optimization:

1. Add tie high / low cells:

   Type the following instructions in encounter terminal:

   ```
   encounter> setTieHiLoMode –maxFanout 10 –maxDistance 40
   ```

   “**Place → Tie HI/LO → Add…**”

   Press Select button at right of Cell Name field, and select TIEHI and TIELO.

Cell Name	**TIEHI TIELO**

   Press OK.

2. Synthesis clock tree:

   “**Clock → Synthesize Clock Tree…**”

   Press Gen Spec…

   Add “CLKBUFX2, CLKBUFX3, CLKBUFX4, CLKBUFX6, CLKBUFX8, CLKBUFX12, CLKBUFX16, CLKBUCX20, CLKINVX1, CLKINVX2, CLKINVX3, CLKINVX4, CLKINVX6, CLKINVX8, CLKINVX12, CLKINVX16, CLKINVX20".

Press OK.

Press OK.

Observe the "**Rise Phase Delay, Fall Phase Delay, Trig. Edgs Skew, Rise Skew, and Fall Skew**" in the file clock_report/clock.postCTS.report.

3. Trial route:

   "**Route → Trial Route…**"

Medium Effort	Enable

   Press OK.

4. Post-CTS timing analysis:

   "**Timing → Extract RC…**"

RC Corner to Output	slow

   Press OK.

   "**Timing → Report Timing…**"

Design stage	Post-CTS
All other options	Default value

   Press OK.

   WNS = ?

   TNS = ?

   Density = ?

5. Post-CTS timing optimization:

   "**Optimize → Optimize Design…**"

Design stage	Post-CTS
Hold	Enable
MaxFanout	Enable
All other options	Default value

   Press OK.

   Observe congestion distribution and optDesign summary.

   Setup Mode:

   WNS = ?

   TNS = ?

   Density = ?

   Hold Mode:

   WNS = ?

   TNS = ?

   Density = ?

6. Save Design:

   "**File → Save Design…**"

File name	PostCTS.enc

   Press Save.

G. Global & Detail Routing:

1. Connect standard cell pins:

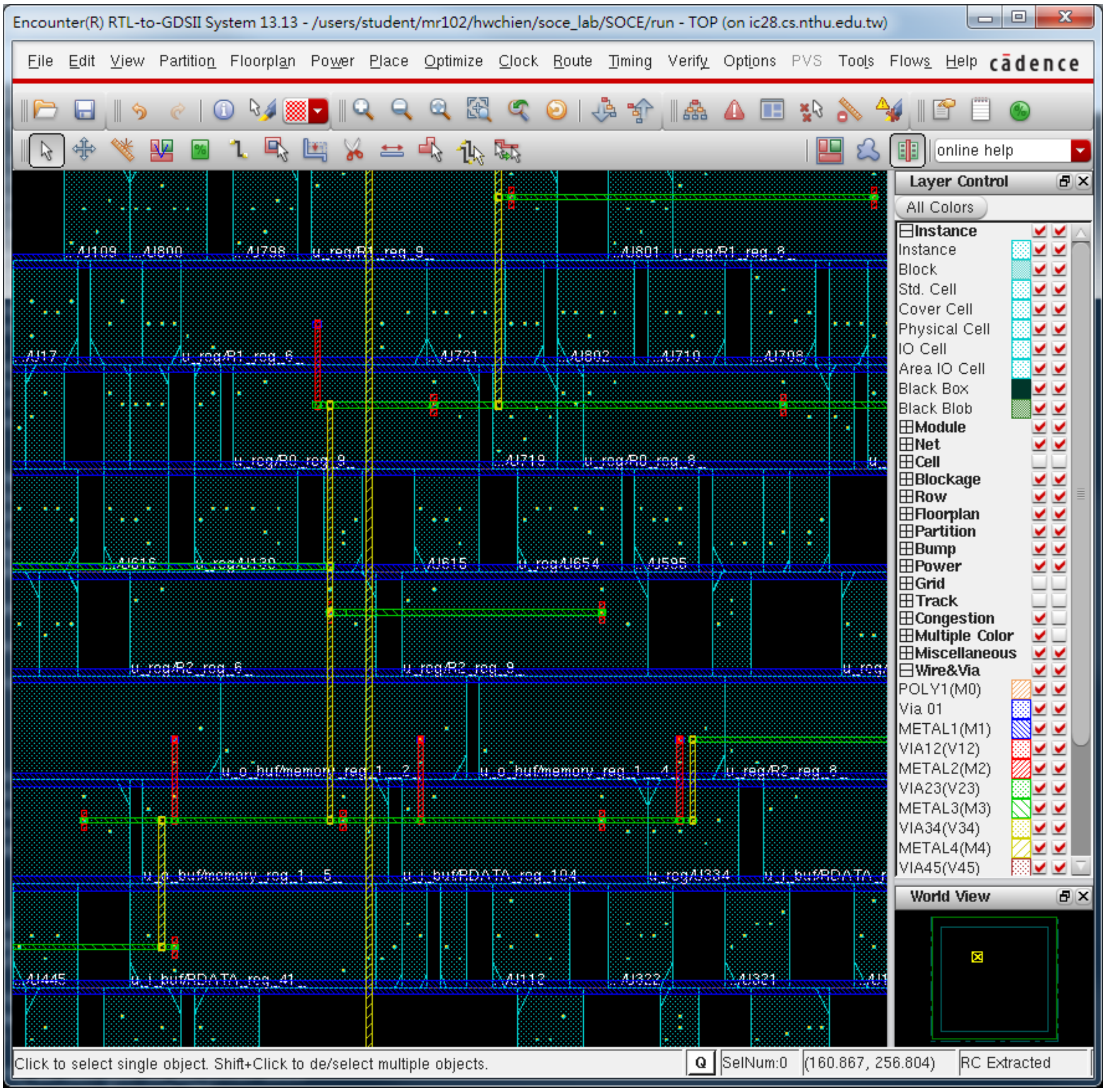
   "**Route → Special Route…**"

Net(s)	VSS VDD
Block pins	Disable
Pad pins	Disable
Pad rings	Disable
Follow Pins	Enable
Floating Stripes	Disable
All other options	Default value

Press OK.

What's the difference before and after this step?

What are the blue bold lines?



Encounter(R) RTL-to-GDSII System 13.13 - /users/student/mr102/hwchien/soce_lab/SOCE/run - TOP (on ic28.cs.nthu.edu.tw)

Click to select single object. Shift+Click to de/select multiple objects.

SelNum:0 (160.867, 256.804) RC Extracted

File Edit View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options PVS Tools Flows Help cadence
online help
U109 U800 U798 u_reg/R1_reg_9_ U801 u_reg/R1_reg_8_
U17 u_reg/R1_reg_6_ U721 U802 U710 U708
u_reg/R0_reg_9_ U719 u_reg/R0_reg_8_
U616 u_reg/U139 U615 u_reg/U654 U595
u_reg/R2_reg_6_ u_reg/R2_reg_9_
u_o_buf/memory_reg_1__2_ u_o_buf/memory_reg_1__4_ u_reg/R2_reg_8_
u_o_buf/memory_reg_1__5_ u_i_buf/RDATA_reg_104_ u_reg/U334 u_i_buf/RDATA_r
U445 u_i_buf/RDATA_reg_41_ U112 U322 U321
Layer Control
All Colors
Instance
Instance
Block
Std. Cell
Cover Cell
Physical Cell
IO Cell
Area IO Cell
Black Box
Black Blob
Module
Net
Cell
Blockage
Row
Floorplan
Partition
Bump
Power
Grid
Track
Congestion
Multiple Color
Miscellaneous
Wire&Via
POLY1(M0)
Via 01
METAL1(M1)
VIA12(V12)
METAL2(M2)
VIA23(V23)
METAL3(M3)
VIA34(V34)
METAL4(M4)
VIA45(V45)
World View

2. Global & detail routing:

“**Route → NanoRoute → Route…**”

Global Route	Enable
Detail Route	Enable
Fix Antenna	Enable
Timing Driven	Enable
SI Driven	Enable
All other options	Default value

Press Attribute:

NetType(s)	Enable
Clock Nets	Enable
Weight	10
Spacing	1
Avoid Detour → True	Enable
All other options	Default value

Press OK.

Press OK.

Observe total number of violations.

Total number of DRC violations = ? (See the terminal)

3. Post-Route timing analysis:

“**Option →Set Mode → Specify RC Extraction Mode …**”

PostRoute	Enable
All other options	Default value

Press OK.

“**Option →Set Mode → Specify Analysis Mode …**”

On-Chip Variation	Enable
All other options	Default value

Press OK.

“**Timing → Extract RC…**”

RC Corner to Output	slow

Press OK.

“**Timing → Report Timing…**”

Design stage	Post-Route
All other options	Default value

Press OK.

WNS = ?

TNS = ?

Density = ?

4. Post-Route timing optimization: (Run post-route timing optimization if WNS is negative)

“**Optimize → Optimize Design…**”

Design stage	Post-Route
All other options	Default value

Press OK.

Observe congestion distribution and optDesign summary.

WNS = ?

TNS = ?

Density = ?

If WNS is negative, perform post-route timing optimization again.

5. Verify DRC:

“**Verify → Verify Connectivity…**”

Press OK.

Verification Complete : ? Viols. ? Wrngs.

“**Verify → Verify Geometry→check**”

Geometry Antenna	Enable
All other options	Default value

Press OK.

Verification Complete : ? Viols. ? Wrngs.

“**Verify → Verify Process Antenna…**”

Press OK.

Verification Complete: ? Violations

“**Tools → Violation Browser…**”

Press Save to save violations report.

6. Save Design:

“**File → Save Design…**”

File name	PostRoute.enc

Press Save.

H. Export Data:

1. Add core filler:

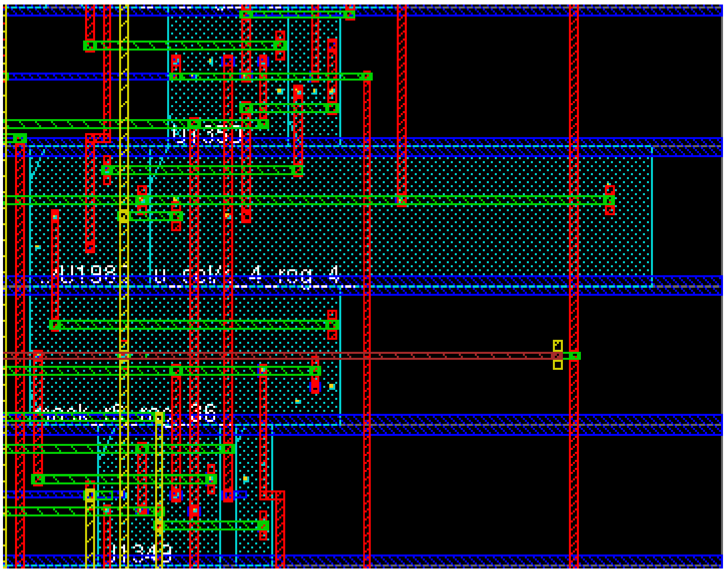
“**Place → Physical Cell → Add Filler…**”

Press Select button at right of Cell Name(s) field, and select all size of filler.

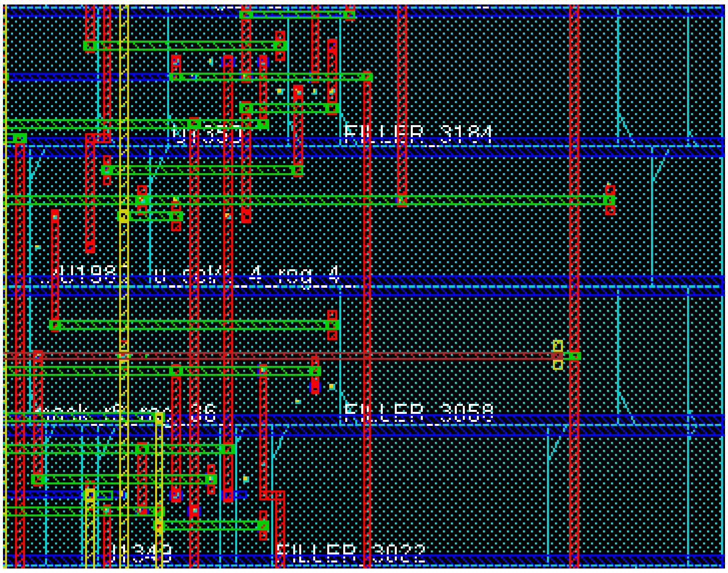
Press OK.

What’s the difference before and after adding filler?

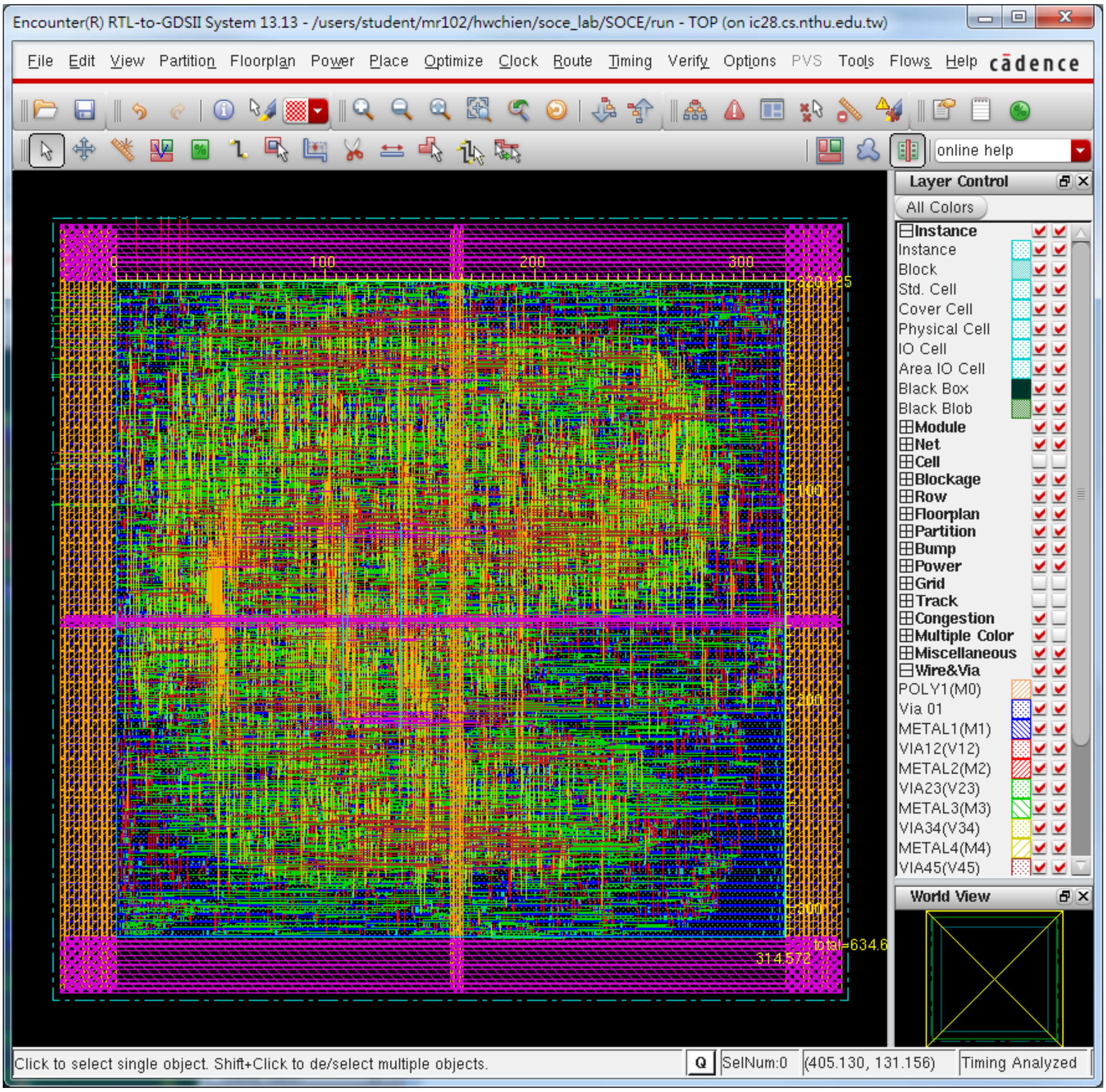
Before adding filler:



After adding filler:



So far, you should see the following view



Click to select single object. Shift+Click to de/select multiple objects. SelNum:0 (405.130, 131.156) Timing Analyzed

2. Save netlist:

   “**File → Save → Netlist…**”

Netlist File	TOP_pr.v
All other options	Default value

   Press OK.

3. Calculate delay:

   “**Timing → Write SDF…**”

File Name	TOP_pr.sdf
ideal clock	**Uncheck**
All other options	Default value

   Press OK.

4. Output stream:

   “**File → Save → GDS/OASIS…**”

Output File	**TOP.gds**

Map File	**streamOut.map**
Units	**1000**
All other options	**Default value**

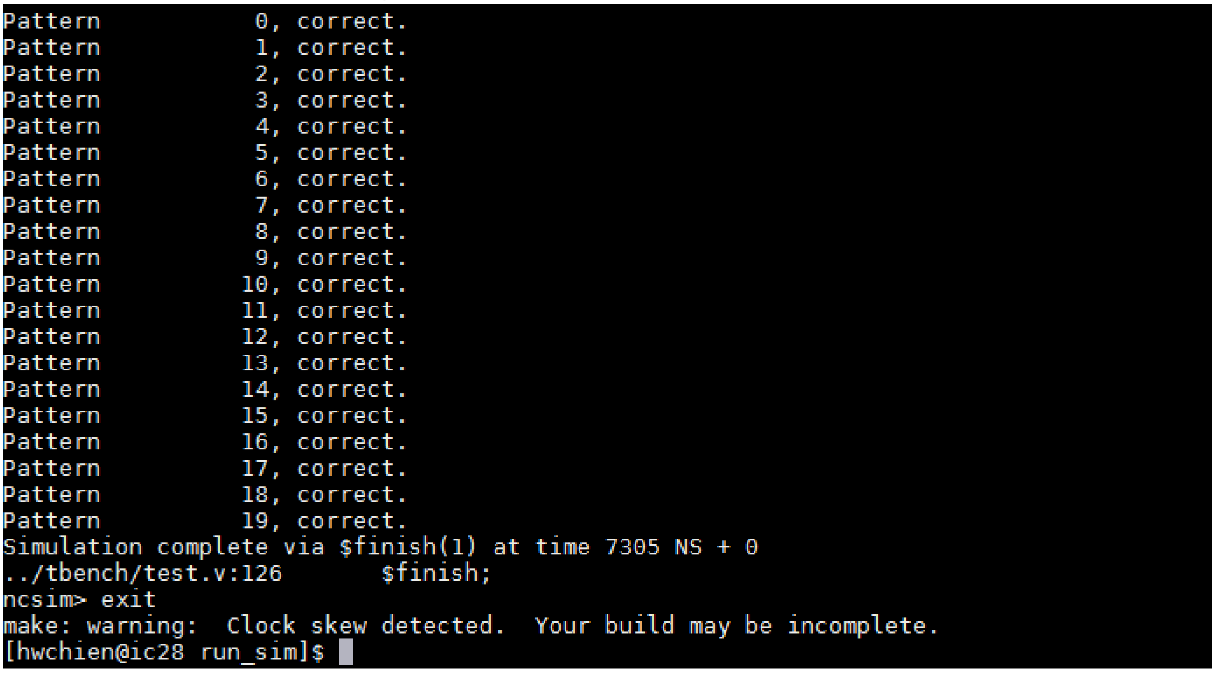
Press OK.

5. Exit:
   "**File → Exit**"

I. Post-layout simulation:

1. Change directory to "run_sim":
   unix% cd ../../run_sim
2. Execute post-layout simulation: (you can reference the content of "Makefile")
   unix% make APR_SIM

You should see the following snapshot:



```
Pattern          0, correct.
Pattern          1, correct.
Pattern          2, correct.
Pattern          3, correct.
Pattern          4, correct.
Pattern          5, correct.
Pattern          6, correct.
Pattern          7, correct.
Pattern          8, correct.
Pattern          9, correct.
Pattern         10, correct.
Pattern         11, correct.
Pattern         12, correct.
Pattern         13, correct.
Pattern         14, correct.
Pattern         15, correct.
Pattern         16, correct.
Pattern         17, correct.
Pattern         18, correct.
Pattern         19, correct.
Simulation complete via $finish(1) at time 7305 NS + 0
../tbench/test.v:126       $finish;
ncsim> exit
make: warning:  Clock skew detected.  Your build may be incomplete.
[hwchien@ic28 run_sim]$
```

3. The timing violation before reset can be ignored.