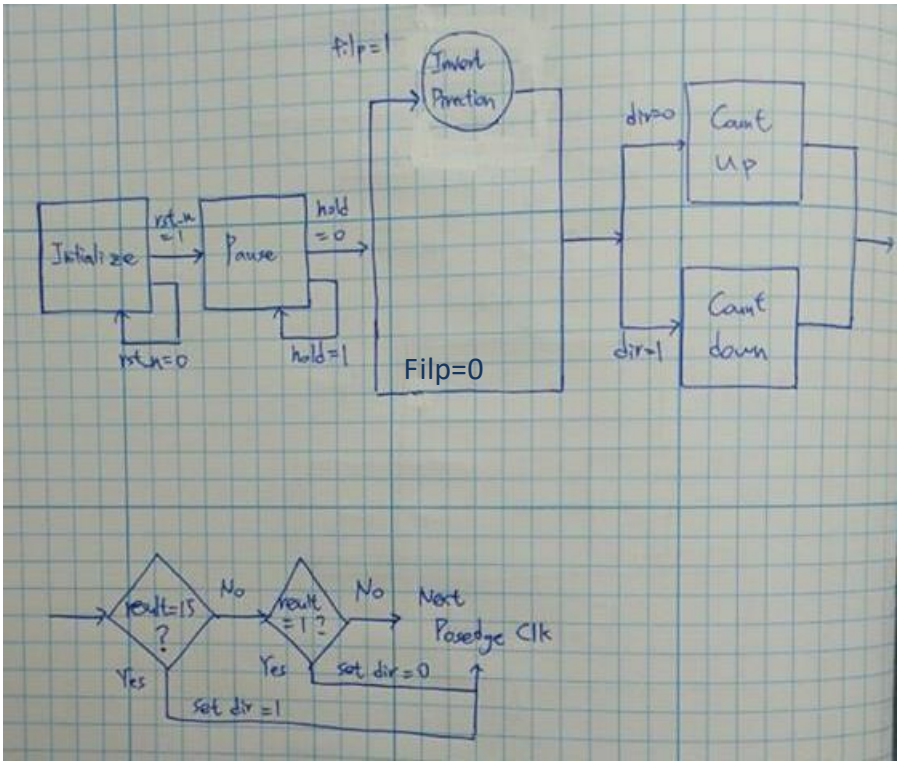
Lab 1: Ping-Pong Counter

September 29, 2016

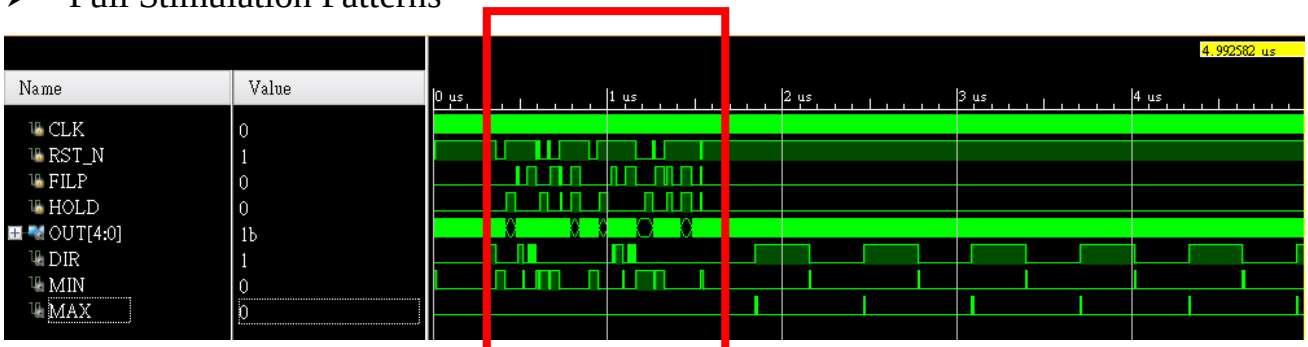
Design Concepts

- Prioritiy of Determination: rst_n > hold > filp
  (That is to say, if rst_n == 0, no matter what hold and filp is, output still maintain initial value.)
- Four states : Initialize, Pause, Count up and Count down.
- Use behavioral modeling to build on architecture and data flow modeling to output result.
- Flow chart:



Stimulation Patterns

- Full Stimulation Patterns



Variation Region

Ping-Pong Counting

Enviroment: Vivado 2016.2

- Variation Region

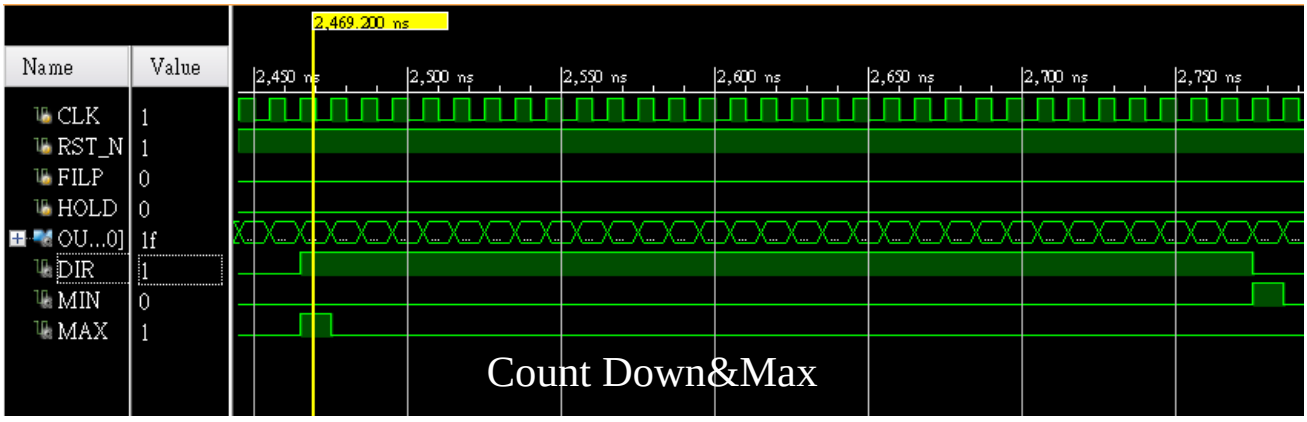
  Three variable: rst_n, filp, hold. Two condition: fit with clk or asynthesize. (asynthesize means signal will change before or later the posedge clk)

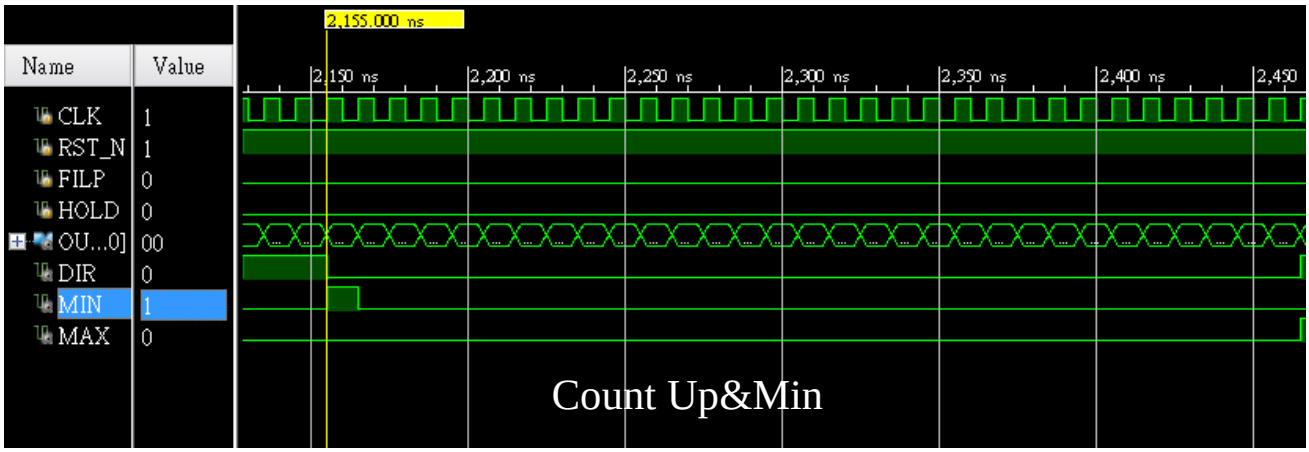
  Variation of Input signals are showed on below form:

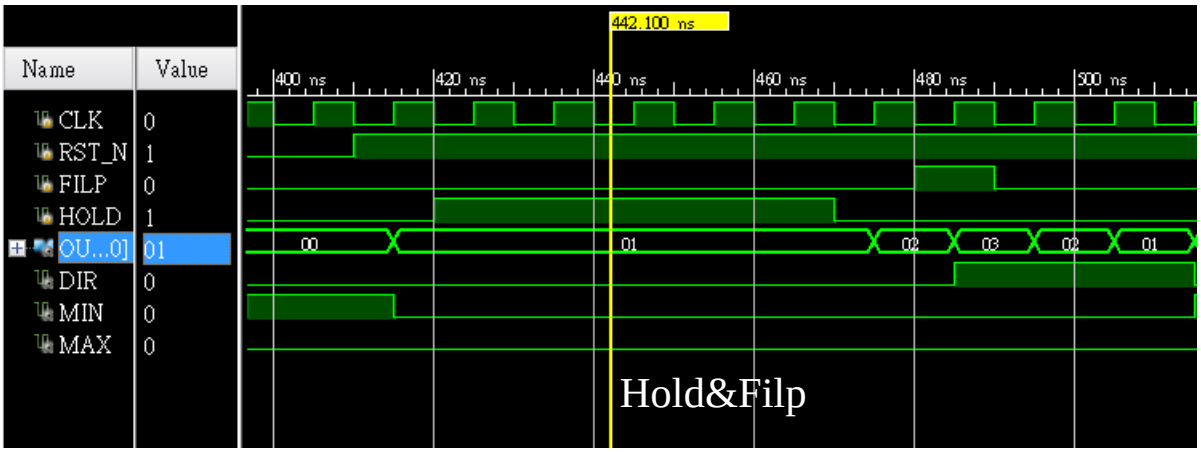
synthesize			asynthesize		
rst_n	filp	hold	rst_n	filp	Hold
0	0	0	0	0	0
1	1	0	1	1	0
1	0	1	1	0	1
0	1	0	0	1	0
0	0	1	0	0	1
1	1	1	1	1	1

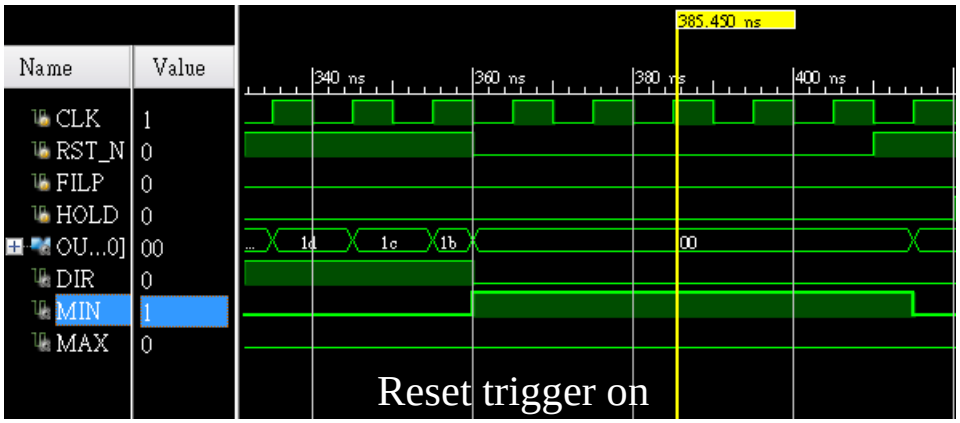
  Because there are too many variations, so I will show each patterns briefly during demo if needs.

- Ping-Pong Counting




2,155.000 ns
Name
Value
CLK
RST_N
FILP
HOLD
OU...0]
DIR
MIN
MAX
1
1
0
0
00
0
1
0
2,150 ns
2,200 ns
2,250 ns
2,300 ns
2,350 ns
2,400 ns
2,450
Count Up&Min


442.100 ns
Name
Value
CLK
RST_N
FILP
HOLD
OU...0]
DIR
MIN
MAX
0
1
0
1
01
0
0
0
400 ns
420 ns
440 ns
460 ns
480 ns
500 ns
00
01
02
03
02
01
Hold&Filp


385.450 ns
Name
Value
CLK
RST_N
FILP
HOLD
OU...0]
DIR
MIN
MAX
1
0
0
0
00
0
1
0
340 ns
360 ns
380 ns
400 ns
1d
1c
1b
00
Reset trigger on