Introduction to Computing System

Homework 3 Answer

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Homework

4.5

(a)

0000 0000 0000 0000
1111 1110 1101 0011

(b)

1. 0001 1110 0100 0011 = 7747
   1111 0000 0010 0101 = -4059
2. 0000 0000 0110 0101 = 101 = 'e'
3. 0000 0110 1101 1001 1111 1110 1101 0011
   $1.10110011111111011010011 \times 2^{-114}$
4. 0001 1110 0100 0011 = 7747
   1111 0000 0010 0101 = 61477

(c)

0001 1110 0100 0011 = Add R7 R1 R3

(d)

0000 0000 0000 0110
1111 1110 1101 0011

4.7

60 opcodes = 6 bits
32 registers = 5 bits
IMM = 32 - 6 - 5 - 5 = 16
IMM range: $-2^{15} - (2^{15} - 1) = -32768 - 32767$.

4.9

Loading of the address of the next instruction into the program counter.

4.15

No instruction can be used to set the RUN latch. In order to re-initiate the instruction cycle, an external input must be applied.

5.4

(a) 8
(b) 6
(c) 6

5.6

(a) 0101 011 010 1 00100
AND R3, R2, #4
(b) 0101 011 010 1 01100
AND R3, R2, #12
(c) 1001 011 010 111111
NOT R3, R2
If zero, no machine is busy
(d) We cannot do this in only one instruction. We need to do an AND with 0000 0000 0100 0000, since the state of machine 6 is in bit [6:6]. This is impossible with the 5-bit immediate value. We could use a second instruction to load this value into a register, and then perform the AND.

5.8

Increasing the number of registers to 32 will need 5 bits to denote the register number. Now, the minimum number of bits needed for the ADD instruction will be 4 (for the opcode) + 3 registers * 5 bits = 19 bits. This cannot fit in the 16-bits allocated for an lc-3 instruction.

5.10

A: BRnzp -171
B: JSR -171
Both A and B result in the PC being changed to (PC+1)-171.
However, B saves the linkage information in R7 and A does not affect R7.

5.13

(a) 0001 011 010 1 00000 (ADD R3, R2, #0)
(b) 1001 011 011 111111 (NOT R3, R3)

0001 011 011 1 00001 (ADD R3, R3, #1)
0001 001 010 0 00011 (ADD R1, R2, R3)

(c) 0001 001 001 1 00000 (ADD R1, R1, #0)

(d) No.

(e) 0101 010 010 1 00000 (AND R2, R2, #0)

5.14

(2): 1001 101 010 111111

(4): 1001 011 110 111111

5.33

It can be inferred that R5 has exactly 5 of the lower 8 bits = 1.

5.40

The signal A indicates if the instruction in IR is a taken branch instruction.

5.41

(a) Y is the P Condition code.

(b) Yes. The error is that the logic should not have the logic gate A.

X should be one whenever the opcode field of the IR matches the opcodes which change the condition code registers.

The problem is that X is 1 for the BR opcode (0000) in the given logic