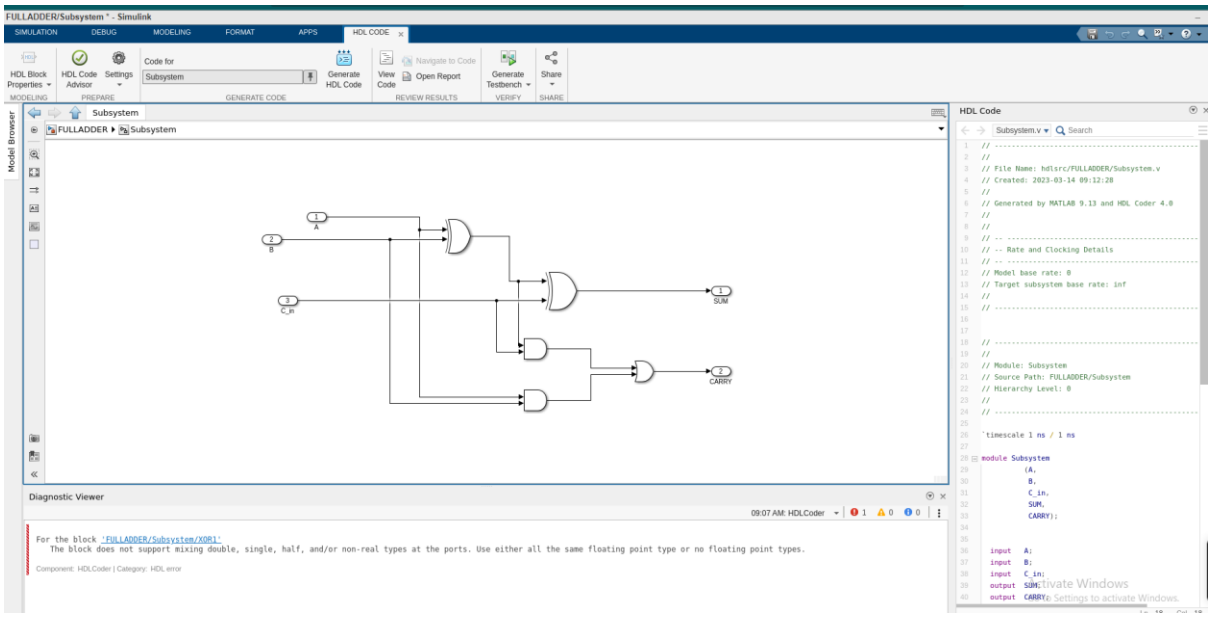
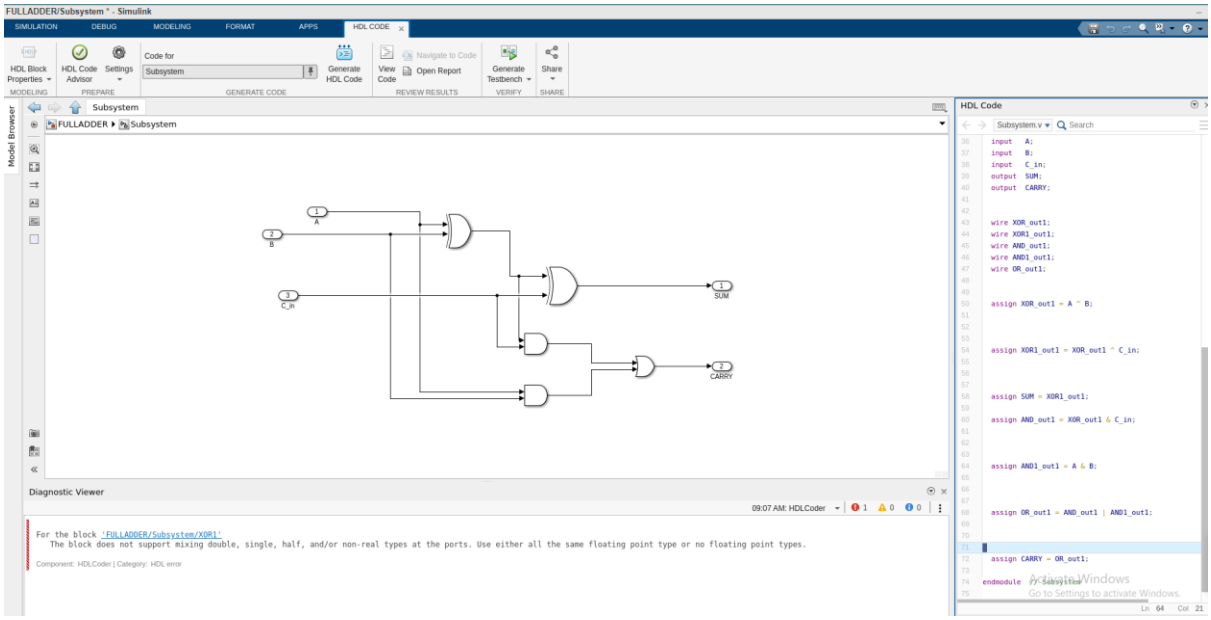
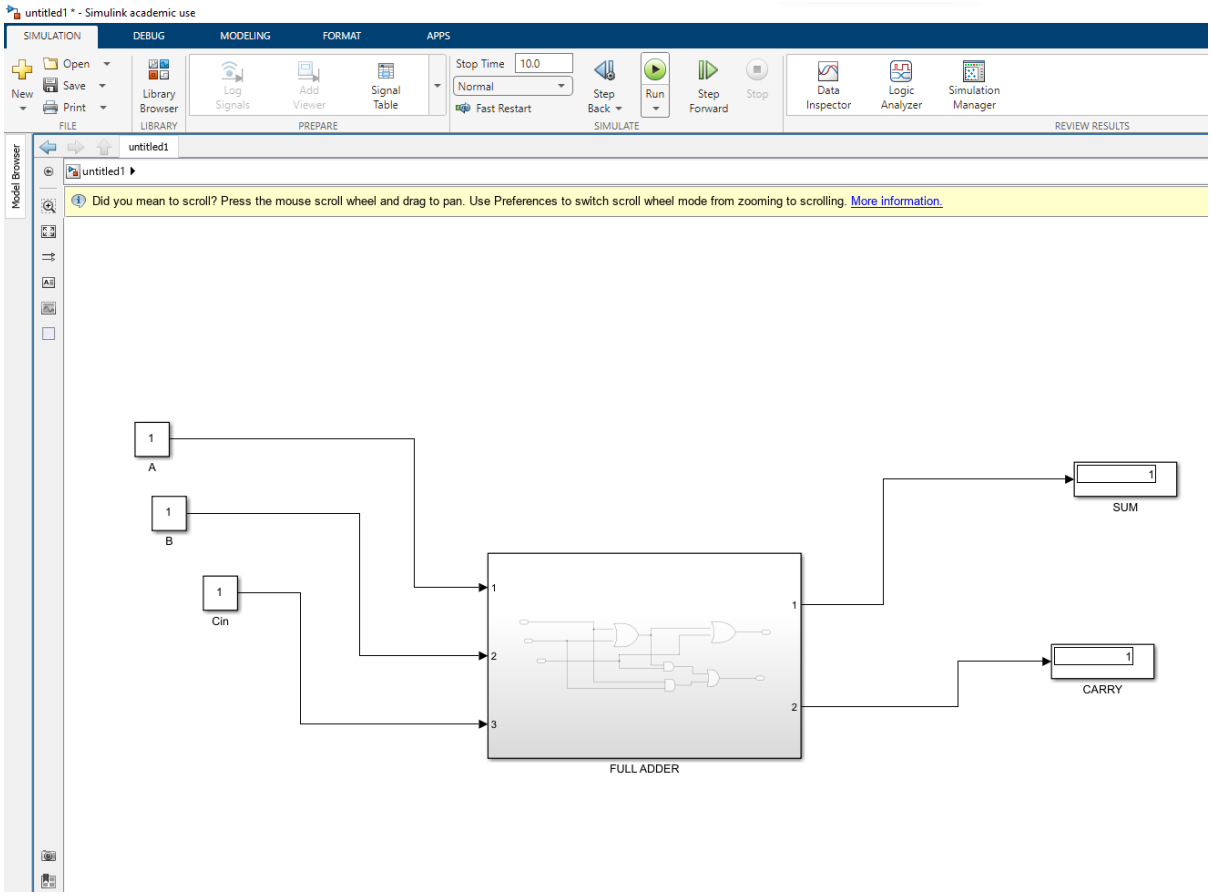
GENERATE VERILOG CODE FOR FULL ADDER.

SOLUTION:-







→VERILOG CODE GENERATED BY HDL CODER:-

// File Name: hdlsrc/FULLADDER/Subsystem.v

// Created: 2023-03-14 09:12:28

//

// Generated by MATLAB 9.13 and HDL Coder 4.0

//

//

// -- ---

// -- Rate and Clocking Details

// -- ---

// Model base rate: 0

// Target subsystem base rate: inf

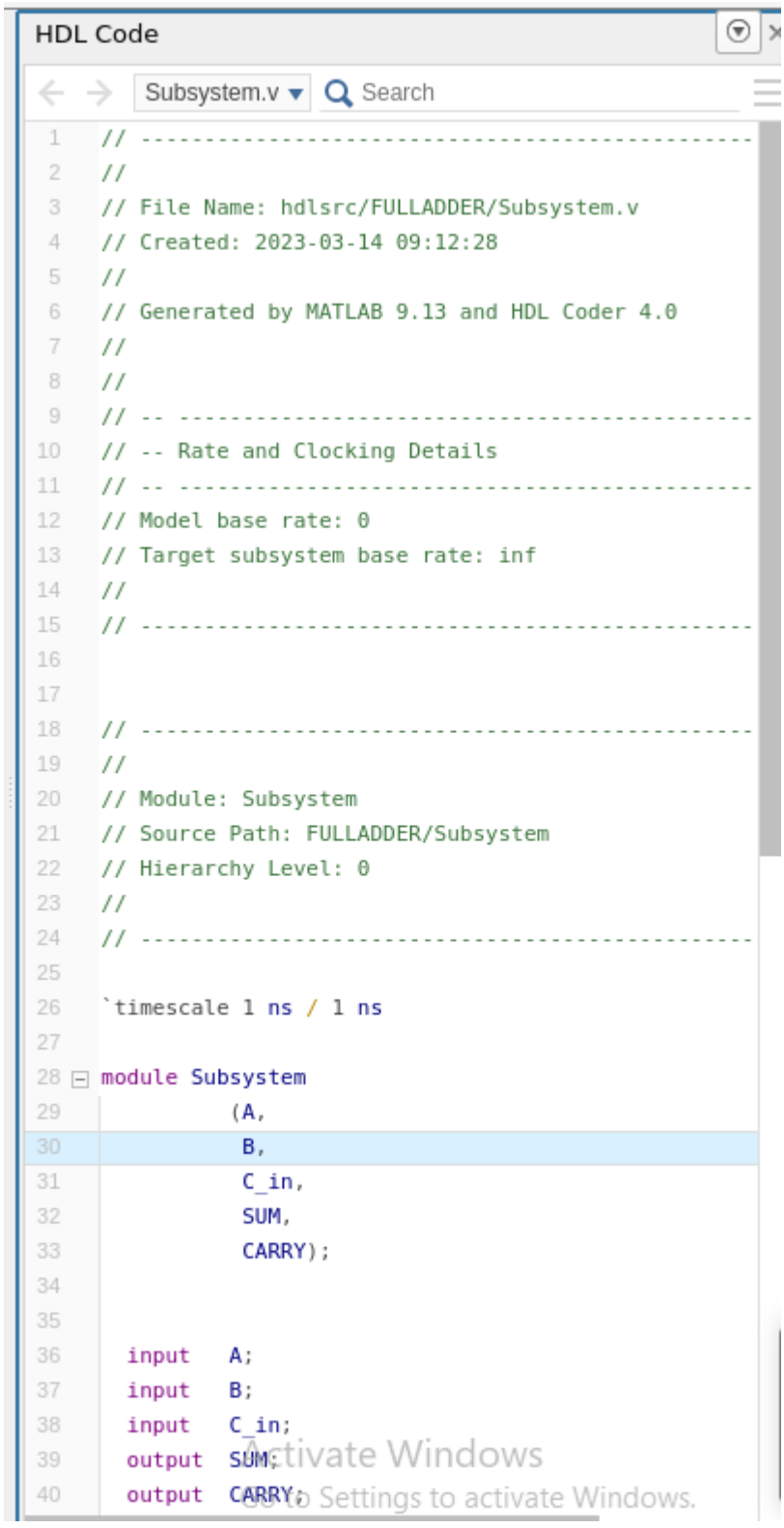
//

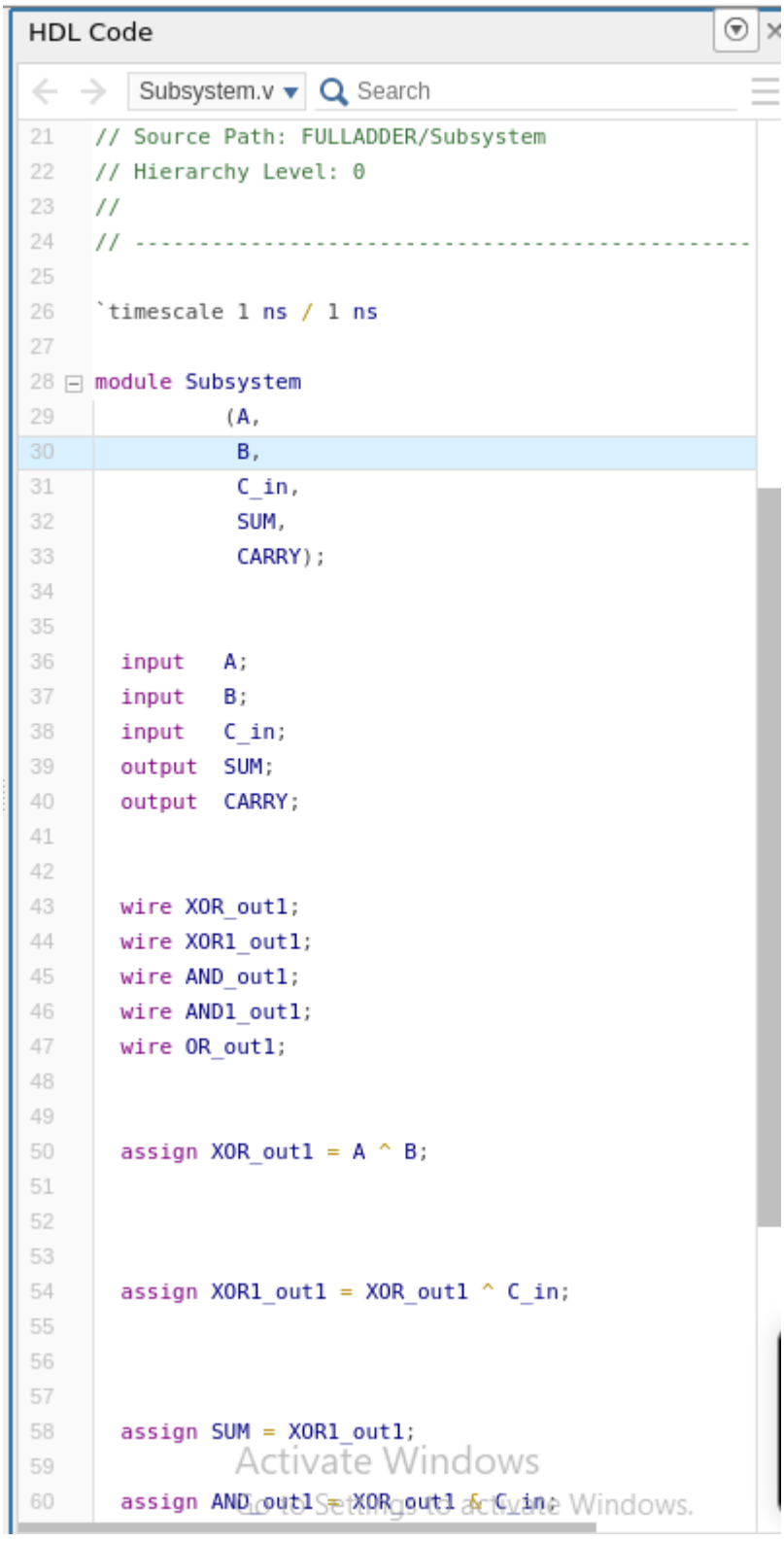
// ---

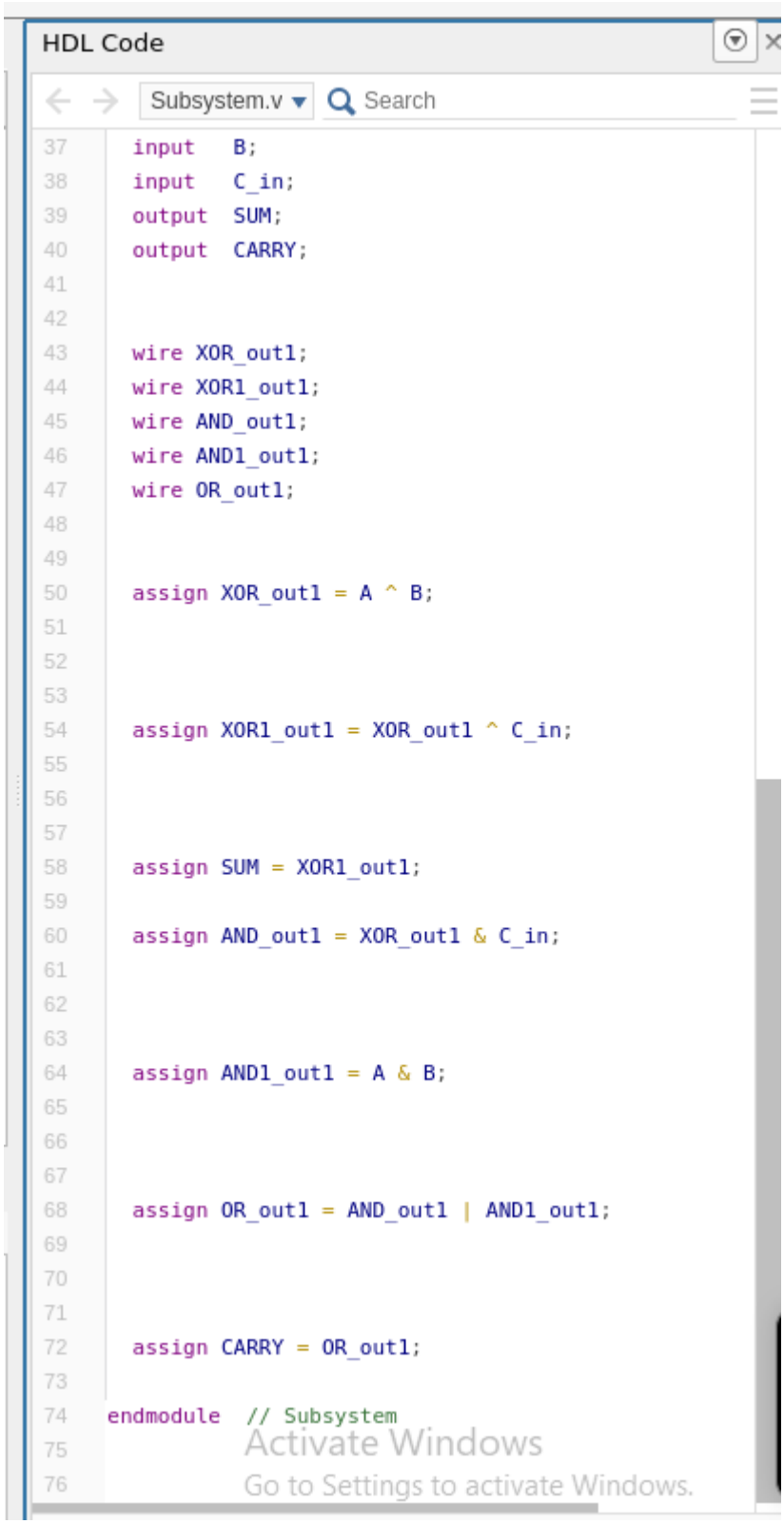
// ---

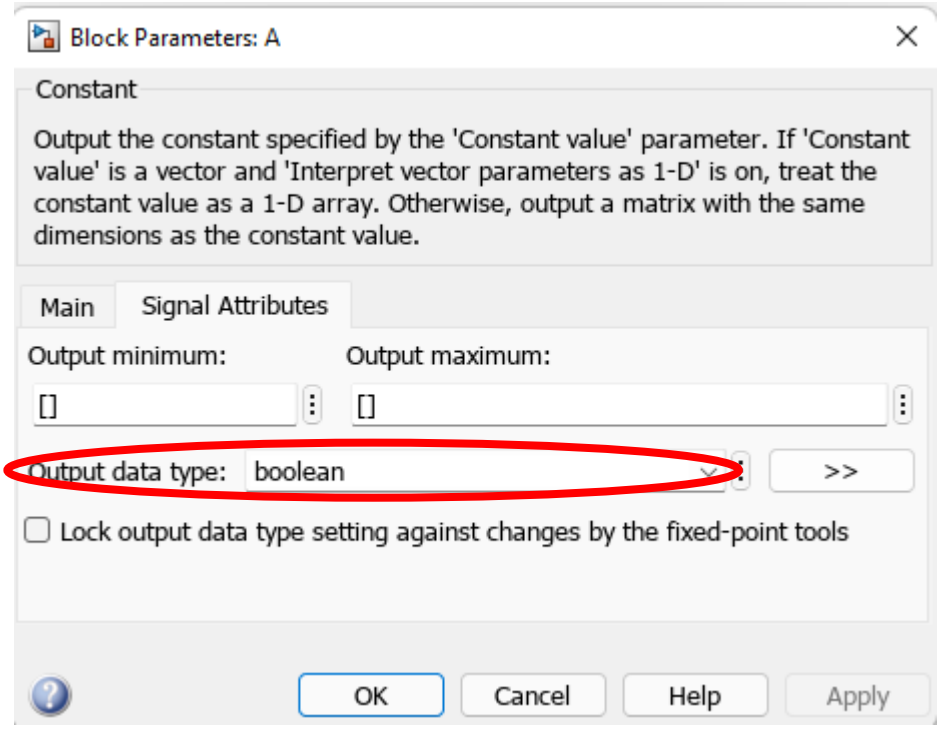
```
//
// Module: Subsystem
// Source Path: FULLADDER/Subsystem
// Hierarchy Level: 0
//
// -------------------------------------------------------------

`timescale 1 ns / 1 ns
module Subsystem
        (A,
         B,
         C_in,
         SUM,
         CARRY);
 input   A;
 input   B;
 input   C_in;
 output  SUM;
 output  CARRY;
 wire XOR_out1;
 wire XOR1_out1;
 wire AND_out1;
 wire AND1_out1;
 wire OR_out1;
 assign XOR_out1 = A ^ B;
 assign XOR1_out1 = XOR_out1 ^ C_in;
 assign SUM = XOR1_out1;
 assign AND_out1 = XOR_out1 & C_in;
 assign AND1_out1 = A & B;
 assign OR_out1 = AND_out1 | AND1_out1;
 assign CARRY = OR_out1;
```

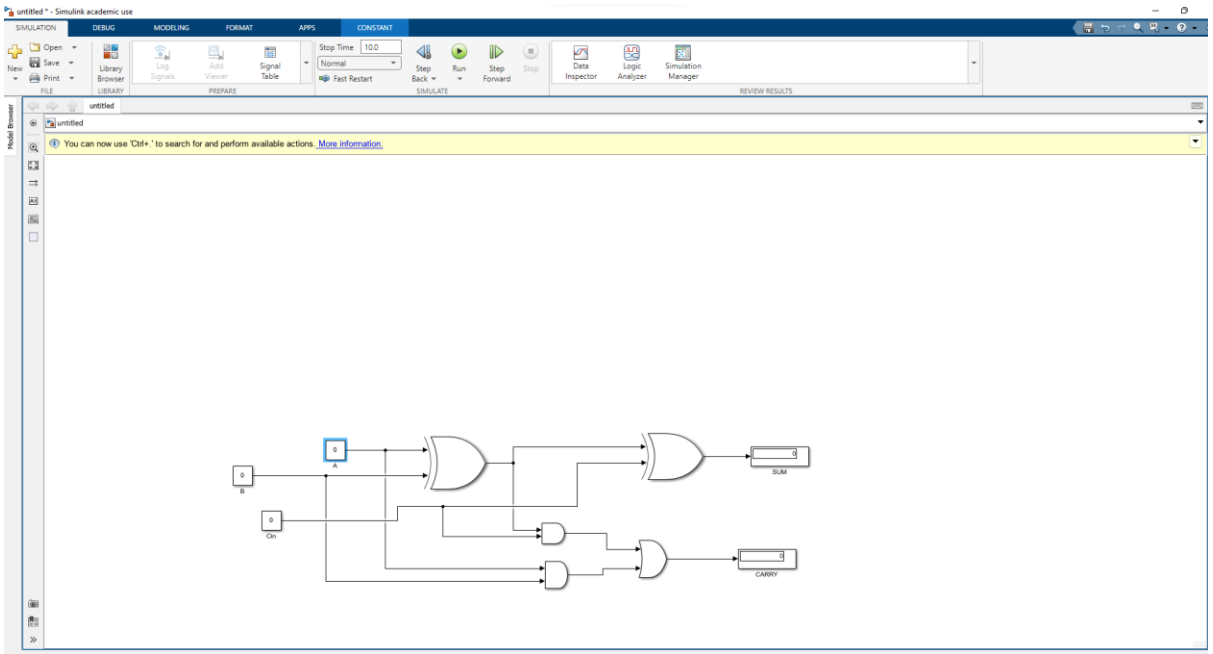
```
endmodule  // Subsystem
```

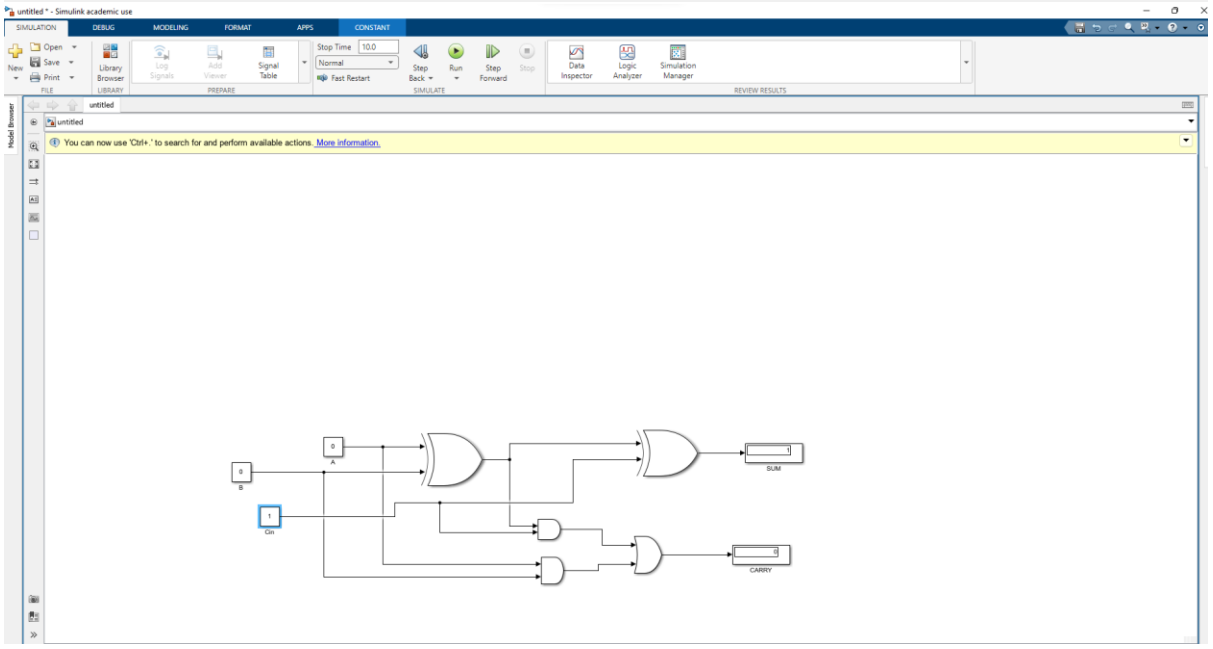

HDL Code
Subsystem.v
Search
// ---
//
// File Name: hdlsrc/FULLADDER/Subsystem.v
// Created: 2023-03-14 09:12:28
//
// Generated by MATLAB 9.13 and HDL Coder 4.0
//
//
// -- ---
// -- Rate and Clocking Details
// -- ---
// Model base rate: 0
// Target subsystem base rate: inf
//
// ---
// ---
//
// Module: Subsystem
// Source Path: FULLADDER/Subsystem
// Hierarchy Level: 0
//
// ---
`timescale 1 ns / 1 ns
module Subsystem
(A,
B,
C_in,
SUM,
CARRY);
input A;
input B;
input C_in;
output SUM;
output CARRY;
Activate Windows
Go to Settings to activate Windows.


HDL Code
Subsystem.v
Search
// Source Path: FULLADDER/Subsystem
// Hierarchy Level: 0
//
// ---
`timescale 1 ns / 1 ns
module Subsystem
(A,
B,
C_in,
SUM,
CARRY);
input A;
input B;
input C_in;
output SUM;
output CARRY;
wire XOR_out1;
wire XOR1_out1;
wire AND_out1;
wire AND1_out1;
wire OR_out1;
assign XOR_out1 = A ^ B;
assign XOR1_out1 = XOR_out1 ^ C_in;
assign SUM = XOR1_out1;
assign AND_out1 = XOR_out1 & C_in;
Activate Windows
Go to Settings to activate Windows.


HDL Code
Subsystem.v
Search
input B;
input C_in;
output SUM;
output CARRY;
wire XOR_out1;
wire XOR1_out1;
wire AND_out1;
wire AND1_out1;
wire OR_out1;
assign XOR_out1 = A ^ B;
assign XOR1_out1 = XOR_out1 ^ C_in;
assign SUM = XOR1_out1;
assign AND_out1 = XOR_out1 & C_in;
assign AND1_out1 = A & B;
assign OR_out1 = AND_out1 | AND1_out1;
assign CARRY = OR_out1;
endmodule // Subsystem
Activate Windows
Go to Settings to activate Windows.


Block Parameters: A
Constant
Output the constant specified by the 'Constant value' parameter. If 'Constant value' is a vector and 'Interpret vector parameters as 1-D' is on, treat the constant value as a 1-D array. Otherwise, output a matrix with the same dimensions as the constant value.
Main
Signal Attributes
Output minimum:
Output maximum:
[]
[]
Output data type:
boolean
>>
Lock output data type setting against changes by the fixed-point tools
OK
Cancel
Help
Apply


untitled * - Simulink academic use
SIMULATION
DEBUG
MODELING
FORMAT
APPS
CONSTANT
Stop Time
10.0
Normal
Fast Restart
Step Back
Run
Step Forward
Stop
Data Inspector
Logic Analyzer
Simulation Manager
Library Browser
Signal Table
untitled
You can now use 'Ctrl+.' to search for and perform available actions. More information.
A
B
Cin
SUM
CARRY


untitled * - Simulink academic use
SIMULATION
DEBUG
MODELING
FORMAT
APPS
CONSTANT
Stop Time
10.0
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Fast Restart
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You can now use 'Ctrl+.' to search for and perform available actions. More information.
A
B
Cin
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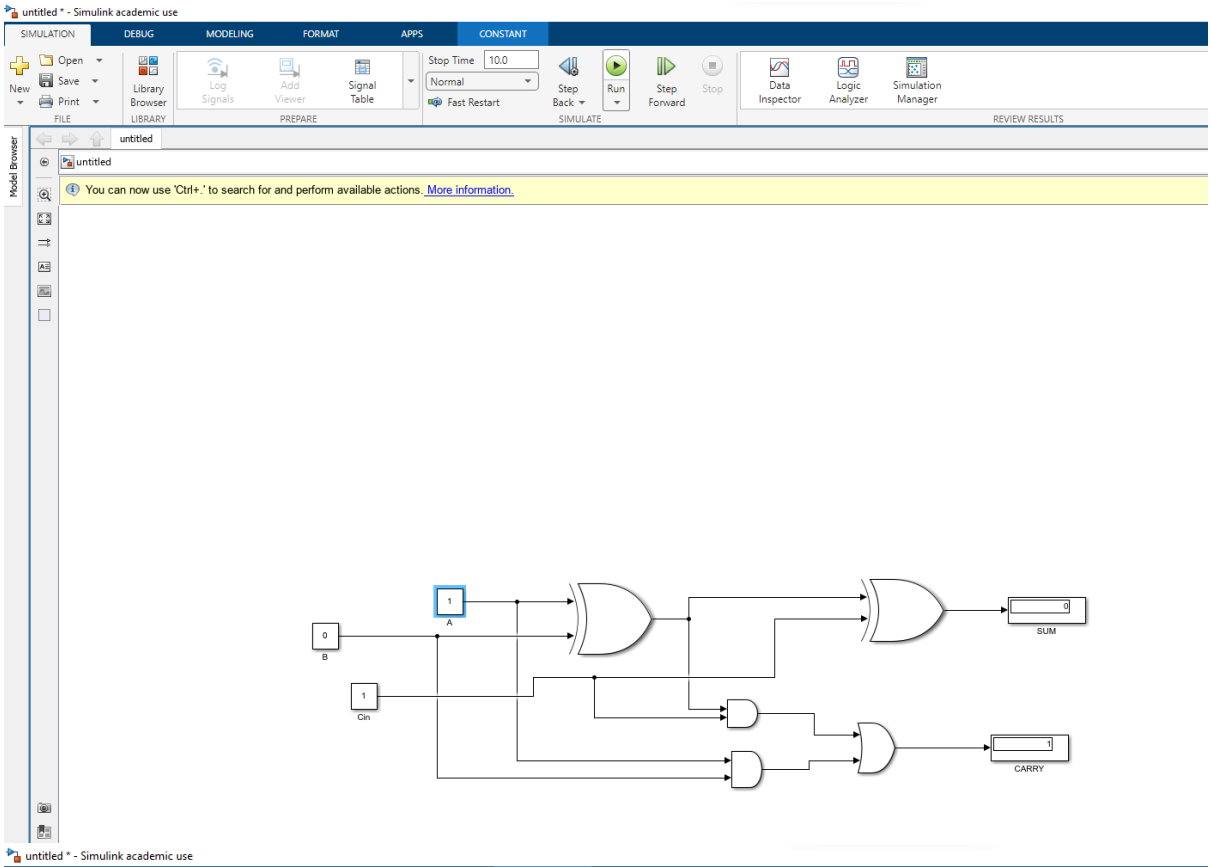
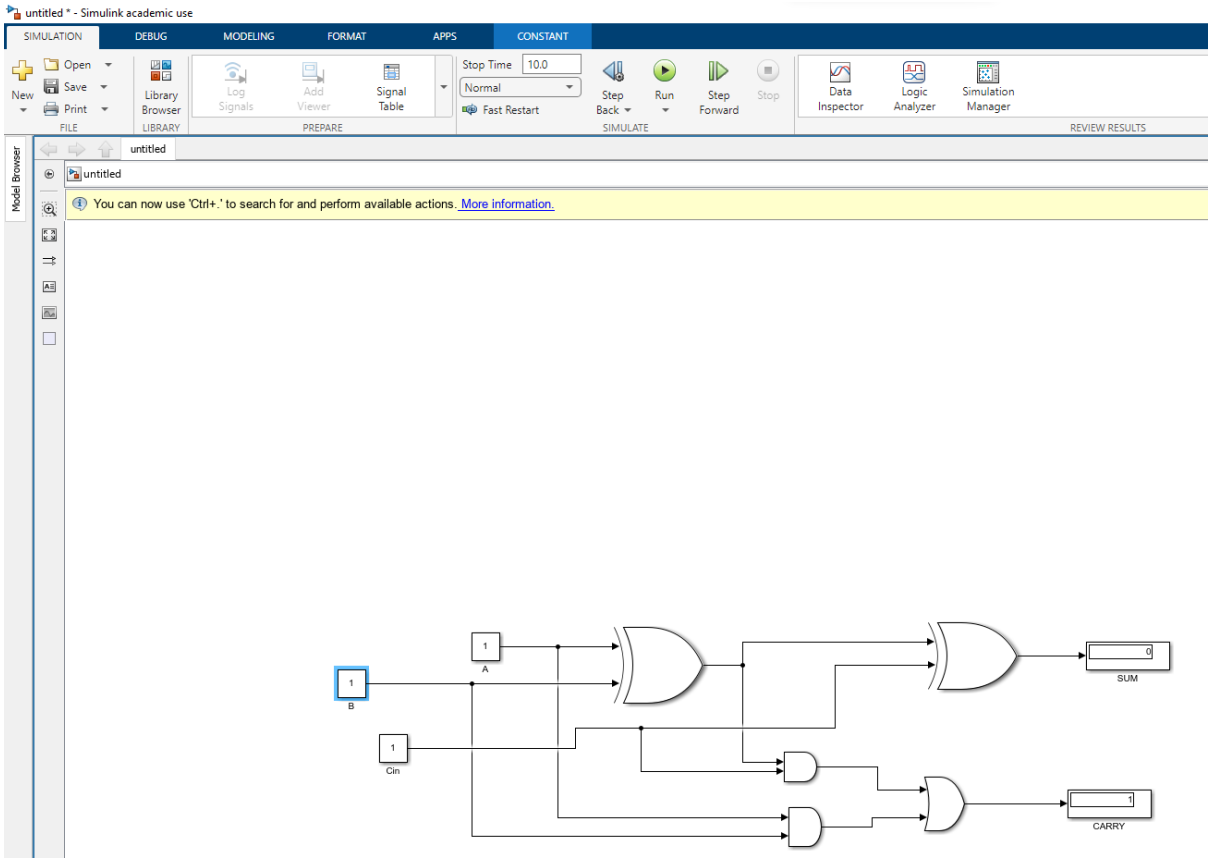
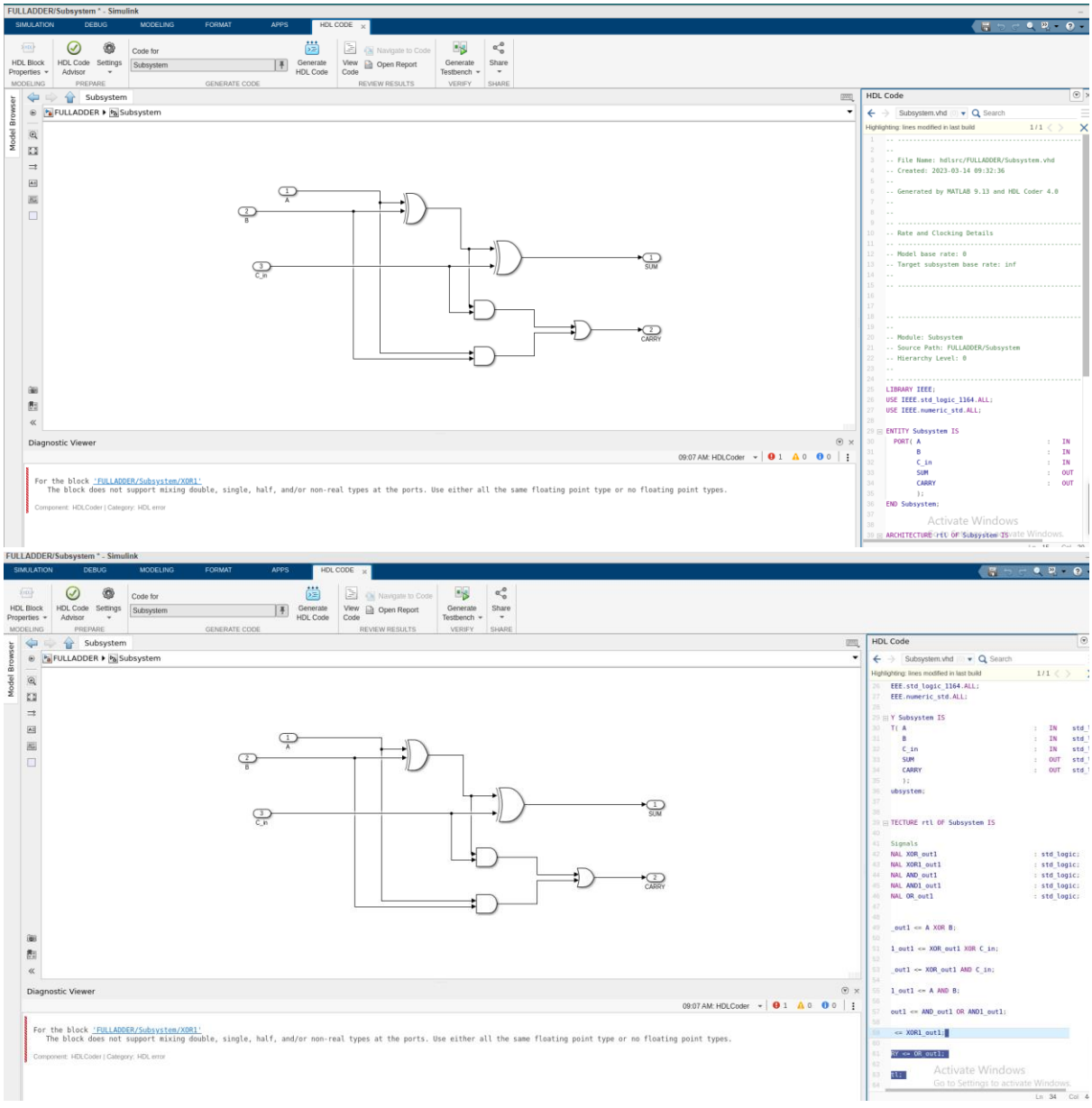
CARRY

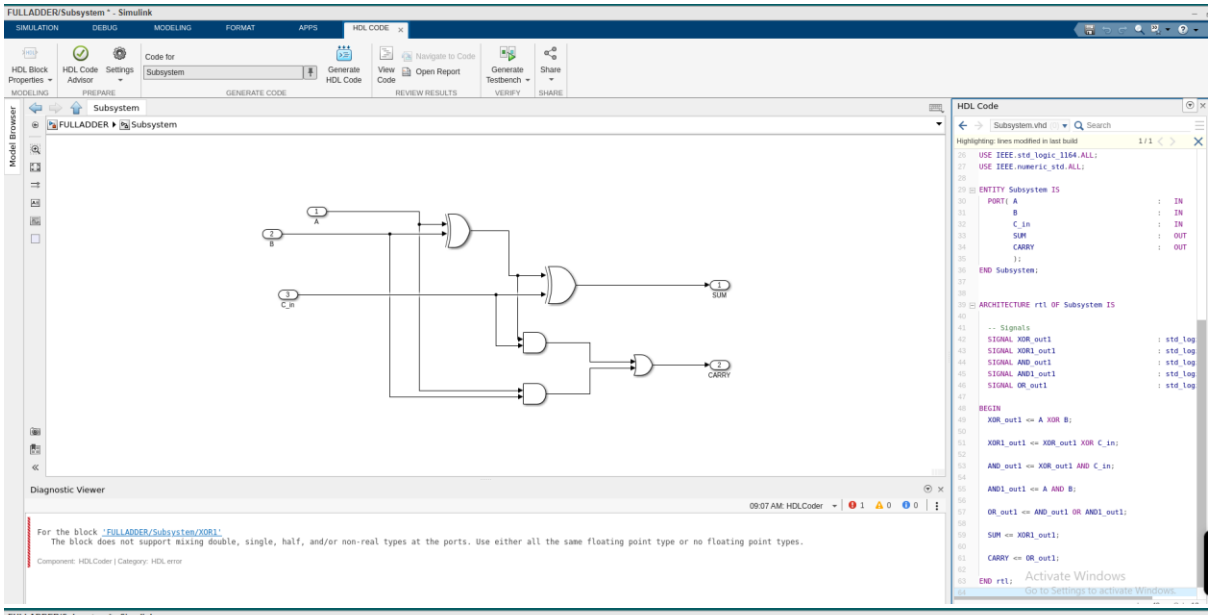

untitled * - Simulink academic use
SIMULATION
DEBUG
MODELING
FORMAT
APPS
CONSTANT
New
Open
Save
Print
FILE
Library Browser
LIBRARY
Log Signals
Add Viewer
Signal Table
PREPARE
Stop Time
10.0
Normal
Fast Restart
Step Back
Run
Step Forward
Stop
SIMULATE
Data Inspector
Logic Analyzer
Simulation Manager
REVIEW RESULTS
Model Browser
untitled
You can now use 'Ctrl+.' to search for and perform available actions. More information.
1
A
0
B
1
Cin
0
SUM
1
CARRY

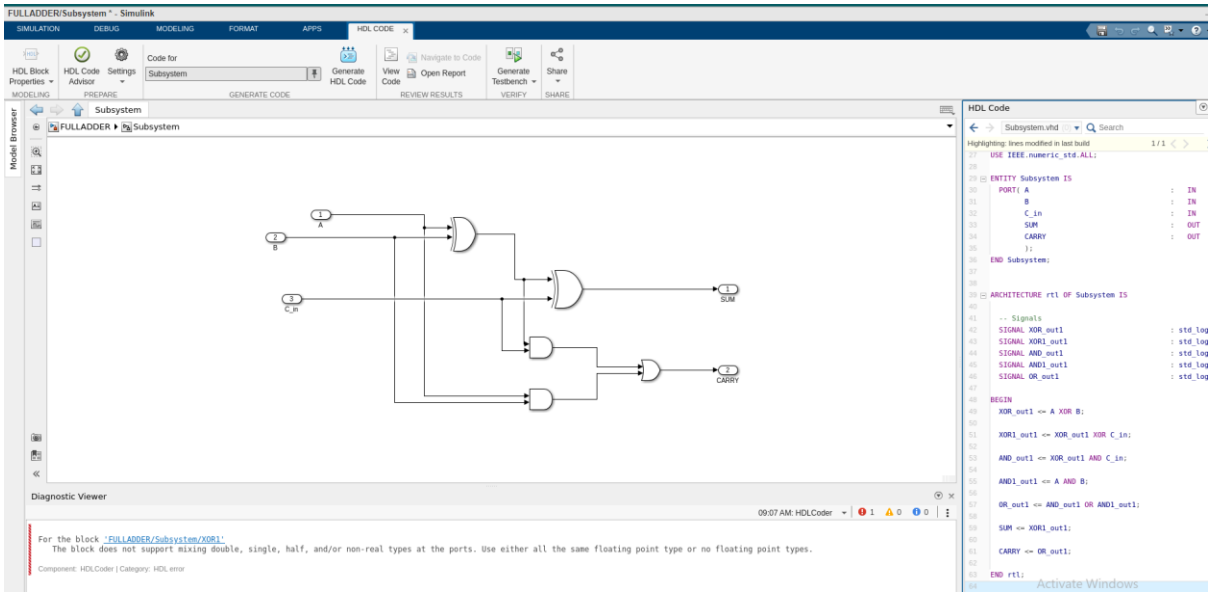

untitled * - Simulink academic use
SIMULATION
DEBUG
MODELING
FORMAT
APPS
CONSTANT
New
Open
Save
Print
FILE
Library Browser
LIBRARY
Log Signals
Add Viewer
Signal Table
PREPARE
Stop Time
10.0
Normal
Fast Restart
Step Back
Run
Step Forward
Stop
SIMULATE
Data Inspector
Logic Analyzer
Simulation Manager
REVIEW RESULTS
Model Browser
untitled
You can now use 'Ctrl+.' to search for and perform available actions. More information.
1
A
1
B
1
Cin
0
SUM
1
CARRY

. Generate VHDL code for Fulladder.

Solution:-




FULLADDER/Subsystem * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
HDL CODE
HDL Block Properties
HDL Code Advisor
Settings
Code for
Subsystem
Generate HDL Code
View Code
Navigate to Code
Open Report
Generate Testbench
Share
MODELING
PREPARE
GENERATE CODE
REVIEW RESULTS
VERIFY
SHARE
Model Browser
Subsystem
FULLADDER ▸ Subsystem
A
B
C_in
SUM
CARRY
Diagnostic Viewer
09:07 AM: HDLCoder
For the block 'FULLADDER/Subsystem/XOR1'
The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
Component: HDLCoder | Category: HDL error
HDL Code
Subsystem.vhd
Search
Highlighting: lines modified in last build
1 / 1
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;
ENTITY Subsystem IS
PORT(A : IN
B : IN
C_in : IN
SUM : OUT
CARRY : OUT
);
END Subsystem;
ARCHITECTURE rtl OF Subsystem IS
-- Signals
SIGNAL XOR_out1 : std_log
SIGNAL XOR1_out1 : std_log
SIGNAL AND_out1 : std_log
SIGNAL AND1_out1 : std_log
SIGNAL OR_out1 : std_log
BEGIN
XOR_out1 <= A XOR B;
XOR1_out1 <= XOR_out1 XOR C_in;
AND_out1 <= XOR_out1 AND C_in;
AND1_out1 <= A AND B;
OR_out1 <= AND_out1 OR AND1_out1;
SUM <= XOR1_out1;
CARRY <= OR_out1;
END rtl;
Activate Windows
Go to Settings to activate Windows.


FULLADDER/Subsystem * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
HDL CODE
HDL Block Properties
HDL Code Advisor
Settings
Code for
Subsystem
Generate HDL Code
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Model Browser
Subsystem
FULLADDER ▸ Subsystem
A
B
C_in
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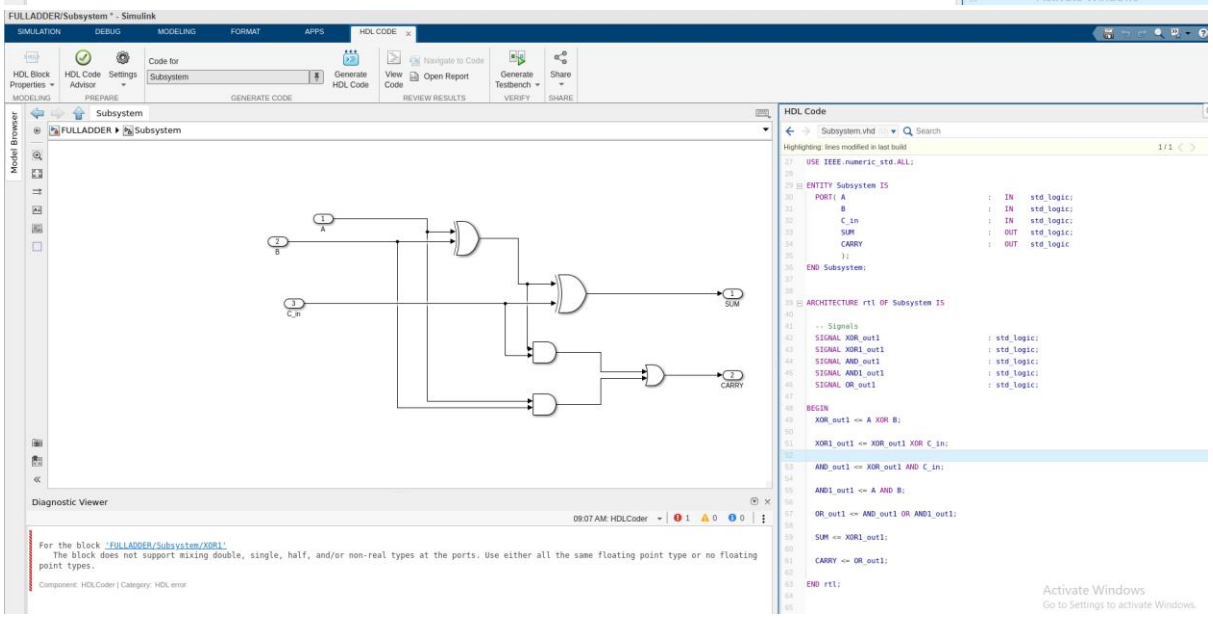
Component: HDLCoder | Category: HDL error
HDL Code
Subsystem.vhd
Search
Highlighting: lines modified in last build
1 / 1
USE IEEE.numeric_std.ALL;
ENTITY Subsystem IS
PORT(A : IN
B : IN
C_in : IN
SUM : OUT
CARRY : OUT
);
END Subsystem;
ARCHITECTURE rtl OF Subsystem IS
-- Signals
SIGNAL XOR_out1 : std_log
SIGNAL XOR1_out1 : std_log
SIGNAL AND_out1 : std_log
SIGNAL AND1_out1 : std_log
SIGNAL OR_out1 : std_log
BEGIN
XOR_out1 <= A XOR B;
XOR1_out1 <= XOR_out1 XOR C_in;
AND_out1 <= XOR_out1 AND C_in;
AND1_out1 <= A AND B;
OR_out1 <= AND_out1 OR AND1_out1;
SUM <= XOR1_out1;
CARRY <= OR_out1;
END rtl;
Activate Windows


FULLADDER/Subsystem * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
HDL CODE
HDL Block Properties
HDL Code Advisor
Settings
Code for
Subsystem
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FULLADDER ▸ Subsystem
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09:07 AM: HDLCoder
For the block 'FULLADDER/Subsystem/XOR1'
The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
Component: HDLCoder | Category: HDL error
HDL Code
Subsystem.vhd
Search
Highlighting: lines modified in last build
1 / 1
USE IEEE.numeric_std.ALL;
ENTITY Subsystem IS
PORT(A : IN std_logic;
B : IN std_logic;
C_in : IN std_logic;
SUM : OUT std_logic;
CARRY : OUT std_logic
);
END Subsystem;
ARCHITECTURE rtl OF Subsystem IS
-- Signals
SIGNAL XOR_out1 : std_logic;
SIGNAL XOR1_out1 : std_logic;
SIGNAL AND_out1 : std_logic;
SIGNAL AND1_out1 : std_logic;
SIGNAL OR_out1 : std_logic;
BEGIN
XOR_out1 <= A XOR B;
XOR1_out1 <= XOR_out1 XOR C_in;
AND_out1 <= XOR_out1 AND C_in;
AND1_out1 <= A AND B;
OR_out1 <= AND_out1 OR AND1_out1;
SUM <= XOR1_out1;
CARRY <= OR_out1;
END rtl;
Activate Windows
Go to Settings to activate Windows.

→VHDL CODE GENERATED BY HDL CODER OF MATLAB SIMULINK:-

```
-- -------------------------------------------------------------

--

-- File Name: hdlsrc/FULLADDER/Subsystem.vhd

-- Created: 2023-03-14 09:32:36

--

-- Generated by MATLAB 9.13 and HDL Coder 4.0

--

--

-- -------------------------------------------------------------

-- Rate and Clocking Details

-- -------------------------------------------------------------

-- Model base rate: 0

-- Target subsystem base rate: inf

--

-- -------------------------------------------------------------

-- -------------------------------------------------------------

--

-- Module: Subsystem

-- Source Path: FULLADDER/Subsystem

-- Hierarchy Level: 0

--

-- -------------------------------------------------------------

LIBRARY IEEE;

USE IEEE.std_logic_1164.ALL;
```

```
USE IEEE.numeric_std.ALL;
ENTITY Subsystem IS
  PORT( A                    :   IN    std_logic;
        B                    :   IN    std_logic;
        C_in                 :   IN    std_logic;
        SUM                  :   OUT   std_logic;
        CARRY                :   OUT   std_logic
        );
END Subsystem;


ARCHITECTURE rtl OF Subsystem IS

  -- Signals
  SIGNAL XOR_out1            : std_logic;
  SIGNAL XOR1_out1           : std_logic;
  SIGNAL AND_out1            : std_logic;
  SIGNAL AND1_out1           : std_logic;
  SIGNAL OR_out1             : std_logic;
BEGIN
  XOR_out1 <= A XOR B;
  XOR1_out1 <= XOR_out1 XOR C_in;
  AND_out1 <= XOR_out1 AND C_in;
  AND1_out1 <= A AND B;
  OR_out1 <= AND_out1 OR AND1_out1;
  SUM <= XOR1_out1;
  CARRY <= OR_out1;
END rtl;
```

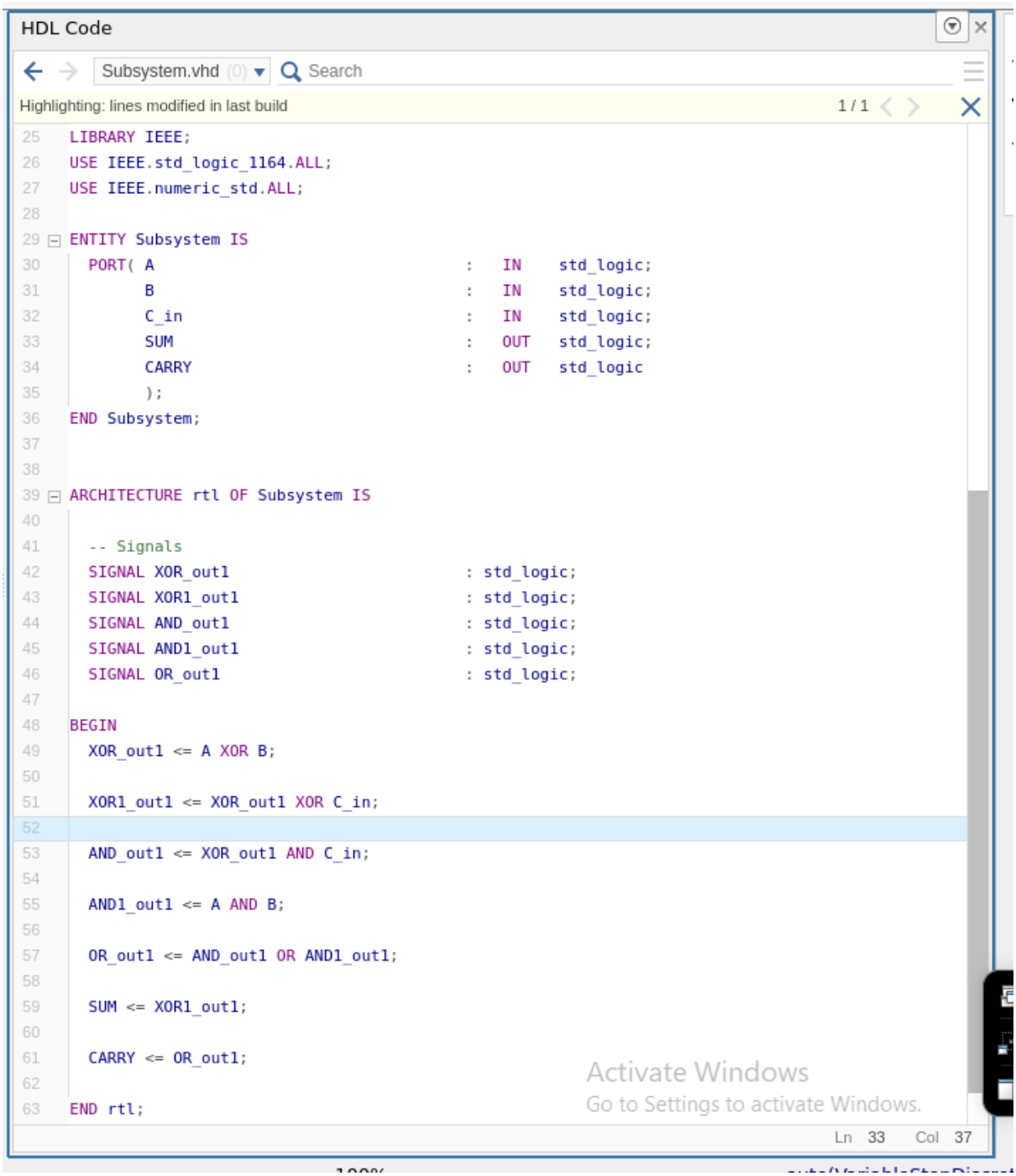
HDL Code

Subsystem.vhd (0) Search

Highlighting: lines modified in last build 1 / 1

```
1  -- -------------------------------------------------------------
2  --
3  -- File Name: hdlsrc/FULLADDER/Subsystem.vhd
4  -- Created: 2023-03-14 09:32:36
5  --
6  -- Generated by MATLAB 9.13 and HDL Coder 4.0
7  --
8  --
9  -- -------------------------------------------------------------
10 -- Rate and Clocking Details
11 -- -------------------------------------------------------------
12 -- Model base rate: 0
13 -- Target subsystem base rate: inf
14 --
15 -- -------------------------------------------------------------
16
17
18 -- -------------------------------------------------------------
19 --
20 -- Module: Subsystem
21 -- Source Path: FULLADDER/Subsystem
22 -- Hierarchy Level: 0
23 --
24 -- -------------------------------------------------------------
25 LIBRARY IEEE;
26 USE IEEE.std_logic_1164.ALL;
27 USE IEEE.numeric_std.ALL;
28
29 ENTITY Subsystem IS
30   PORT( A                                 :   IN    std_logic;
31         B                                 :   IN    std_logic;
32         C_in                              :   IN    std_logic;
33         SUM                               :   OUT   std_logic;
34         CARRY                             :   OUT   std_logic
35         );
36 END Subsystem;
37
38
39 ARCHITECTURE rtl OF Subsystem IS
```


Ln 44 Col 31


HDL Code
Subsystem.vhd (0)
Search
Highlighting: lines modified in last build
1 / 1
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;
ENTITY Subsystem IS
PORT(A : IN std_logic;
B : IN std_logic;
C_in : IN std_logic;
SUM : OUT std_logic;
CARRY : OUT std_logic
);
END Subsystem;
ARCHITECTURE rtl OF Subsystem IS
-- Signals
SIGNAL XOR_out1 : std_logic;
SIGNAL XOR1_out1 : std_logic;
SIGNAL AND_out1 : std_logic;
SIGNAL AND1_out1 : std_logic;
SIGNAL OR_out1 : std_logic;
BEGIN
XOR_out1 <= A XOR B;
XOR1_out1 <= XOR_out1 XOR C_in;
AND_out1 <= XOR_out1 AND C_in;
AND1_out1 <= A AND B;
OR_out1 <= AND_out1 OR AND1_out1;
SUM <= XOR1_out1;
CARRY <= OR_out1;
END rtl;
Activate Windows
Go to Settings to activate Windows.
Ln 33 Col 37