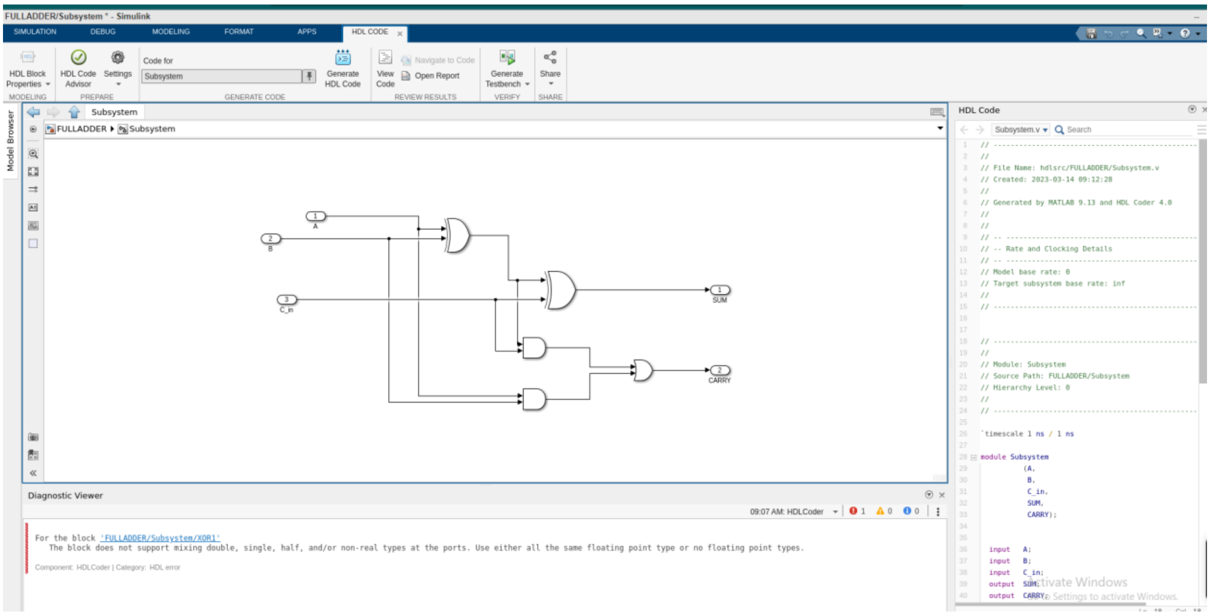
GENERATE VERILOG CODE FOR FULL ADDER.

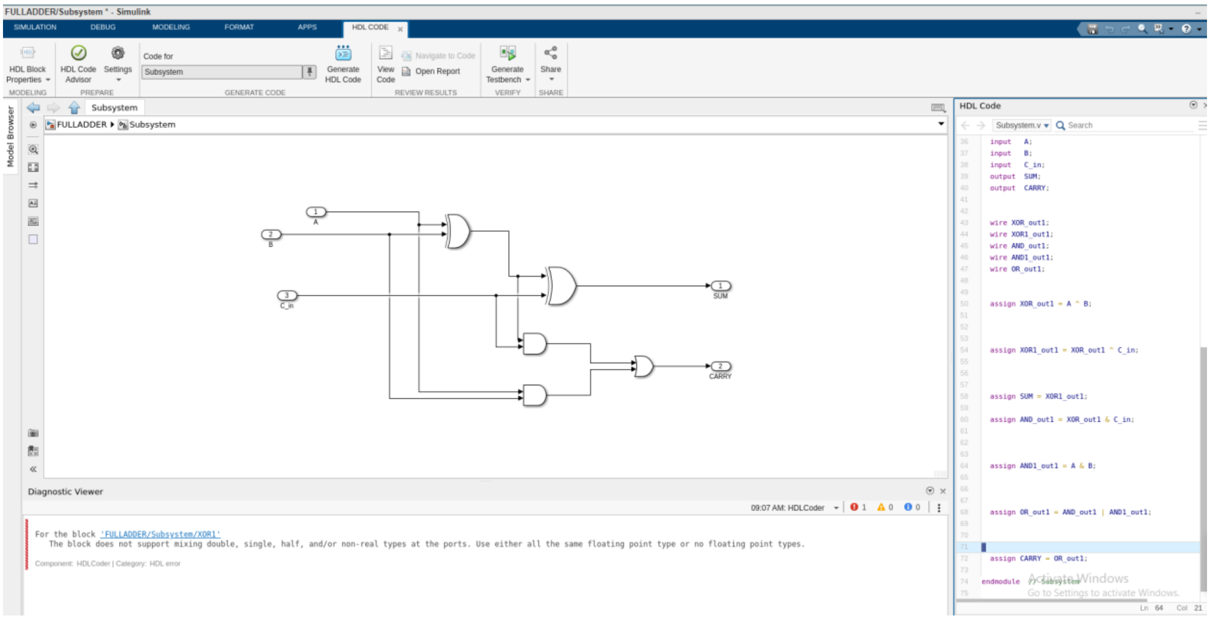
SOLUTION:-



```
For the block 'FULLADDER/Subsystem/XOR1'
  The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
```

Component: HDLCoder | Category: HDL error

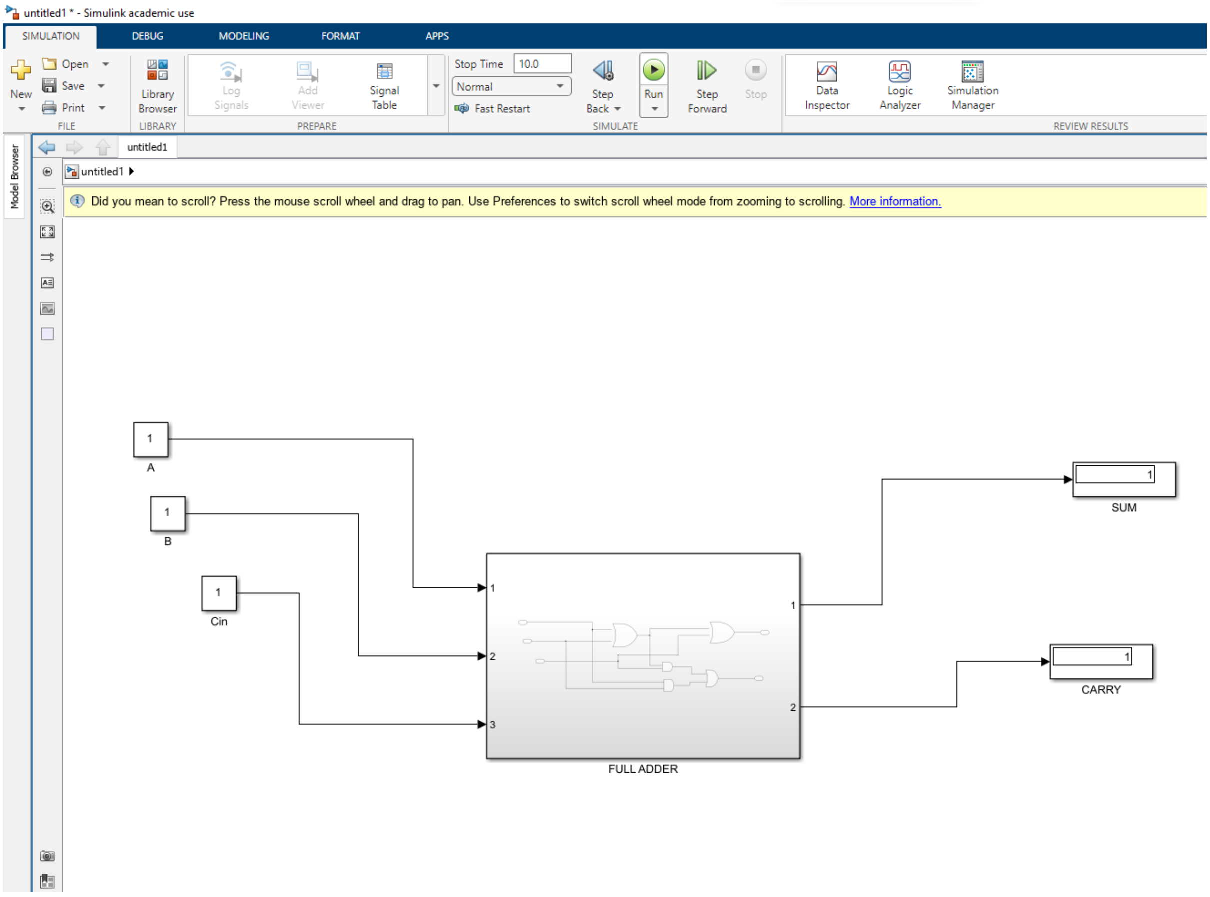
```verilog
// -------------------------------------------------------------
//
// File Name: hdlsrc/FULLADDER/Subsystem.v
// Created: 2023-03-14 09:12:28
//
// Generated by MATLAB 9.13 and HDL Coder 4.0
//
//
// -- -------------------------------------------------------------
// -- Rate and Clocking Details
// -- -------------------------------------------------------------
// Model base rate: 0
// Target subsystem base rate: inf
//
// -------------------------------------------------------------


// -------------------------------------------------------------
//
// Module: Subsystem
// Source Path: FULLADDER/Subsystem
// Hierarchy Level: 0
//
// -------------------------------------------------------------

`timescale 1 ns / 1 ns

module Subsystem
          (A,
           B,
           C_in,
           SUM,
           CARRY);


  input   A;
  input   B;
  input   C_in;
  output  SUM;
  output  CARRY;
```



```
For the block 'FULLADDER/Subsystem/XOR1'
  The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
```

Component: HDLCoder | Category: HDL error

```verilog
  input   A;
  input   B;
  input   C_in;
  output  SUM;
  output  CARRY;


  wire XOR_out1;
  wire XOR1_out1;
  wire AND_out1;
  wire AND1_out1;
  wire OR_out1;


  assign XOR_out1 = A ^ B;



  assign XOR1_out1 = XOR_out1 ^ C_in;



  assign SUM = XOR1_out1;

  assign AND_out1 = XOR_out1 & C_in;



  assign AND1_out1 = A & B;



  assign OR_out1 = AND_out1 | AND1_out1;



  assign CARRY = OR_out1;

endmodule  // Subsystem
```



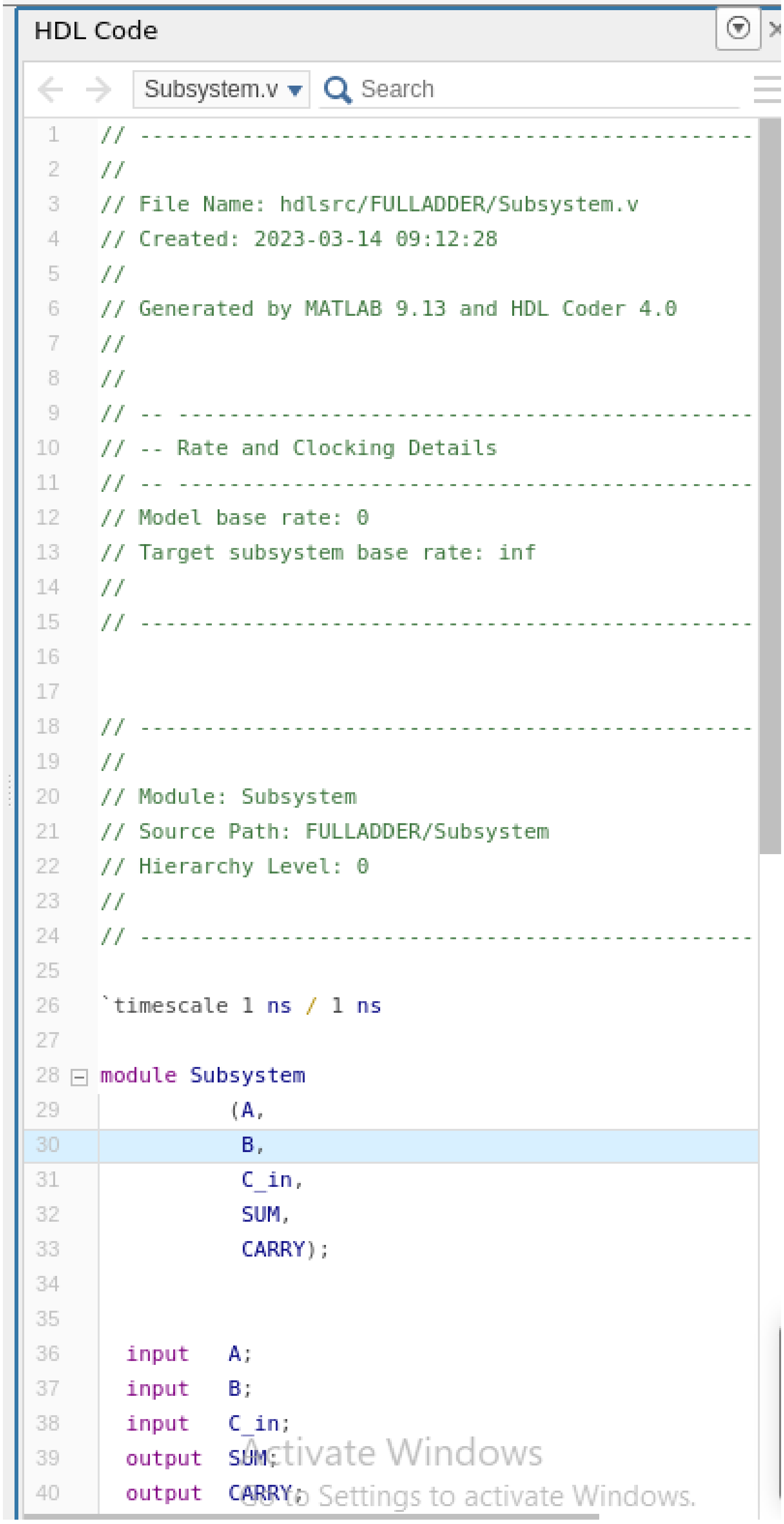
Did you mean to scroll? Press the mouse scroll wheel and drag to pan. Use Preferences to switch scroll wheel mode from zooming to scrolling. More information.

→VERILOG CODE GENERATED BY HDL CODER:-

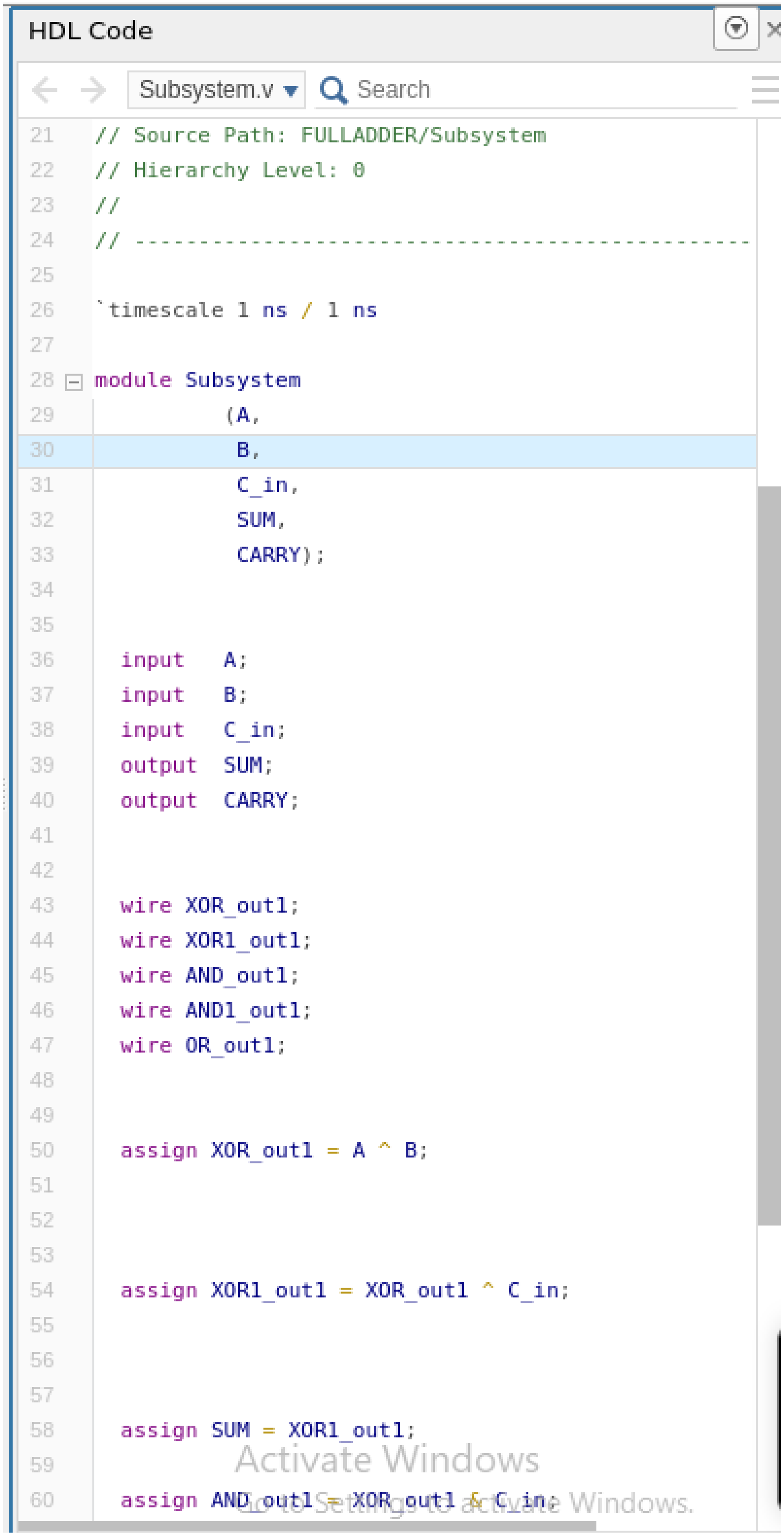
```
// File Name: hdlsrc/FULLADDER/Subsystem.v

// Created: 2023-03-14 09:12:28

//

// Generated by MATLAB 9.13 and HDL Coder 4.0

//

//

// -- -------------------------------------------------------------

// -- Rate and Clocking Details

// -- -------------------------------------------------------------

// Model base rate: 0

// Target subsystem base rate: inf

//

// -------------------------------------------------------------

// -------------------------------------------------------------
```

```
//
// Module: Subsystem
// Source Path: FULLADDER/Subsystem
// Hierarchy Level: 0
//
// ------------------------------------------------------------

`timescale 1 ns / 1 ns
module Subsystem
          (A,
           B,
           C_in,
           SUM,
           CARRY);
  input   A;
  input   B;
  input   C_in;
  output  SUM;
  output  CARRY;
  wire XOR_out1;
  wire XOR1_out1;
  wire AND_out1;
  wire AND1_out1;
  wire OR_out1;
  assign XOR_out1 = A ^ B;
  assign XOR1_out1 = XOR_out1 ^ C_in;
  assign SUM = XOR1_out1;
  assign AND_out1 = XOR_out1 & C_in;
  assign AND1_out1 = A & B;
  assign OR_out1 = AND_out1 | AND1_out1;
  assign CARRY = OR_out1;
```

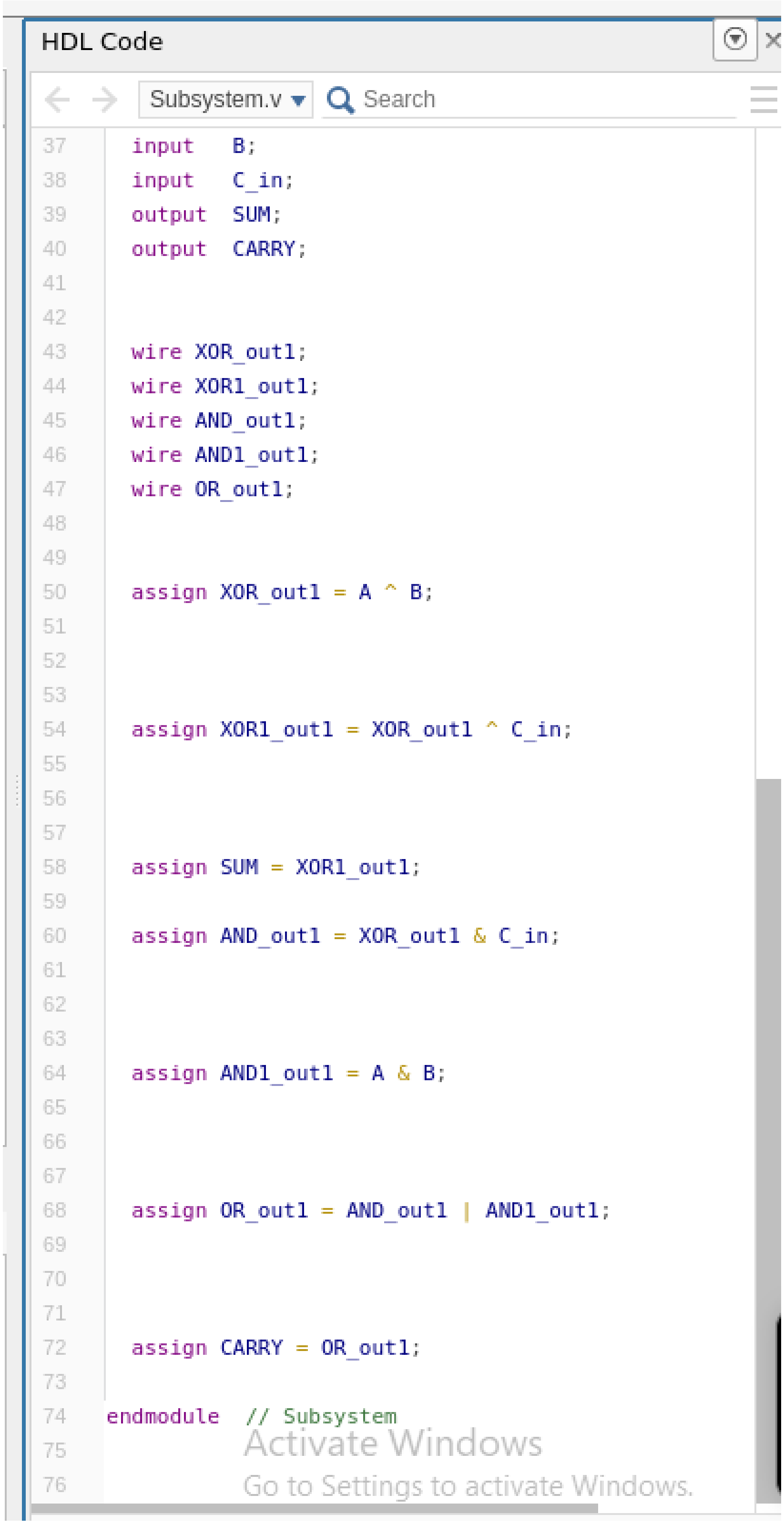
```
endmodule  // Subsystem
```



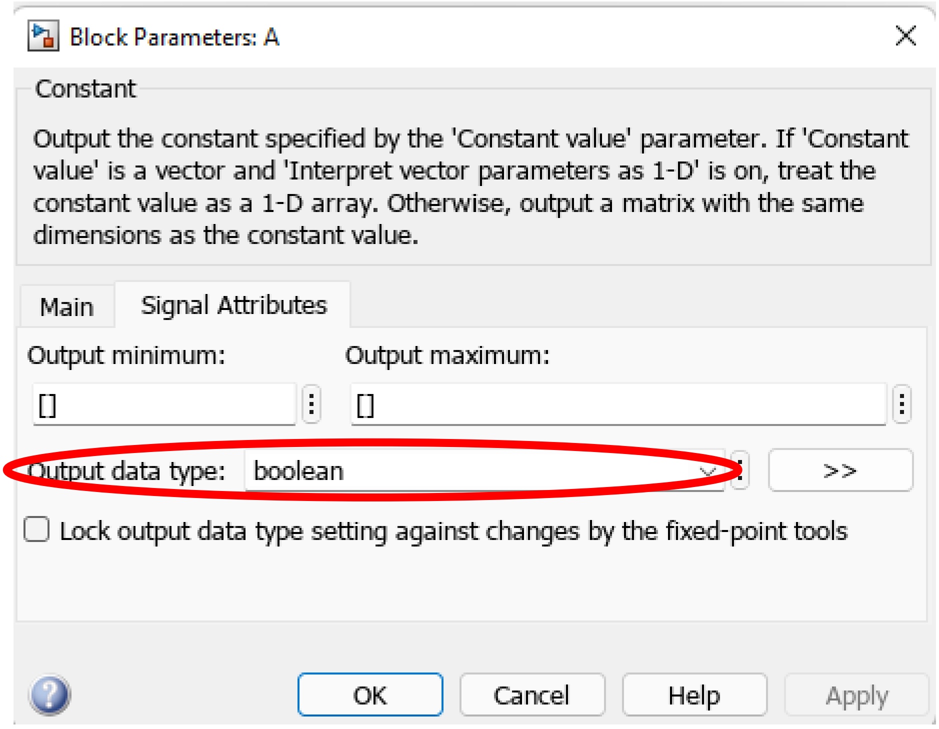
```
// ------------------------------------------------
//
// File Name: hdlsrc/FULLADDER/Subsystem.v
// Created: 2023-03-14 09:12:28
//
// Generated by MATLAB 9.13 and HDL Coder 4.0
//
//
// -- ---------------------------------------------
// -- Rate and Clocking Details
// -- ---------------------------------------------
// Model base rate: 0
// Target subsystem base rate: inf
//
// ------------------------------------------------


// ------------------------------------------------
//
// Module: Subsystem
// Source Path: FULLADDER/Subsystem
// Hierarchy Level: 0
//
// ------------------------------------------------

`timescale 1 ns / 1 ns

module Subsystem
          (A,
           B,
           C_in,
           SUM,
           CARRY);


  input   A;
  input   B;
  input   C_in;
  output  SUM;
  output  CARRY;
```



```verilog
// Source Path: FULLADDER/Subsystem
// Hierarchy Level: 0
//
// -------------------------------------------------

`timescale 1 ns / 1 ns

module Subsystem
          (A,
           B,
           C_in,
           SUM,
           CARRY);


  input   A;
  input   B;
  input   C_in;
  output  SUM;
  output  CARRY;


  wire XOR_out1;
  wire XOR1_out1;
  wire AND_out1;
  wire AND1_out1;
  wire OR_out1;


  assign XOR_out1 = A ^ B;



  assign XOR1_out1 = XOR_out1 ^ C_in;



  assign SUM = XOR1_out1;

  assign AND_out1 = XOR_out1 & C_in;
```



```verilog
  input   B;
  input   C_in;
  output  SUM;
  output  CARRY;


  wire XOR_out1;
  wire XOR1_out1;
  wire AND_out1;
  wire AND1_out1;
  wire OR_out1;


  assign XOR_out1 = A ^ B;



  assign XOR1_out1 = XOR_out1 ^ C_in;



  assign SUM = XOR1_out1;

  assign AND_out1 = XOR_out1 & C_in;



  assign AND1_out1 = A & B;



  assign OR_out1 = AND_out1 | AND1_out1;



  assign CARRY = OR_out1;

endmodule  // Subsystem
```



Block Parameters: A

Constant

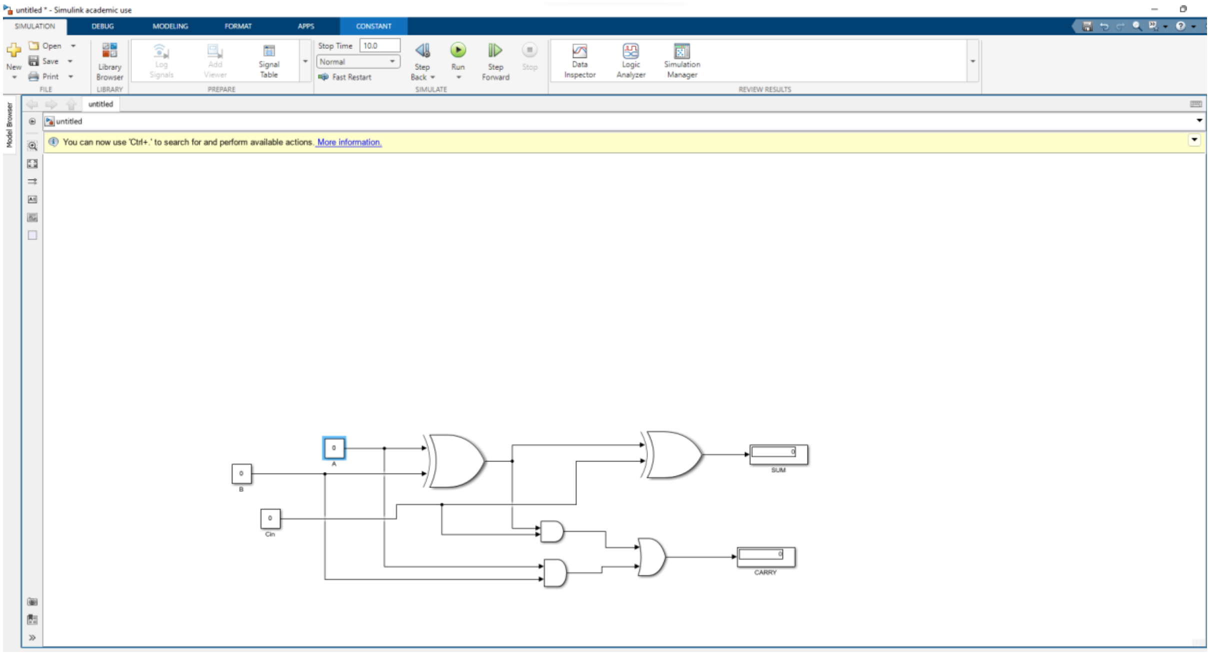
Output the constant specified by the 'Constant value' parameter. If 'Constant value' is a vector and 'Interpret vector parameters as 1-D' is on, treat the constant value as a 1-D array. Otherwise, output a matrix with the same dimensions as the constant value.

Output minimum: []

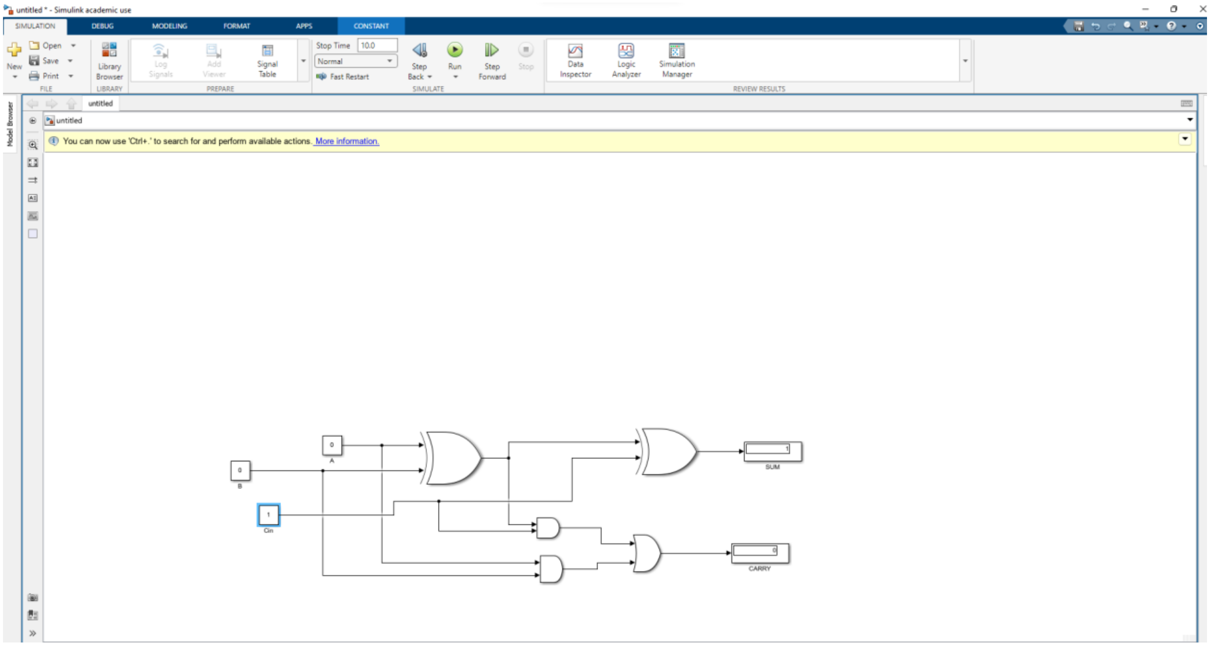
Output maximum: []

Output data type: boolean

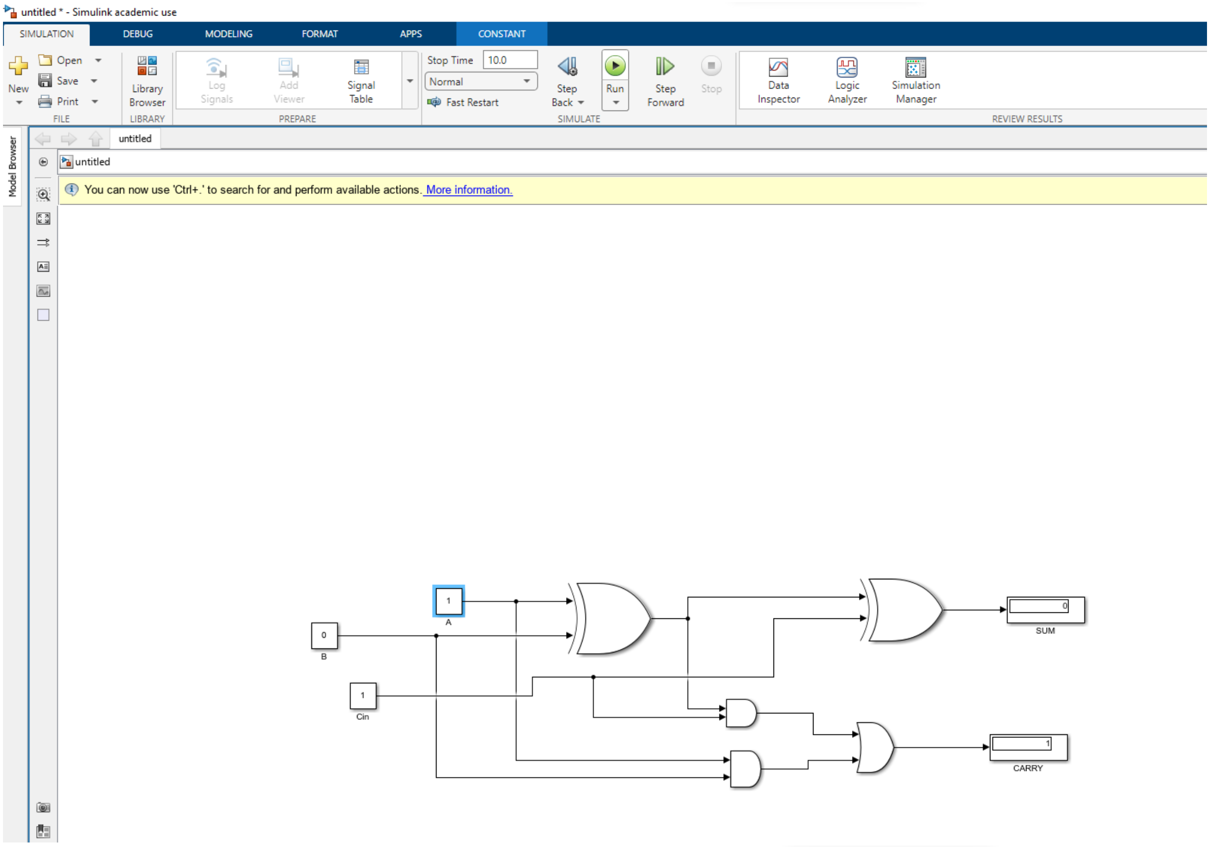
□ Lock output data type setting against changes by the fixed-point tools


untitled * - Simulink academic use

You can now use 'Ctrl+.' to search for and perform available actions. More information.


untitled * - Simulink academic use

You can now use 'Ctrl+.' to search for and perform available actions. More information.

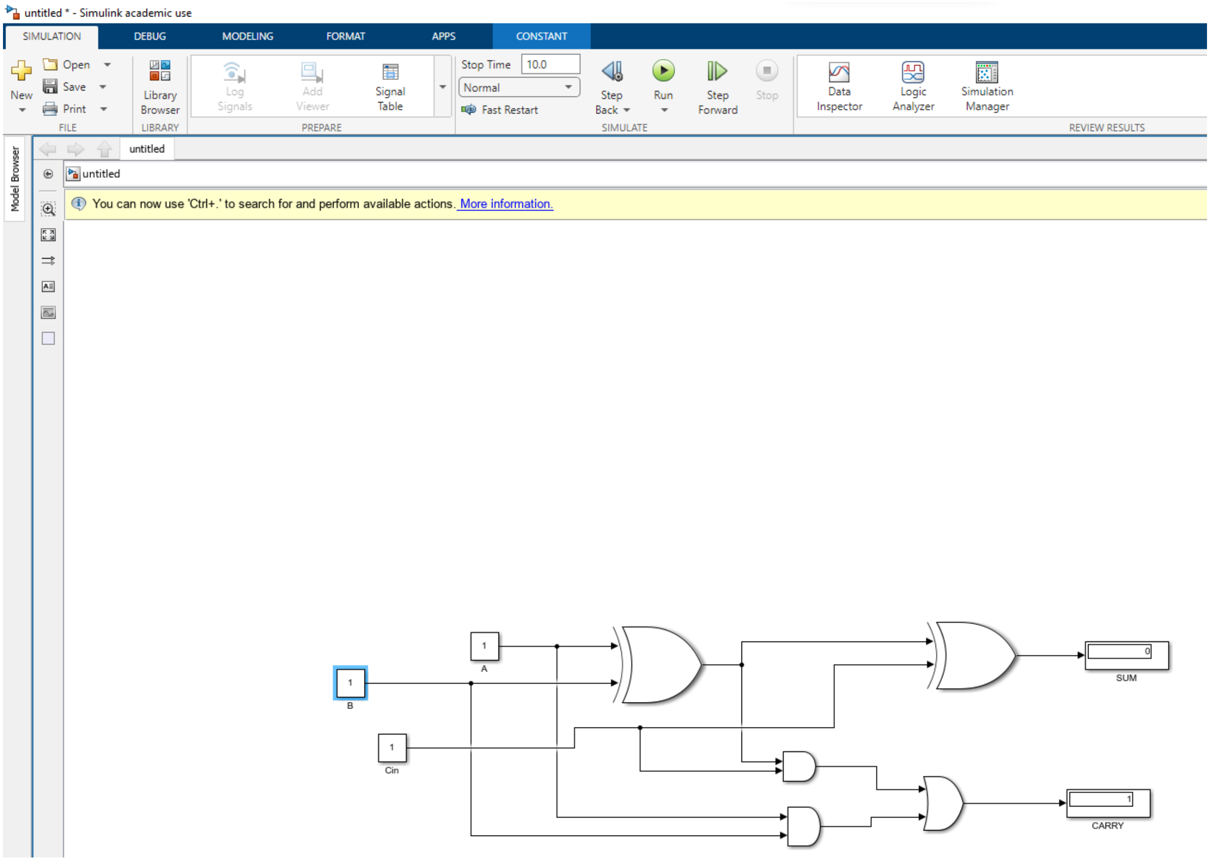


untitled * - Simulink academic use

Stop Time 10.0

Normal

You can now use 'Ctrl+.' to search for and perform available actions. More information.



untitled * - Simulink academic use

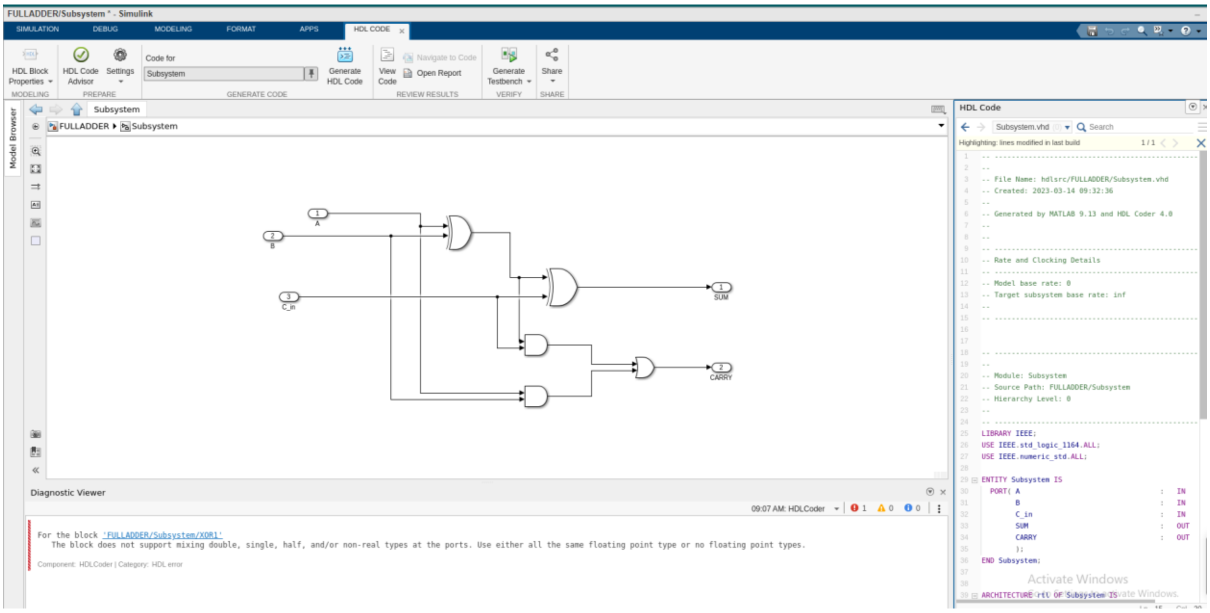
Stop Time 10.0

Normal

You can now use 'Ctrl+.' to search for and perform available actions. More information.

. Generate VHDL code for Fulladder.

Solution:-



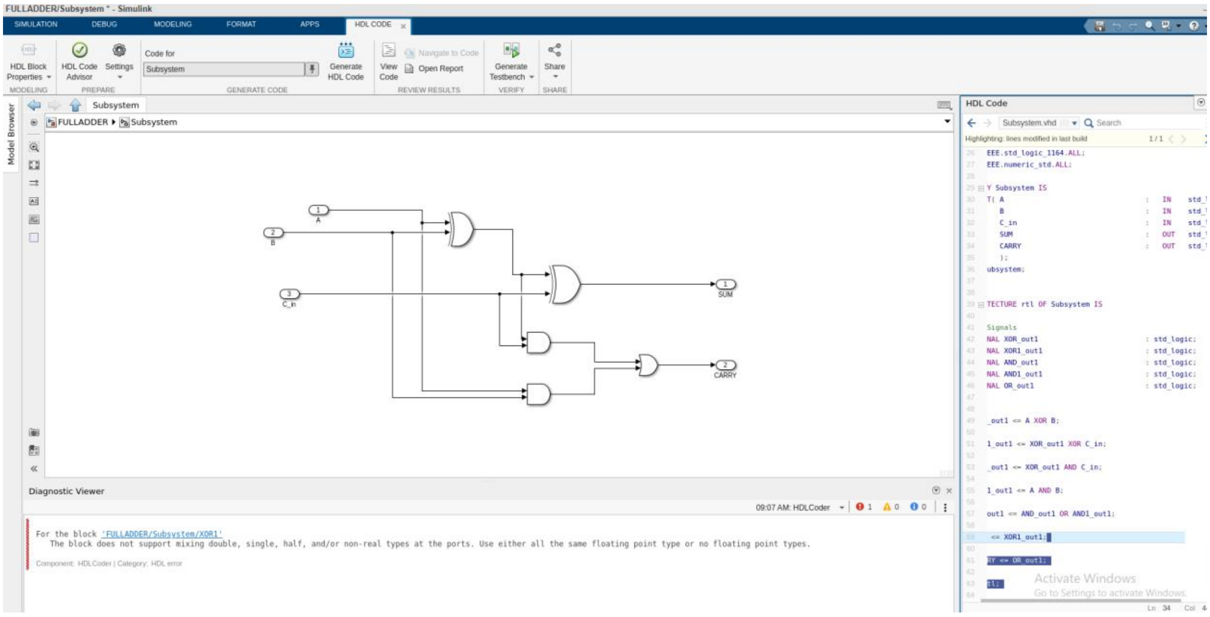
```
-- -------------------------------------------------------------
--
-- File Name: hdlsrc/FULLADDER/Subsystem.vhd
-- Created: 2023-03-14 09:32:36
--
-- Generated by MATLAB 9.13 and HDL Coder 4.0
--
--
-- -------------------------------------------------------------
-- Rate and Clocking Details
-- -------------------------------------------------------------
-- Model base rate: 0
-- Target subsystem base rate: inf
--
-- -------------------------------------------------------------


-- -------------------------------------------------------------
--
-- Module: Subsystem
-- Source Path: FULLADDER/Subsystem
-- Hierarchy Level: 0
--
-- -------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

ENTITY Subsystem IS
  PORT( A                              :   IN
        B                              :   IN
        C_in                           :   IN
        SUM                            :   OUT
        CARRY                          :   OUT
        );
END Subsystem;


ARCHITECTURE rtl OF Subsystem IS
```

Diagnostic Viewer

09:07 AM: HDLCoder

```
For the block 'FULLADDER/Subsystem/XOR1'
   The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
```

Component: HDLCoder | Category: HDL error



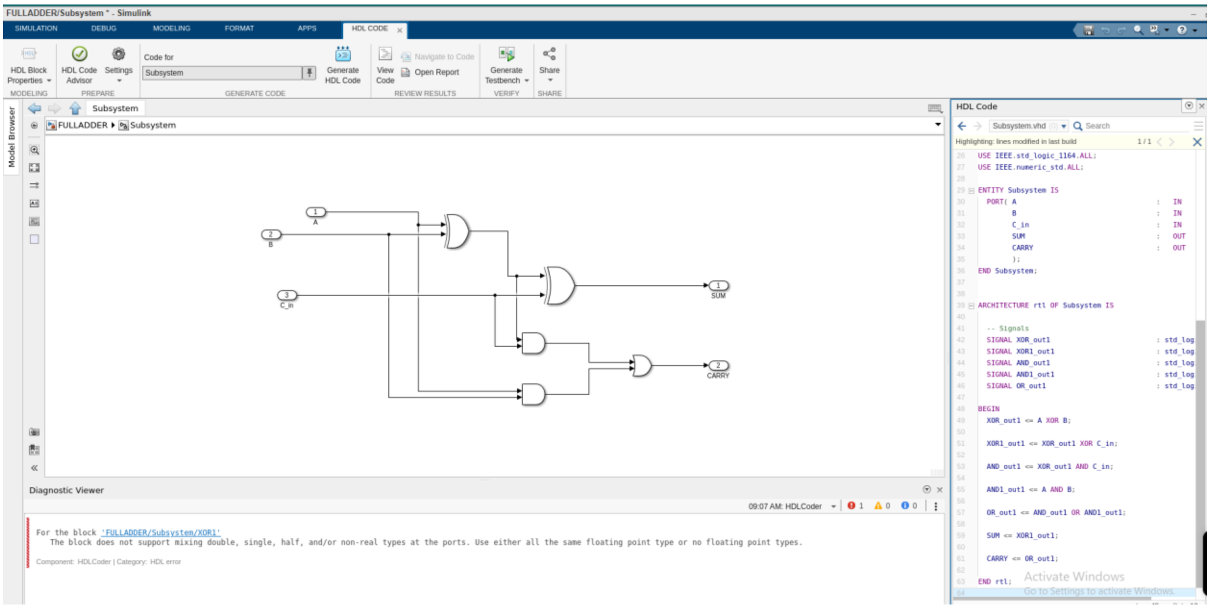
```
EEE.std_logic_1164.ALL;
EEE.numeric_std.ALL;

Y Subsystem IS
T( A                              :   IN    std_
   B                              :   IN    std_
   C_in                           :   IN    std_
   SUM                            :   OUT   std_
   CARRY                          :   OUT   std_
   );
ubsystem;


TECTURE rtl OF Subsystem IS

Signals
NAL XOR_out1                          : std_logic;
NAL XOR1_out1                         : std_logic;
NAL AND_out1                          : std_logic;
NAL AND1_out1                         : std_logic;
NAL OR_out1                           : std_logic;


_out1 <= A XOR B;

1_out1 <= XOR_out1 XOR C_in;

_out1 <= XOR_out1 AND C_in;

1_out1 <= A AND B;

out1 <= AND_out1 OR AND1_out1;

 <= XOR1_out1;

RY <= OR_out1;

tl;
```

Diagnostic Viewer

09:07 AM: HDLCoder

```
For the block 'FULLADDER/Subsystem/XOR1'
   The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
```

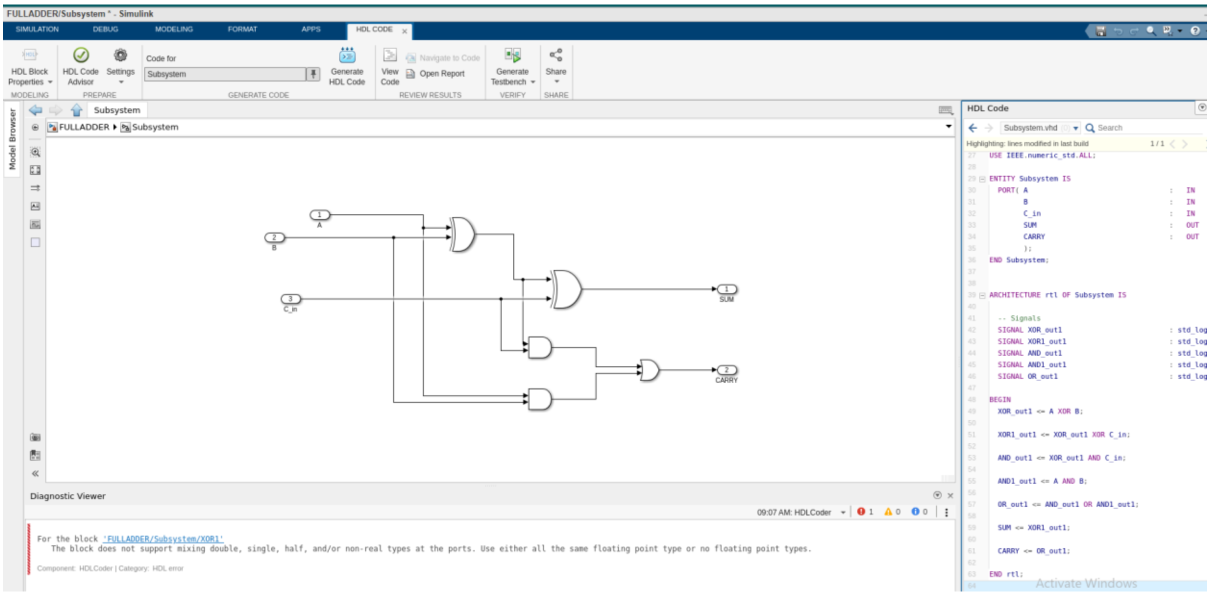
Component: HDLCoder | Category: HDL error



```
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

ENTITY Subsystem IS
  PORT( A                                 :   IN
        B                                 :   IN
        C_in                              :   IN
        SUM                               :   OUT
        CARRY                             :   OUT
        );
END Subsystem;


ARCHITECTURE rtl OF Subsystem IS

  -- Signals
  SIGNAL XOR_out1                         : std_log
  SIGNAL XOR1_out1                        : std_log
  SIGNAL AND_out1                         : std_log
  SIGNAL AND1_out1                        : std_log
  SIGNAL OR_out1                          : std_log

BEGIN
  XOR_out1 <= A XOR B;

  XOR1_out1 <= XOR_out1 XOR C_in;

  AND_out1 <= XOR_out1 AND C_in;

  AND1_out1 <= A AND B;

  OR_out1 <= AND_out1 OR AND1_out1;

  SUM <= XOR1_out1;

  CARRY <= OR_out1;

END rtl;
```

```
For the block 'FULLADDER/Subsystem/XOR1'
   The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
```

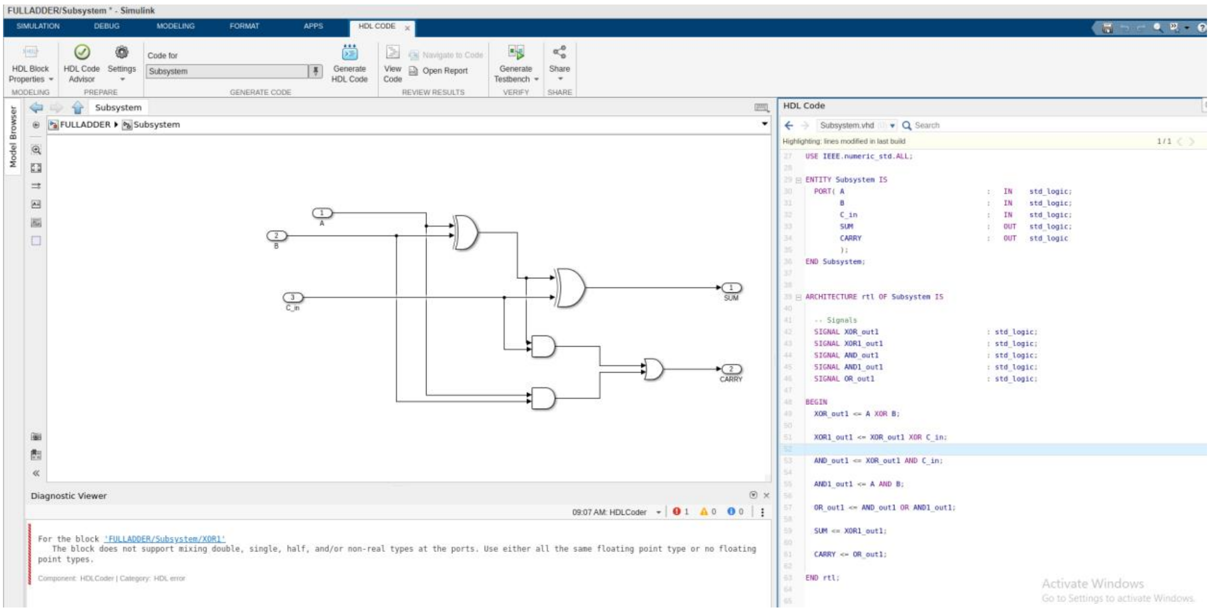
Component: HDLCoder | Category: HDL error



```
USE IEEE.numeric_std.ALL;

ENTITY Subsystem IS
  PORT( A                                 :   IN
        B                                 :   IN
        C_in                              :   IN
        SUM                               :   OUT
        CARRY                             :   OUT
        );
END Subsystem;


ARCHITECTURE rtl OF Subsystem IS

  -- Signals
  SIGNAL XOR_out1                         : std_log
  SIGNAL XOR1_out1                        : std_log
  SIGNAL AND_out1                         : std_log
  SIGNAL AND1_out1                        : std_log
  SIGNAL OR_out1                          : std_log

BEGIN
  XOR_out1 <= A XOR B;

  XOR1_out1 <= XOR_out1 XOR C_in;

  AND_out1 <= XOR_out1 AND C_in;

  AND1_out1 <= A AND B;

  OR_out1 <= AND_out1 OR AND1_out1;

  SUM <= XOR1_out1;

  CARRY <= OR_out1;

END rtl;
```

```
For the block 'FULLADDER/Subsystem/XOR1'
   The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
```

Component: HDLCoder | Category: HDL error



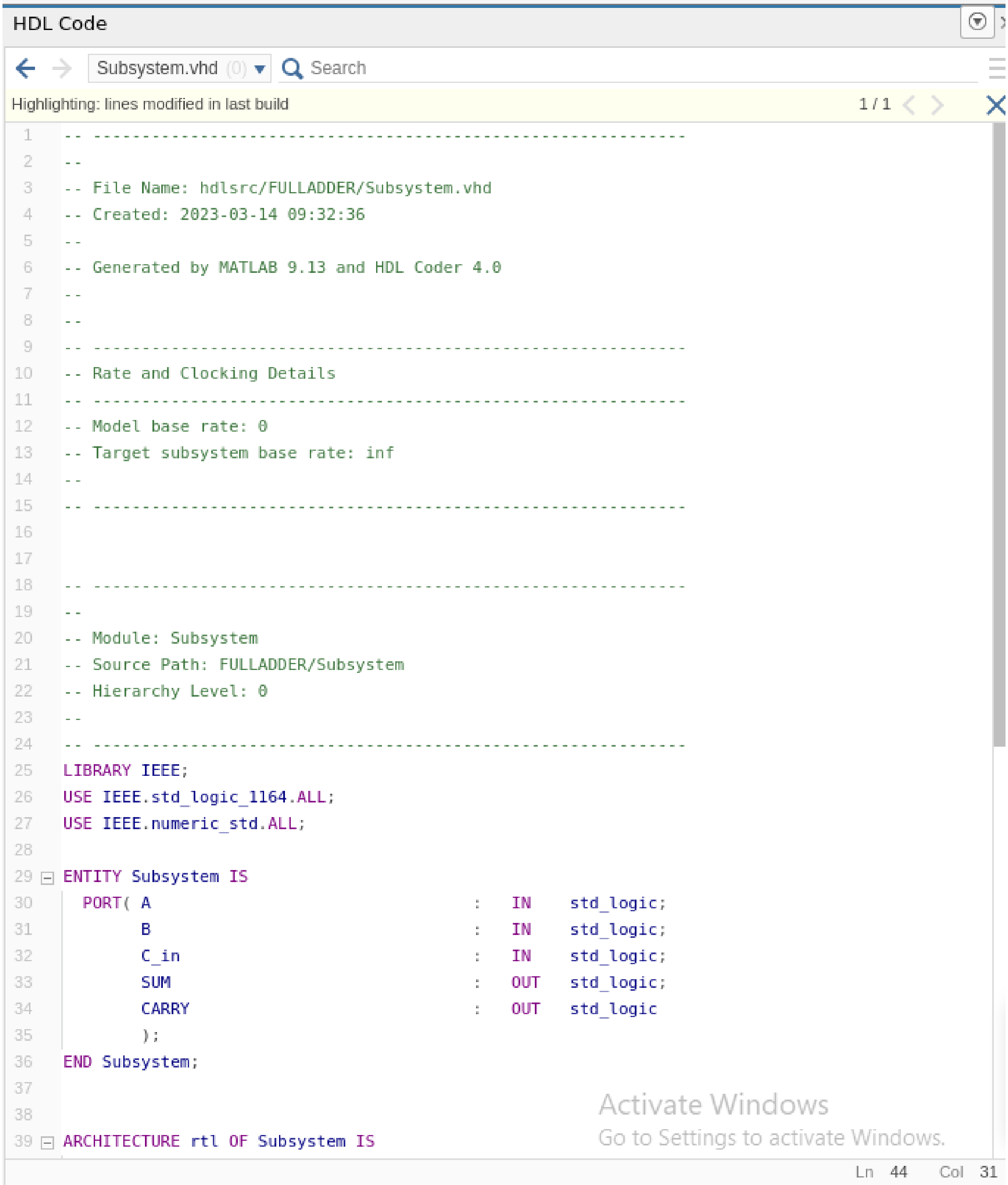
```
USE IEEE.numeric_std.ALL;

ENTITY Subsystem IS
  PORT( A                                 :   IN    std_logic;
        B                                 :   IN    std_logic;
        C_in                              :   IN    std_logic;
        SUM                               :   OUT   std_logic;
        CARRY                             :   OUT   std_logic
        );
END Subsystem;


ARCHITECTURE rtl OF Subsystem IS

  -- Signals
  SIGNAL XOR_out1                         : std_logic;
  SIGNAL XOR1_out1                        : std_logic;
  SIGNAL AND_out1                         : std_logic;
  SIGNAL AND1_out1                        : std_logic;
  SIGNAL OR_out1                          : std_logic;

BEGIN
  XOR_out1 <= A XOR B;

  XOR1_out1 <= XOR_out1 XOR C_in;

  AND_out1 <= XOR_out1 AND C_in;

  AND1_out1 <= A AND B;

  OR_out1 <= AND_out1 OR AND1_out1;

  SUM <= XOR1_out1;

  CARRY <= OR_out1;

END rtl;
```

```
For the block 'FULLADDER/Subsystem/XOR1'
   The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating
point types.
```

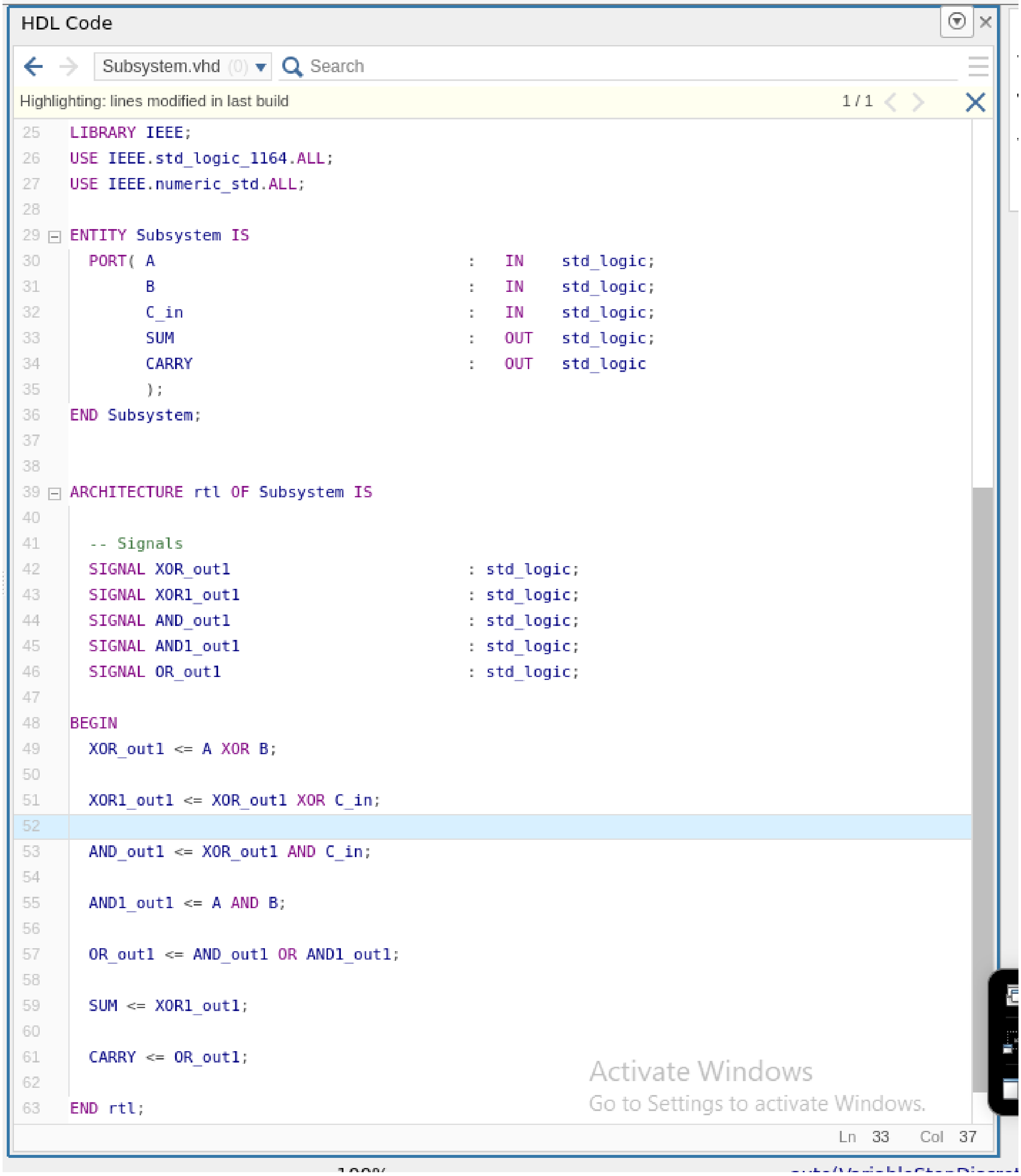
Component: HDLCoder | Category: HDL error

→VHDL CODE GENERATED BY HDL CODER OF MATLAB SIMULINK:-

```
-- -------------------------------------------------------------
--
-- File Name: hdlsrc/FULLADDER/Subsystem.vhd
-- Created: 2023-03-14 09:32:36
--
-- Generated by MATLAB 9.13 and HDL Coder 4.0
--
--
-- -------------------------------------------------------------
-- Rate and Clocking Details
-- -------------------------------------------------------------
-- Model base rate: 0
-- Target subsystem base rate: inf
--
-- -------------------------------------------------------------
-- -------------------------------------------------------------
--
-- Module: Subsystem
-- Source Path: FULLADDER/Subsystem
-- Hierarchy Level: 0
--
-- -------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

ENTITY Subsystem IS
  PORT( A                                 :   IN    std_logic;
        B                                 :   IN    std_logic;
        C_in                              :   IN    std_logic;
        SUM                               :   OUT   std_logic;
        CARRY                             :   OUT   std_logic
        );
END Subsystem;


ARCHITECTURE rtl OF Subsystem IS

  -- Signals
  SIGNAL XOR_out1                         : std_logic;
  SIGNAL XOR1_out1                        : std_logic;
  SIGNAL AND_out1                         : std_logic;
  SIGNAL AND1_out1                        : std_logic;
  SIGNAL OR_out1                          : std_logic;
BEGIN
  XOR_out1 <= A XOR B;
  XOR1_out1 <= XOR_out1 XOR C_in;
  AND_out1 <= XOR_out1 AND C_in;
  AND1_out1 <= A AND B;
  OR_out1 <= AND_out1 OR AND1_out1;
  SUM <= XOR1_out1;
  CARRY <= OR_out1;
END rtl;
```



```
-- -------------------------------------------------------------
--
-- File Name: hdlsrc/FULLADDER/Subsystem.vhd
-- Created: 2023-03-14 09:32:36
--
-- Generated by MATLAB 9.13 and HDL Coder 4.0
--
--
-- -------------------------------------------------------------
-- Rate and Clocking Details
-- -------------------------------------------------------------
-- Model base rate: 0
-- Target subsystem base rate: inf
--
-- -------------------------------------------------------------


-- -------------------------------------------------------------
--
-- Module: Subsystem
-- Source Path: FULLADDER/Subsystem
-- Hierarchy Level: 0
--
-- -------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

ENTITY Subsystem IS
  PORT( A                               :   IN    std_logic;
        B                               :   IN    std_logic;
        C_in                            :   IN    std_logic;
        SUM                             :   OUT   std_logic;
        CARRY                           :   OUT   std_logic
        );
END Subsystem;


ARCHITECTURE rtl OF Subsystem IS
```



Highlighting: lines modified in last build

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

ENTITY Subsystem IS
  PORT( A                                 :   IN    std_logic;
        B                                 :   IN    std_logic;
        C_in                              :   IN    std_logic;
        SUM                               :   OUT   std_logic;
        CARRY                             :   OUT   std_logic
        );
END Subsystem;


ARCHITECTURE rtl OF Subsystem IS

  -- Signals
  SIGNAL XOR_out1                         : std_logic;
  SIGNAL XOR1_out1                        : std_logic;
  SIGNAL AND_out1                         : std_logic;
  SIGNAL AND1_out1                        : std_logic;
  SIGNAL OR_out1                          : std_logic;

BEGIN
  XOR_out1 <= A XOR B;

  XOR1_out1 <= XOR_out1 XOR C_in;

  AND_out1 <= XOR_out1 AND C_in;

  AND1_out1 <= A AND B;

  OR_out1 <= AND_out1 OR AND1_out1;

  SUM <= XOR1_out1;

  CARRY <= OR_out1;

END rtl;
```