Specification of FC8080

Terrestrial Digital Multimedia Broadcast
RF tuner & Demodulator

Data Sheet
Preliminary
Ver. 0.95

Confidential

Contents

Revision History

Version	Date	Modifications
Ver. 0.5	2013. 02. 25	Preliminary initial release
Ver. 0.6	2013. 03. 04	Package pin name, application circuit revision
Ver. 0.7	2013. 03. 13	POD information revision
Ver. 0.8	2013. 03. 22	AMR table, ESD test result added
Ver. 0.9	2013. 04. 06	QFN pin map revision
		WLCSP pin map revision
Ver. 0.95	2013. 04 .23	Performance update, Pin description update

1. Overview

1.1. Introduction

The FCI FC8080 chip is a highly integrated device for terrestrial digital multimedia Broadcasting. FC8080 has all of the performance needed to enable the full range of T-DMB application. It consists of two main blocks, RF tuner and channel decoder.

RF block supports single-band (Band-III). It is a highly integrated component working with a single 1.2V power supply. Because direct-conversion architecture is used in RF block, additional components such as bulky IF SAW filter and other IF matching components are no longer required. For the direct-conversion, it has low noise fractional-N type frequency synthesizer and VCO. RF block contains LNA, down-conversion mixer, channel selection filter (CSF), and LO distribution network for Band-3.

Baseband block is a integrated circuit provides channel decoder for Digital Multimedia Broadcasting(DMB) signals based on ETS 300 401 (EUREKA-147). It is also in compliance with the function of Korea DAB/DMB (TTAS.KO -07.0024 and TTAS.KO-07.0026) standard. It contains 10-bit Analog to Digital Converter (ADC) for IF input, OFDM demodulator, Reed Solomon decoder and convolutional de-interleaver for providing forward error correcting. For Audio data, It uses MPEG I/II Layer II (MUSICAM) algorithm. It provides EBI2 LCD Interface of Qualcomm QSC series modem chip, SPI and I2C as a HOST interface. When it is used I2C as host interface, serial TS interface is supported for data transmission also.

1.2. Features

- Highly integrated digital device for DAB receiver (Eureka 147)
- Korea DAB/DMB (TTAS.KO -07.0024 and TTAS.KO-07.0026) standard compliant
- DAB OFDM channel demodulator and decoder
  - Fully integrated, supports all DAB functions and modes (I, II, III and IV)
  - Automatic Mode Detection (AMD)
  - Full data rate of 1.8Mbit can be decoded
  - Automatic frame and time synchronization and fast channel re-acquisition
  - Digital AGC with a wide gain control range
  - Demodulation and decoding of up to 64 sub-channels (UEP/EEP)
  - TII decoder
  - Automatic multiplex re-configuration
- Integrated high-density SRAM supporting time and frequency de-interleaving
  - Simple memory concept. Do not require external memory for DAB operation
- Interfaces
  - Parallel Host Interface
    - ✓ 3-bit control pins, 4-bit data bus, it is compatible with Qualcomm QSC series modem chip.
  - Serial Host Interface
    - ✓ SPI : up to 38.4MHz
    - ✓ I2C : up to 1.0MHz for control and up to 38.4MHz serial TS interface for data
  - Support max. 4 services (audio, video and data stream) of Data service
  - MPEG-2 Serial-TS output
    - ✓ Various TS clock : 1.024 ~ 38.4MHz
  - Be able to decode 2 video data with RS encoded stream
  - Automatically internal hardware reset drive without external reset pin
- Electrical Characteristics
  - Embedded LDO for Power
  - Supply voltages : 1.2V for core and 1.8/2.5/3.3V for I/O
  - Low Power consumption : 20 mA typical @core 1.2V
  - Various power consumption management devices for this application
  - Zero IF support
  - Support various external clock 16.384/19.2/24/24.576/27/27.12/38.4-MHz
  - Band Frequency
    - ✓ Band-III : 170 ~ 215 MHz

- Sensitivity : -104.5 dBm
  - ✓ Noise Figure : 2.7 dB
  - ✓ Adjacent Channel Sensitivity : 50 dB typical
  - ✓ Far Off Sensitivity : 55 dB typical

❑ Physical Characteristics

- 25 Pin WLCSP package with 2.14x2.09 mm^2
- 32 Pin QFN package with 4x4 mm^2

1.3. Block Diagram

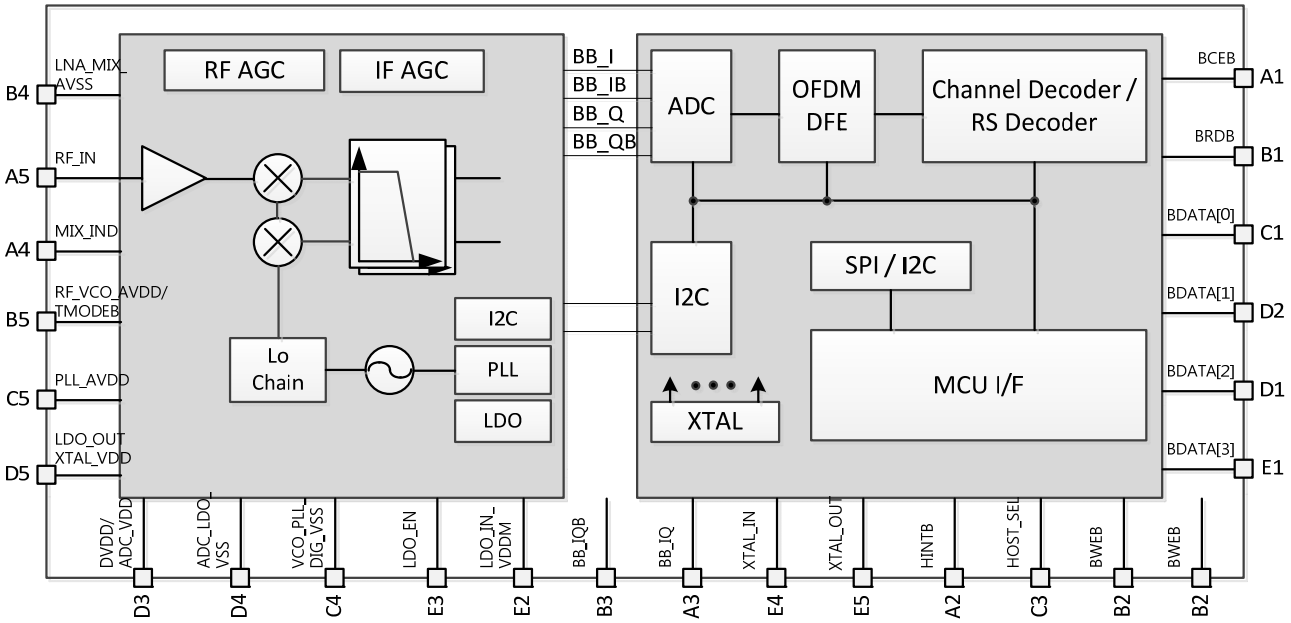

Figure 1. FC8080 Block Diagram

1.4. RF Tuner

RF tuner has a direct-conversion structure that converts Band-3 signal around DC frequency. RF AGC and MIX AGC are controlled by the on-chip demodulator, and they regulate signal level to a proper value for the internal tuner blocks. The on-chip demodulator controls the gain of the PGA (Programmable Gain Amplifier), and PGA supply uniform signal to ADC as a result. A low noise fractional-N type frequency synthesizer and a VCO are integrated for generating LO(Local Oscillator) signal to direct-conversion.

1.5. Functional Description

1.5.1. Frame Synchronization and Mode Detection

Frame synchronization could get the start position of a frame and transmission mode by calculating the energy range of the sampling data.

1.5.2. Automatic Gain Control (AGC)

AGC should preserve the amplitude of received signal to uniformity automatically.
It is affected to control the level of Viterbi soft decision signal.

1.5.3. Fast Fourier Transform (FFT)

FFF transform time signal of sub-carrier to frequency signal according to DMB transmission mode.

1.5.4. QPSK Demodulator

QPSK demodulator includes differential demodulation, QPSK de-mapping and frequency de-interleaving function, etc.

1.5.5. Time de-interleaver / de-puncture

Time de-interleaver is capable of decoding 4 channels simultaneously. Also it can process independent of channel size with adapting effective de-interleaving technique. It satisfies Eureka-147 specification.

1.5.6. Viterbi Decoder/Inverse Energy Disposal Scrambler

Viterbi decoder should decode convolutional code that is adequate to mobile channel receiver. It uses Maximum Likelihood Sequence Estimation. It is capable of decoding channel that is RCPC code of 1/4 to 8/9 variable code rate.

1.5.7. Convolutional De-interleaver

The function of Convolutional De-Interleaver is to transform burst error to random error. It

should detect sync byte of 204 bytes RS frame.

1.5.8. RS Decoder

RS decoder should adapt (204, 188) shorten RS specification. It is capable of 8 byte error correction of 204 bytes.

1.5.9. Clock Generator

The DMB Baseband Chip operates using internal clocks generated from various external clock source like as 16.384/19.2/24/24.576/27/27.12/38.4MHz oscillator.