AP8224C2 Data Sheet

high performance 32 Bit audio applications processor

Version

Date	version	description
2018/2/12	V0.1	First Edition
2018/2/22	V0.2	Change the pin order
2018/2/26	V0.21	Recommended chip from the maximum power input 5.5V Reduce to 5V
2018/3/15	V0.22	Power test conditions explain part of the increase
2018/5/3	V0.23	Remove doc Errors in the header information

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1. Outline

Kernel and storage

➢ high performance 32 Place RISC Core, the highest frequency 240MHz ,
stand by DSP Instruction, integration FPU Support for floating-point operations

➢ FFT Accelerator: maximum support 1024 Point complex FFT / IFFT
Operation, or 2048 The real point FFT / IFFT Operation

➢ integrated 224KB SRAM (Including 4KB TCM), 32KB
(I-Cache), 32KB (D-Cache)

➢ Internal 16Mbit SPI FLASH Storing code and data

➢ Internal EFUSE Configuration Memory

➢ 2 line SDP (Serial Debug Port) Debug port, have broken
Point debugging and code tracing capability

➢ 40 Interrupt vectors

➢ 4 Interrupt priority level

Audio frequency

➢ 3 road Audio-ADC , SNR≥94dB

➢ ADC Sample rate support 8kHz / 11.0125kHz / 12kHz /
16kHz / 22.025kHz / 24kHz / 32kHz / 44.1kHz / 48kHz

➢ Maximum support 1 Analog microphone, microphone with simulation AGC
(AGC) function

➢ Maximum support 4 Digital microphone

➢ 3 road DAC , SNR≥105dB

➢ DAC Sample rate support 8kHz / 11.0125kHz / 12kHz /
16kHz / 22.025kHz / 24kHz / 32kHz / 44.1kHz / 48kHz

➢ Support Direct Drive 16Ω or 32Ω Headphone maximum output power
40mW

➢ 1 More S / PDIF Interface supports receive or send (semi-double
Workers), support HDMI Audio and ARC

Power, clock and reset

➢ DC 3.3V ~ 5V Power supply @ LDOIN

➢ Built-in (5V turn 3.3V , 3.3V turn 1.2V) LDO Chip
powered by

➢ RC 12MHz And clock source PLL PLL clock source

➢ stand by 12 ~ 40MHz Crystal or external clock
(≤40MHz) Direct input @ GPIO_B4

➢ Support crystal-free run

➢ Internal POR (Power on Reset), LVD (low voltage
Detection) and Watchdog

➢ A variety of low-power modes:

- CPU Down
- System down
- Dormancy
- Deep Sleep

Peripherals

➢ 4 Basic timer (TIM1 , TIM2 , TIM5 ,
TIM6)

➢ 2 General-purpose timers (TIM3 , TIM4),band PWM with
PWC Features

➢ Up to 13 More GPIO

➢ all GPIO It can be configured as an external interrupt input and wake-up source

➢ GPIO It can be configured to pull-up, pull-down, high impedance down current source, etc.
Features

➢ USB 2.0 full speed(OTG) Controller, support 6 One end
Point, built-in PHY

➢ 1 Standard SPI Master Interface @ max. 30MHz

➢ 1 More SPI Slave Interface @ max.30MHz

➢ 1 Full-duplex UART @ max.3Mbps , Flow control support

➢ 1 More I2C Master / slave controller @ max.400kHz

➢ 1 More 12-bit SAR-ADC (Successive approximation ADC) @
max. 450KHz The sampling rate may be assigned 6 External IO aisle, 2 Internal
voltage sampling channels

DMA

➢ 9 aisle DMA , Full memory addressing, can be assigned to any peripheral (OTG with I2C except)

➢ Unique memory and IO Inter automatically launch and capture mechanism (referred to as DMA-GPIO), Can simulate a variety of communication and timing control

Software Development Support

➢ Audio algorithms support list:

- decoding: MP2 , MP3 , WMA , APE , FLAC , AAC , MP4 , M4A , WAV (IMAADPCM & PCM), AIF , AIFC
- coding: MP2 / MP3 , IMA-ADPCM
- Audio:
  - echo
  - Mixing
  - 3D surround
  - Virtual Bass
  - Electric sound / tone / voice change
  - Parametric equalizer (EQ)
  - Dynamic range compression (DRC)
  - Echo Cancellation (AEC)
  - Noise suppression
  - Frequency shift (antilarsen)
  - Howling detection and suppression

➢ SDK (Software Development Kit) rich connotation. Including a rich work can Example And numerous middleware.

➢ based on Eclipse of IDE with GCC translater

➢ stand by FreeRTOS

➢ all C Programming, code portability easy

Firmware burning and protection

➢ Debugger support, or dedicated writer Flash Burner Lite Burn Flash

➢ Bootloader Built-in dual Bank Upgrade mechanism

➢ stand by 32bit In user key to encrypt the firmware

➢ chip 64-bit unique ID

EMC (Electromagnetic Compatibility)

➢ Support spread spectrum clock

➢ chip ESD Live HBM 4kV

Packaging and temperature

➢ QSOP24

➢ Environmental Operating Temperature: - 40 ℃ to 85 ℃

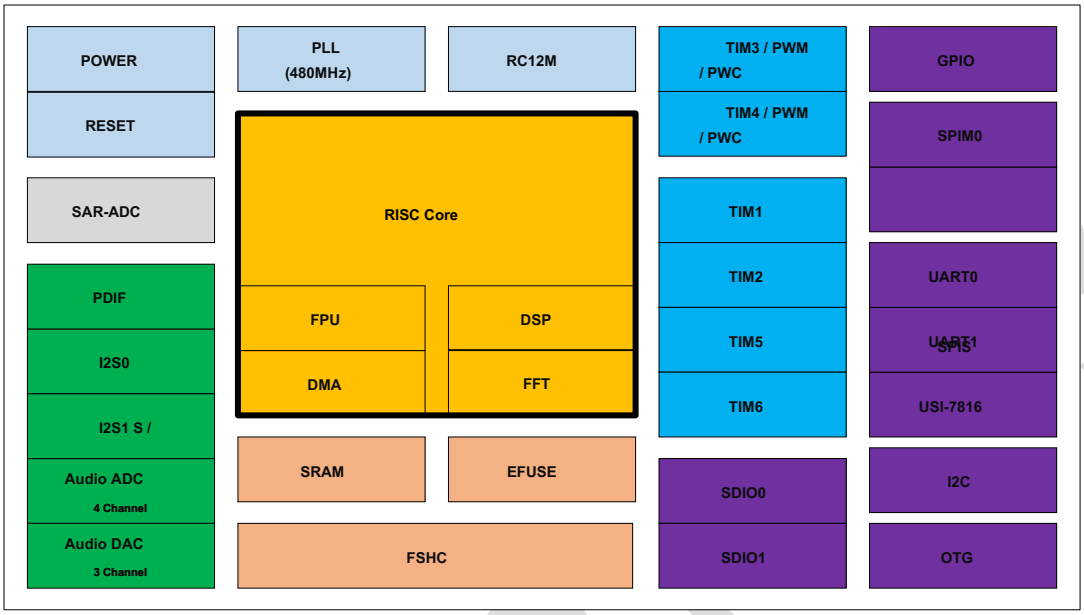
Applications

➢ Portable Bluetooth Speaker

➢ Portable headphones

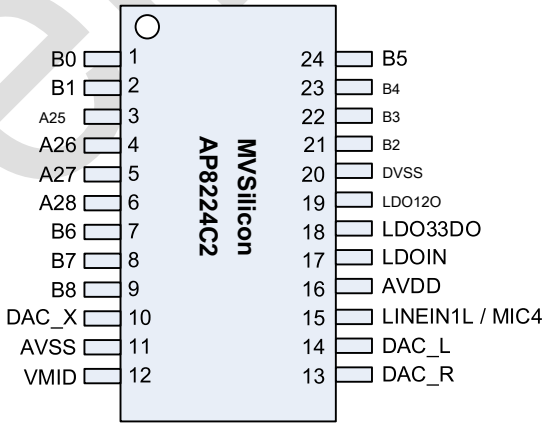
➢ Kara OK Sound Card

2. Schematic



Map 1. Chip structure diagram

3. Pin definitions and descriptions



Map 2. Chip pin definitions

4. GPIO Pin Description

table 1 Chip Pin Type Description

The type of mark	description
I	Digital input PAD
O	Digital Output PAD
AI	Analog Input PAD
AO	Analog Output PAD
I / O	input Output PAD
PWR	power supply PAD
GND	Ground PAD

table 2 Chip pin Description Pin

Number name		Types of	Function Description multiplex
1	GPIO_B0	I / O	UART1_TXD / I2C_SCL / TIM3_PWM / TIM3_PWC / SW_CLK
2	GPIO_B1	I / O	UART1_RXD / I2C_SDA / TIM4_PWM / TIM4_PWC / SW_D
3	GPIO_A25	I / O	ADC4 / SPDIF_AI / SPIS_MISO / SPIM_MISO / I2S0_LRCLK / I2S1_LRCLK / DMIC_DAT
4	GPIO_A26	I / O	ADC5 / SPDIF_AI / SPIS_CLK / SPIM_CLK / I2S0_BCLK / I2S1_BCLK / DMIC0_CLK
5	GPIO_A27	I / O	ADC6 / SPDIF_AI / SPIS_MOSI / SPIM_MOSI / I2S0_DO / DMIC1_CLK / SPDIF_DO / TIM3_PWM / TIM3_PWC
6	GPIO_A28	I / O	ADC7 / SPDIF_AI / SPIS_CS / I2S0_DI / DMIC1_DAT / SPDIF_DI / TIM4_PWM / TIM4_PWC
7	GPIO_B6	I / O	ADC12 / FMR / UART1_RXD / I2C_SDA
8	GPIO_B7	I / O	ADC13 / FML / UART1_TXD / I2C_SCL
9	GPIO_B8	I / O	Multiplexing is EFUSE VDD
10	DAC_X	AO	Audio frequency X Channel output
11	AVSS	GND	Analog ground
12	VMID	AO	The audio module internal voltage reference
13	DAC_R	AO	Audio frequency R Channel output
14	DAC_L	AO	Audio frequency L Channel output
15	LINEIN1_L / MIC4	AI	Analog audio input or MIC Entry
16	AVDD	PWR	Analog Power Input
17	LDOIN	PWR	Total Chip Power Input
18	LDO33DO	PWR	digital 3.3V Power Output
19	LDO12DO	PWR	Core Power Output
20	DVSS	GND	Digital Ground
twenty one	GPIO_B2	I / O	USB_DM / UART1_TXD / I2C_SCL / TIM3_PWM / TIM3_PWC
twenty two	GPIO_B3	I / O	USB_DP / UART1_RXD / I2C_SDA / TIM4_PWM / TIM4_PWC

Pin Number name		Types of	Function Description multiplex
twenty three	GPIO_B4	I / O	HOSC_XI
twenty four	GPIO_B5	I / O	HOSC_XO

Description:

1) GPIO press A , B Divided 2 Group, which A group 4 A, B group 9 A.

2) all GPIO The default power-state of high impedance input.

table 3 GPIO Power on state And level

name	I / O status	Level status
GPIO_A [28:25]	Floating	High resistance
GPIO_B [8: 0]	Floating	High resistance

3) Chip CMOS Process, and it suggested no other devices connected GPIO Do pull the pin on the inside or pull-down configuration, so as to avoid electric

Which led to the accumulation of charge IO Produce current consumption.

4) GPIO During a chip reset and after the performance, divided into two cases:

a) Power-on reset (POR), Will GPIO Cancel Other multiplexing function, return to the high impedance input level state. Table 3 .

b) Watchdog (watchdog) Software reset or system reset by register settings lets GPIO Before holding reset configuration, such as

Multiplexing relationship, the input and output of the pull-down state and the like; and may be expressed as a) Consistent.

5. Chip electrical characteristics

5.1. Chip Conditions

table 4 Chip recommended conditions of use

parameter	Mark	Minimum	Typical	Maximum	Units	
Ambient operating temperature		- 40		85	℃	
Chip power input range	LDOIN	3.3		5	V	
Analog power modules	AVDD		3.3		V	
Internal LDO Digital power modules	LDO33DO		3.3		V	
Core Operating Voltage	LDO12O		1.2		V	

5.2. digital IO Electrical characteristics

table 5 digital IO DC Characteristics

symbol	meaning	Minimum	Typical	Maximum	Units	Test Conditions
VIH	Input High	2.2		3.6	V	VDD33 = 3.3V
VIL	Input low	-0.3		1.0	V	VDD33 = 3.3V
IL	Input leakage current	--10		10	μA	
VOH	Output high	3.0			V	@ IOH = 8mA
VOL	Output low			0.3	V	@ IOL = 8mA

table 6 digital IO Driving force and the vertical pullup

name	The corresponding port	Ordinary	reinforced	unit	Test Conditions
Driving force	GPIO_A18 All outside GPIO	8		mA	VDD33 = 3.3V ,typical
	GPIO_A18	8	twenty four	mA	VDD33 = 3.3V ,typical
pull up	all GPIO	20	70	μA	VDD33 = 3.3V ,typical
drop down	all GPIO	20	70	μA	VDD33 = 3.3V ,typical
Pull-down current source	all GPIO	2.9		mA	VDD33 = 3.3V ,typical

5.3. Audio Performance

table 7 Audio DAC performance @ 44.1KHz

parameter	Test Conditions	Min	Typ	Max	Units
Bit wide				20	Bits
Sampling Rate		8		48	kHz
Dynamic Range	@ Fin = 1kHz , - 60dBFS , AWeighted		98		dB
SNR	@ Fin = 1kHz , 0dBFS , A- Weighted		105		dB
THD + N	@ Fin = 1kHz , - 6dBFS , A- Weighted		--81		dB

parameter	Test Conditions	Min	Typ	Max	Units
Output Swing			1.067		Vrms
Internal channel gain mismatch			0.027		dB
Group delay			756		μs
Phase deviation			0.285		degree
Crosstalk (L / R)			--119		dB

table 8 Audio ADC performance @ Line-in aisle, 44.1KHz

parameter	Test Conditions	Min	Typ	Max	Units
Bit wide				16	Bits
Sampling Rate		8		48	kHz
Analog gain control range		- 44		12	dB
input resistance			15		kΩ
Dynamic Range	No Filter @ Fin = 1kHz		93		dB
	A-Weighted @ Fin = 1kHz		95		dB
SNR	No Filter @ 900mVrms , Fin = 1kHz		92		dB
	A-Weighted @ 900mVrms , Fin = 1kHz		94		dB
THD + N	@ 900mVrms , Fin = 1kHz		- 88		dB
Internal channel gain mismatch			0.033		dB
Group delay			680		us
Crosstalk (L / R)			-99.3		dB

table 9 Audio ADC performance @ The microphone channels, 44.1kHz

parameter	Test Conditions	Min	Typ	Max	Units
Bit wide				16	Bits
Sampling Rate		8		48	kHz
Analog gain control range Do not use GainBoost		--20		39.6 dB	
	use GainBoost	--20		59.6 dB	
input resistance			4		kΩ
Dynamic Range	No Filter		92		dB
	A-Weighted		94		dB
SNR	No Filter		91		dB
	A-Weighted		93		dB
THD + N	Do not use GainBoost		- 85		dB

parameter	Test Conditions	Min Typ Max Units			
	use GainBoost		--80		dB
Internal channel gain mismatch			0.12		dB
Group delay			680		us
Crosstalk (L / R)			--110		dB

6. Operating frequency and power consumption

6.1. And operating frequency clock source

Two-chip clock sources: RC 12MHz (Referred to as RC12M) And clock PLL PLL clock. After a chip reset is to use RC12M Operation when the user runs the firmware, and then select the kernel of the system bus clock source code. can choose:

a) Overall reserved RC12M Clock runs (note that there are many restrictions on the use of peripheral);

b) Switch to the overall PLL clock;

c) Most of the switching systems and the core module to PLL Clock, using the reserved portion of the module RC12M clock.

d) Crystal-free work

The operating frequency and chip clock source and the operating mode related to the selected clock source, substantially the following table.

table 10 And operating frequency clock source

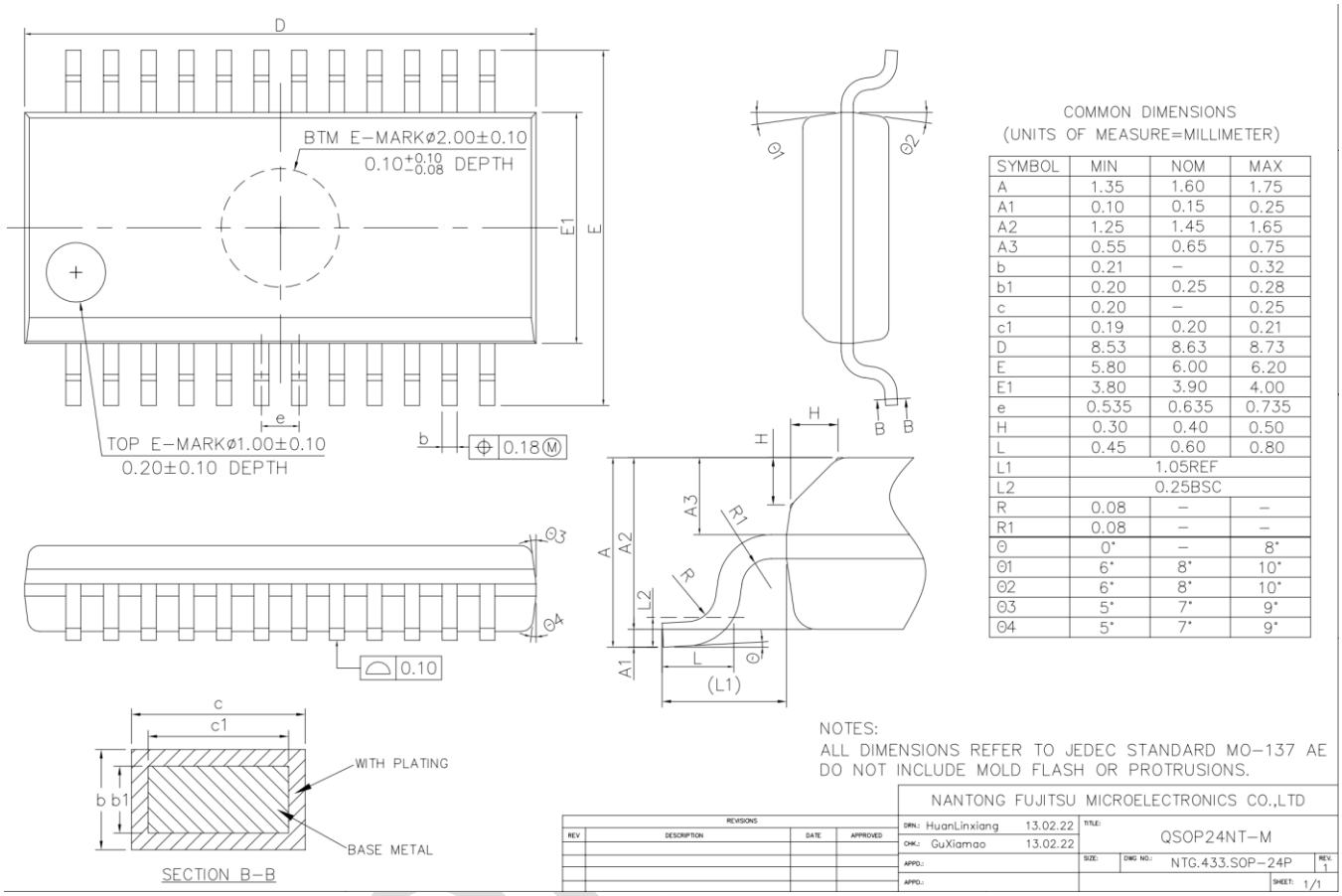
Clock Source	MCU Operating frequency (MHz)	The maximum error	Explanation
RC12M clock	To 12	- ~ 29% + twenty one%	Extreme pressure and temperature drift drift
PLL Clock (closed loop) 240		80ppm	@ 12MHz Crystal

6.2. Typical power consumption mode

table 11 Typical power consumption mode

A typical mode	Electric current	condition
RC12M clock	7.51mA	CPU run while (1) Code that works in the kernel RC12M ,
PLL clock	38mA	CPU run while (1) Code that works in the kernel 240MHz , 12M Crystals.
Free crystal	34.5mA	CPU run while (1) Code that works in the kernel 240MHz No crystal body.
Deep sleeping	TBD	

7. Package size



SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.21	–	0.32
b1	0.20	0.25	0.28
c	0.20	–	0.25
c1	0.19	0.20	0.21
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.535	0.635	0.735
H	0.30	0.40	0.50
L	0.45	0.60	0.80
L1	1.05REF		
L2	0.25BSC		
R	0.08	–	–
R1	0.08	–	–
θ	0°	–	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

Map 3. Form and dimensions of the package

8. Welding and storage

Storage Temperature Range: - 65 To 150 Degrees Celsius.

AP8224C2 is a moisture sensitive component. The moisture sensitivity classification is **Class 3.**

It's important that the parts are handled under precaution and a proper manner. The handling , baking and out-of-pack storage conditions of the moisture sensitive components are described in IPC / JEDC S-STD-033A.

The Technologies recommends utilizing the standard precautions listed below.

1. Calculated shelf life in Sealed Bag: 12 months at <40 ℃ and <90% relative humidity (RH)

2. Peak Package Body Temperature: 250 ℃

3. After bag is opened , devices that will be subjected to reflow solder of other high temperature process must be:

   a. Mounted within 168 hours of factory condition ≤30 ℃ / 60% RH

   b. Stored at <10% RH if not used

4. Devices require baking , before mounting if:

   a. Humidity indicator card is> 10% when read at 23 ± 5 ℃ immediately after moisture barrier bag is opened

   b. Items 3a or 3b is not met

5. If baking is required , please refer to J-STD-033 standard for low temperature (40 ℃) baking requirement in Tape / Reel form.

9. statement

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