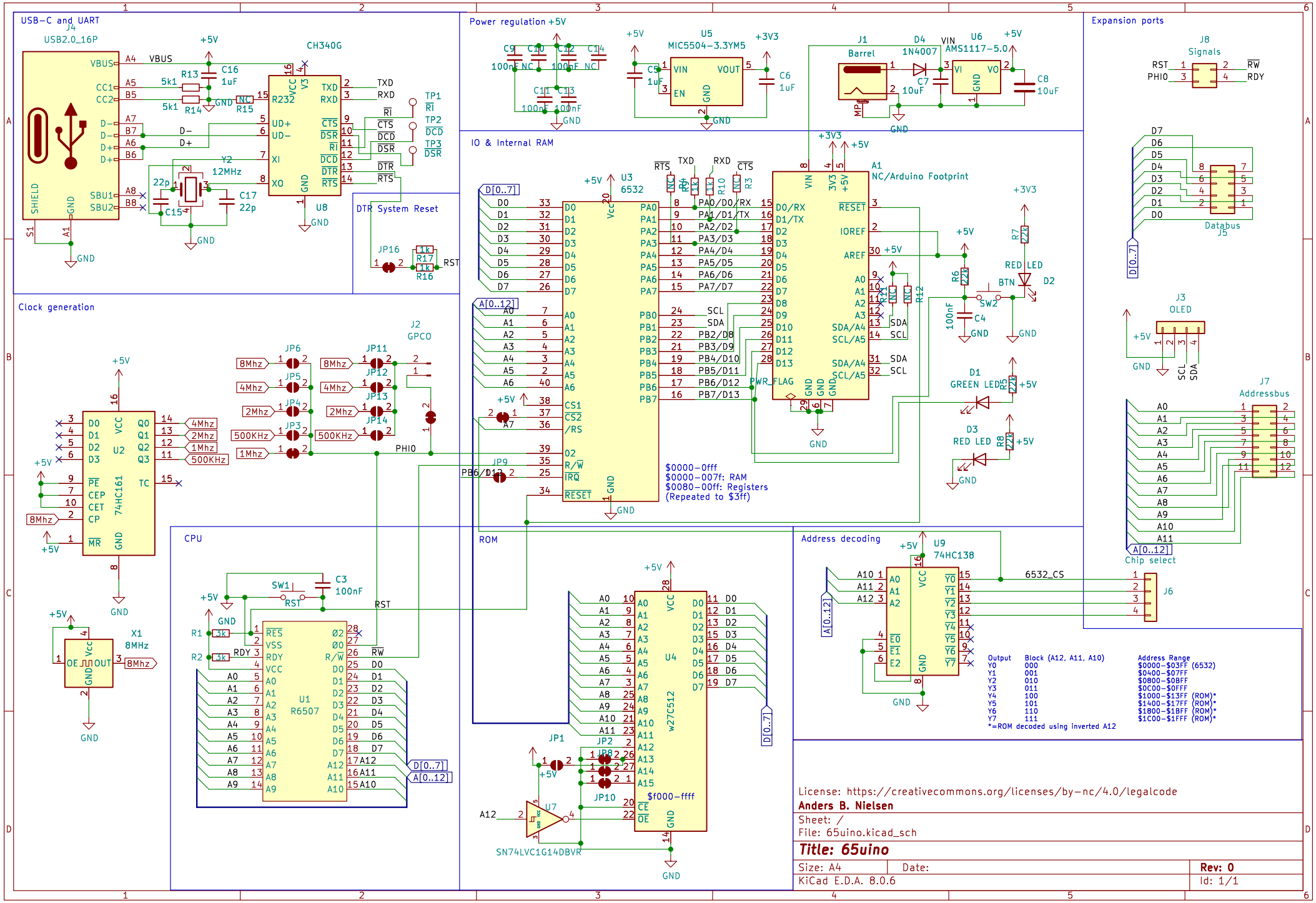
USB-C and UART
J4
USB2.0_16P
CH340G
U8
R232
VBUS
CC1
CC2
D-
D+
SHIELD
GND
S1
A1
SBU1
SBU2
R13 5k1
R14 5k1
C16 1uF
R15 NC
Y2 12MHz
C15 22p
C17 22p
TXD
RXD
RI
CTS
DSR
DCD
DTR
RTS
TP1 RI
TP2 DCD
TP3 DSR
DTR System Reset
JP16
R17 1k
R16 1k
RST
Power regulation +5V
C9 100nF
C10 NC
C12 100nF
C14 NC
C11 100nF
C13 100nF
U5
MIC5504-3.3YM5
VIN
VOUT
EN
C5 1uF
C6 1uF
+3V3
J1
Barrel
D4
1N4007
C7 10uF
U6
AMS1117-5.0
VI
VO
C8 10uF
Expansion ports
J8
Signals
RST
PHI0
RW
RDY
Databus
J5
D[0..7]
J3
OLED
SCL
SDA
J7
Addressbus
A[0..12]
Chip select
IO & Internal RAM
U3
6532
PA0/D0/RX
PA1/D1/TX
PA2/D2
PA3/D3
PA4/D4
PA5/D5
PA6/D6
PA7/D7
PB0
PB1
PB2/D8
PB3/D9
PB4/D10
PB5/D11
PB6/D12
PB7/D13
CS1
CS2
/RS
O2
R/W
IRQ
RESET
PWR_FLAG
A1
NC/Arduino Footprint
IOREF
AREF
SDA/A4
SCL/A5
R7 22k
R6 22k
RED LED
BTN
SW2
D2
C4 100nF
D1
GREEN LED
R5 22k
D3
RED LED
R8 22k
$0000-0ffff
$0000-007f: RAM
$0080-00ff: Registers
(Repeated to $3ff)
Clock generation
J2
GPCO
JP6
JP5
JP4
JP3
JP11
JP12
JP13
JP14
8Mhz
4Mhz
2Mhz
500KHz
1Mhz
PHI0
U2
74HC161
PE
CEP
CET
CP
MR
TC
X1
8MHz
OE
OUT
CPU
U1
R6507
SW1
RST
C3 100nF
R1 3k
R2 3k
RDY
RW
D[0..7]
A[0..12]
ROM
U4
w27C512
$f000-ffff
JP1
JP2
JP8
JP10
U7
SN74LVC1G14DBVR
Address decoding
U9
74HC138
6532_CS
J6
Output Block (A12, A11, A10) Address Range
Y0 000 $0000-$03FF (6532)
Y1 001 $0400-$07FF
Y2 010 $0800-$08FF
Y3 011 $0C00-$0FFF
Y4 100 $1000-$13FF (ROM)*
Y5 101 $1400-$17FF (ROM)*
Y6 110 $1800-$1BFF (ROM)*
Y7 111 $1C00-$1FFF (ROM)*
*=ROM decoded using inverted A12
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Anders B. Nielsen
Sheet: /
File: 65uino.kicad_sch
Title: 65uino
Size: A4
Date:
Rev: 0
KiCad E.D.A. 8.0.6
Id: 1/1