

Logic Guide



Logic Guide

Introduction and Contents

Introduction

As the world leader in logic, Texas Instruments (TI) offers a full spectrum of logic functions and technologies that range from the mature bipolar and bipolar complementary metal-oxide semiconductor (BiCMOS) families to the latest advanced-CMOS families. TI offers process technologies with the logic performance and features needed in today's electronic markets while maintaining support for traditional logic products.

TI's product offerings include the following process technologies or device families:

- AC, ACT, AHC, AHCT, ALVC, AUC, AUP, AVC, FCT, HC, HCT, LV-A, LV-AT, LVC, TVC
- ABT, ABTE, ALB, ALVT, BCT, HSTL, LVT, LV1T, LV4T
- CB3Q, CB3T, CBT, CBT-C, CBTLV, FB, FIFO's, GTL, GTLP, JTAG, I²C, VME
- ALS, AS, F, LS, LSF, S, TTL

Today's applications are evolving with greater functionality and smaller size. TI's goal is to help designers easily find the ideal logic technology or function they need. Logic families are offered at every price/performance node along with benchmark delivery, reliability, and worldwide support. TI maintains a firm commitment to remain in the market with both leading-edge and mature logic lines.

Logic suppliers have historically focused on speed and low power as the priorities for product family improvement. As shown below, improved performance is offered by many new TI product technologies such as AUC (1.8 V) and ALVC (3.3 V) depending on operating voltage requirements. Other technologies such as AUP focus on delivering "best-in-class" low-power performance.

Data sheets can be downloaded from the TI Web site at www.ti.com or ordered through your local sales office or TI authorized distributor. (See back cover.)

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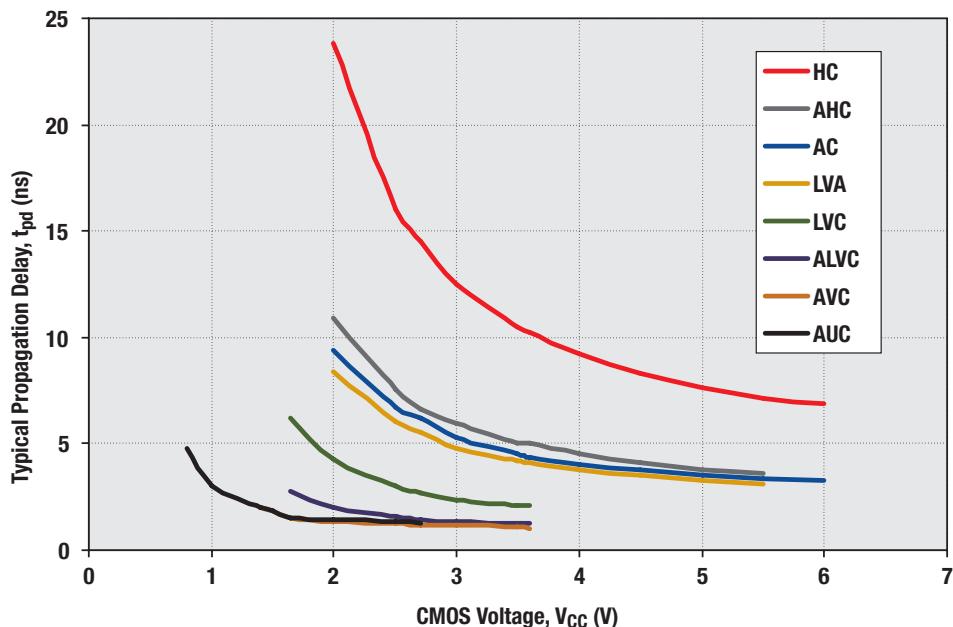
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CMOS Voltage vs. Speed



Logic Overview

World of TI Logic

Some logic families have been in the marketplace for years, the oldest is well into its fifth decade. The following section gives the logic user a visual guide to the technology families that are available and their optimal voltage levels.

0.8-V Logic

AUC, AUP

1.2-V Logic

AUC, AUP, AVC

1.5-V Logic

AUC, AUP, AVC

1.8-V Logic

ALVC, AUC, AUP, AVC, LVC, LV1T

2.5-V Logic

ALVC, ALVT, AUC, AUP, AVC,
CBTLV, LV, LV1T, LV-A, LVC

3.3-V Logic

AC, AHC, ALB, ALVC, ALVT,
AUP, AVC, CBLTV, LV, LV-A,
LVC, LVT, LV1T, AUP1T

5-V+ Logic

CD4K

5-V Logic

ABT, AC/ACT, AHC, AHCT, ALS,
AS, BCT, CBT, F, LV, LV1T, LV-A,
LS, S, TTL, CD4K, FCT2

Specialty

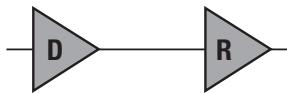
BTL, ETL, GTL, GTLP, HSTL,
SSTL, SSTV, TVC, VME, LSF

Logic Overview

IC Basics: Comparison of Switching Standards

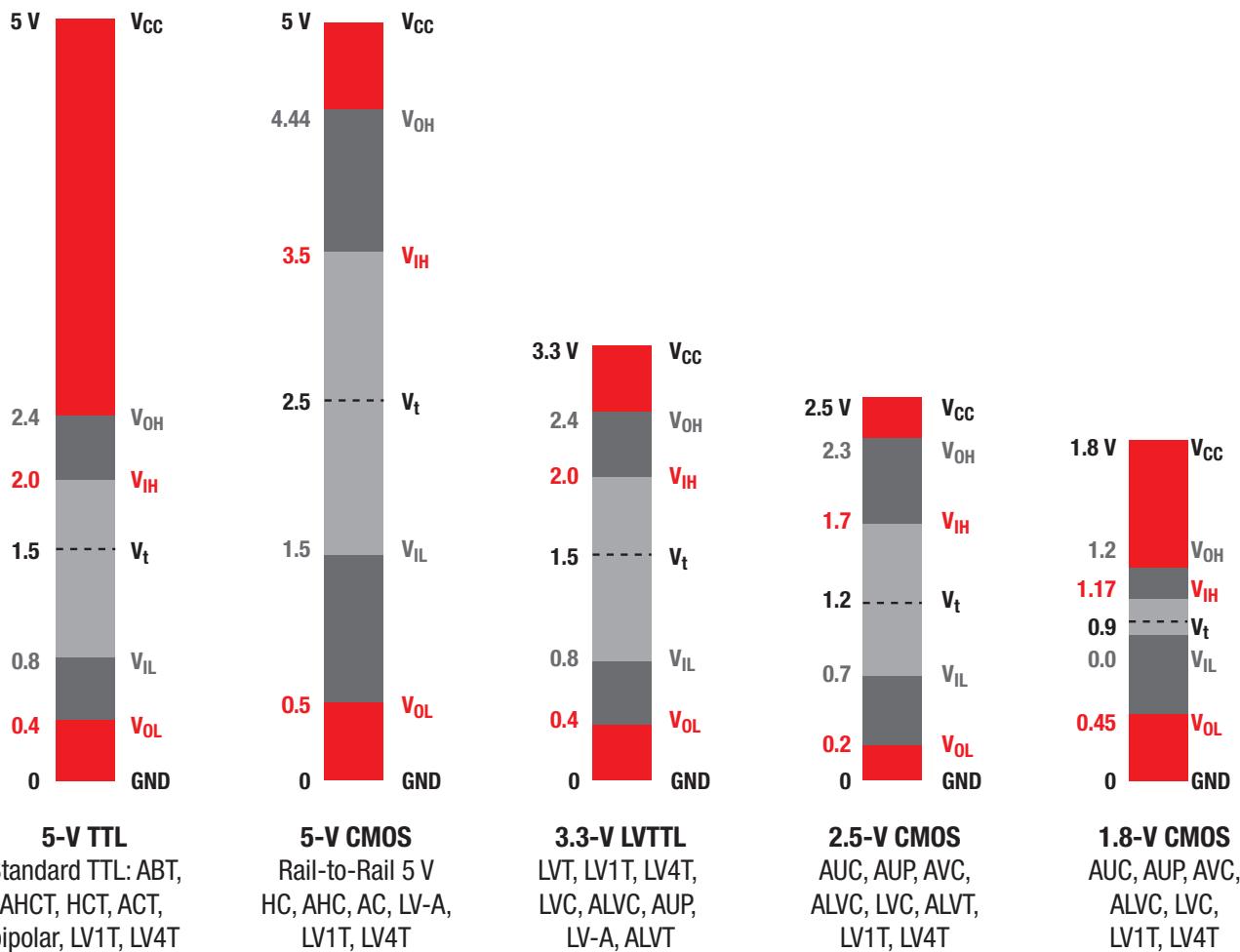
Shown below are the switching input/output comparison table and graphic that illustrate V_{IH} and V_{IL} , which are the minimum switching levels for guaranteed operation. V_t is the approximate switching level and the V_{OH} and V_{OL} levels are the guaranteed outputs for the V_{CC} specified.

Is V_{OH} higher than V_{IH} ?
Is V_{OL} less than V_{IL} ?



D \ R	5 TTL	5 CMOS	3 LVTTL	2.5 CMOS	1.8 CMOS
5 TTL	Yes	No	Yes*	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes*

* Requires V_{IH} Tolerance



Logic Overview

Technology Function Matrix

		Functions												Special Features			Process									
Families	Voltage	Buffers/Line Drivers	Configurable Logic	Flip-Flops	Combination Logic	Counters	Shift Registers	Encoders/Multiplexers	Decoders/Demultiplexers	Comp/Parity Gen.	Gates	Schmitt Triggers	Analog Switches	Transceivers	Level Translators	Phase Lock Loops	Bus Switches	Bushold	Series Damping Resistors	Live Insertion	Oversupply-tolerate Inputs	Power-off Output Disable	Power-up Reset	Bipolar	CMOS	BiCMOS
AUC	0.8, 1.8, 2.5	✓																					✓			
AUP	0.8, 1.8, 3.3	✓	✓	✓																			✓	✓		
ALVC	1.8, 3.3	✓		✓																			✓	✓		
AUP1T	1.8, 3.3	✓																					✓			
AVC	1.8, 3.3	✓		✓																			✓	✓		
LSF	1.8, 3.3, 5																						✓			
LV1T	1.8, 3.3, 5	✓																					✓			
LVC	1.8, 3.3, 5	✓	✓	✓	✓	✓																	✓	✓		
TS	1.8, 3.3, 5																						✓	✓		
TVC	1.8, 3.3, 5																						✓	✓		
AC	3.3, 5	✓		✓			✓	✓	✓	✓													✓	✓		
AHC	3.3, 5	✓		✓				✓	✓	✓													✓	✓		
HC	3.3, 5	✓		✓			✓	✓	✓	✓													✓	✓		
LV-A	3.3, 5	✓		✓			✓	✓	✓	✓													✓	✓		
ALB	3.3	✓																						✓		
ALVT	3.3	✓		✓																				✓		
CB3Q	3.3							✓	✓									✓						✓		
CB3T	3.3								✓	✓								✓						✓		
CBTLV	3.3								✓	✓								✓						✓		
GTL	3.3																	✓						✓		
GTLP	3.3																	✓						✓		
LVT	3.3	✓		✓														✓						✓		
VME	3.3																	✓						✓		
ABT	5	✓		✓					✓	✓								✓						✓		
ABTE	5																	✓						✓		
ACT	5	✓		✓				✓	✓	✓							✓	✓					✓			
AHCT	5	✓		✓				✓	✓	✓							✓	✓					✓			
ALS	5	✓		✓				✓	✓	✓							✓	✓					✓			
AS	5	✓		✓				✓	✓	✓							✓	✓					✓			
BCT	5	✓		✓					✓	✓							✓	✓					✓			
CBT	5								✓	✓							✓	✓					✓			
CBT-C	5								✓	✓							✓	✓					✓			
F	5	✓		✓				✓	✓	✓							✓						✓			
FB	5																✓						✓			
FCT	5	✓		✓				✓	✓	✓							✓						✓			
HCT	5	✓		✓				✓	✓	✓							✓	✓					✓			
LS	5	✓		✓				✓	✓	✓							✓	✓					✓			
LV-AT	5	✓		✓					✓	✓							✓						✓			
S	5	✓		✓				✓	✓	✓							✓	✓					✓			
TTL	5	✓		✓				✓	✓	✓							✓	✓					✓			
CD4000	5, 10, 12 to 18	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓								

Logic Families

AUC and AUP1G

Advanced Ultra-Low-Voltage CMOS

AUC

Key Features

- 1.8-V optimized performance
- V_{CC} specified at 2.5 V, 1.8 V, and 1.2 V
- 3.6-V I/O tolerance
- I_{off} spec for partial power down
- ESD protection
- Low noise

Applications

- Telecommunications equipment
- High-performance workstations
- PCs and networking servers
- Portable consumer electronics

Packaging Options

- BGA MicroStar Junior™
- DSBGA
- LFBGA
- SC70
- SM8
- SON
- SOT-23
- SOT
- TSSOP
- TVSOP
- UQFN
- US8
- VQFN



AUC Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 1.8 V
SN74AUC1G125	2.7	-9/9	1.5
SN74AUC1G32	2.7	-9/9	1.5
SN74AUC245	2.7	-9/9	1.7
SN74AUC1G04	2.7	-9/9	1.2
SN74AUC1G66	2.7	-9/9	0.2

Advanced Ultra-Low-Power

AUP1G

Key Features

- Low static-/dynamic-power consumption
- Wide operating V_{CC} range
- Input hysteresis allows for slow input transition
- Best in class for speed-power optimization
- I_{off} spec for partial power down
- ESD protection

Packaging Options

- DSBGA
- SC70
- SM8
- SON
- SOT-23
- SOT
- UQFN
- US8
- X2SON



AUP1G Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V	I_{CC} (μ A)
SN74AUP1G07	3.6	-4/4	3.3	0.9
SN74AUP1G34	3.6	-4/4	4.1	0.9
SN74AUP1G08	3.6	-20/20	4.3	0.9
SN74AUP1G32	3.6	-20/20	4.6	0.9
SN74AUP1G00	3.6	-20/20	4.8	0.9

Logic Families

ALVC, AUP1T and AVC

Advanced Low-Voltage CMOS

ALVC

Key Features

- V_{CC} specified at 3.3 V, 2.5 V, and 1.8 V
- Balanced drive
- Bus-hold option
- Low noise
- Damping resistor options
- ESD protection

Applications

- Automotive
- Memory Interfaces
- Datapath communication

Packaging Options

- BGA MicroStar Junior™
- SSOP
- LFBGA
- TSSOP
- PDIP
- TVSOP
- SO
- VQFN
- SOIC

ALVC Device Examples

Device	V _{CC} (V)	Drive (mA)	t _{pd(MAX)} (ns) at 3.3 V
SN74ALVC125	3.6	-24/24	2.8
SN74ALVCH16373	3.6	-24/24	3.6
SN74ALVC164245	6	-24/24	5.8

Advanced Ultra-Low-Power

AUP1T

Key Features

- Low voltage input switching levels of 1.8 V and 2.5 V allows for low threshold level
- Accepts 1.8-V to 2.5-V logic level for high or low
- Only requires a single voltage to achieve level shifting function
- V_{CC} of either 2.5 V or 3.3 V

Applications

- Portable electronics
- Automotive
- Signal conditioning

Packaging Options

- DSBGA
- SON
- SC70
- SOT-23



AUP1T Device Examples

Device	V _{CC} (V)	Drive (mA)	t _{pd(MAX)} (ns) at 1.8 V	I _{CC} (μ A)
SN74AUP1T17	3.6	-4/4	10	0.9
SN74AUP1T08	3.6	-4/4	10.8	0.9
SN74AUP1T32	3.6	-4/4	10.8	0.9

Advanced Very-Low-Voltage CMOS

AVC

Key Features

- V_{CC} specified at 3.3 V, 2.5 V, and 1.8 V
- 3.3-V I/O tolerance
- Sub-2.0-ns max t_{pd} at 2.5 V
- Bus-hold option
- I_{off} for partial power down
- Dynamic output control

Packaging Options

- BGA MicroStar Junior™
- TSSOP
- DSBGA
- SC70
- UQFN
- SM8
- US8
- X2SON
- SOT



Applications

- High-performance workstations
- PCs
- Networking servers
- Telecommunication equipment

AVC Device Examples

Device	V _{CC} (V)	Drive (mA)	t _{pd(MAX)} (ns) at 3.3 V
SN74AVC16245	3.6	-12/12	1.7
SN74AVC16373	3.6	-12/12	2.8
SN74AVC16244	3.6	-24/24	3.5

Logic Families

LSF and LV1T/LV4T

Bidirectional Voltage-Level Translators

LSF

Key Features

- Bidirectional voltage translation without a directional pin
- Less than 1.5-ns t_{pd}
- Supports high speed translation
- Supports hot insertion
- Bidirectional voltage translation between:
 - 1.0 V \leftrightarrow 1.8/2.5/3.3/5 V
 - 1.2 V \leftrightarrow 1.8/2.5/3.3/5 V
 - 1.8 V \leftrightarrow 2.5/3.3/5 V
 - 2.5 V \leftrightarrow 3.3/5 V
 - 3.3 V \leftrightarrow 5 V

Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I²C, and other Interfaces in telecom infrastructure
- Industrial
- Automotive
- Personal computing
- Solid State Drive
- Base Transceiver Station
- Wireless Infrastructure
- Notebook



Packaging Options

- SON
- X2SON
- DSBGA
- VQFN

LSF Device Examples

Device	V _{CC} (V)	R _{on(MAX)} (Ω)	t _{pd(MAX)} (ns) at 3.3 V
LSF0101	5	30	0.2
LSF0108	5	30	0.2
LSF0102	5	30	0.2

Low-Voltage CMOS Technology

LV1T/LV4T

Key Features

- Up/down translation with a single power rail
- Down translation from up to 5.5-V to V_{CC} level
- Optimized and balanced output drive (7 mA at 3.3-V V_{CC})
- No need for damping resistor
- Lowered switching threshold

Applications

- Computing
- Wearables
- Personal electronics
- Automotive and industrial
- Notebook

Packaging Options

- SC70
- SOT-23
- TSSOP
- VQFN



LV1T/LV4T Device Examples

Device	V _{CC} (V)	Drive (mA)	t _{pd(MAX)} (ns) at 3.3 V
SN74LV1T34	5.5	-8/8	8.0
SN74LV4T125	5.5	-16/16	5.5
SN74LV1T08	5.5	-8/8	5.5

Logic Families

LVC/LVC1G and TVC

Low-Voltage CMOS

LVC/LVC1G

Key Features

- V_{CC} specified at 3.3 V, 2.5 V, and 1.8 V
- 5-V I/O tolerance
- Series damping resistor option
- I_{off} spec for partial power down
- ESD protection

Applications

- Portable electronics
- Telecommunications equipment
- Networking servers
- Routing, clock buffering, and muxing
- Personal computing

Packaging Options

- BGA MicroStar Junior™
- SOIC
- CDIP
- SON
- CFP
- SOT-23
- DSBGA
- SOT
- LCCC
- SSOP
- LFBGA
- TSSOP
- PDIP
- TVSOP
- SC70
- UQFN
- SM8
- US8
- SO
- USON
- VQFN
- X2SON

LVC/LVC1G Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74LVC1G125	5.5	-32/32	4.5
SN74LVC245A	3.6	-24/24	6.3
SN74LVC14A	3.6	-24/24	6.4
SN74LVC1G08	5.5	-32/32	3.6

Translation Voltage Clamp

TVC

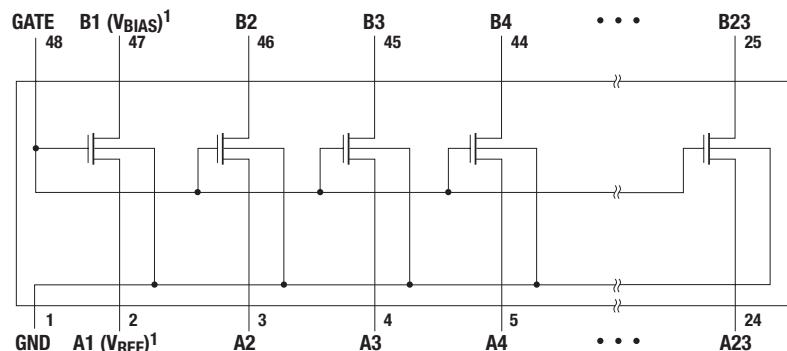
Key Features

- Overshoot protection
- Voltage translator or voltage clamp
- Abs 7 V to -0.5 V
- Flow-through pinout for ease of PCB trace routing
- Direct interface with GTL+ levels
- ESD protection

Applications

- Automotive
- Medical
- Defense, aerospace

Logic Diagram (Positive Logic)



TVC Device Examples

Device	V_{CC} (V)	$R_{on(MAX)}$ (Ω)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74TVC3306	5.0	32	0.4
SN74TVC3010	5.0	12.5	4.0
SN74TVC16222A	5.5	12.5	4.0

Logic Families

AC/ACT, AHC/AHCT and HC/HCT

Advanced CMOS

AC/ACT

Key Features

- Balanced propagation delay
- Inputs are TTL-voltage compatible (ACT)
- Low power consumption
- ESD protection
- Center V_{CC} pin and GND configurations minimize high-speed switching noise

Applications

- Buffer registers
- Defense, aerospace
- Working registers
- I/O ports

Packaging Options

- CDIP
- CFP
- CPGA
- LCCC
- SO
- SOIC
- SSOP
- TSSOP
- PDIP

AC/ACT Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74ACT245	5.5	-24/24	9.0
SN74AC373	6.0	-24/24	10.5
SN74ACT08	5.5	-24/24	10

Advanced High-Speed CMOS

AHC/AHCT

Key Features

- Low noise without characteristic overshoot/undershoot
- Low power consumption
- Small propagation delay (5.5 ns)
- 5 V and input tolerance at 3.3 V
- Pin-for-pin compatibility

Applications

- Industrial
- Defense, aerospace
- Medical

Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SC70
- SO
- SOIC
- SOT-23
- SOT
- SSOP
- TSSOP
- TVSOP
- VQFN

AHC/AHCT Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74AHC245	5.5	-8/8	6.5
SN74AHC123A	5.5	-8/8	14
SN74AHC1G08	5.5	-50/50	7

High-Speed CMOS

HC/HCT

Key Features

- Low noise without characteristic overshoot/undershoot
- Low power consumption
- Small propagation delay (5.5 ns)
- TTL voltage-compatible inputs (HCT)
- Balanced propagation delay and transition times
- Wide operating temperature

Applications

- Automotive
- Buffer/storage registers
- Frequency synthesis and multiplication
- Shift registers
- Pattern generators

Packaging Options

- CDIP
- CFP
- TSSOP
- TVSOP
- SO
- SOIC
- SSOP
- LCCC
- PDIP

HC/HCT Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 6 V
SN74HC245	6.0	-7.8/7.8	22
CD74HC123	6.0	-5.2/5.2	68
CD74HC164	6.0	-5.2/5.2	38

Logic Families

GTL and CBTLV

Gunning Transceiver Logic (Plus)

GTL

Key Features

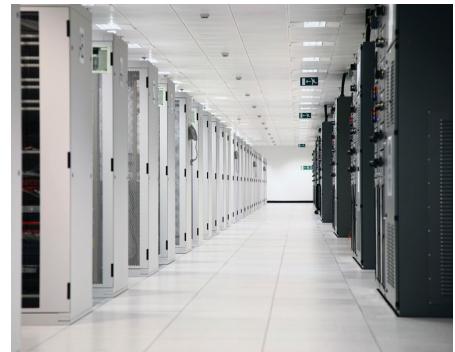
- 3.3-V or 3.3/5-V V_{CC} operation with 5-V LVTTL inputs and outputs
- High point-to-point frequencies with acceptable short-backplane frequencies
- I_{off} for partial-power-down mode
- Bias V_{CC} circuitry allows easy internal precharging of backplane I/O pins
- Bus hold
- Reduced line reflections and EMI for improved overall signal integrity

Applications

- Telecommunications equipment
- Servers
- Platform health management

Packaging Options

- CFP
- SC70
- SSOP
- TSSOP
- VQFN



GTL Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74GTL2014	3.6	50	8.0
SN74GTL2010	5.5	64	5.5
SN74GTL2003	5.5	64	5.5
SN74GTL2007	5.5	16	10

Low-Voltage Crossbar Technology

CBTLV

Key Features

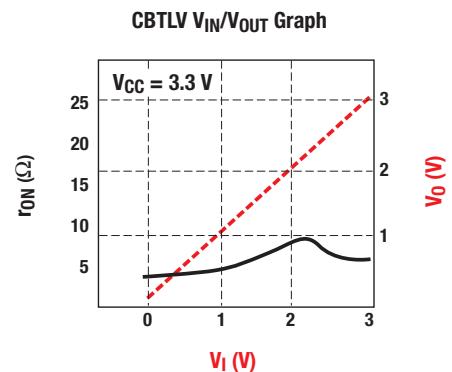
- Rail-to-rail switching (0 to V_{CC})
- Low r_{on} (5Ω)
- Low input/output capacitance
- High current capacity per channel
- ESD protection
- Undershoot diode clamp
- I_{off} for partial-power-down mode
- Supports both digital and analog applications

Applications

- Multiprocessor systems
- Bus-exchange switches
- Memory interleaving
- Bus-byte swapping

Packaging Options

- BGA MicroStar Junior™
- SC70
- SO
- SOIC
- SOT-23
- SSOP
- TSSOP
- TVSOP
- UQFN
- VQFN



CBTLV Device Examples

Device	V_{CC} (V)	$R_{on(MAX)}$ (Ω)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74CBTLV3257	3.6	7	0.25
SN74CBTLV16211	3.6	40	0.25
SN74CBTLV3125	3.6	40	0.25

Logic Families

CB3Q and CB3T

Low-Voltage, High-Bandwidth Bus-Switch Technology

CB3Q

Key Features

- Low and flat r_{on} characteristics over operating range
- High bandwidth
- 0- to 5-V rail-to-rail switching on data I/O ports
- Bidirectional flow with near-zero propagation delay
- Low power consumption
- ESD protection
- Undershoot clamp diodes

Applications

- Broadband communications
- Networking infrastructure equipment
- Gigabit Ethernet routers
- Video processing
- Servers
- Workstations

Packaging Options

- BGA MicroStar Junior™
- LFBGA
- SSOP
- TSSOP
- TVSOP
- US8
- VQFN

CB3Q Device Examples

Device	V _{CC} (V)	R _{on(MAX)} (Ω)	t _{pd(MAX)} (ns) at 3.3 V
SN74CB3Q3306A	3.6	9	0.2
SN74CB3Q3125	3.6	9	0.2
SN74CB3Q3257	3.6	9	0.2

High-Speed CMOS

CB3T

Key Features

- 3.3-V bus switch with translation fully supports mixed-mode signal operation
- 5-V input to 3.3-V output level shift with $V_{CC} = 3.3$ V
- 5-V and 3.3-V input to 2.5-V output level shift with $V_{CC} = 2.5$ V
- High current capacity per channel
- I_{off} for partial-power-down mode
- ESD protection

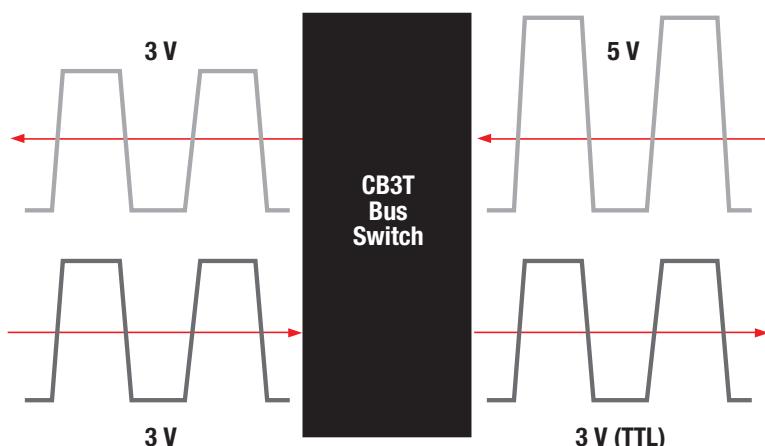
Applications

- Laptop computers
- PDAs
- Cell phones
- Docking stations

Packaging Options

- BGA MicroStar Junior™
- SSOP
- TSSOP
- TVSOP
- US8
- VQFN
- SC70
- SM8
- SOIC
- SOT-23

Mix-Mode Signal Operation



CB3T Device Examples

Device	V _{CC} (V)	R _{on(MAX)} (Ω)	t _{pd(MAX)} (ns) at 3.3 V
SN74CB3T1G125	3.6	8	0.25
SN74CB3T3125	3.6	8	0.25
SN74CB3T3306	3.6	8	0.25
SN74CB3T3245	3.6	8.5	0.25

Logic Families

LV-A/LV-AT, ALB and ALVT

Low Voltage

LV-A/LV-AT

Key Features

- V_{CC} specified at 5.0 V, 3.3 V, and 2.5 V
- Inputs are TTL voltage compatible (LV-AT)
- 5-V I/O tolerance
- I_{off} spec for partial power down
- ESD protection
- Low noise

Applications

- Portable electronics
- Buffer memory address registers
- Bidirectional bus drivers
- I/O ports

Packaging Options

- BGA MicroStar Junior™
- SSOP
- PDIP
- TSSOP
- SO
- TVSOP
- SOIC
- VQFN

LV-A/LV-AT Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74LV245A	5.5	-16/16	8.5
SN74LV123A	5.5	-12/12	15
SN74LV244AT	5.5	-16/16	9.5

Advanced Low-Voltage BiCMOS

ALB

Key Features

- State-of-the-art, advanced low-voltage BiCMOS technology design for 3.3-V operation
- Schottky diodes on all inputs to eliminate overshoot and undershoot
- Small high-speed switching noise
- Flow-through architecture that optimizes PCB layout

Applications

- Workstations
- Telecommunications equipment
- Advanced peripherals

Packaging Options

- SSOP
- TSSOP
- TVSOP



ALB Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74ALB16244	3.6	-25/25	2.0
SN74ALB16245	3.6	-25/25	2.0

Advanced Low-Voltage CMOS Technology

ALVT

Key Features

- V_{CC} specified at 3.3 V and 2.5 V
- High-drive output: up to 64 mA
- 5-V I/O tolerance
- Power-up 3 state
- Partial power down (I_{off})
- Hot insertion
- Bus hold

Applications

- Backplane
- Bus-driving
- Digital logic systems

Packaging Options

- BGA MicroStar Junior™
- TSSOP
- LFBGA
- TVSOP
- SSOP

ALVT Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 2.5 V
SN74ALVTHR16245	3.6	-12/12	4.3
SN74ALVTH16374	3.6	-32/64	3.8
SN74ALVTH162244	3.6	-12/12	4.2
SN74ALVTH16373	3.6	-32/64	4.2

Logic Families

LVT, ABT/ABTE and ALS/AS/S/LS

Low-Voltage BiCMOS Technology

LVT

Key Features

- 5.5-V maximum input voltage
- Specified 2.7-V to 3.6-V supply voltage
- I/O structures support live insertion
- Rail-to-rail switching for driving CMOS
- $t_{pd} < 4.6$ ns
- Allows mixed-signal operation
- Low-input leakage current

Applications

- Computing
- Wearables
- Personal electronics
- Automotive and industrial

Packaging Options

- BGA MicroStar
- BGA MicroStar Junior™
- CDIP
- CFP
- LCCC
- LFBGA
- LQFP
- SO
- SOIC
- SSOP
- TSSOP
- TVSOP
- VQFN

LVT Device Examples

Device	V _{CC} (V)	Drive (mA)	t _{pd(MAX)} (ns) at 3.3 V
SN74LVTH16245A	3.6	-32/64	3.3
SN74LVTH245A	3.6	-32/64	3.5
SN74LVTH16244A	3.6	-32/64	4.1
SN74LVTH125	3.6	-32/64	3.5

Advanced BiCMOS Technology

ABT/ABTE

Key Features

- Low power dissipation
- ESD protection
- Distributed V_{CC} and GND pin configuration minimizes high-speed noise
- Bus hold on data inputs eliminates the need for external pullup/pulldown resistors

Applications

- Buffer registers
- I/O ports
- Working registers

Packaging Options

- CDIP
- CFP
- LCCC
- LQFP
- PDIP
- SO
- SOIC
- SSOP
- TSSOP
- TVSOP
- QFN

ABT/ABTE Device Examples

Device	V _{CC} (V)	Drive (mA)	t _{pd(MAX)} (ns) at 5 V
SN74ABT245B	5.5	-32/64	3.9
SN74ABT125	5.5	-32/64	4.9
SN74ABT244A	5.5	-32/64	4.6

Schottky Logic

ALS/AS/S/LS

Key Features

- PNP inputs reduce DC loading
- Hysteresis at inputs improves noise margins
- Low power consumption
- Short propagation delays and high clock frequencies
- Fully compatible with most TTL circuits
- Wide operating temperature

Applications

- Test and measurement
- Three-state memory address drivers
- Bus-oriented receivers/transceivers
- Balanced transmission lines

Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC
- SSOP
- TSSOP

ALS/AS/S/LS Device Examples

Device	V _{CC} (V)	Drive (mA)	t _{pd(MAX)} (ns) at 5 V
SN54ALS245A	5.5	-12/12	10
SN74ALS1034	5.5	-15/24	8.0
SN54AS373	5.5	-12/32	6.0
SN74LS07	5.5	40	30

Logic Families

BCT, CBT/CBT-C and F

BiCMOS Technology

BCT

Key Features

- Low power consumption
- ESD protection
- Distributed V_{CC} and GND pins minimize noise generated by simultaneous switching of outputs
- Designed to facilitate incident-wave switching for line impedances of 25Ω or greater
- Controlled baseline

Applications

- Asynchronous data bus communication
- 3-state memory address drivers
- Clock drivers
- Bus-oriented receivers and transmitters

Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC
- SSOP
- TSSOP

BCT Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74BCT125A	5.5	-15/64	7.7
SN74BCT2245	5.5	-12/12	7.8
SN74BCT245	5.5	-15/64	7

Crossbar Technology

CBT/CBT-C

Key Features

- Internal termination for control inputs
- High bandwidth
- Low and flat ON-state resistance characteristics
- Low differential and rising/falling edge skew
- TTL-compatible input levels
- ESD protection

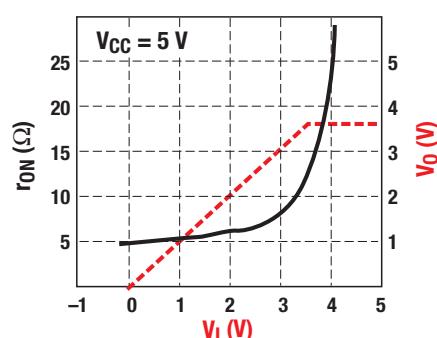
Applications

- DDR-II
- Bus exchange application
- Automotive

Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC
- SSOP
- TSSOP

CBT V_{IN}/V_{OUT} Graph



CBT/CBT-C Device Examples

Device	V_{CC} (V)	$R_{on(MAX)}$ (Ω)	$t_{pd(MAX)}$ (ns) at 5 V
SN74CBT16211A	5.5	12	0.25
SN74CBT3306C	5.5	12	0.15

Fast Logic

F

Key Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Operational over the full military temperature range
- Fully synchronous operation for counting
- Fully independent clock circuit

Applications

- Stacked or pushdown registers
- Buffer storage
- Accumulator registers
- Asynchronous data bus communication

Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC
- SSOP

F Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74F245	5.5	-15/64	7.0
SN74F373	5.5	-3/24	13
SN74F04	5.5	-1/20	6

Logic Families

CD4000, TTL and FCT

CMOS Logic

CD4000

Key Features

- Medium-speed operation: $t_{PLH} = 60$ ns at $V_{DD} = 10$ V
- Standardized, symmetrical output characteristics
- Separate serial outputs synchronous to both positive and negative clock edges for cascading

Applications

- Logical comparators
- Adders/subtractors
- Parity generators and checkers
- Serial-to-parallel data conversion
- Remote control holding register

Packaging Options

- CDIP
- CDIP SB
- CFP
- PDIP
- SO
- SOIC
- TSSOP

CD4000 Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 10 V
CD4069UB	20	-6.8/6.8	60
Device	V_{CC} (V)	$R_{on(MAX)}$ (Ω)	$t_{pd(MAX)}$ (ns) at 5 V
CD40106B	18	240	0.02
CD4051B	18	240	0.08
CD4066B	18	240	0.02

Transistor-Transistor Logic

TTL

Key Features

- Synchronous operation
- Individual preset to each flip-flop
- Fully independent clear input
- Gated output-control lines for enabling or disabling the outputs
- Load control line
- Diode-clamped inputs
- High noise immunity
- Wide operating temperature

Applications

- High-speed counting designs
- Bus buffer register
- Interfacing with high-level circuits
- Driving high-current loads

Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC

TTL Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN7407	5.25	40	30
SN7400	5.25	-0.4/16	5.0

Fast CMOS Technology

FCT

Key Features

- Edge-rate control circuitry for significantly improved noise characteristics
- I_{off} supports partial-power-down mode operation
- ESD protection
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels

Applications

- Programmable dividers
- Transmission lines
- High-speed, low-power bus
- Bus interface

Packaging Options

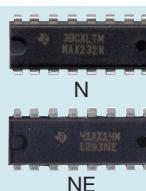
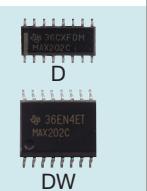
- CDIP
- CFP
- LCC
- PDIP
- SOIC
- SSOP
- TSSOP

FCT Device Examples

Device	V_{CC} (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
CD74FCT273	5.25	-15/48	13
CD74FCT245	5.25	-15/64	7.0

Resources

Package Options

Pins	PDIP	SOIC	SOP	SSOP	QSOP	TSSOP	VSSOP
8	 P	 D	 PS	 DCT		 PW	
10							 DGS
14		 D	 NS	 DB		 PW	
16	 N  NE DW	 D	 NS	 DB	 DBQ	 PW	
18	 N	 DW					
20	 N	 DW	 NS	 DB	 DBQ	 PW	
24	 NT	 DW	 NS	 DB	 DBQ	 PW	
28		 DW		 DB	 DL	 PW	
38						 DBT	
48				 DL		 DGG	
56				 DL		 DGG	
64						 DGG	

Resources

Package Options

Pins	TVSOP	SOT	QFN	MicroQFN	WCSP	XLGA	Pins	BGA
3		DBZ PK					8	YFP
4		DCY DZD			YZP YZV YFM		12	ZXU
5		DBV DCK DRL DRT		DPW	YZP YEA/YZA		20	VFBGA GQN/ZQN
6		DCK DBV DRL DRT DCQ	DRS	DRY DSF	YZP YFP YEA/YZA YFC		24	VFBGA GQL/ZQL
8		DCN	DRG DRJ	DQE RSE	YFP YZP YEA/YZA		48	ZAH ZQC
9					YFP		54	ZRD
10			DRC	RSE	YZP		56	VFBGA GQL/ZQL
12			RSF RGY	RUE RUC	YFC YZT		72	ZST
14	DGV		RGT RTE RGY	RSV	YFP		83	ZRG
16	DGV		RGW RGY		YFP		96	VFBGA GKE/ZKE
20	DGV		RTW RGE RHL RGE					ZRL
24	DGV						114	VFBGA GKF/ZKF
25					YFP			
30					YFC			
32			RGJ RSM RHB					
36			RHH					
42			RVA					
48	DGV							
56	DGV		RHU RGQ					
80		01ADH2M AVC16831NN DBB						

Resources

Related Logic Resources

Little Logic Guide

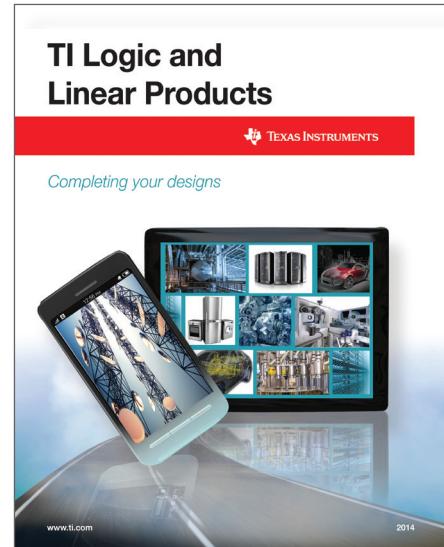
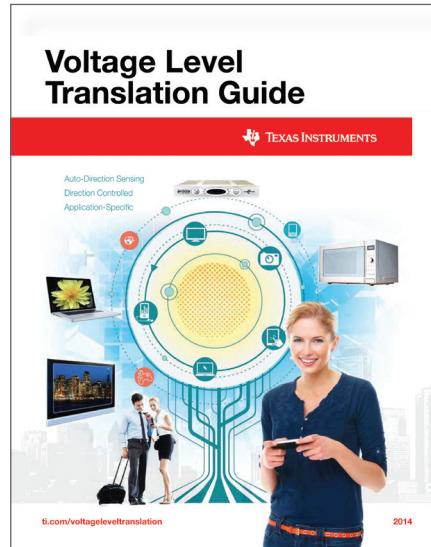
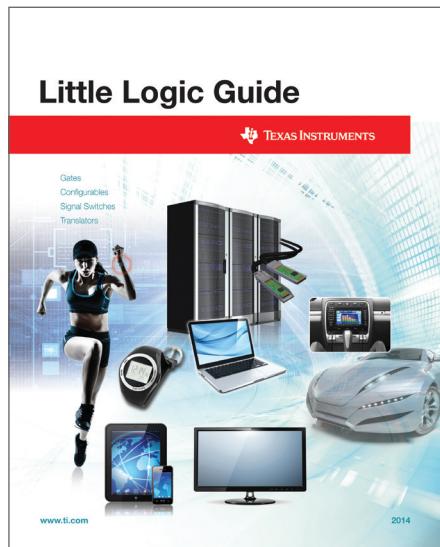
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