EXTERNAL 32.768 kHz CRYSTAL OSCILLATOR

1. Introduction

This document describes an external 32.768 kHz oscillator circuit for use with the Si4700/01/02/03. It provides the required components, the schematic, and recommended layout guidelines.

2. Oscillator Circuit Description

The circuit makes use of an unbuffered inverter, four external resistors, two capacitors, and a 32.768 kHz crystal.

3. Schematic and Bill of Materials

Figure 1 shows the external oscillator circuit schematic. Table 1 shows the bill of materials with component values, vendors, and descriptions.

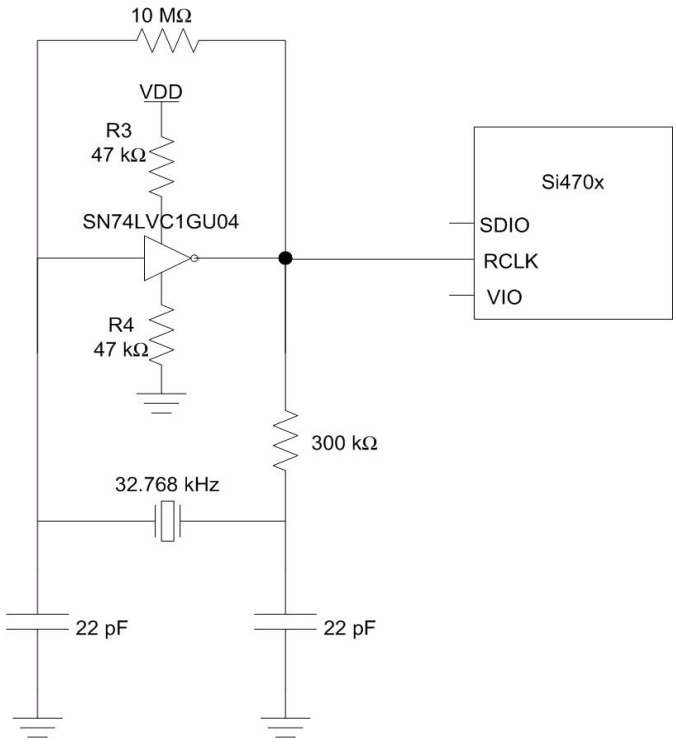

Figure 1. 32.768 kHz Crystal Oscillator Circuit Schematic

3.1. Schematic Description

Resistors R3 and R4 limit the current driving capability of the unbuffered inverter. This maintains current consumption of the circuit at approximately 8 uA when VIO = 3.3 V. Resistor R2 biases the inverter to its linear operating region to start and maintain oscillation. In order to not exceed the maximum crystal power dissipation, the total power delivered to the crystal must be controlled. The resistor R1 provides this current limiting in the example circuit shown in Figure 1 and has been tuned to ensure that the 1 uW power limit for the ECS-.327-12.5-13 is not exceeded. For a different crystal check the data sheet to ensure that the maximum power dissipation is not exceeded. Capacitors C1 and C2 provide the required load capacitance for crystal oscillation at the desired 32.768 kHz frequency.

3.2. Bill of Materials

Table 1. Bill of Materials

Item	Qty	Refdes	Description	Value	Footprint	MFG/Vendor	MFG/Vendor_PN
1	2	C1,C2	CAP,SM,0402	22 pf	CC0402	Kemet	C0402C220J5GAC-TU
2	1	R1	RES,SM,0402	300 k	RC0402	Vishay	CRCW0402304JRT7
3	1	R2	RES,SM,0402	10 M	RC0402	Vishay	CRCW0402106JRT7
4	2	R3,R4	RES,SM,0402	47 k	RC0402	Vishay	CRCW0402473JRT7
5	1	X1	32.768 kHz QUARTZ CRYSTAL, 12.5 pF, ±20 ppm, ECS-.327-12.5-13		2X6	ECS	ECS-.327-12.5-13
6	1	U1	SN74LVC1GU04, unbuffered single inverter, 1.65 to 5.5 V, SC70-5		SC70-5	TEXAS INSTRU-MENTS	SN74LVC1GU04

4. Layout Recommendations

The input of the inverter is a high impedance node and is sensitive to noise. For this reason, special care should be taken to isolate this portion of the circuit from digital signals or other noise sources. Surrounding this node by a ground trace or plane is recommended.

Figure 2 shows the sensitive portions of the circuit, and Figure 3 shows an example of using ground fill to isolate the input of the inverter from digital signals.

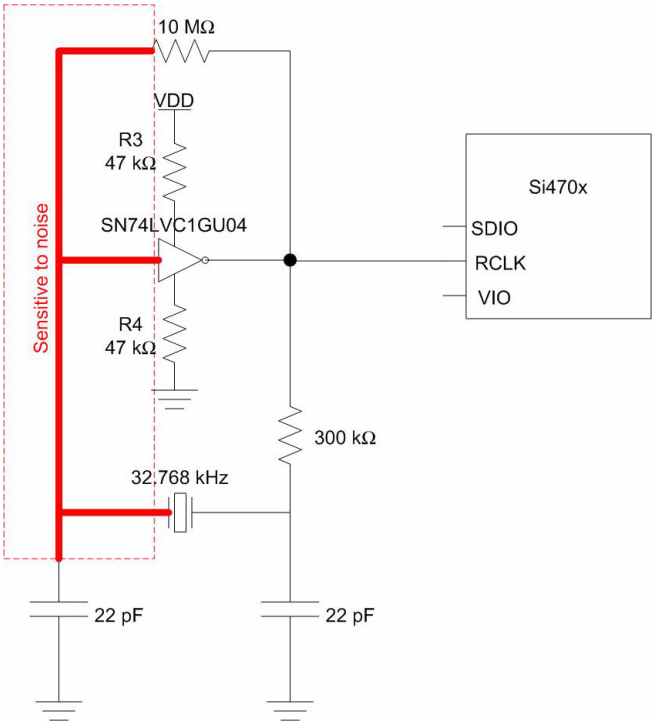

Figure 2. 32.768 kHz Crystal Oscillator Circuit with Noise Sensitive Areas Highlighted

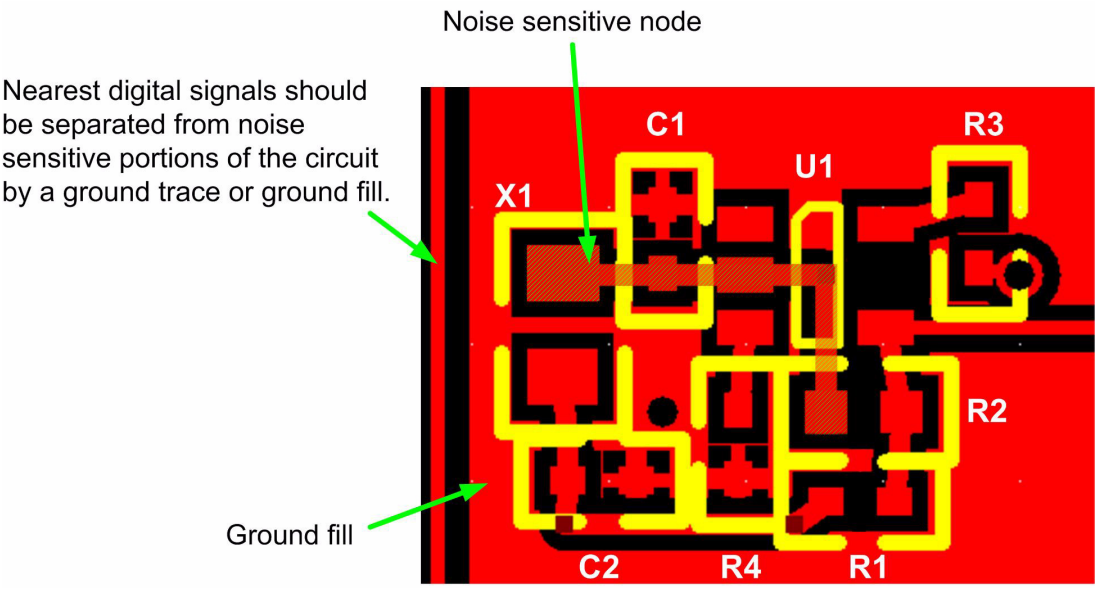

Figure 3. Example Layout Showing the Use of Ground Fill to Minimize Noise

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