COMPUTER ARCHITECTURE

32-BIT ALU & TESTBENCH

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Introduction:

In this lab, we will design the 32-bit Arithmetic Logic Unit (ALU). The ALU will become an important part of the MIPS microprocessor that we will build later labs.
In this lab we will design an ALU in SystemVerilog.we will also write a SystemVerilog testbench and testvector file to test the ALU.

SystemVerilog code:

```
module alu (input logic [31:0]    a,b,
        input logic [3:0]     f,
        output logic [31:0] y,
        output logic     [3:0] zero);

    reg [31:0] s;

    always @(*)
        begin
            case(f)

                //add
                2: y = a + b;

                //Sub
                6: y = a - b;

                //Lst
                7:
                 begin
                    s = a - b;
                      if(s[31])
                        y = 32'h00000001;
                      else
                        y = 32'h00000000;
                 end

                //And
                1: y = a & b;
```

```
                //Or
                3: y = a | b;
                default: y = 32'h00000000;
            endcase

            //set zero flag
            zero = y ? 0 : 1;

        end

endmodule
```

Simulation and Testing:

Now we can test the 32-bit ALU in ModelSim through a set of input vectors in the test vectors file.

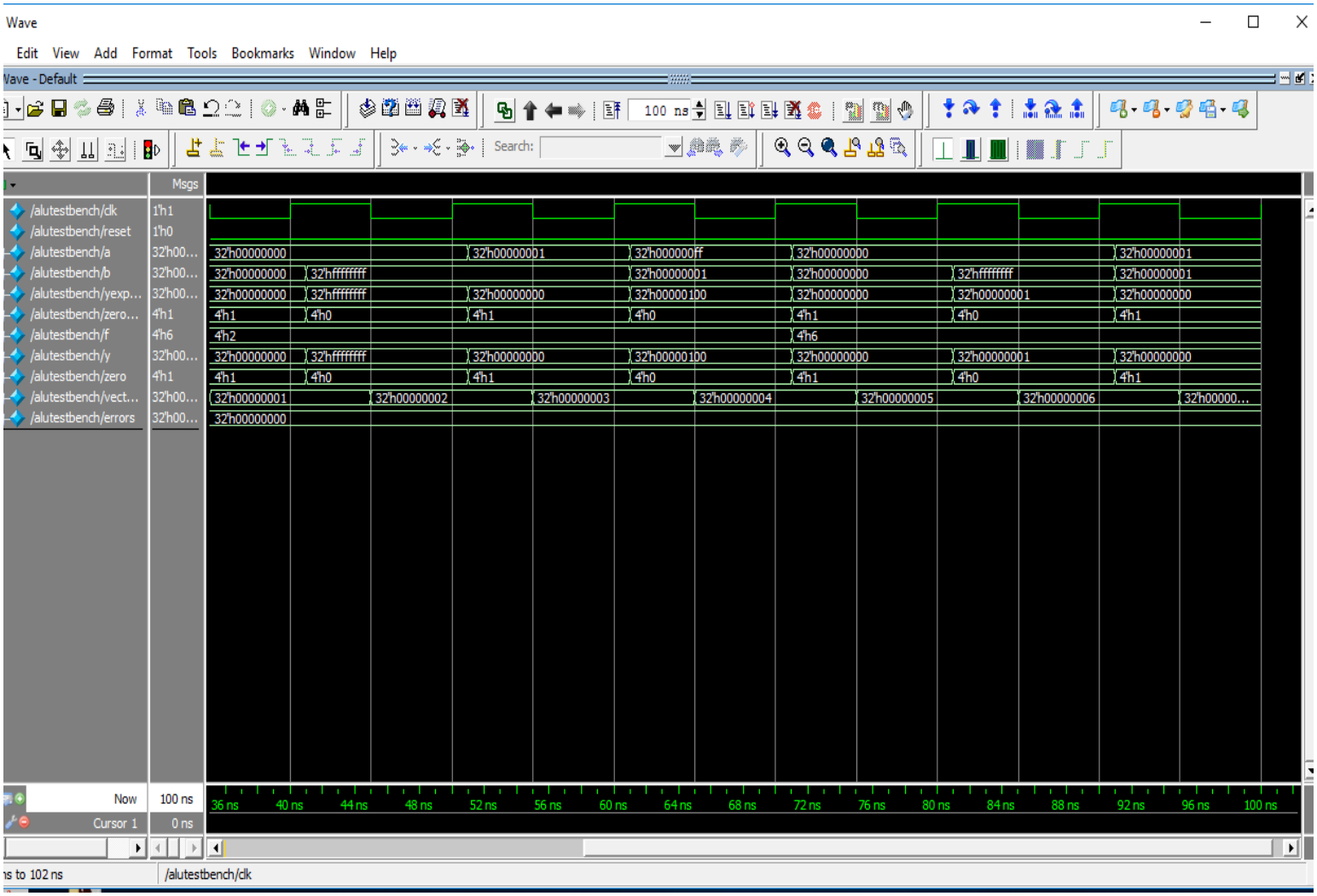
```
00000000_00000000_2_00000000_1
00000000_ffffffff_2_ffffffff_0
00000001_ffffffff_2_00000000_1
000000ff_00000001_2_00000100_0
00000000_00000000_6_00000000_1
00000000_ffffffff_6_00000001_0
00000001_00000001_6_00000000_1
00000100_00000001_6_000000ff_0
00000000_00000000_7_00000000_1
00000000_00000001_7_00000001_0
00000000_ffffffff_7_00000000_1
00000001_00000000_7_00000000_1
ffffffff_00000000_7_00000001_0
ffffffff_ffffffff_1_ffffffff_0
ffffffff_12345678_1_12345678_0
12345678_87654321_1_02244220_0
00000000_ffffffff_1_00000000_1
ffffffff_ffffffff_3_ffffffff_0
12345678_87654321_3_97755779_0
00000000_ffffffff_3_ffffffff_0
00000000_00000000_3_00000000_1
```

And we will use the testbench file to test the ALU and for simulation.

```
module alutestbench();

    reg clk,reset;
    reg [31:0] a, b, yexpected;
    reg [3:0]zeroexpected;
    reg [3:0] f;
    wire[31:0] y;
    wire[3:0] zero;
    reg [31:0] vectornum, errors;
    reg [103:0] testvectors [10000:0];

    //instansiate device under test
    alu dut(a, b, f, y, zero);

    //generate clock
    always
        begin
            clk = 1; #5; clk = 0; #5;
        end

    //at start of test, load vectors and pulse
      reset
    initial
        begin
            $readmemh("vectors.tv",testvectors);
            vectornum = 0; errors = 0;
            reset = 1; #27; reset = 0;
        end

    //apply test vectors on rising edge of clk
    always @(posedge clk)
        begin
            #1; {a,b,f,yexpected,zeroexpected}
=testvectors[vectornum];

        end
```

```
    //check results on falling edge of clk
    always @(negedge clk)

        if(~reset)
        begin
            if(y !== yexpected | zero !==
zeroexpected)
            begin
                $display("Error: inputs =
a:%h,b:%h,F:%h",a,b,f);
                $display("Y Output = %h (%h
expected)", y,yexpected);
                $display("Zero Output = %h (%h
expected)", zero,zeroexpected);
                errors = errors + 1;
            end

            vectornum = vectornum + 1;

            if(vectornum===21)
            begin
                $display("%d tests completed
                with %d errors",
                vectornum,errors);
                $finish;
            end

        end


endmodule
```

Screenshot of Test waveforms



Hours spent on project: 1½ days on average.

Thank You