Marble – datasheet

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Michał Gąska, michalgaska2@gmail.com

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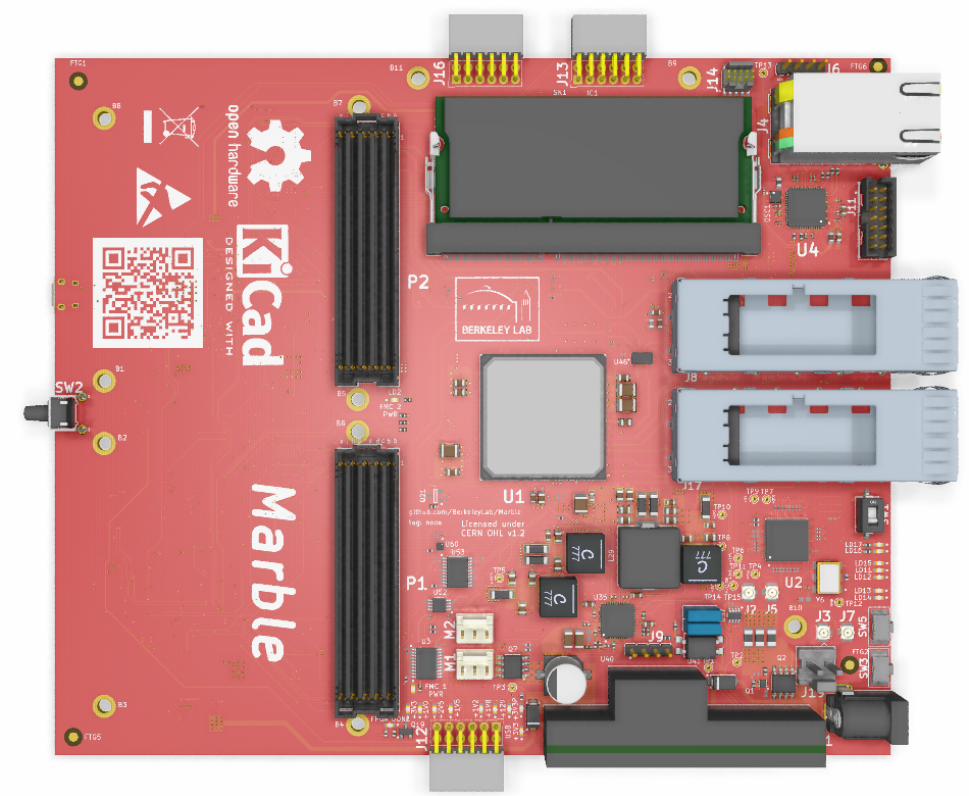

Introduction

Marble is a fully open source dual FMC currier board designed for The Accelerator Technologies Group of the Engineering Division of Lawrence Berkeley National Laboratory. This document presents the technical documentation of the Marble module divided into individual functional sections. Design files are made in KiCad and are licensed under the CERN OHL v. 1.2.

Contents

1 Overview to Marble module

> Design files are open source and can be downolad from Gilhub:
> https://github.com/BerkeleyLab/Marble

Marble is a dual FMC currier module based on an Kintex-7 FPGA. The block diagram of the module is shown in figure 1.

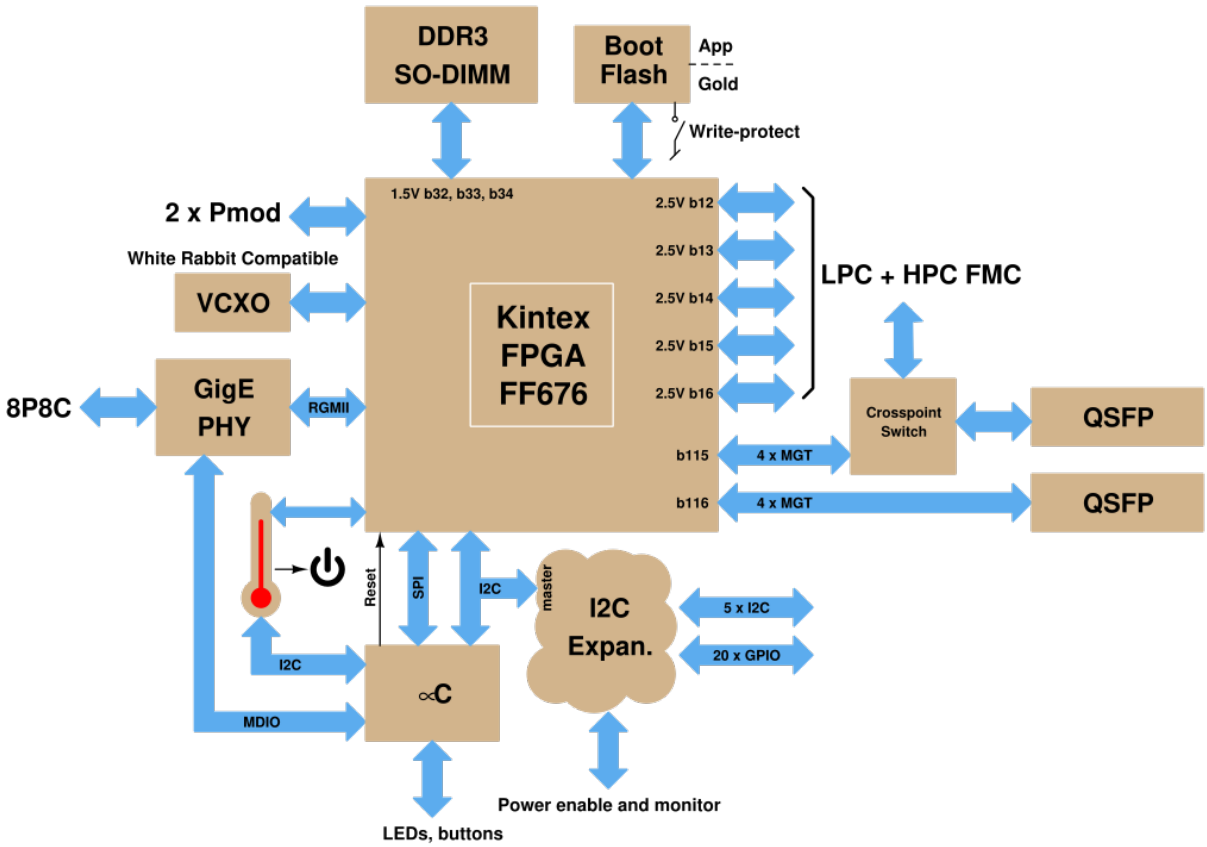

Figure 1: Marble block diagram.

The board has the following functionalities and features:

1. Xilinx Kintex-7 FPGA XC7K160T-2FFG676C
2. Supports FPGA golden image
3. DDR3 204-SODIMM memory module connector. The board supports up to 4 GB memory.
4. Two FMC HPC connectors but not all signals are connected to the FPGA.
5. 1Gb Ethernet with PoE
6. Built-in clock generator that supports White Rabbit synchronization
7. Various input clock configurations
8. Two QSFP cages that support data transfer up to 40 GB/s each

9. Built-in USB JTAG which works with OpenOCD
10. Module Management Controller with UART console

2 FPGA

The board is equipped with FPGA Kintex-7 XC7K160T-2FFG676C and the occupancy of each bank is shown below:

1. bank 12 HR +2.5V FMC2 LA 00-16 (plus SPI, Self JTAG)
2. bank 13 HR +2.5V FMC2 HA
3. bank 14 HR +2.5V FMC2 LA 17-33 (plus config, PMOD)
4. bank 15 HR +2.5V FMC1 LA 00-16 (plus I2C, UART, PMOD)
5. bank 16 HR +2.5V FMC1 LA 17-33 (plus RGMII)
6. bank 32 HP +1.5V DDR3
7. bank 33 HP +1.5V DDR3 (plus PMOD, White Rabbit)
8. bank 34 HP +1.5V DDR3

The S25FL128SAGMFIR01 confuguration memory is connected to the FPGA chip. By default, the FPGA chip loads the configuration from the flash memory after correct power cycle. The module is equipped with a switch (fig 2) that blocks the programming of the configuration memory. When the switch is in the ON position, Write Protection is enabled. WP signal status can be read via I2C IO expander.

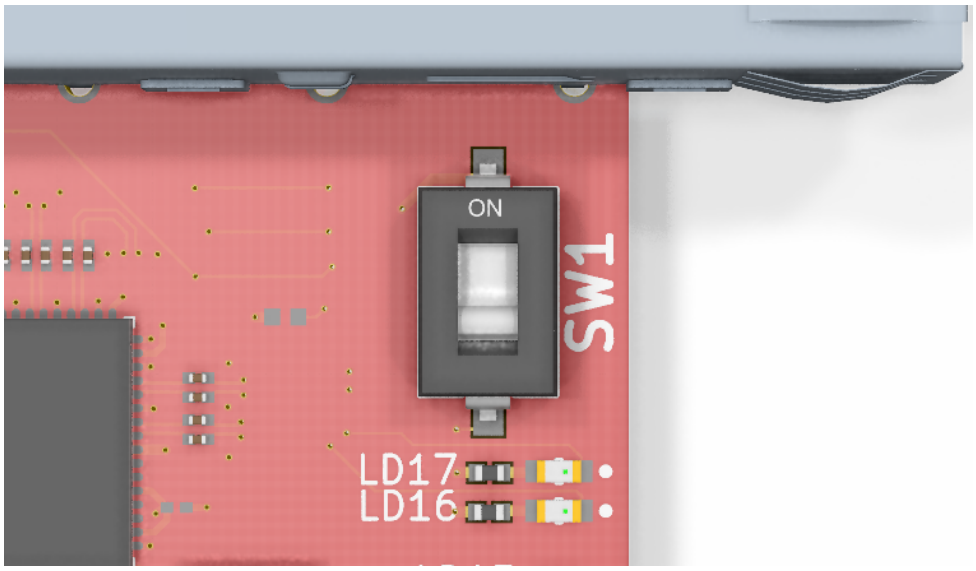

Figure 2: Memory write protection switch.

2.1 FPGA reset

During power system startup, the U60 chip keeps the PROGRAM_B signal low. When a valid supply voltage is detected on the last power-up sequence, U60 changes state on the PROGRAM_B signal which causes the configuration file to be loaded from flash memory.

The SW5 button is designed to manually reset the FPGA chip. Additionally, the reset signal can be provided from the MMC.

2.2 JTAG

There are 3 sources of JTAG for FPGA:

1. external JTAG (highest priority)
2. internal USB-JTAG (midle priority)
3. selfe JTAG (lowest priority)

2.2.1 External JTAG

When the external JTAG is connected to J11, GNDDetect signal from the connector switches the multiplexer to pass JTAG signals from the connector to the FPGA, after un plugging cable, the GNDDetect signal is not present and the multiplexer conects internal USB-JTAG to FPGA.

When external JTAG is connected, any other JTAG sources are not available.

2.2.2 Internal USB-JTAG

Internal USB-JTAG is done by using the first data channel of FT4323 which can work as a JTAG. When the micro USB cable is connected, +5V from USB bus switches the multiplexer to pass data from FT4323 to FPGA.

2.2.3 Selfe JTAG

Internal selfe JTGA can be used only when USB cable and external JTAG are not connected. In this configuration FPGA JTAG signals are connected to FPGA Bank 12:

1. JTAG TDI » Self_FPGA_TDI (IO_L10P)
2. JTAG TCK » Self_FPGA_TCK (IO_L10N)
3. JTAG TMS » Self_FPGA_TMS (IO_L20P)
4. JTAG TDO » Self_FPGA_TDO (IO_L20N)

2.3 LEDs

Two general purpose LEDs are connected to the FPGA chip:

1. LED16 - connected to pin IO_L18P_33
2. LED17 - connected to pin IO_25_33

3 SO-DIMM

The size of the DDR3 memory can be determined by the user by assembling the appropriate SO-DIMM module to the board. The use of a 204 pin SO-DIMM connector allows up to 4 GB of RAM to be connected to the FPGA. An I2C interface is provided to the memory module so that additional information about the module can be read. The default power supply for memory and HP banks is set to 1.5V and can only be changed by changing resistors. ECC is not supported by the module.

4 GTH Routing

Gigabit transceivers routing can bo configured be the microcontroller. Transceivers form Bank 116 are permanrntly connected to QSFP module. Transceivers form Bank 115 can be routed in 3 ways:

1. 4 transceivers connected to other QSFP module
2. 4 transceivers connected to FMC P2
3. 2 transceivers connected to FMC P2 and 2 transceivers connected to FMC P1

Transceivers routing configuration can be set by the microcontroller. Three signals control the multiplexers which provide high quality signal switching. Gigabit multiplexer switching can be done from the UART console. By default, the multiplexers are set to route signals to the second QSFP connector. In the table 1, the MUXx columns correspond to the controlling logical state.

MUX3	MUX2	MUX1	MGT4	MGT5	MGT6	MGT7
0	0	0	FCM2-DP0	FMC2-DP1	FMC2-DP2	FMC1-DP1
0	0	1	FCM2-DP0	FMC2-DP1	FMC1-DP0	FMC1-DP1
0	1	0	FCM2-DP0	FMC2-DP1	FMC2-DP2	FMC2-DP3
0	1	1	FCM2-DP0	FMC2-DP1	FMC1-DP0	FMC2-DP3
1	X	X	QSFP2:3/10	QSFP2:1/12	QSFP2:2/11	QSFP2:4/9

Table 1: GTH transceivers routing table

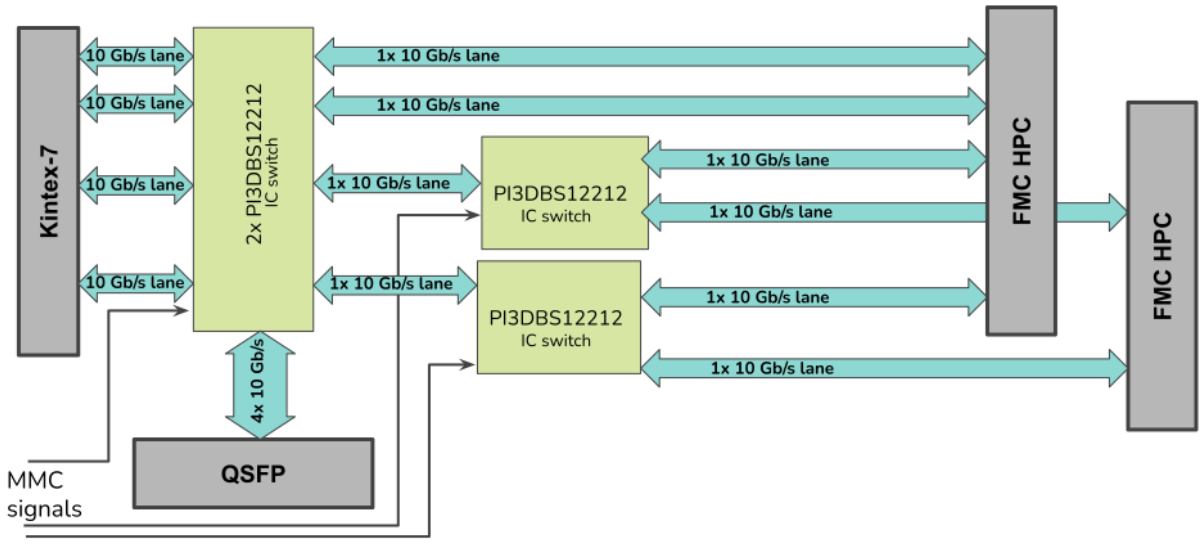

Figure 3: Transceivers routing block diagram.

5 Clocking

This section describes how and where clock signals are routed. There are 3 on-board clock sources:

1. White Rabbit clock generator - provides following clocks:
   (a) 125 Mhz connected to the clock mux
   (b) 125 Mhz connected to the FPGA bank 33; can operate as a DDR3 reference clock
   (c) 25 Mhz for MMC and Ethernet PHY
2. Si570 - provides variable clock frequencies for 10 Mhz to 280 Mhz; connected to the clock mux
3. VCXO - provides 20 Mhz clock for FPGA bank 33

Marble supports external clock sources from FMC and from U.FL connectors. Thanks to the clock mux, any clock input can be connected to any FPGA MGT clock inputs. Clock routing and Si570 frequency can be changed over I2C from the house-keeping microcontroller.

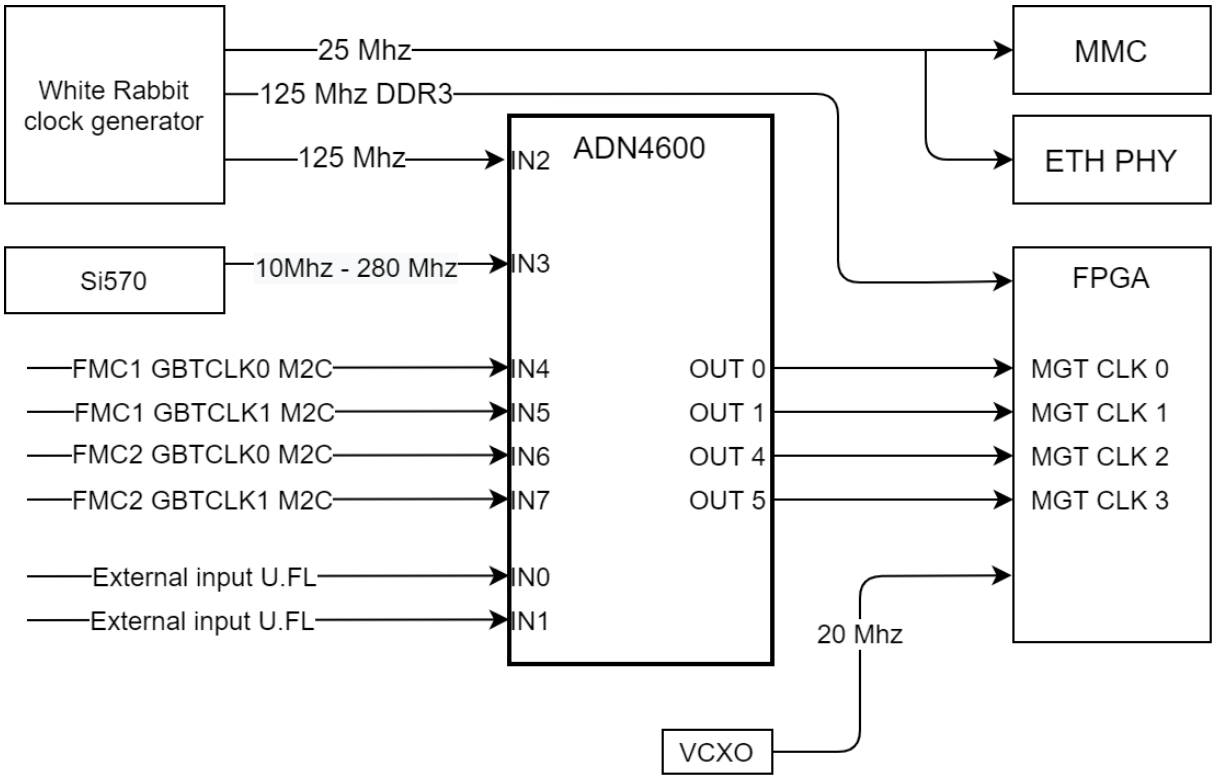

Figure 4: Marble clocking scheme

6 PMOD connectors

Marble has 3 PMOD connectors that support 3.3V logic level:

1. 2 of them are connected to FPGA (J12 and J13)
2. 1 is connected the MMC (J6)

	PMOD 1 (J12) FPGA	PMOD 2 (J13) FPGA	PMOD (J16) MMC
Pmodx_C_0	IO_L6N_14	IO_L7P_33	PB9 (SEL)
Pmodx_C_1	IO_L7N_14	IO_L2N_33	PC3 (MOSI)
Pmodx_C_2	IO_25_14	IO_L4N_33	PC2 (MISO)
Pmodx_C_3	IO_L7P_14	IO_L7N_33	PB10 (SCK)
Pmodx_C_4	IO_0_14	IO_L2P_33	PB14 (EINT1)
Pmodx_C_5	IO_L5N_15	IO_L8P_33	PB15
Pmodx_C_6	IO_L4P_15	IO_L4P_33	PD6 (UART4 RX)
Pmodx_C_7	IO_L5P_15	IO_L3N_33	PD5 (UART4 TX)

Table 2: PMODs connectors pins assignment

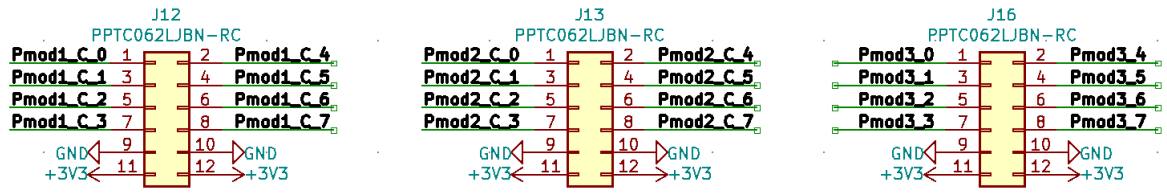

Figure 5: PMODs pinout

7 QSFP

Marble is equipted with 2 QSFP cages (6). Each can support 40 Gb/s of data transfer:

1. QSFP number 1 - high-speed lines are directly connected to the FPGA bank 116
2. QSFP number 2 - high-speed lines are connected to the FPGA bank 115 through the gigabit multiplexer.

QSFPs control signals are connected to the I2C IO expander (U34)(7) which is accessible from FPGA or MMC.

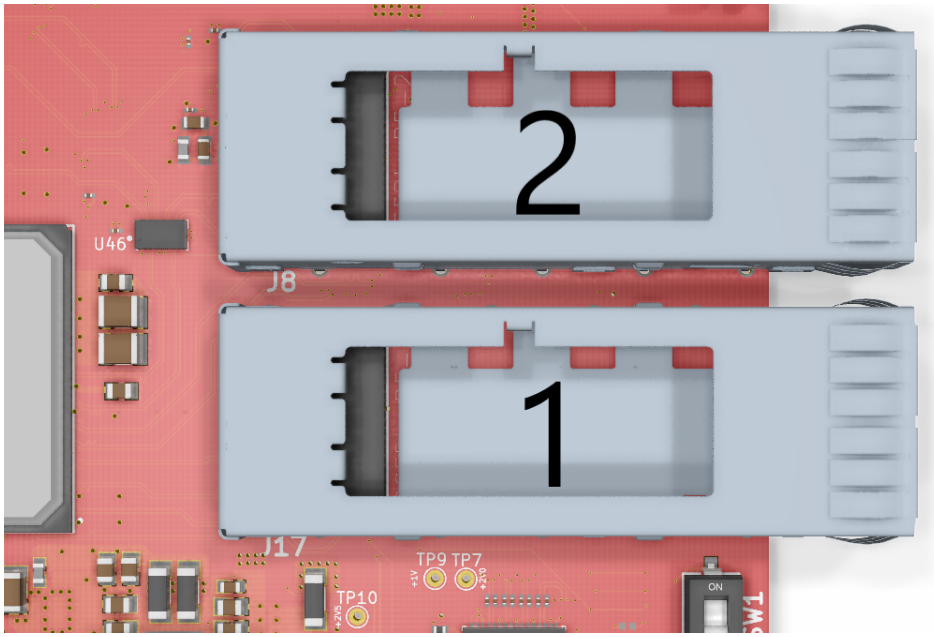

Figure 6: QSFP cages

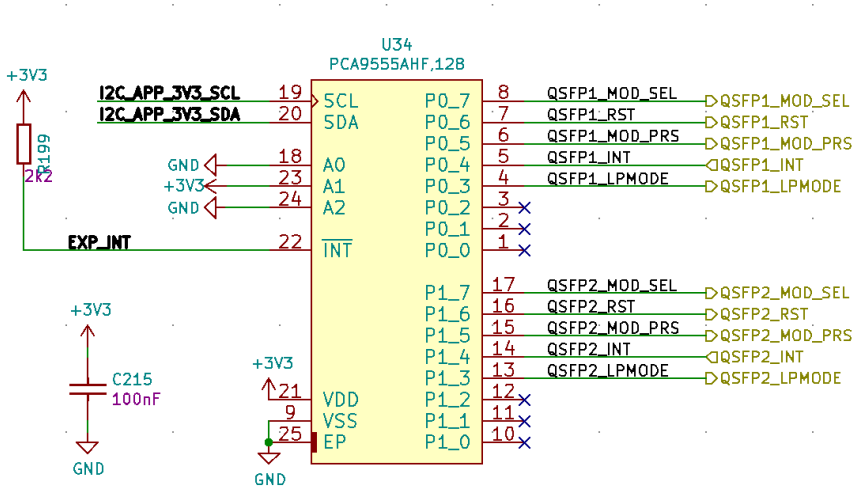

Figure 7: I2C IO expander which controls QSFPs signals

8 Ethernet

Marble is equipped with Ethernet PHY (88E1512) which supports 10/100/1000BASE-T. PHY is connected to the FPGA bank 16 via RGMII interfejs:

RGMII signal	FPGA pin
RGMII_RXD0	IO_L4N_16
RGMII_RXD1	IO_0_16
RGMII_RXD2	IO_L1P_16
RGMII_RXD3	IO_L1N_16
RGMII_RX_DV	IO_L4P_16
RGMII_RX_CLK	IO_L14P_16
RGMII_TXD0	IO_L6N_16
RGMII_TXD1	IO_L6P_16
RGMII_TXD2	IO_L8N_16
RGMII_TXD3	IO_L8P_16
RGMII_TX_EN	IO_L10P_16
RGMII_TX_CLK	IO_L11N_16
PHY_RSTn	IO_L10N_16

Table 3: RGMII pins assignment

Using MDIO interface PHY can be monitored by housekeeping microcontroller. IP address and MAC address are stored in the MMC's internal EEPROM memory (EEPROM functionality is emulated in the internal flash). The MDIO address is set to 1 but it can be changed by changing the resistor on the module.

9 FMC

The connection of both FMC connectors is shown below:

1. **FMC P1** signal connection:
   (a) LA00...LA33 - connected to FPGA banks 15 and 16.
   (b) HA00...HA23 - *not connected*.
   (c) HB00...HA21 - *not connected*.
   (d) CLK[0..1]_M2C - connected to FPGA bank 15.
   (e) GBTCLK[0..1]_M2C - connected to CLK MUX IN4 and IN5.
   (f) DP[0]_M2C - connected to high speed MUX.
   (g) DP[0]_C2M - connected to high speed MUX.
   (h) JTAG - conneted to MMC.
   (i) I2C - connected to I2C bus shared with MMC and FPGA
2. **FMC P2** signal connection:
   (a) LA00...LA33 - connected to FPGA banks 12 and 14.
   (b) HA00...HA23 - connected to FPGA bank 13.
   (c) HB00...HA21 - *not connected*.
   (d) CLK[0..1]_M2C - connected to FPGA banks 12 and 14.
   (e) GBTCLK[0..1]_M2C - connected to CLK MUX IN6 and IN7.
   (f) DP[0..3]_M2C - connected to high speed MUX.
   (g) DP[0..3]_C2M - connected to high speed MUX.
   (h) JTAG - conneted to MMC.
   (i) I2C - connected to I2C bus shared with MMC and FPGA

10 USB-UART

The USB-UART bridge (FT4232H) has 2 channels of UART:

10.1 FPGA UART

FPGA UART occupies FT4323's channel 3. UART signals are connected to bank 15 to pins:

1. TX input IO_L1P_15
2. RX output IO_0_15

10.2 MMC UART

MMC UART occupies FT4323's channel 4. UART is used as a housekeeping microcontroller console. Terminal configuraton is 1N8 115200 baudrate.

11 Power

The power for the module is provided by TE Connector(3-641119-2) - J19 (fig. 8) or by standard barrel connectos (Type A: 5.5 mm OD, 2.1 mm ID) - J1. Input voltage range: 10V - 18V. Additionally, PoE can be used to power the module.

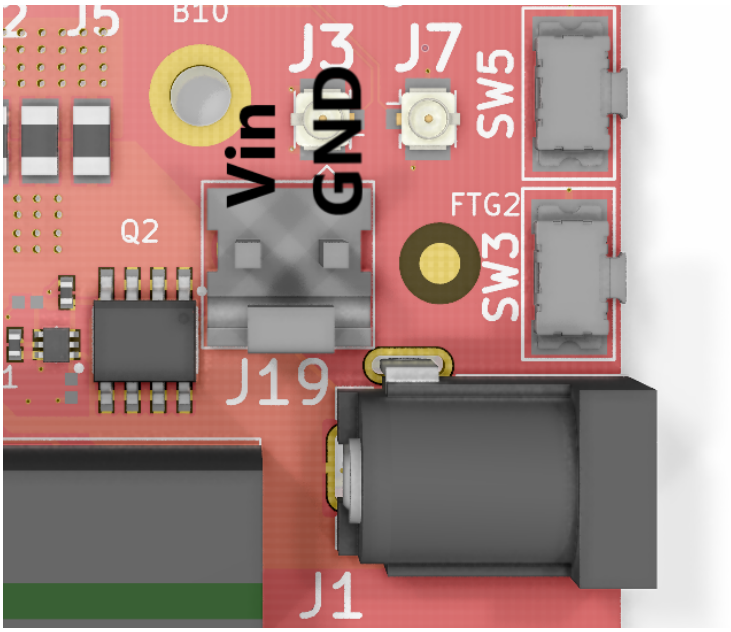

Figure 8: J19 connector with indicated Vin and GND

When the power is connected, the board starts automatically. If there is a failure of any power rail, the LED corresponding to it will not light up.

Block diagram of Marble's power tree is shown in figure 9. The USB-UART bridge is powered from the micro usb connector via an converter (U22). The supervising microcontroller has a separate converter (U18) connected directly to the power input. The main voltages supplying the FPGA are produced by U35 - the programmable power management system. U35 turns on the individual power channels in the proper sequence and provides power to the additional converter (U58) and LDOs (U31, U36, U37, U47).

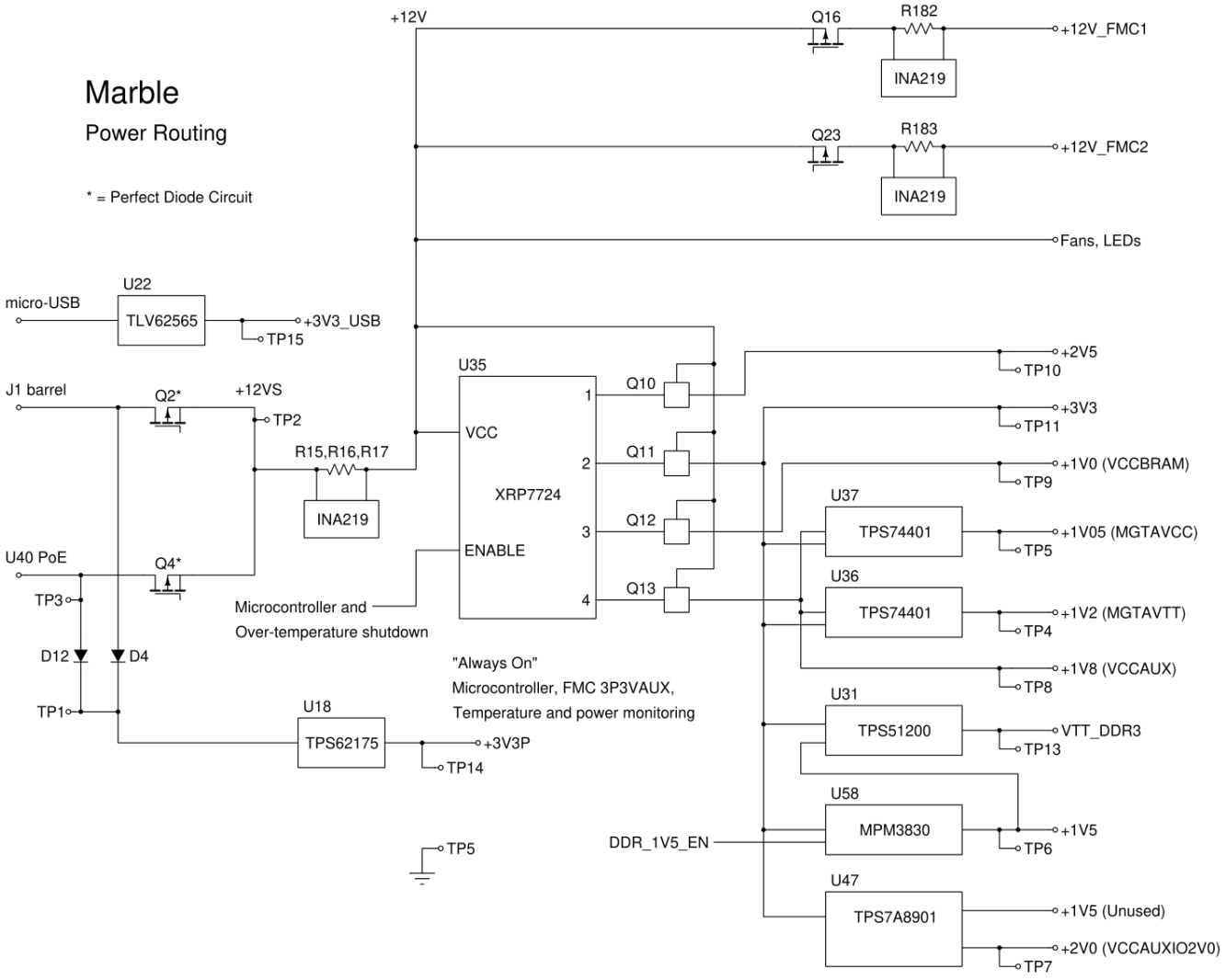

Figure 9: Marble power routing

Power supply features:

1. Over-temperature protection.
2. Power rails for the FPGA can be switched off and on by the microcontroller.
3. All power rails generated by XRP7724 can be monitored by the microcontroller and they are equipped with over-current protection.
4. Current consumption, voltage and rails status can be read by microcontroller.
5. The presence of the power rails is indicated by LED diodes
6. 12V power supply for both FMCs can be controlled independently by the microcontroller. Additionally, current can be measured.

11.1 FANs controller

The fan control and temperature monitoring of the FPGA chip was done with the MAX6639 chip. The fans can be automatically controlled by measuring the temperature on the diode

inside the FPGA. If the temperature exceeds a preset alarm threshold an ALERT signal will be issued. If the temperature continues to rise and exceeds another threshold, an "OVER-TEMP" signal will be issued and the FPGA will automatically power down. Through the I2C interface it is possible to read and write all configuration registers. Additionally, signals from both fan tachometers are monitored.

Two additional temperature sensors based on the LM75 chip provide temperature measurements around the main power converter and under the FMC P1 card. By default they are set to shut down the main power inverter when it exceeds 75 degrees.

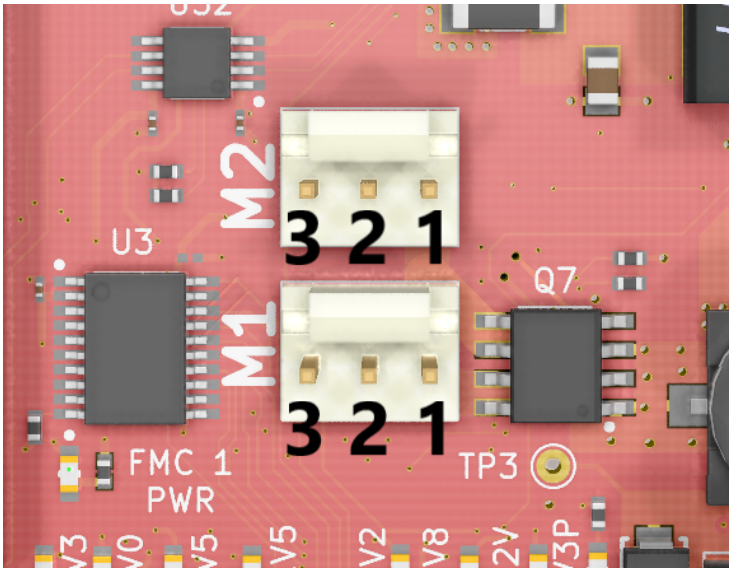

Figure 10: FANs connectors

	M1		M2
1	GND	1	GND
2	12V	2	12V
3	Tacho	3	Tacho

Table 4

12 MMC

Module Management Controller (MMC) is based on STM32F207 microcontroller and provides housekeeping functions such as:

1. Simple UART console over USB-UART bridge to control all functions
2. Monitoring voltage, current consumption and warnings signals on power rails
3. Temperature monitoring at several locations
4. Controlling and monitoring fans

5. Configuring clock multiplexer
6. Configuring MGT switches
7. Reseting FPGA and controling booting
8. Programming Power Management Controller
9. Controlling FMC power delivery and the presence of the cards
10. Ensuring communication over MDIO with Ethernet PHY
11. Ensuring communication over SPI with FPGA

MMC programing can be done by using external tools such as STM Nucleo-SWD programmer, SEGGER J-LINK Mini

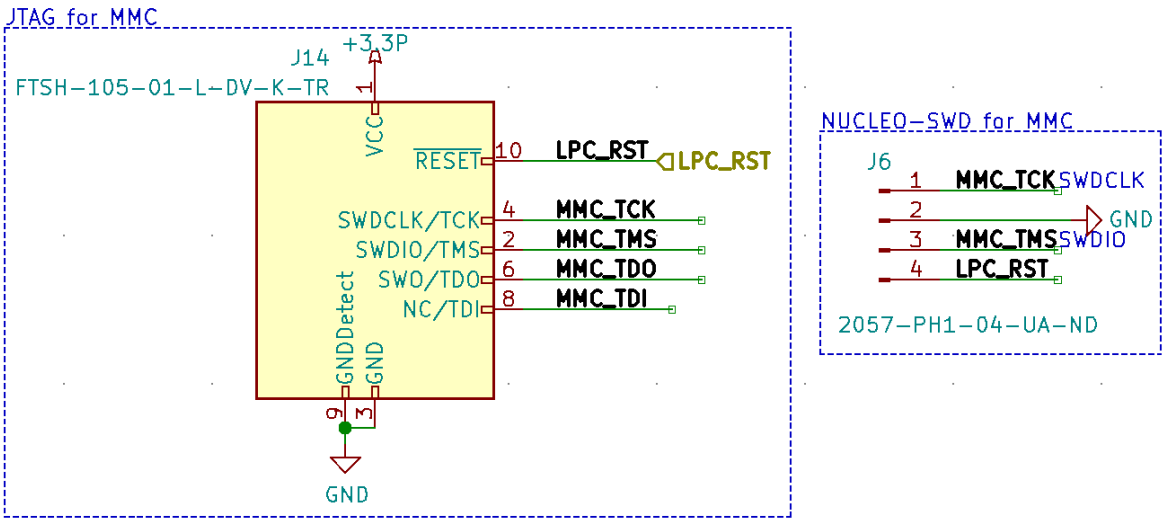

Figure 11: MMC JTAG and SWD interfaces

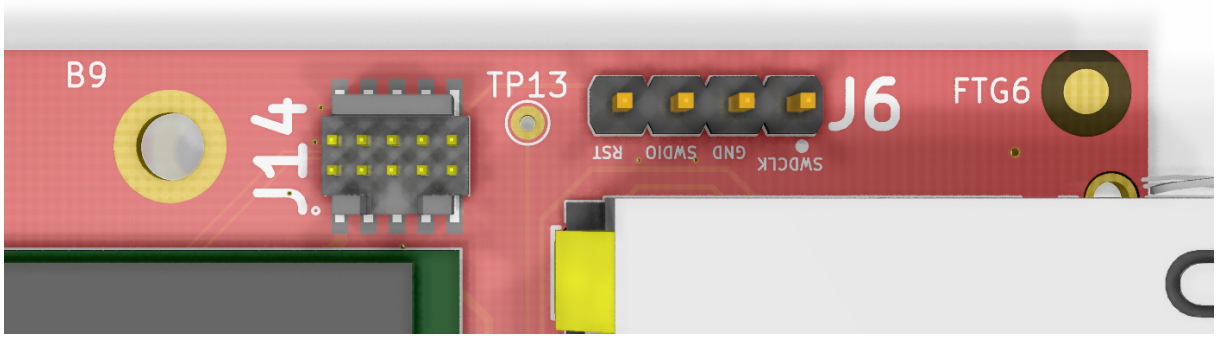

Figure 12: MMC JTAG and SWD connectors

12.1 LEDs

Three general purpose LEDs are connected to the MMC chip:

1. LED11 - connected to pin PE1
2. LED12 - connected to pin PE2
3. LED15 - connected to pin PE0

12.2 I2C Tree

Marble is equipped with two I2C buses (block diagram is shown in fig. 13):

1. I2C_PM - supports devices for power management, temperature measurement and fan control
2. I2C_FPGA -This bus is shared between the MMC and the FPGA chip. Through an I2C switch, it is connected to:
   (a) FMC 1 and FMC 2
   (b) Clock mux
   (c) SO-DIMM module
   (d) QSFP 1 and QSFP 2
   (e) Current measurement devices, Si570 and IO expanders

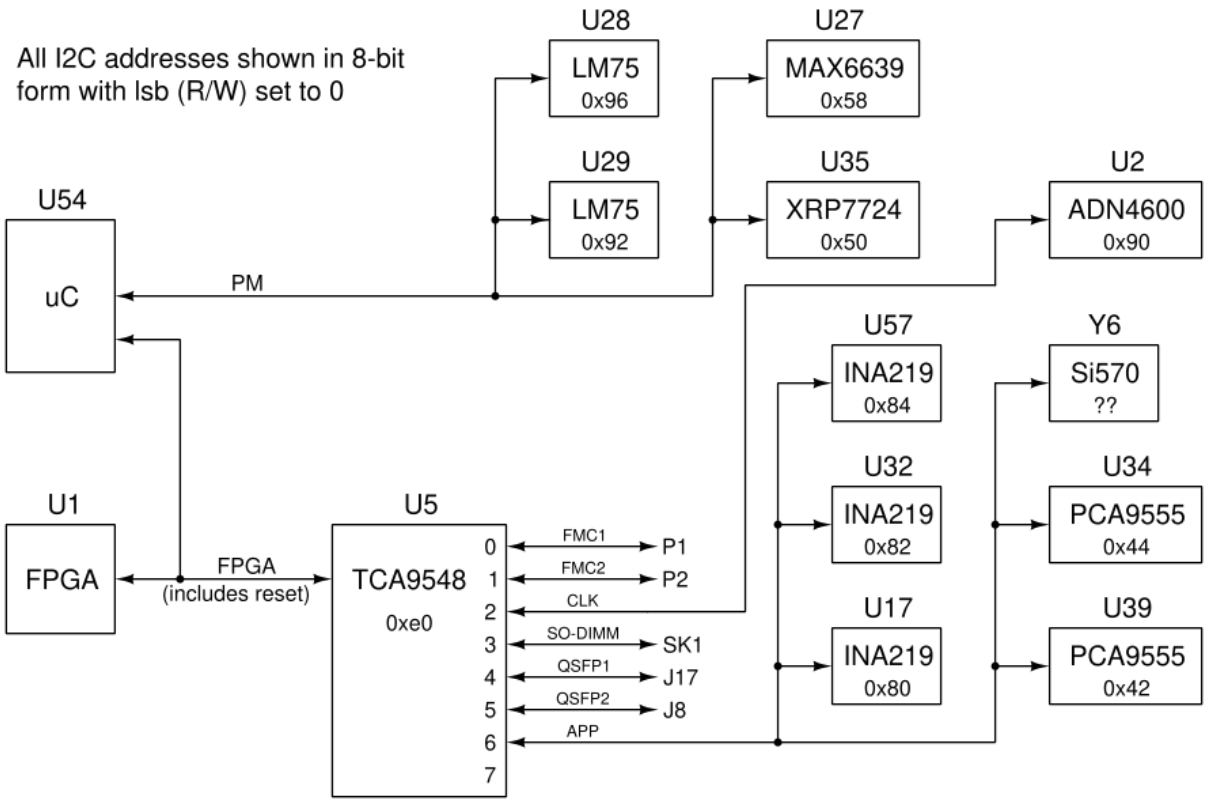

Figure 13: I2C map

13 Mechanical dimensions

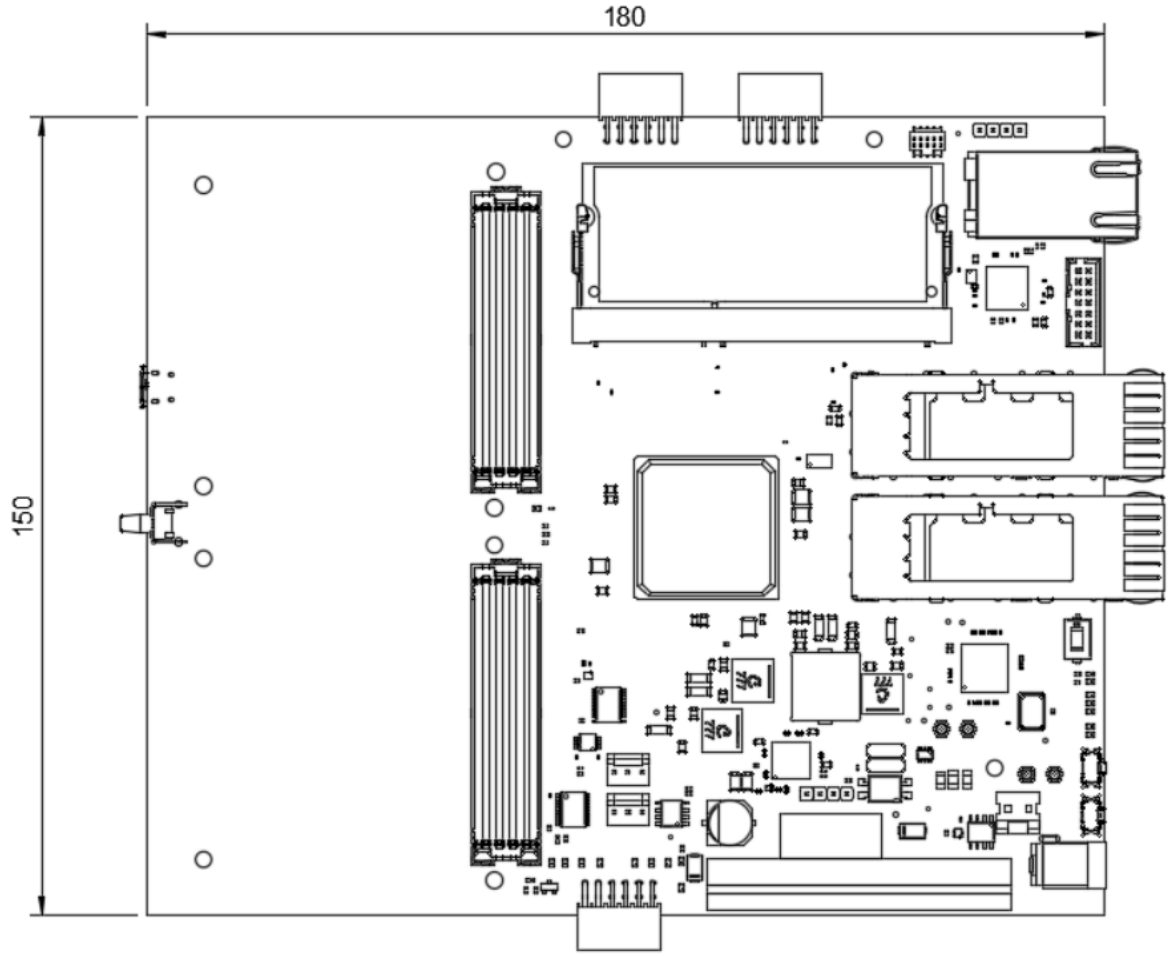

Figure 14: The mechanical dimensions of Marble

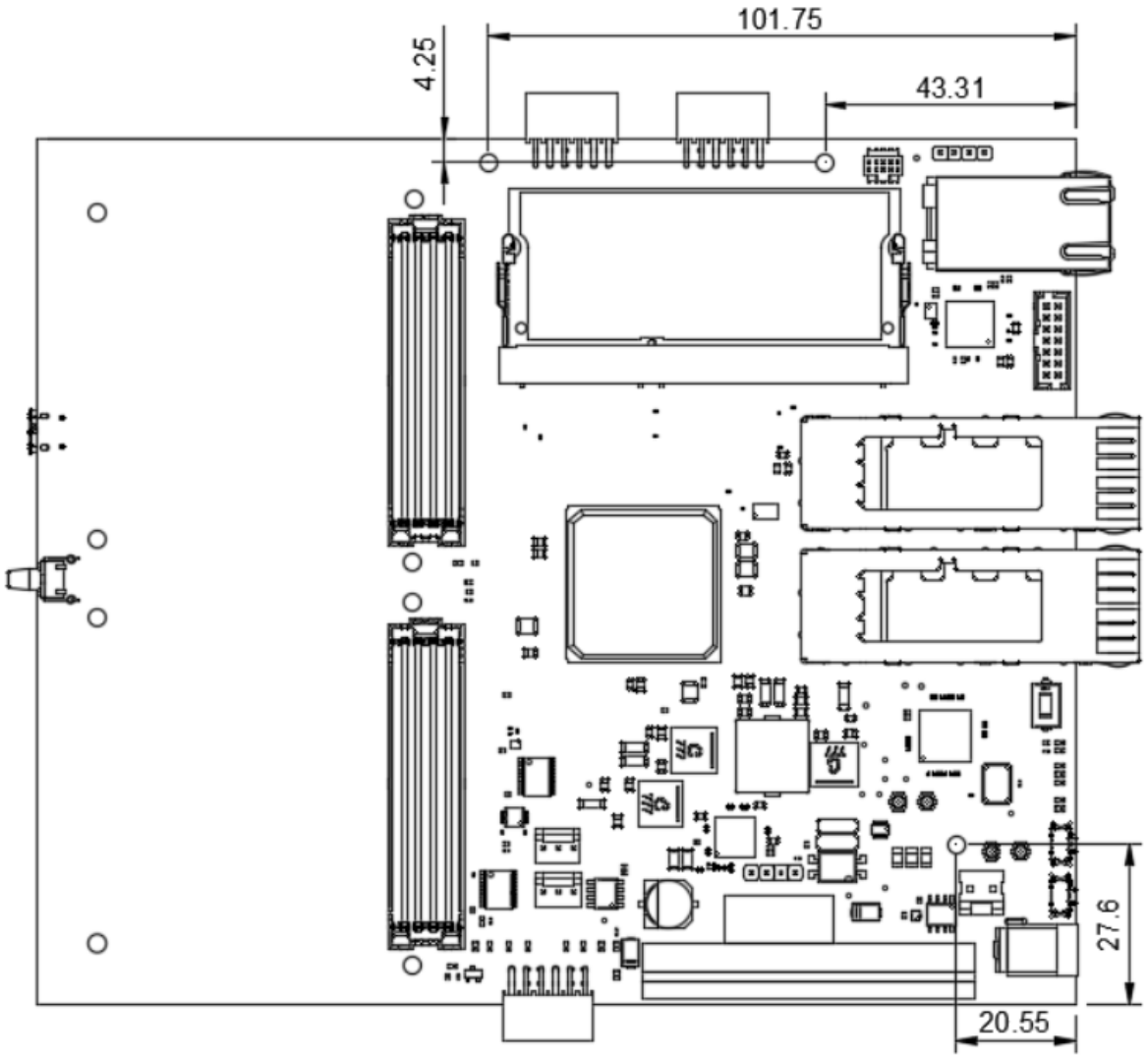

Figure 15: The position of mounting holes

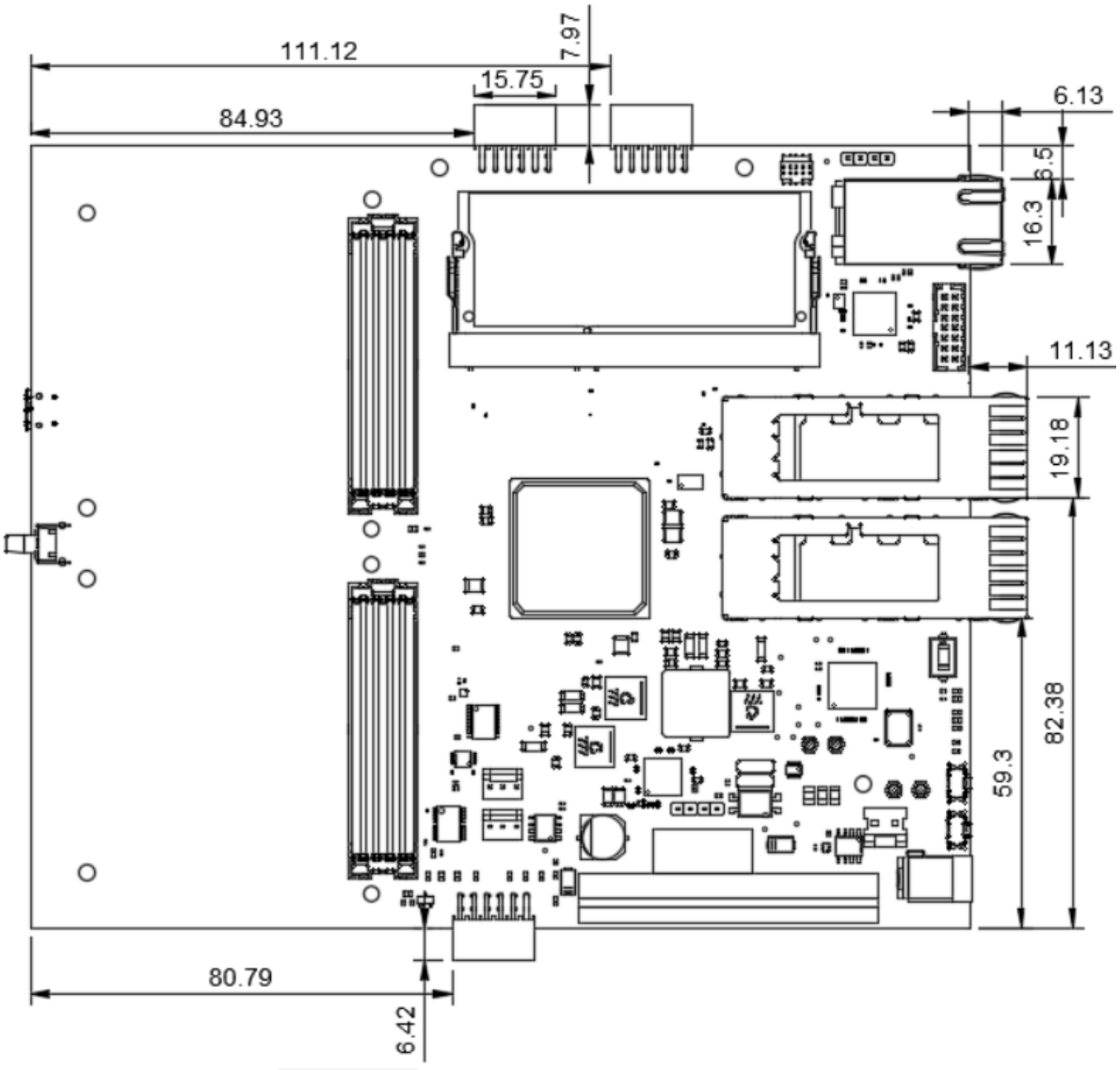

Figure 16: The position of the protruding connectors

14 Appendix

14.1 Power supply test points

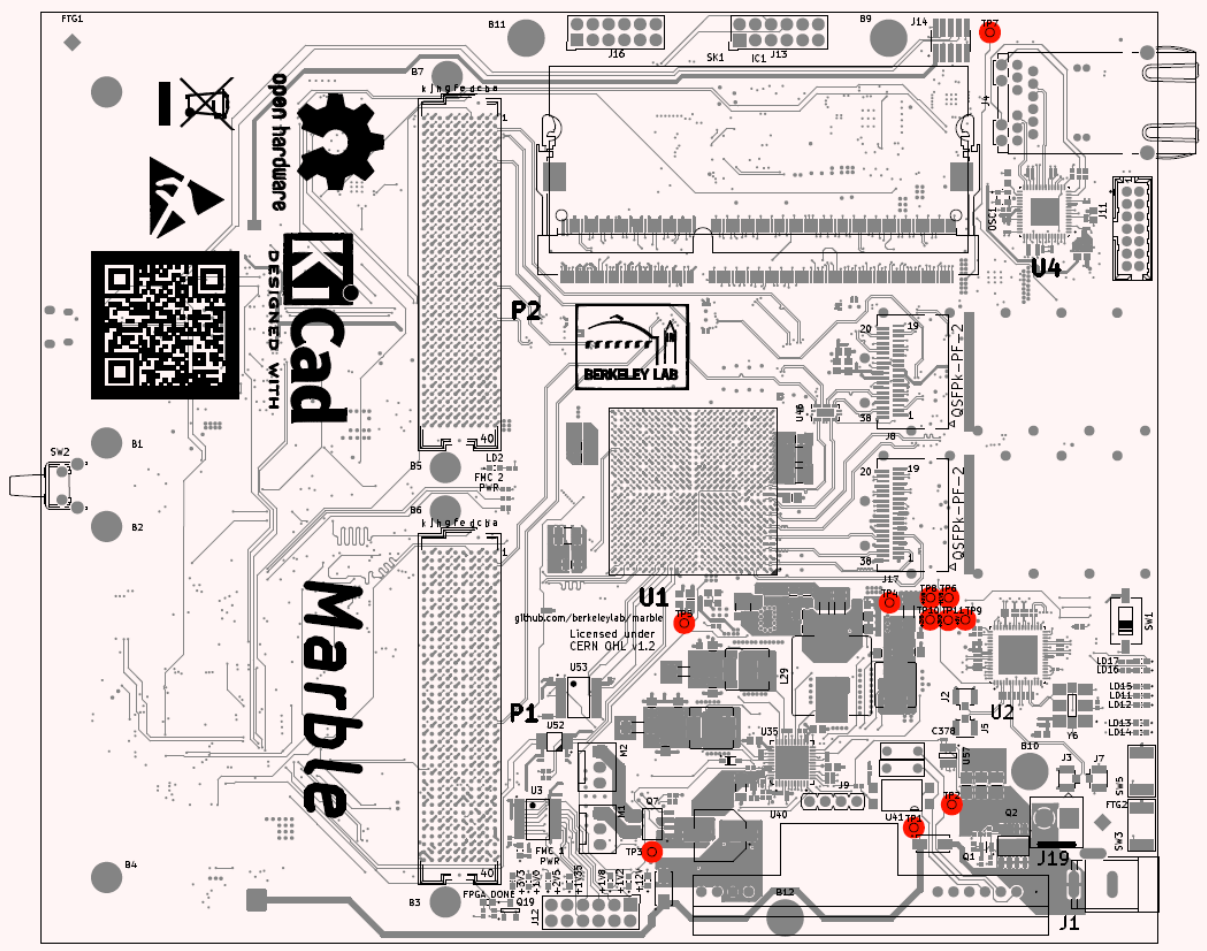

Figure 17: Test point map

TODO: add an individual number for test points and the description

References