AN0002: Hardware Design Considerations

This application note is intended for system designers who require an overview of the hardware design considerations for EFM32 32-bit MCUs and the MCU portion of EZR32 Wireless MCU and EFR32 Wireless Gecko portfolio devices.

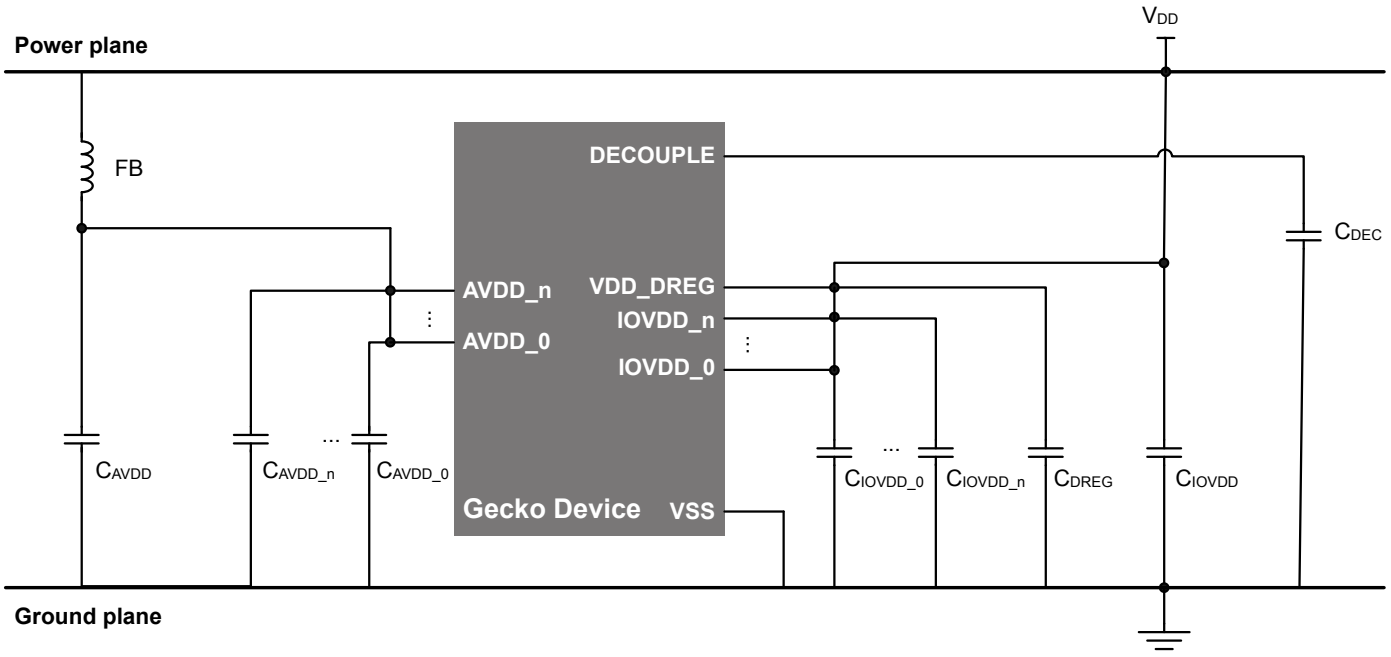
Topics that are covered specifically are how to provide a robust power supply to the chip, connection to the debug interface, and external clock sources. The scope is to provide an introduction to potential design challenges, and reference designs for the EFM32 Gecko and Tiny Gecko series of microcontrollers are also included.

For simplicity, EFM32 is used throughout this document to represent the existing EFM32 Wonder Gecko, Gecko, Giant Gecko, Leopard Gecko, Tiny Gecko, Zero Gecko, or Happy Gecko MCU series, EZR32 is used to represent the EZR32 Wireless MCUs, Wireless Gecko is used to represent the EFR32 Wireless Gecko portfolio devices, and EFM32 Gemstones is used to represent the next-generation Gecko MCUs (Pearl Gecko, Jade Gecko, and future devices).

For more information on hardware layout considerations for the radio portion of EZR32 Wireless MCUs and EFR32 Wireless Gecko devices, see application notes, "AN629: Si4460/61/63/64/67/68 RF ICs Layout Design Guide," "AN698: PCB Design with an Ember EM35x," and "AN930: EFR32 2.4 GHz Matching Guide."

KEY POINTS

- Decoupling capacitors are crucial to ensuring the integrity of the device's power supplies.
- The debug interface consists of two communication pins (SWCLK and SWDIO).
- External clock sources must be connected to the device correctly for proper operation.
- This application note includes:
  - This PDF document
  - Reference Design (zip)
    - OrCAD schematic design files
    - PDF Schematics
    - Symbol libraries (OrCAD, CSV, and Edif formats)



1. Power Supply

1.1 Introduction

Even though the EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko devices support a wide voltage range and have an exceptionally small average current consumption, proper decoupling is crucial. As for all digital circuits, current is drawn in short pulses occurring on the clock edges. Particularly when several I/O lines are switching simultaneously, current pulses on the power supply lines can be in the order of several hundred mA. If the I/O lines are not loaded, the pulse width may be only a few ns. Therefore, even if the average current consumption of the EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko is very small, the current drawn during short pulses can be considerable.

These kinds of current spikes cannot be properly delivered over long power supply lines without introducing considerable noise in the supply voltage. This noise is reduced by using decoupling capacitors which act as supplementing current sources during these short transients.

1.2 Power Supply Decoupling — EFM32 and EZR32

All power pins must be connected to external decoupling capacitors. Different topologies have different performance in terms of component cost and supply noise suppression. In the following subsections one standard and one improved topology are presented. The first is favorable due to its low component cost, whereas the second has better supply noise suppression. The latter is relevant when higher ADC accuracy is required.

Decoupling capacitors make the current loop between supply, MCU, and ground as short as possible for high frequency transients. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pin, ground pin, and PCB (Printed Circuit Board) ground plane.

All external decoupling capacitors should have a temperature range reflecting the environment in which the EFM32 or EZR32 should be used. Ceramic capacitors with X5R material with a change in capacitance of ±15% over the temperature range -55 °C – +85°C would be a good choice covering the entire operating temperature range of the EFM32 or EZR32 with a reasonable accuracy.

1.2.1 Standard Decoupling

The figure below illustrates a standard approach for decoupling.

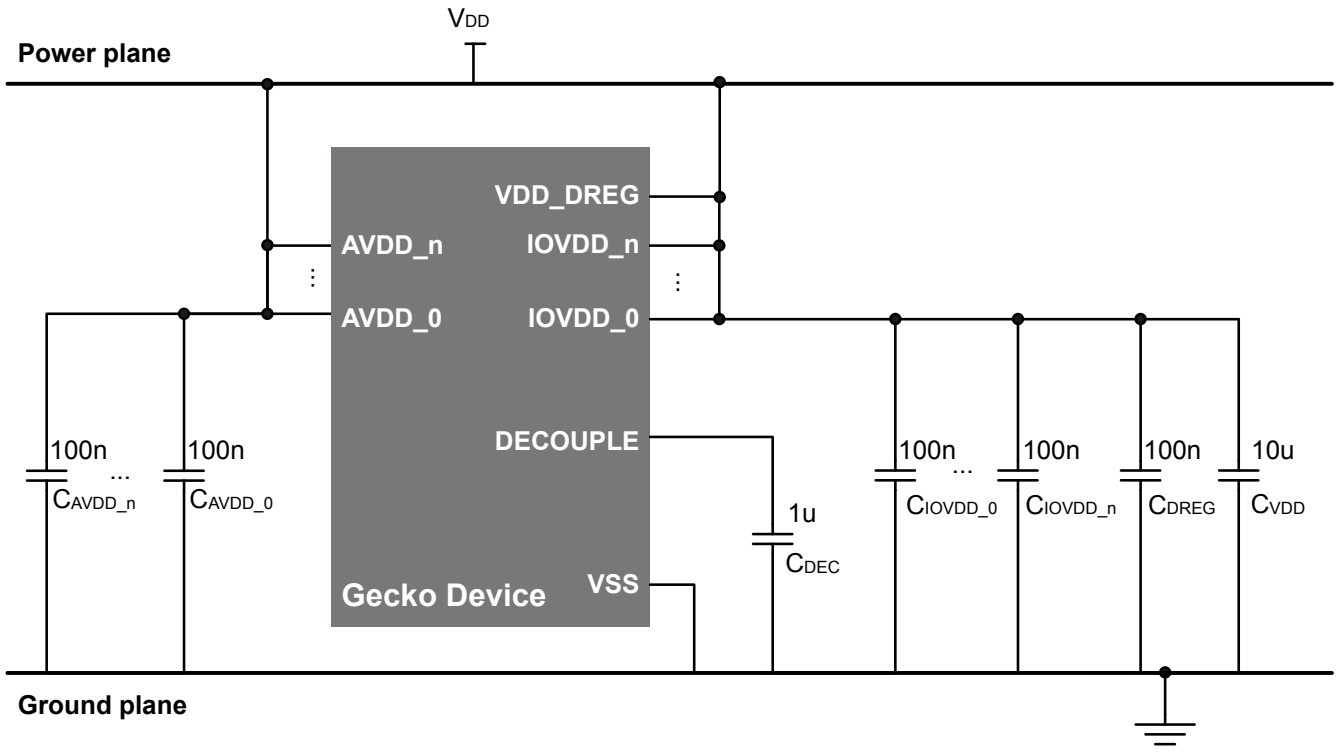


Figure 1.1. Power Supply — Standard Decoupling

The topology consists of one large common capacitor (C_{VDD}) of around 10 µF along with one 100 nF capacitor for each power pin (C_{AVDD_i}, C_{IOVDD_i} and C_{DREG}). In general each separate power net should have one common, or bulk, capacitor of around 10 µF, plus one 100 nF capacitor for each power pin on that net.

This topology is preferable since it is simple and utilizes few components, while the noise suppression performance is sufficient for many applications.
Note: The number of analog power pins (AVDD_n), I/O power pins (IOVDD_n), and ground pins (VSS) depends on the device package. Please refer to the device data sheet for package and pinout information.

1.2.2 Decoupling With Improved Supply Noise Suppression

In the following figure, a decoupling approach providing better noise suppression and isolation between the digital and analog power pins is illustrated. This topology is a good alternative when, for example, higher ADC accuracy is required.

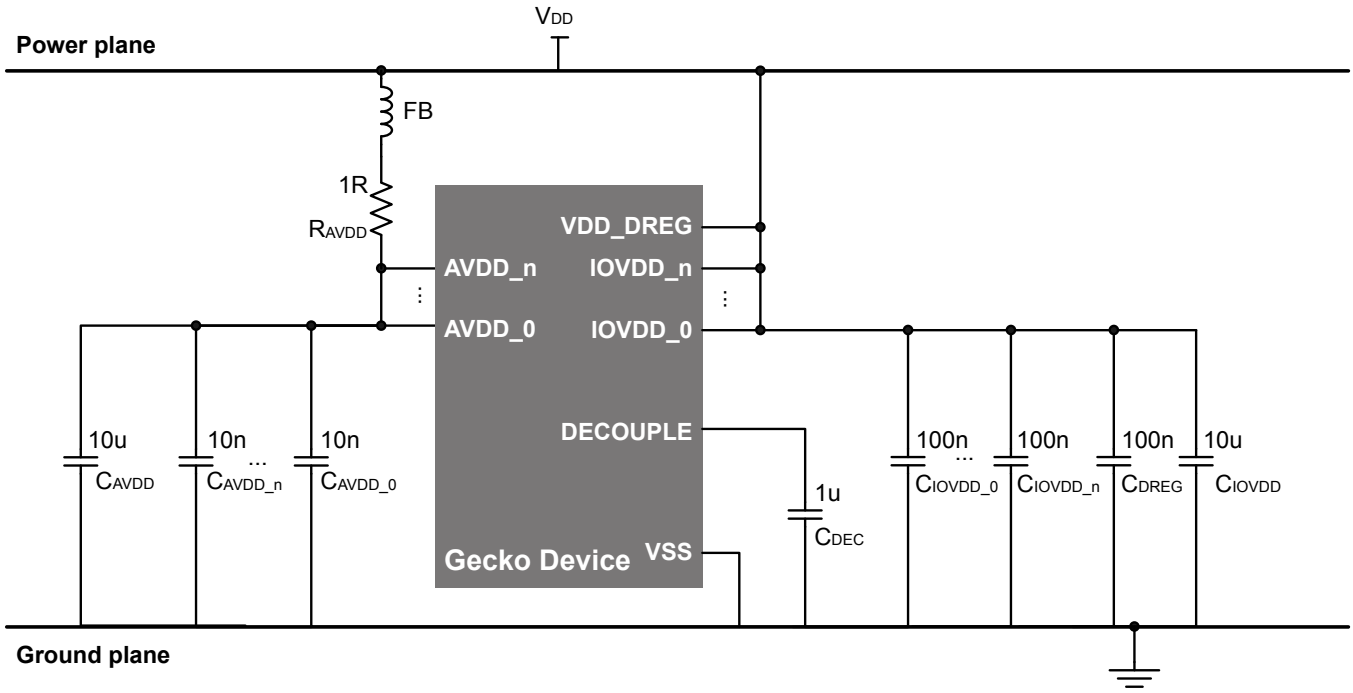


Figure 1.2. Power Supply — Better Noise Suppression and Isolation

The topology separates the analog and the digital power domain by using a ferrite bead and a resistor in addition to the capacitors.

The ferrite bead gives a relatively high impedance path between the power plane and the analog power pins during current pulses, effectively reducing the noise in the power plane. Evidently, the series resistance of the ferrite bead must be so small that it does not give a significant dc voltage drop. An EMI/RFI suppressor similar to BLM21B102S could be a good choice for the ferrite bead.

The resistor is also inserted in order to improve the isolation between the power domains. The resistor value should be small in order to prevent a high dc drop; however, it also should offer some isolation. A value of 1 Ω is a good trade-off.

Both domains should have a large common capacitor (C_{IOVDD} and C_{AVDD}) of around 10 µF, in addition to one capacitor per power pin. For the digital domain, the capacitors (C_{IOVDD_i}) can be around 100 nF, whereas for the analog domain the capacitors (C_{AVDD_i}) should be 10 nF.

During power-on, the AVDD_x pins must not be powered up after the IOVDD_x and VDD_DREG pins. If the rise time of the power supply is short, the filter in Figure 1.2 Power Supply — Better Noise Suppression and Isolation on page 3 can cause a significant delay on the AVDD_x pins. Therefore, the topology in this figure should not be used if the internal resistance of the power supply is less than 7 Ω. If the power supply has a smaller internal resistance than 7 Ω, the topology in the figure below should be used instead.

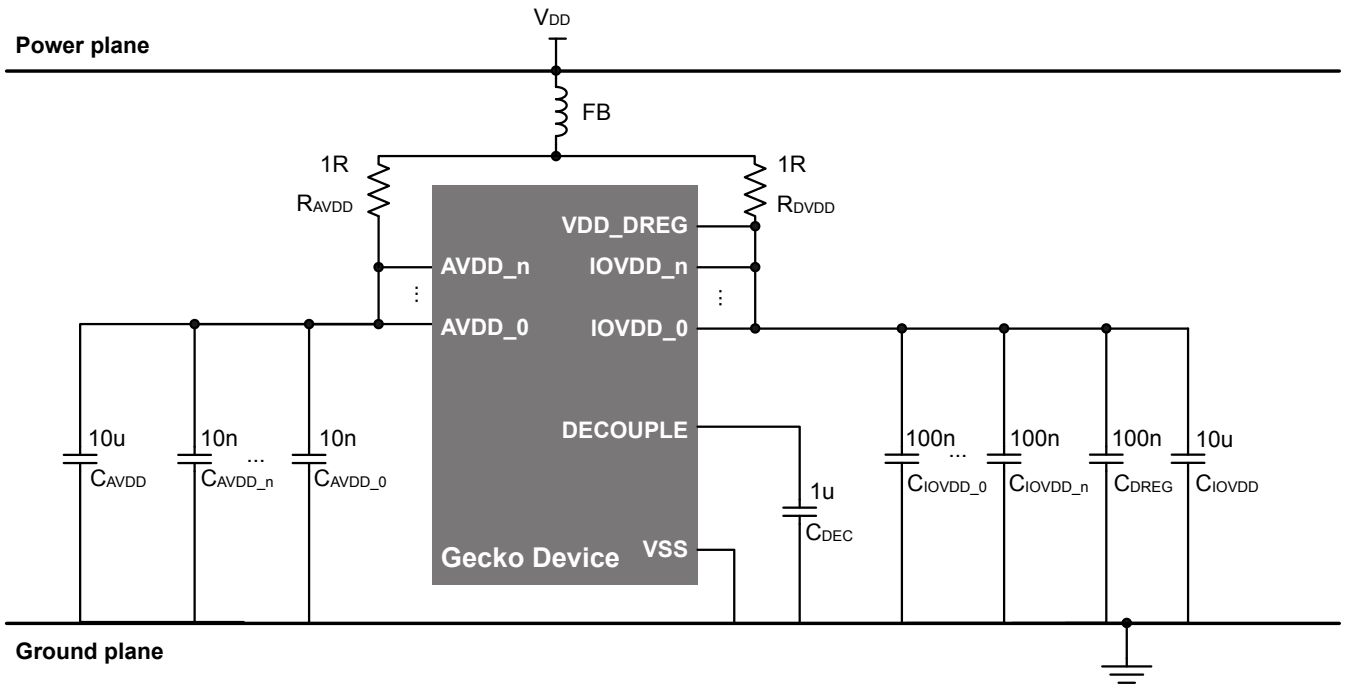


Figure 1.3. Power Supply — Internal Resistance Less than 7 Ω

1.2.3 DECOUPLE Pin

This pin is to provide external decoupling to the internal regulated supply power. This capacitor, C_{DEC}, (ref. Figure 1.1 Power Supply — Standard Decoupling on page 2) should be in the order of 1 µF to filter transients from this power domain.

1.3 Power Configurations For Devices with a DC-DC Converter — EFM32 Gemstones and Wireless Gecko

This section covers external power configurations for the EFM32 Gemstones and Wireless Gecko devices that contain an internal DC-DC converter (DC-DC). Use of the DC-DC on these parts is optional, and these devices share many of the power supply decoupling requirements as the EFM32 or EZR32 devices without a DC-DC as discussed in the previous section (1.2 Power Supply Decoupling — EFM32 and EZR32). When utilizing the DC-DC, these devices require additional external components and can utilize several hardware configurations to suit different applications.

As with devices without a DC-DC, all power pins must be connected to ground via external decoupling capacitors. Tradeoffs between component cost and performance discussed previously still apply, and the figures in the following subsections are presented without the optional main supply ferrite bead as discussed in section 1.2.2 Decoupling With Improved Supply Noise Suppression.

Depending on the application requirements, users can choose between a number of different power configurations, each with slightly different external component topologies and software configurations. These topologies are discussed in the following subsections and illustrated with typical connection diagrams. The flowchart in Figure 1.4 Power Configuration Decision Flow Chart on page 5 provides a guide to choosing the correct power configuration for a given application. In all cases, the devices boot into power configuration 0: STARTUP. From this mode, it is possible for software to dynamically switch to any of the other power modes.

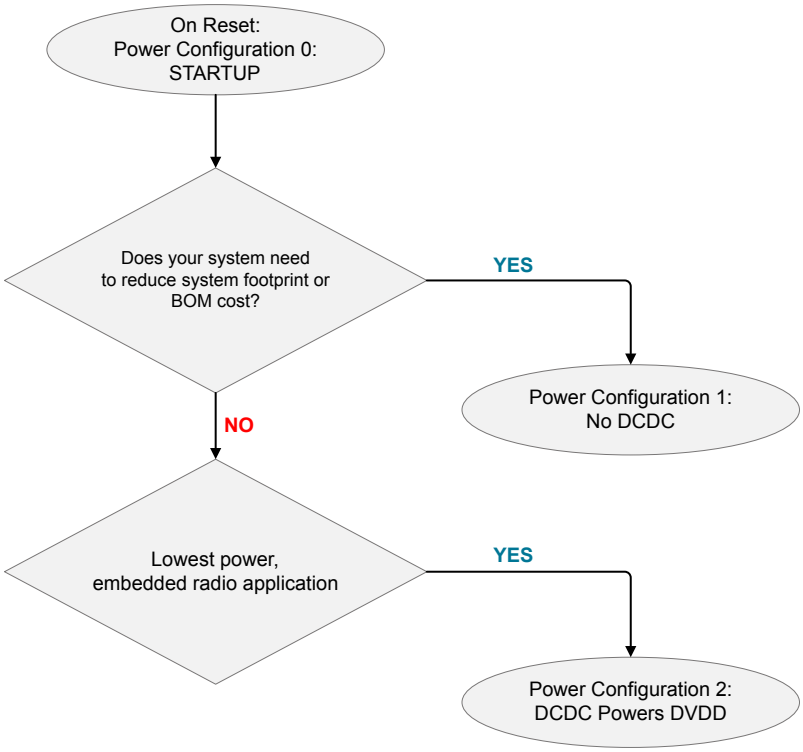


Figure 1.4. Power Configuration Decision Flow Chart

An important design requirement for EFM32 Gemstones and Wireless Gecko devices is the relative voltages applied to the VREGVDD, AVDD, DVDD, IOVDD, and DECOUPLE pins. The VREGVDD and AVDD pins must be connected to each other at the same voltage, and this must be the highest voltage in the system. In addition, the following relative voltages must be maintained in any system using the EFM32 Gemstones and Wireless Gecko with DC-DC:

- VREGVDD = AVDD (Must be the highest voltage in the system)
- VREGVDD >= DVDD
- VREGVDD >= PAVDD
- VREGVDD >= RFVDD
- VREGVDD >= IOVDD
- DVDD >= DECOUPLE

These requirements apply to all systems, regardless of power configuration or topology. Please see the device data sheet for absolute maximum rating and additional details regarding relative system voltage constraints.

All decoupling capacitors should be placed as close as possible to each of their respective power supply pin, ground pin, and PCB (Printed Circuit Board) ground plane. Additionally, each separate power net should have one common, or bulk, capacitor of around 10 µF, plus one 100 nF capacitor for each power pin on that net.

All external decoupling capacitors should have a temperature range reflecting the environment in which the EFM32 Gemstones and Wireless Gecko should be used. Ceramic capacitors with X5R material with a change in capacitance of ±15% over the temperature range -55 °C – +85°C would be a good choice covering the entire operating temperature range of the EFM32 Gemstones and Wireless Gecko with a reasonable accuracy.
Note: The number of analog power pins (AVDD_n), I/O power pins (IOVDD_n), digital power pins (DVDD_n), and ground pins (VSS) depends on the device package. Please refer to the device data sheet for package and pinout information.

1.3.1 Power Configuration 0: STARTUP

The EFM32 Gemstones and Wireless Gecko devices boot into an initial power configuration (STARTUP) from which all other power configurations can be entered. Figure 1.5 Power Configuration 0: STARTUP on page 6 shows the minimum power connections needed for the EFM32 Gemstones and Wireless Gecko to power up in STARTUP mode. These minimum power connections include powering VREGVDD, AVDD, and IOVDD from the main power supply. In this configuration, the DC-DC module is bypassed internally, and the digital logic and connected DECOUPLE pin are powered using the internal digital regulator.

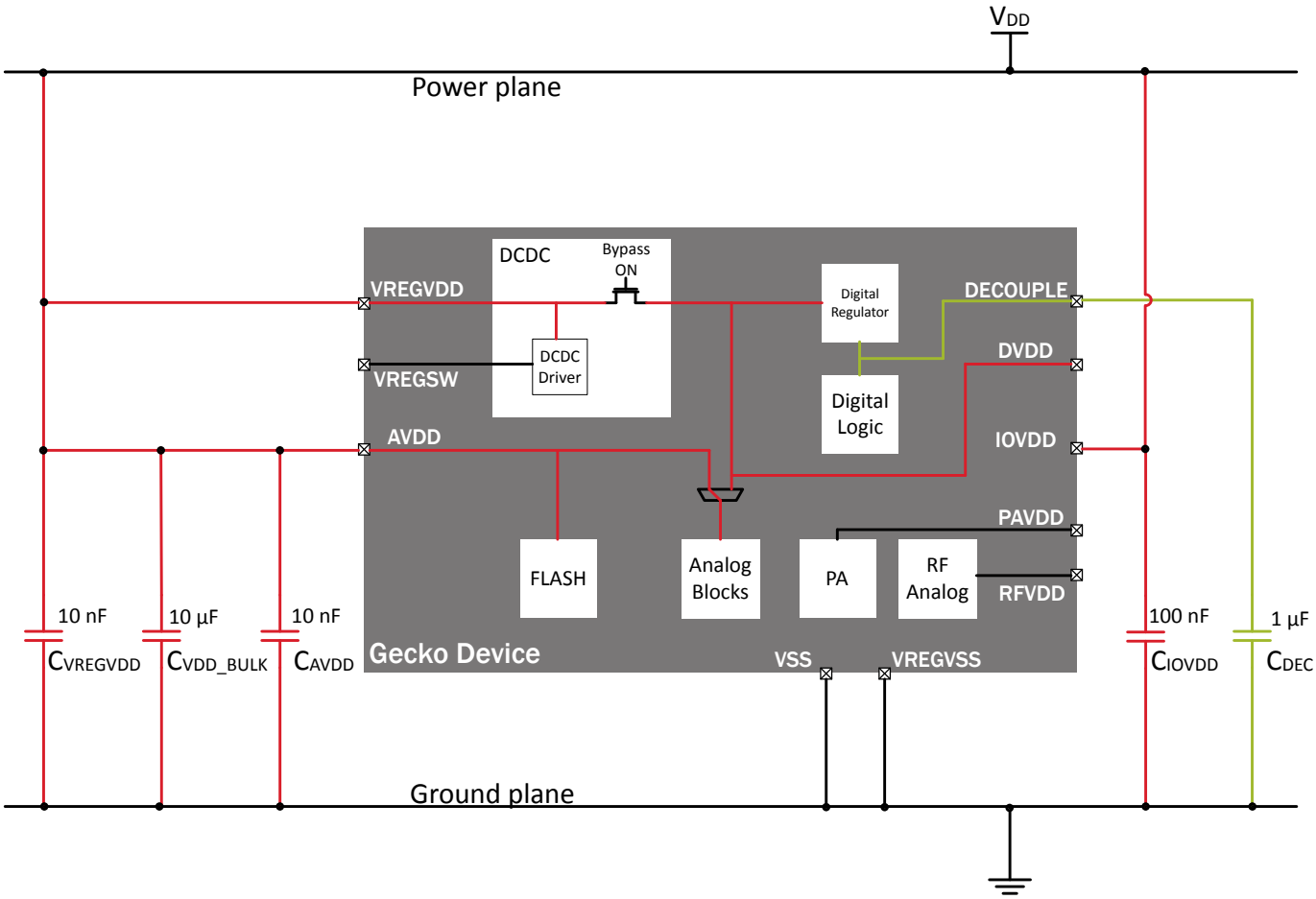


Figure 1.5. Power Configuration 0: STARTUP

While the external power circuit topology should be chosen based on the application's needs, the device will always boot into the STARTUP configuration. Software must change the power configuration settings to utilize the DC-DC and any associated external components as described in the following subsections.
Note: Figure 1.5 Power Configuration 0: STARTUP on page 6 represents the minimum power connections for the device, not a recommended operating topology. To choose a hardware power configuration, please consult Figure 1.4 Power Configuration Decision Flow Chart on page 5, section 1.3.2 Power Configuration 1: NODCDC, and section 1.3.3 Power Configuration 2: DCDCTODVDD for guidance.

1.3.2 Power Configuration 1: NODCDC

In applications requiring pin compatibility with EFM32 devices containing no DC-DC converter, or in systems where it is advantageous to reduce the system footprint or BOM cost by excluding the external DC-DC inductor (L_{VREGSW}), power configuration 1 (NODCDC) should be used. This configuration is shown in Figure 1.6 Power Configuration 1: NODCDC on page 7. In the NODCDC power configuration, VREGVDD, AVDD, DVDD, RFVDD (if present), and PAVDD (if present) are powered from the main supply. The DC-DC module is internally bypassed, and all power supply nets should be equipped with decoupling capacitors. Digital logic and the DECOUPLE pin are driven by the internal digital regulator.

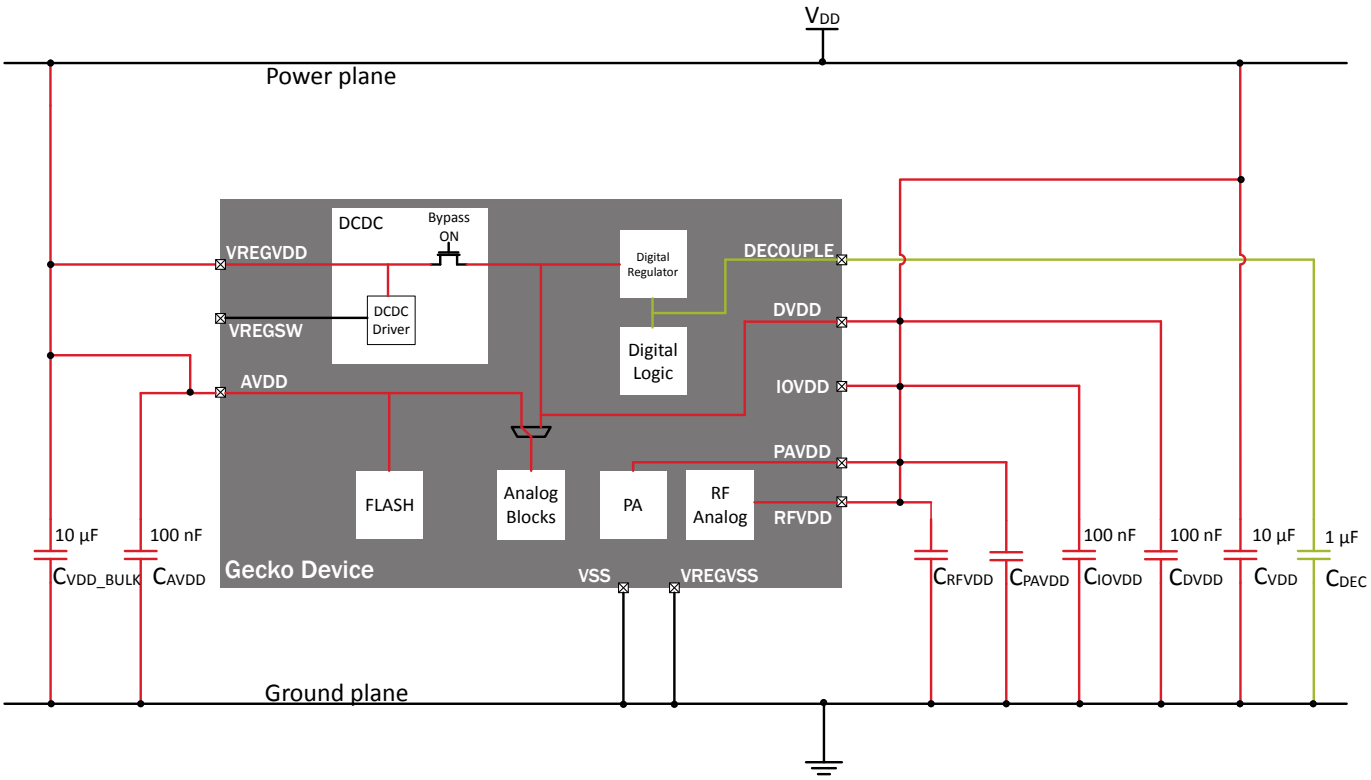


Figure 1.6. Power Configuration 1: NODCDC

Note: PAVDD and RFVDD are present only on embedded radio devices, and are not present on EFM32 Gemstone devices.

1.3.3 Power Configuration 2: DCDCTODVDD

Power configuration 2 (DCDCTODVDD) allows users of the EFM32 Gemstones and Wireless Gecko devices to realize the benefits of the DC-DC converter to acheive energy savings in embedded applications. This topology requires an external inductor and capacitor on the DC-DC output pin, VREGSW, in addition to the standard decoupling capacitors on each power net. Figure 1.7 Power Configuration 2: DCDCTODVDD on page 8 below illustrates a typical connection scenario for the DCDCTODVDD power configuration.

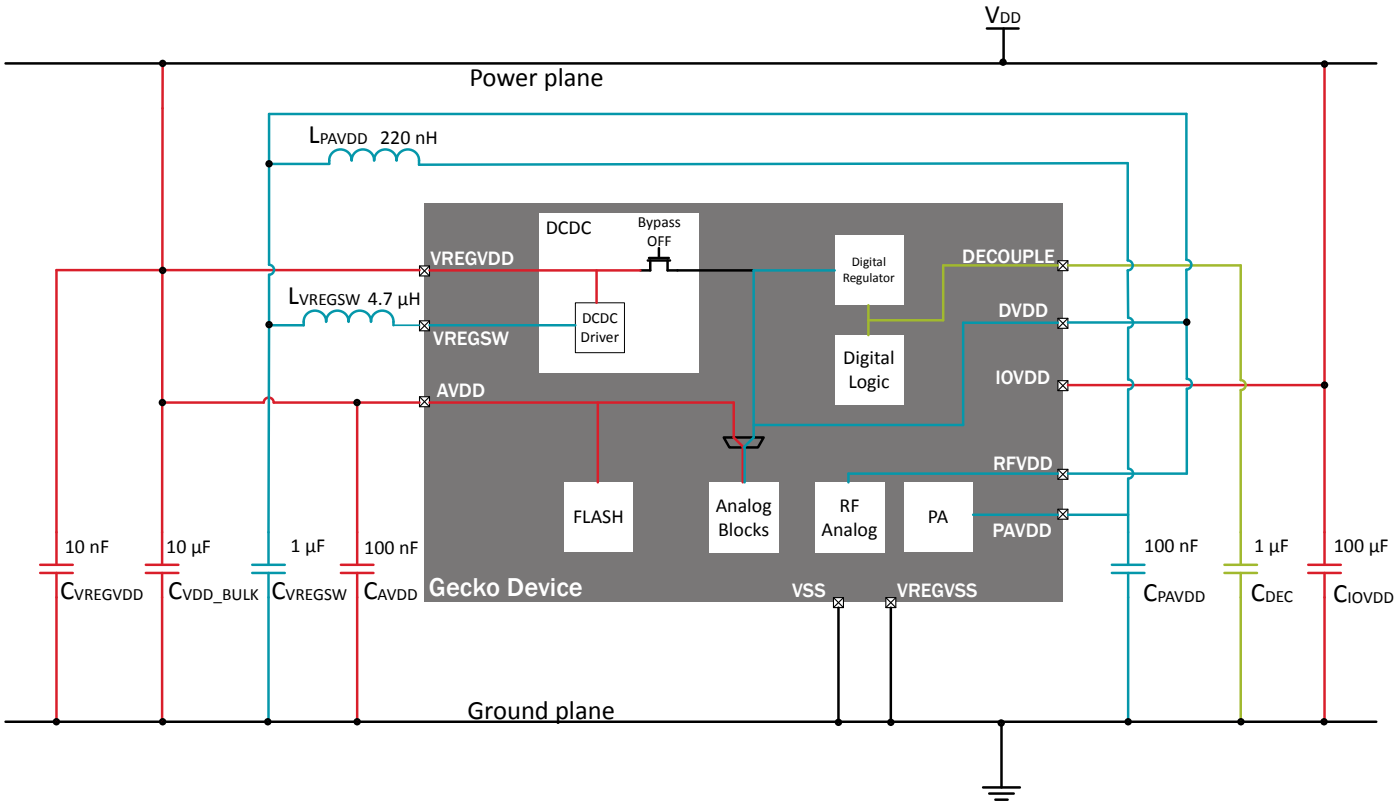


Figure 1.7. Power Configuration 2: DCDCTODVDD

In the DCDCTODVDD power configuration, the recommended value for the inductor L_{VREGSW} is 4.7 µH, and the value of the capacitor C_{VREGSW} should be 1 µF. In the event that the main supply voltage drops to a level where it becomes inefficient for the DCDC to drive VREGSW, software can switch the DCDC into bypass mode, whereby the DCDC block is effectively off and DVDD, RFVDD, and PAVDD are driven internally by VREGVDD as opposed to the VREGSW output. When the supply voltage margin returns, software can switch bypass mode to OFF, and the DCDC will again drive DVDD, RFVDD, and PAVDD via the VREGSW pin.

In applications where noise immunity on PAVDD is of particular concern, an additional LC filter may be used on this supply, as shown in Figure 1.7 Power Configuration 2: DCDCTODVDD on page 8. Recommended component values for the optional LC filter are L = 0.22 µH and C = 0.1 µF. To reduce BOM cost, and if power loss is not a concern for the PA, a lower quality inductor may be used for the LC filter that follows L_{VREGSW}.

In the event that a higher radio output power is required, the DCDCTODVDD power configuration offers the flexibility to power PAVDD from the main supply, while continuing to power DVDD, IOVDD, and RFVDD from the output of the DCDC module. This power configuration is illustrated in Figure 1.8 Power Configuration 2: DCDCTODVDD with PAVDD Powered from Main Supply on page 9.

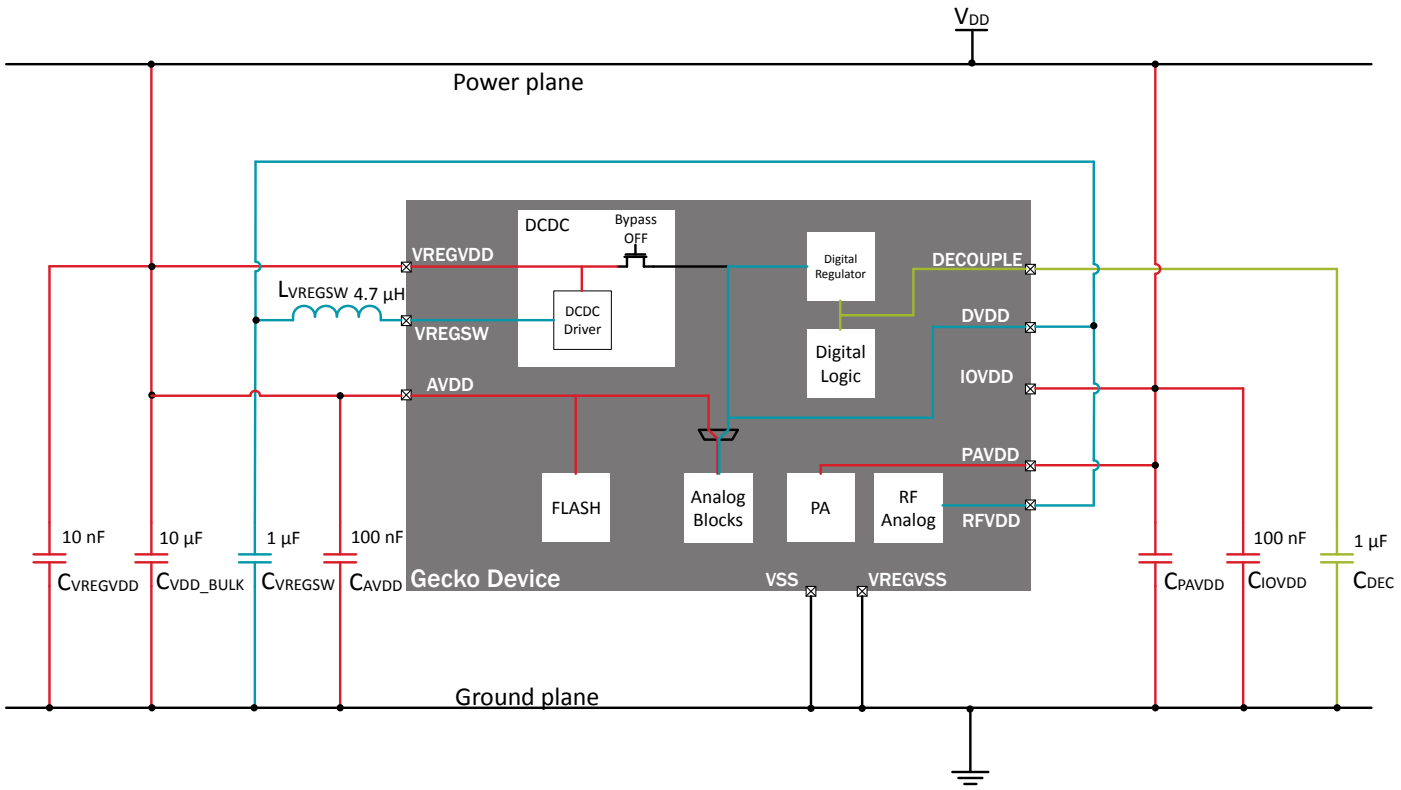


Figure 1.8. Power Configuration 2: DCDCTODVDD with PAVDD Powered from Main Supply

Note: PAVDD and RFVDD are present only on embedded radio devices and are not present on EFM32 Gemstone devices.

2. Debug Interface and External Reset Pin

2.1 Debug Interface — SWD (EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko)

The SWD interface is supported by all EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko devices. The SWD debug interface consists of the SWCLK (clock input) and SWDIO (data in/out) lines, in addition to the optional SWO (serial wire output). The SWO line is used for instrumentation trace and program counter sampling, and is not needed for programming and normal debugging. However, it can be valuable in advanced debugging scenarios, and it is therefore recommended to include this line in a design.

The connection to an ARM 20-pin debug connector is shown in the following figure. Pins with no connection should be left unconnected.

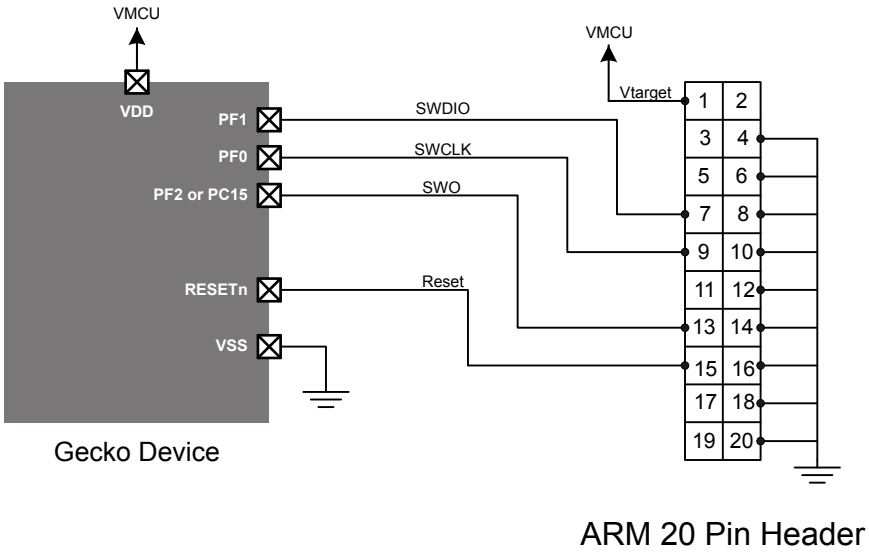


Figure 2.1. Connecting the Gecko Device to an ARM 20-pin Debug Header

Note: The V_{target} connection is not for supplying power, only sensing the target voltage.

2.2 Debug Interface — JTAG (EFM32 Gemstones and Wireless Gecko)

The JTAG debug interface is supported by the EFM32 Gemstones and Wireless Gecko devices and consists of the TDI (data input), TDO (data output), TCLK (clock), and TMS (input mode select) lines. TDI carries input data, and is sampled on the rising edge of TCLK. TDO carries output data and is shifted out on the falling edge of TCLK. TCLK is the debug clock line. Finally, TMS is the input mode select signal, and is used to navigate through the Test Access Port state machine.

The connection to an ARM 20-pin debug connector is shown in the following figure. Pins with no connection should be left unconnected.

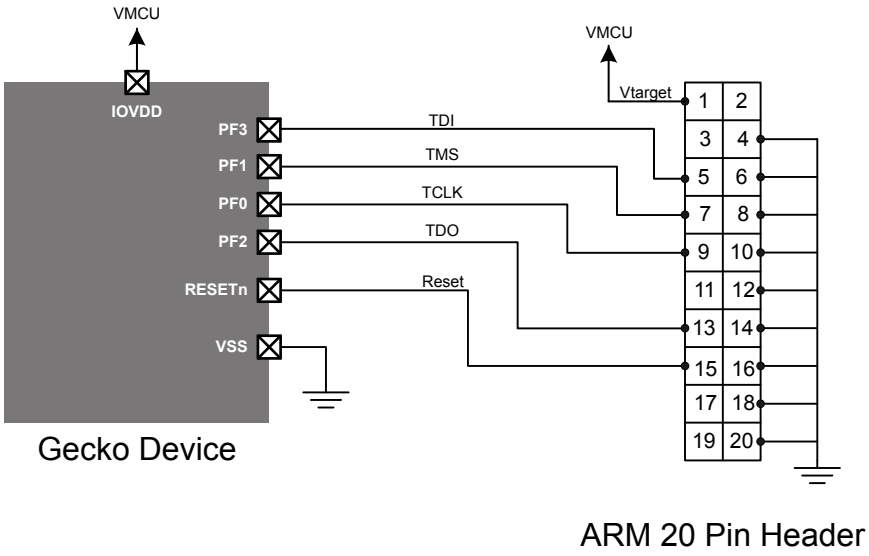


Figure 2.2. Connecting the Gecko Device to an ARM 20-pin Debug Header

Note: The V_{target} connection is not for supplying power, only sensing the target voltage.

2.3 External Reset Pin (RESETn)

Forcing the RESETn pin low generates a reset of the EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko. The RESETn pin includes an internal pull-up resistor and can therefore be left unconnected if no external reset source is required. Also connected to the RESETn line is a low-pass filter which prevents noise glitches from resetting the EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko. The characteristics of the pullup and input filter is identical to the corresponding characteristic of a GPIO pin, which is found in the device data sheet.

Note: To apply an external reset source to this pin, drive this pin low during reset. The internal pull-up ensures that the reset is released. This pin should not be connected to an external pull-up or driven high while the device is unpowered, as this could damage the device. This is also important when using back-up power mode, as the internal pull-up automatically switches to the back-up power rail, which could end up back-powering the entire system through the external pull up.

3. External Clock Sources

3.1 Introduction

The EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko support different external clock sources to generate the low and high frequency clocks in addition to the internal LF and HF RC oscillators. The possible external clock sources for both the LF and HF domains are external oscillators (square or sine wave) or crystals/ceramic resonators. This section describes how the external clock sources should be connected.

For additional information on the external oscillators, refer to the application note AN0016: "Oscillator Design Considerations." Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or in Simplicity Studio using the [**Application Notes**] tile.

3.2 Low Frequency Clock Sources

The external low frequency clock can be generated from a crystal/ceramic resonator or from an external clock source.

3.2.1 Low Frequency Crystals and Ceramic Resonators — EFM32 or EZR32

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 3.1 Low Frequency Crystal on page 12. The crystal is to be connected across the LFXTAL_N and LFXTAL_P pins of the EFM32 or EZR32.

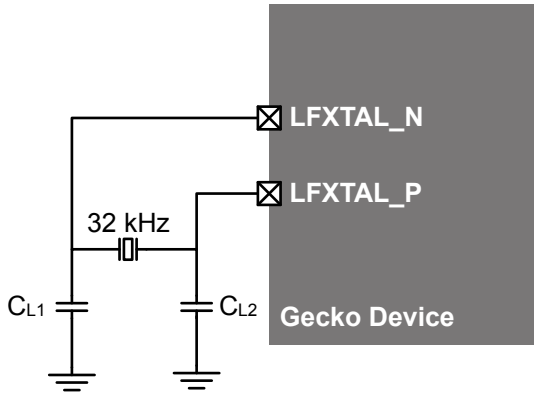


Figure 3.1. Low Frequency Crystal

The crystals/ceramic resonators oscillate mechanically and have an electrical equivalent circuit as shown in Figure 3.2 Equivalent Circuit of a Crystal/Ceramic Resonator on page 12. In the electrical circuit, C_S represents the motional capacitance, L_S the motional inductance, R_S the mechanical losses during oscillation, and C_0 the parasitic capacitance of the package and pins. C_{L1} and C_{L2} represent the load capacitance. This circuit is valid for both crystals and ceramic resonators.

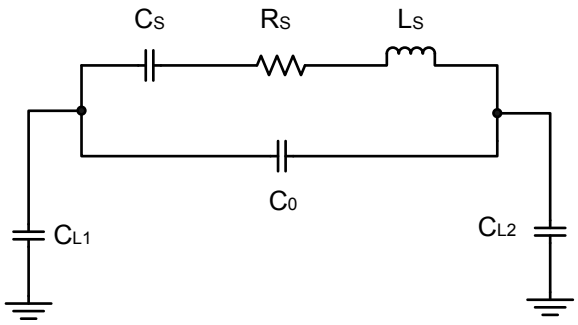


Figure 3.2. Equivalent Circuit of a Crystal/Ceramic Resonator

3.2.2 Low Frequency Crystals and Ceramic Resonators — EFM32 Gemstones and Wireless Gecko

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 3.3 Low Frequency Crystal - EFM32 Gemstones and Wireless Gecko on page 13. The crystal is to be connected across the LFXTAL_N and LFXTAL_P pins of the EFM32 Gemstones and Wireless Gecko. This circuit is valid for both crystals and ceramic resonators.

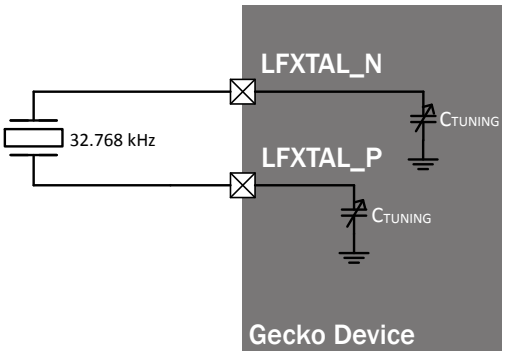


Figure 3.3. Low Frequency Crystal - EFM32 Gemstones and Wireless Gecko

The difference between this crystal configuration and that of the EFM32 or EZR32 is that the need for external load capacitors C_{L1} and C_{L2} have been eliminated. These load capacitors are now on-chip and can be tuned by software. The EFM32 Gemstones and Wireless Gecko devices support low frequency crystals with load capacitance in the range of 6 pF to 18 pF. Check device specific data sheets and reference manuals for load capacitance values and instructions for tuning the internal load capacitances.

3.2.3 Low Frequency External Clocks

The EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko can also be clocked by an LF external clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels. The external clock signal can either be a square wave or sine signal with a frequency of 32.768 kHz. The external clock source must be connected as indicated in Figure 3.4 Low Frequency External Clock on page 13.

When a square wave source is used, the LFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%, as specified in the device data sheet. When a sine source is used, the amplitude must be in accordance with the device data sheet. The sine signal is buffered through the LFXO buffer, whose input is ac-coupled.

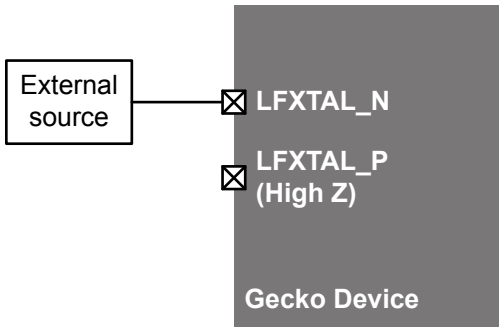


Figure 3.4. Low Frequency External Clock

3.3 High Frequency Clock Sources

The external high frequency clock can be generated from a crystal/ceramic resonator or from an external square or sine wave source.

3.3.1 High Frequency Crystals and Ceramic Resonators — EFM32 or EZR32

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 3.5 High Frequency Crystal Oscillator on page 14. The crystal should be connected across the HFXTAL_N and HFXTAL_P pins.

The electrical equivalent circuit of the HF crystal/ceramic resonators is equal to the one for LF crystals/ceramic resonators in the figure below.

Placement of C_L is important for proper operating frequency.

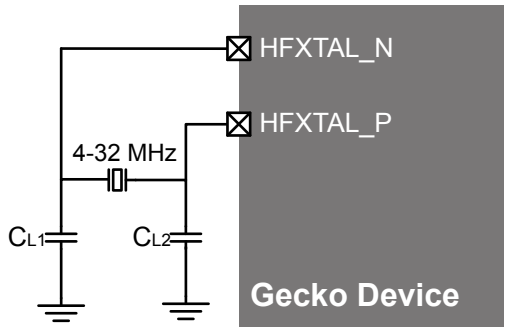


Figure 3.5. High Frequency Crystal Oscillator

3.3.2 High Frequency Crystals and Ceramic Resonators — EFM32 Gemstones and Wireless Gecko

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 3.6 High Frequency Crystal Oscillator - EFM32 Gemstones and Wireless Gecko on page 14. The crystal should be connected across the HFXTAL_N and HFXTAL_P pins.

The difference between this crystal configuration and that of the EFM32 or EZR32 is that the need for external load capacitors C_{L1} and C_{L2} have been eliminated. These load capacitors are now on-chip and can be tuned by software. The EFM32 Gemstones and Wireless Gecko devices support high frequency crystals with load capacitance in the range of 6 pF to 12 pF. Check device specific data sheets and reference manuals for load capacitance values and instructions for tuning the internal load capacitances.

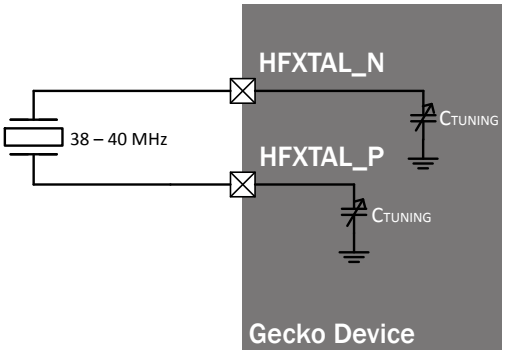


Figure 3.6. High Frequency Crystal Oscillator - EFM32 Gemstones and Wireless Gecko

Note: Some devices are subject to the 38 - 40 MHz frequency limit for the high frequency crystal oscillator, whereas other devices will have a wider frequency range. Please consult the device-specific data sheet for more information.

3.3.3 High Frequency External Clocks

The EFM32, EZR32, EFM32 Gemstones, and Wireless Gecko can also be clocked by an external HF clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle and signal levels. The external clock signal can either be square wave or a sine signal with a frequency in accordance with the device data sheet. The external clock source must be connected as indicated in Figure 3.7 External High Frequency Clock on page 15.

When a square wave source is used, the HFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%. Refer to the device data sheet for further details. When a sine source is used, the sine amplitude must be in accordance with what is specified in the device data sheet. The sine signal is buffered through the HFXO buffer, whose input is ac-coupled.

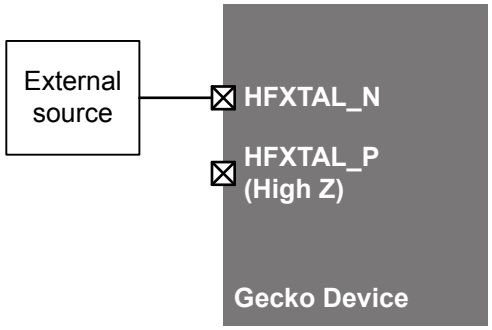


Figure 3.7. External High Frequency Clock

4. Reference Design

When starting a new EFM32 or EZR32 design, some parts of the layout are almost always required regardless of the application. Attached to this application note are example schematics for power decoupling, reset, external clocks, and debug interface. Using this reference design as a template can improve development speed in the early stages of a new design. The reference design and included symbols are compatible with Cadence OrCAD 9.0 and later versions.

This application note does not include footprints for the devices, but these can be found in `*.bxl` format on http://www.silabs.com.

4.1 Contents

The application note folder includes several zip files with the following contents:

- CSV pin list files
- Edif symbols
- OrCAD OLB symbols
- OrCAD DSN example schematics
- PDF example schematics

The schematics and symbols are included for the following device families:

- EFM32ZG
- EFM32HG
- EFM32TG
- EFM32G
- EFM32LG
- EFM32WG
- EFM32GG

A generic symbol is included for the EZR32 family.

4.2 Comments on the Schematics

4.2.1 Power Supply Decoupling

The decouple pin uses a 1 µF capacitor to filter transients in the power domain for the internal voltage regulator.

Each power pin has a 100 nF decoupling capacitor in addition to the common 10 µF decoupling capacitor, as described in 1.2 Power Supply Decoupling — EFM32 and EZR32. The digital power supply is separated from the analog power supply to reduce EMI. To further improve the switching noise of the analog power, an EMI suppressor is put in series between V_{MCU} and the analog power pins.

The active low reset pin is connected to ground through a normally open switch, as well as to the debug interface connector.

4.2.2 Debug Interface

A standard ARM 20-pin debug connector is connected to the EFM32 or EZR32 debug pins.

4.2.3 High/Low Frequency Clock

Both the high and low frequency clock pins are connected to crystal oscillators using two of the recommended crystals from the AN0016 Oscillator Design Considerations application note.

5. Revision History

5.1 Revision 1.44

2015-11-13

Added power configuration and crystal resonator info for EFR32 Wireless Gecko portfolio devices.

5.2 Revision 1.43

2015-10-21

Added power configuration and crystal resonator info for EFM32 Gemstone devices.

Added symbols and schematics for EFM32JG and EZR32PG devices.

5.3 Revision 1.42

2015-03-04

Added symbols and schematics for EFM32HG and EZR32LG devices.

5.4 Revision 1.41

2015-02-13

Added EZR32 devices.

Updated format.

5.5 Revision 1.40

2014-05-07

Added symbols and schematics for EFM32WG and EFM32ZG devices.

Corrected numbering for EM4WU pins for EFM32TG devices in symbols and schematics.

5.6 Revision 1.36

2013-10-14

New cover layout

5.7 Revision 1.35

2013-08-14

Updated section on power supply decoupling

5.8 Revision 1.34

2013-05-08

Added note about decoupling capacitor purpose.

Added new design files for new packages and devices.

5.9 Revision 1.33

2012-03-21

Added CSV and Edif formats for schematic symbols.

5.10 Revision 1.32

2012-03-16

Added OrCAD reference designs and OrCAD symbols for more parts.

5.11 Revision 1.31

November 23th, 2010.

Corrected schematic values.

Added information on power sequencing considerations.

5.12 Revision 1.30

November 17th, 2010.

Added information on alternate schematic recommendations.

5.13 Revision 1.20

September 13th, 2010.

Merged sections on PCB design considerations and external clock sources.

Modified chapter on external clock sources to correspond with AN0016 EFM32 Oscillator Design Considerations.

Added OrCAD and PDF reference designs.

5.14 Revision 1.10

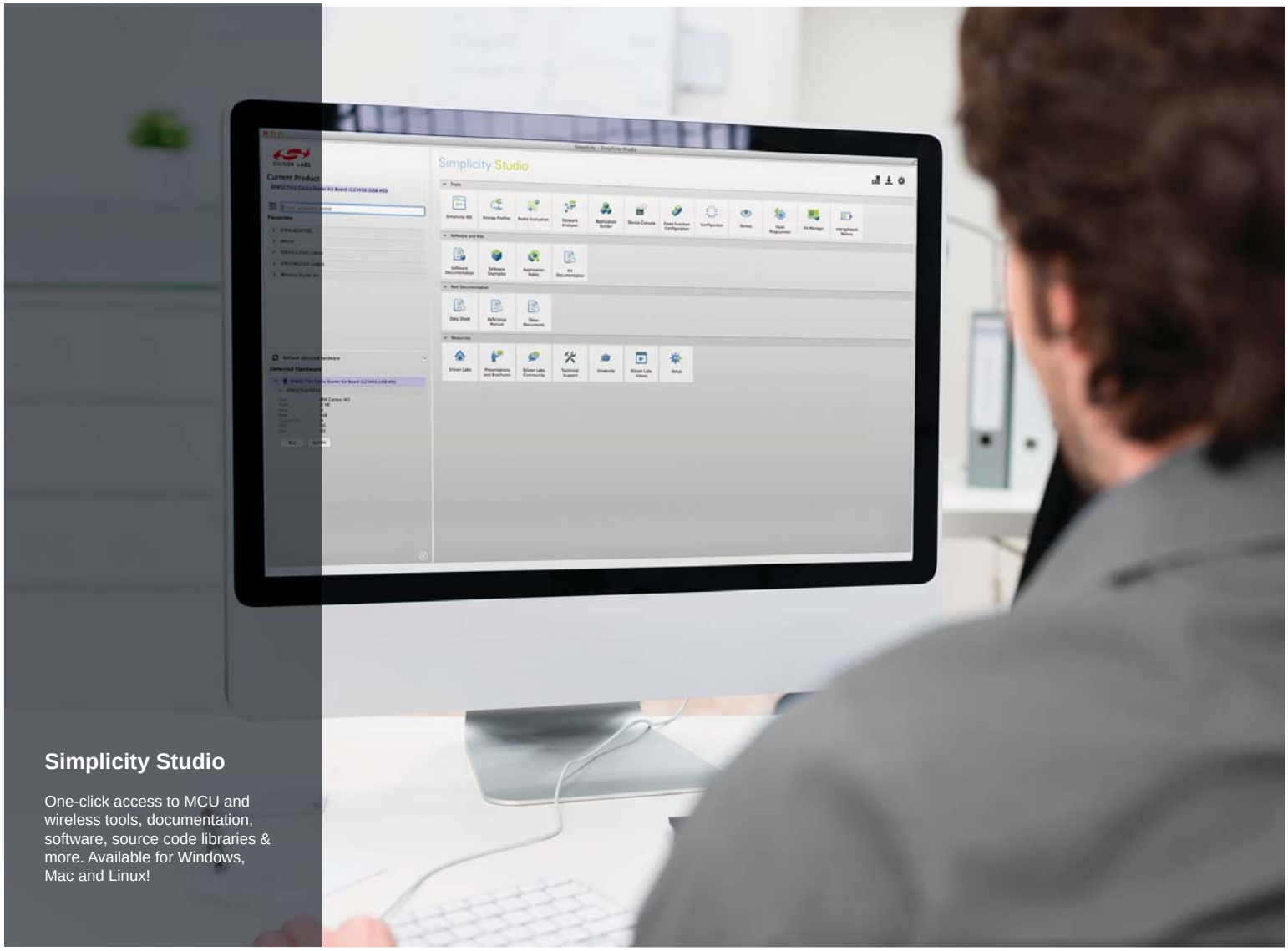
May 6th, 2010.

Added debug interface section.

5.15 Revision 1.00

October 21th, 2009.

Initial revision.



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