CSAtool

User Guide - Version 0.02

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1 Introduction

CSAtool is a MATLAB GUI simulation and modeling environment created for both the analysis and the assisted design of the capacitive DACs of charge-redistribution successive approximation analog-to-digital converters (CR SAR ADCs) in integrated-circuit technologies. In general, this tool allows to estimate both the static and the dynamic performance of such ADCs independently of the chosen technology. This is possible simply providing models that allow the users to size the DAC array capacitive elements with an high degree of customization. Moreover, the tool deals also with a variety of technological parameters which can be customized by the user to fit a particular technology performance. By choosing a specific DAC topology defined by the combination of a capacitive network and a switching algorithm, sizing the capacitive array and setting the technology parameters, the effects of both intrinsic parasitic capacitances and capacitor mismatch on the ADC performance can be estimated. In addition, with the aid of specific modules provided by the tool, also the impact of the parasitic related to each critical array node and/or capacitor (for example the parasitic values coming from a post-layout c-extraction) can be analyzed. Finally, thanks to its simulation speed, which is up to a factor 10^5 faster than those achievable with the most common EDA tools based testbenches, CSAtool offers the chance to perform statistical and montecarlo simulations over a desired number of realizations in a reasonable amount of time.

2 How to Run the Tool

The steps to run the CSAtool on MATLAB are the following:

1. Extract the folder of the CSAtool (/CSAtool) from the compressed file CSAtool.rar.
2. Copy the extracted folder into your MATLAB folder (your desired work directory).
3. Update the MATLAB search path with the new folder (be sure to operate in the directory containing the CSAtool folder).
4. Type `CSAtool` in your MATLAB command window.

3 Overview of the Tool

CSAtool is a simulation environment based on capacitive network models tailored on each specific DAC topology. These models are based on vectors and matrix that reproduce the circuit proerties of a DAC topology. Given few parameters, among which the most important is the desired value of the unit capacitor (the smallest compact capacitive element of the DAC), the tool produce a realization of a desired topology and evaluate its performance. In general the tool does NOT provide dedicated models of capacitors (MiMcaps, MoMcaps, PiPcaps...), but allows the designer to customize all the parameters which are necessary to model any of these options.

The main window of the tool, depicted in figure 1 presents the following sections:

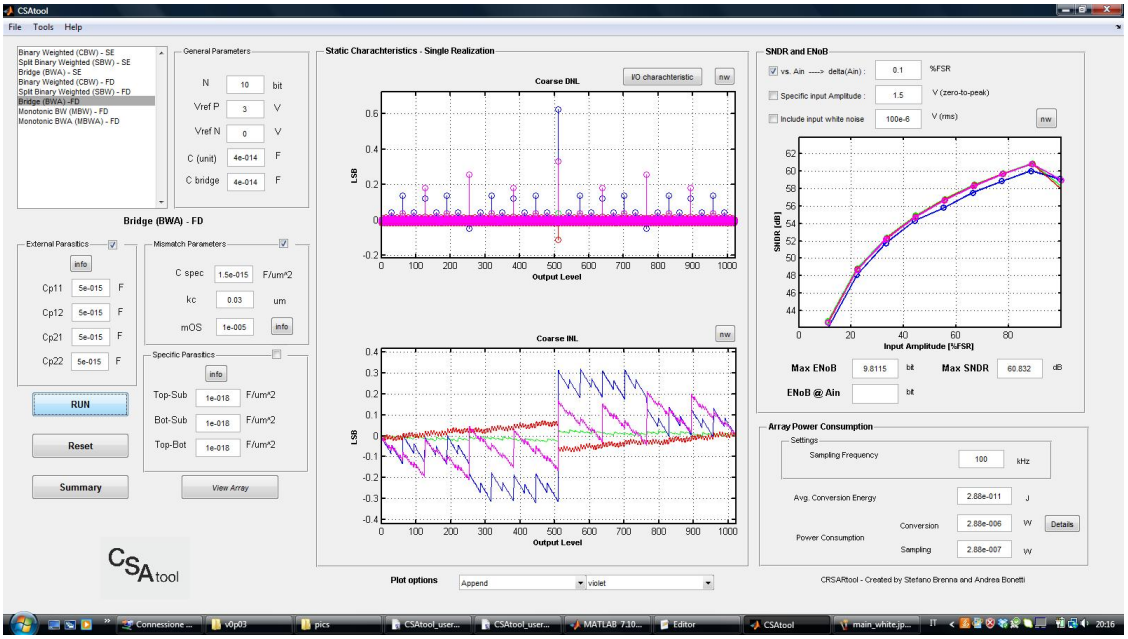

Fig. 1: CSAtool main window.

Topology

The topology of the CSAtool can be selected here among a list of the most common ones, at the top-left corner of the GUI main window. Both the array structure and the used switching scheme determine the topology. In addition, it is possible to choose either the single-ended (SE) or the fully-differential (FD) version.
The implemented models allow to choose among the following topologies:

- `Classic Binary Weighted - CBW (SE and FD)`: traditional binary weighted array combined to a traditional switching algorithm.
- `Split Binary Weighted - SBW (SE and FD)`: binary weighted array where the MSB capacitor is split into a replica of the remaining part of the DAC, combined to the split capacitor array switching algorithm.
- `Binary Weighted with Attenuation Capacitor BWA (SE and FD)`: simmetrical binary weighted array with attenuation capacitor combined to a traditional switching algorithm.
- `Monotonic Binary Weighted MBW (intrinsically FD)`: traditional binary weighted array combined to a monotonic switching algorithm.
- `Monotonic Binary Weighted with Attenuation Capacitor - MBWA (intrinsically FD)`: simmetrical binary weighted array with attenuation capacitor combined to a monotonic switching algorithm

For additional information on the topologies and the switching schemes briefly

described above, please refer to the papers listed in the section *CSAtool Topologies References*.

General Parameters

General parameters section is located to the right of the topology selection list. The number of bits (N) , the input voltage range (difference between $V_{ref,P}$ and $V_{ref,N}$) and the nominal size of the unit C_u and the eventual attenuation capacitor C_b can be arbitrarily set here.

Mismatch Parameters

Each element of the capacitive DAC can be defined as the sum of its nominal value, which is a power of 2 multiple of the unit element, a mismatch contribution and the related parasitic. To contain the mismatch, in real DACs each capacitive bank of the array is typically implemented as the parallel of a desired number of unit capacitors. For this reason the mismatch contribution is here expressed and modeled as the sum of the mismatch of each unit element. Mismatch is absumed to be normally distributed with a zero-mean and a standard deviation which depends on the Pelgrom coefficient k_c and the specific capacitance C_{spec}.

The parameter `Cspec` is specific capacitance and it is defined as follows:

$$C_{spec} = \frac{C}{W_C L_C} \tag{1}$$

Where W_C and L_C are respectively the width and the length of the unit capacitor whose value is C. Moreover, the parameter `kc` can be obtained from the following equation:

$$\sigma\left(\frac{\Delta C}{C}\right) = k_C \sqrt{W_C L_C} + m_{OS} \tag{2}$$

Where $\sigma\left(\frac{\Delta C}{C}\right)$ is the standard deviation of the difference ΔC of identically designed capacitors, normalized to their absolute value C. The parameter m_{OS} is given by the technology. To enable the mismatch effect estimation, the checkbox related section of the main window must be checked.

Intrinsic Parasitics

It is possible to add the values of intrinsic parasitic capacitances that are connected from the top-plate of the designed array (or sub-arrays) to the substrate, and from the the top-plate to the bottom-plate of every unit capacitor used to compose each capacitive bank of the DAC. The area-dependent parasitic capacitances to specify are the ones connected from the top plate of the capacitor to the substrate (Top-Sub), from the bottom plate of the capacitor to the substrate (Bot-Sub) and from the top plate to the bottom plate of the capacitor (Top-Bot). This functionality is provided to give the designer the chance to evaluate the impact of those parasitics which are intrinsic of a particular class of capacitor and depend on its area, which is fixed by its size and specific capacitance.

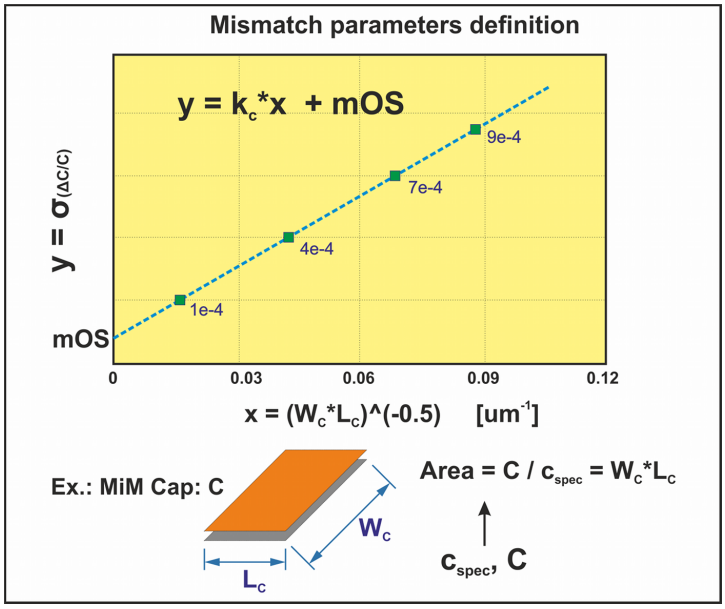

Fig. 2: Definition of the parameters for the mismatch of the capacitors.

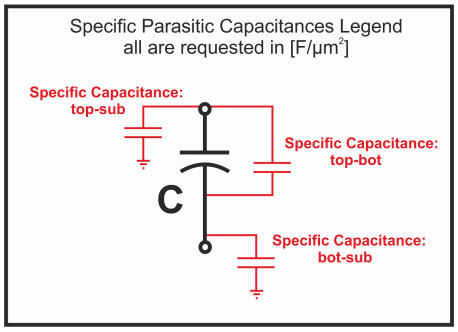

Fig. 3: Specific parasitic capacitances.

Once again, it is worth noting here that in general the tool does NOT provide dedicated models of capacitors (MiMcaps, MoMcaps, PiPcaps...), but allows the designer to customize all the parameters which are necessary to model them. To enable the intrinsic parasitic effect estimation, the checkbox related section of the main window must be checked.

External Parasitics

The values of the external parasitic capacitances affecting the top plate node of DAC can be added here. The parasitic capacitances to specify are the ones connected from the top plate of the capacitive DAC and eventual sub-DACs to the substrate or to any fixed voltage node (for example VDD, VSS or $V_{ref,P}$ and $V_{ref,N}$, if they don't coincide).`Cp11`,`Cp12`,`Cp21` and `Cp22` are the values that can

be set in the most general case, depicted in figure 4. If you have any doubt about the nodes affected by these parasitics, you can press the `View Array` button: an illustration will help you.

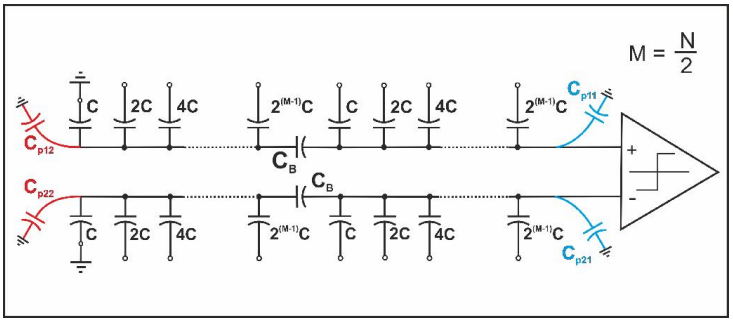

Fig. 4: External parasitic capacitances for a fully differential BWA.

To enable the external parasitic effect estimation, the checkbox related section of the main window must be checked.

Static Characteristics - Single Realization

Both DNL and INL graphs of the ADC are shown here for a single realization, estimated each time you press the `Run` button. By selecting the *append* plot option, successive realizations can be compared on the same graph.

SNDR and ENoB

The dependency of the SNDR on the amplitude of the input signal is plotted here, in the top right section of the main window. To enable this estimation, you can check any of the first two box on the top left. The first box allows to evaluate the SNDR of the customized DAC by points as a function of the input amplitude. The amplitude has a fixed step set by the user in the `delta(Ain)` cell and expressed as fraction of the FSR (i.e. 0.1 means 10 points). Both maximum achievable ENoB and SNDR are reported.

Differently, the second box enables the evaluation of the ENoB at a given input amplitude. To estimate the dynamic performance, the tools simulate a conversion of an input sinusoid sampled well over nyquist, according to the IO charachteristic of the converter, including the current realization mismatch and parasitics. The FFT is then performed on the output to evaluate the desired spectral metrics. This approach also allows to sum a desired input referred white noise, defined by its rms value. This option just models an input referred noise and do not deal directly with its possible sources (comparator, switches...).

Array Power Consumption

By setting the sampling frequency of the ADC, it is possible to estimate the average energy required per conversion. The power consumptions of the conversion and of the sampling phase are also reported and include the impact of parasitics.

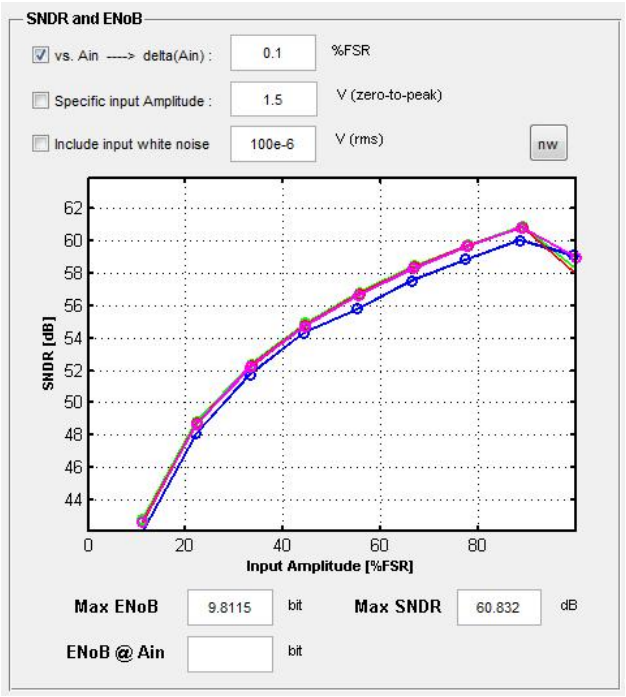

Fig. 5: Dynamic metrics estimation section.

This functionality is currently under development and could result inaccurate for fully differential topologies.

4 Additional Tools

For a further investigation of the static performances, it is possible to use additional tools. These can be selected by clicking on Tools, in the upper part of the CSAtool window.

PPEX Tool

In case the extracted values of the parasitic capacitances are available from a post-layout analysis and/or if the user desired to investigate the effects produced by localized parasitics, PPEX tool allows to add the value of the parasitic capacitance connected from the top plate to the bottom plate of each capacitive bank in the array. This is possible through the dedicated user interface shown in figure 7.

- Which is the difference between PPEX tool and the modules dedicated to `Specific Parasitics` and `External Parasitics` that are already provided in CSAtool main window?

The external parasitics are just those connected from the top-plate of each eventual sub-DAC and the reference nets (substrate, VDD, GND ...).The specific parasitics are top-to-substrate (or reference nets), top-to-bottom, and bottom-to-substrate (or reference nets) stray capacitances that affect in general each unit capacitor, thus also the capacitive banks since each of them is built by multiple unit capacitors. These capacitances are specific so they depend on the area of the unit capacitor and so of each bank; in general they are proportional to the capacitance. PPEXtool offers the chance to estimate the effect of all those parasitics connected from the top to the bottom of any of the capacitive banks, which are not directly dependent on the area but on other issues, for example the layout quality, which depends only on the designer ability. This can be the case of wiring parasitics. Once a parasitic set is loaded and applied, all the analysis available from CSAtool can be performed through the main window and the other modules. It is worth noting here that **the parasitic loaded through PPEXtool sum to the others specified in the main window** and also to the mismatch effect.

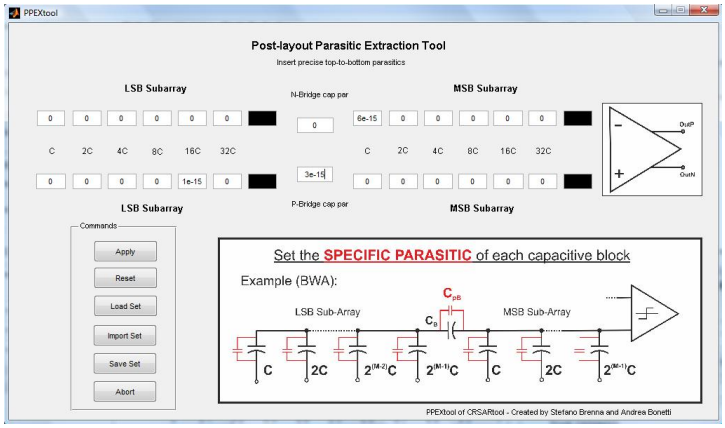

Fig. 6: PPEX module for a 12-bit fully differential BWA.

SSA Tool

This tool provides a statistical analysis of the static performance over a desired number of runs, set by the parameter `Runs`. The parameter `sigma` act as a multiplier for the currently set pelgrom mismatch coefficient k_c. SSA tool output is represented by the standard deviation of DNL and INL as a function of the output code and by the distribution of their maximum absolute value.

ESA Tool

A statistical analysis of the achievable ENoB is presented here. The working principle is the same of SSAtool. The maximum ENoB distribution is evaluated over a desired number of runs, set by the parameter `Runs`. For each realization, the input amplitude of a virtual input sinusoid spans between the given minimum and maximum amplitudes, set by the users as a fraction of the FSR by defining the parameters `Minimum Input` and `Minimum Input`.

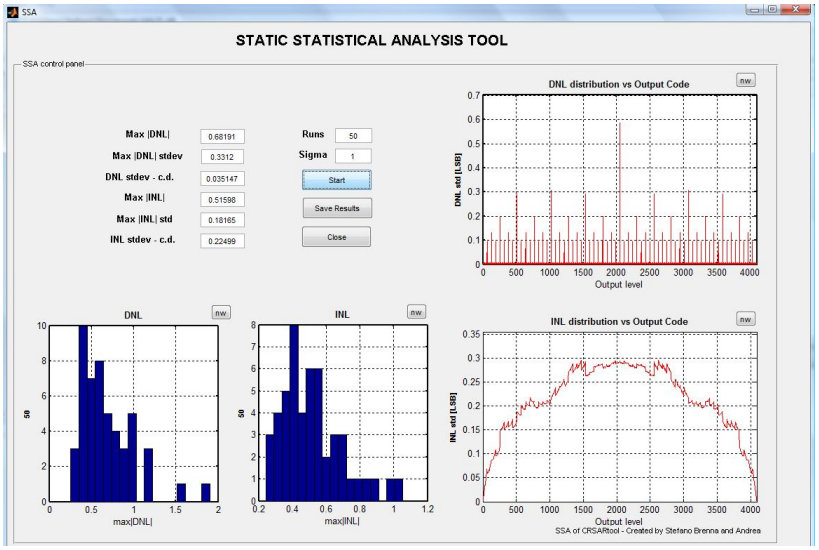

Fig. 7: Static Statistical Analysis module.

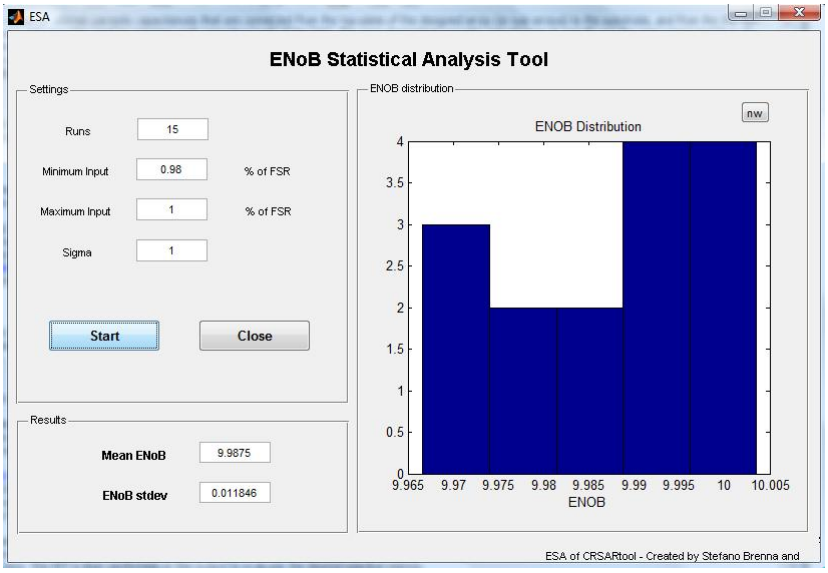

Fig. 8: ESA module GUI.

5 CSAtool Topologies References

The different CSAtool topologies reported in the tool are summarized here. For each of them, a document is given as reference for a better understanding.

Binary Weighted - CBW

McCreary, J.L.; Gray, P.R.; , "All-MOS charge redistribution analog-to-digital conversion techniques. I," *Solid-State Circuits, IEEE Journal of* , vol.10, no.6, pp.371-379, Dec. 1975

Suarez, R.E.; Gray, P.R.; Hodges, D.A.; , "All-MOS charge-redistribution analog-to-digital conversion techniques. II," *Solid-State Circuits, IEEE Journal of* , vol.10, no.6, pp.379-385, Dec. 1975

Split Binary Weighted - SBW

Ginsburg, B.P.; Chandrakasan, A.P.; , "500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC," *Solid-State Circuits, IEEE Journal of* , vol.42, no.4, pp.739-747, April 2007

Binary Weighted with Attenuation Capacitor (Bridge) - BWA

Agnes, A.; Bonizzoni, E.; Maloberti, F.; , "Design of an ultra-low power SA-ADC with medium/high resolution and speed," *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on* , vol., no., pp.1-4, 18-21 May 2008

Monotonic Binary Weighted - MBW

Chun-Cheng Liu; Soon-Jyh Chang; Guan-Ying Huang; Ying-Zu Lin; , "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *Solid-State Circuits, IEEE Journal of* , vol.45, no.4, pp.731-740, April 2010

Monotonic Binary Weighted with Attenuation Capacitor - MBWA

S. Brenna; A. Bonfanti ; A. Abba; F. Caponio, A. L. Lacaita; "Analysis and Optimization of a SAR ADC with Attenuation Capacitor" *37th MIPRO Int. Conf. on Microelectronics* , May 2014

6 Contacts

For further information about the software, please contact: `crsaradctool@gmail.com`

7 Authors

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