Tai Lung RV32I Core

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Background

The FE310-G002 includes a SiFive E31 RISC-V core, which is a high-performance single-issue in-order execution pipeline, with a peak sustainable execution rate of one instruction per clock cycle. The RISC-V core supports Machine mode only as well as the standard Multiply, Atomic, and Compressed RISC-V extensions (RV32IMAC).

RISC-V

```
RV [32, 64, 128] I, M, A, F, D, G, Q, L, C, B, J, T, P, V, N
```

Road map

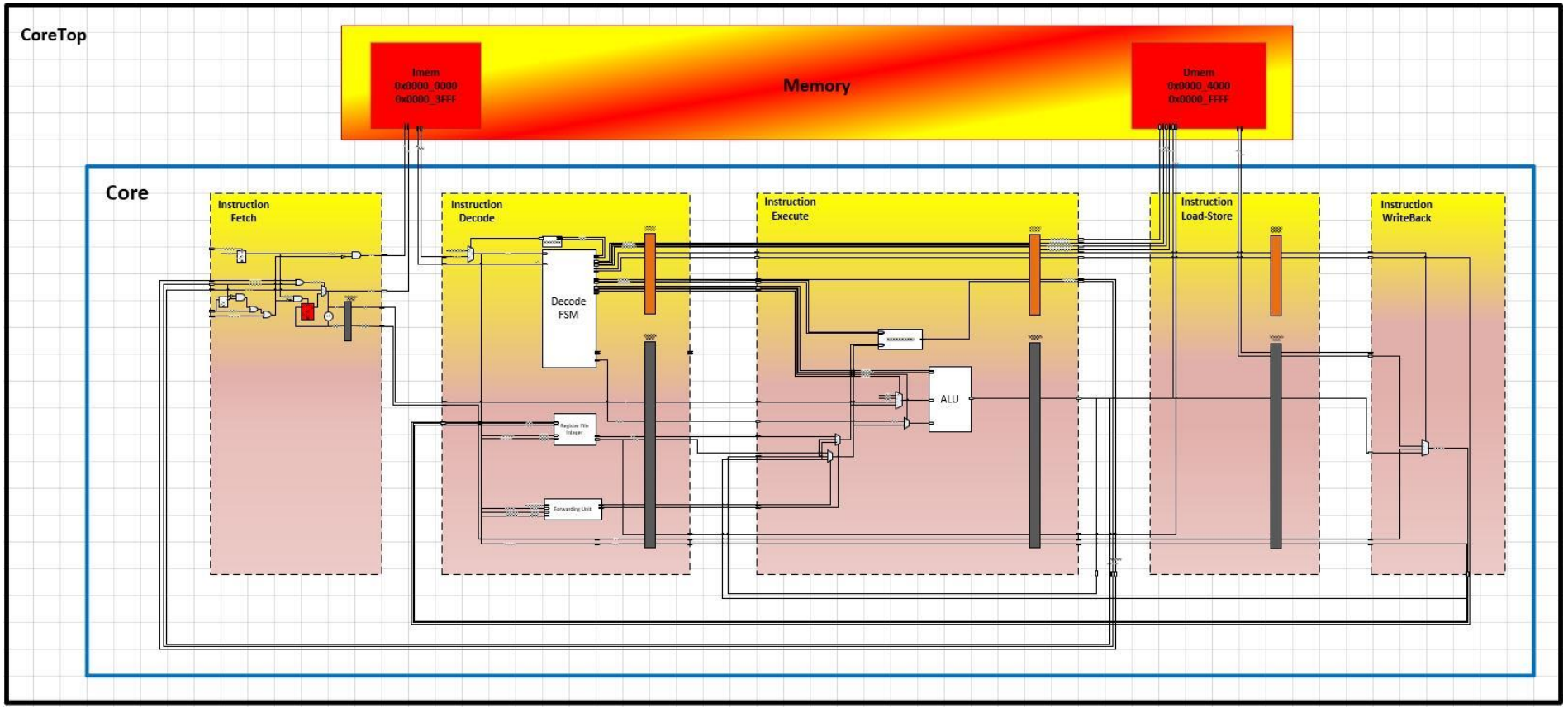

RV32I
May-2022
Kick-off
Sep-2021
FPGA
Sep-2022
Privileged Arch
CSR
Jun-2022
Extensions
M+F
Aug-2022

Specs

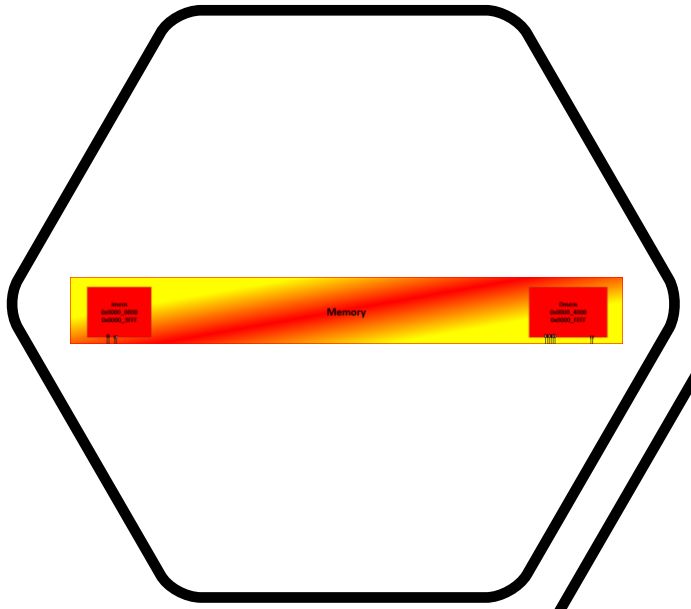
Spec	Tai Lung	SiFive E31
ISA	RV32I	RV32I-MAC
Arch	5 stage pipeline	5-6 variable stages pipeline
Operation frequency	100 [MHz]	320 [MHz]
IPC – instruction per cycle	0.76 (avg)	1 (avg)
Forwarding mechanisim	Yes	Yes
Branch prediction	No	No
cache	no	16Kb 2 way Icache
Power	?	?
Area	?	?

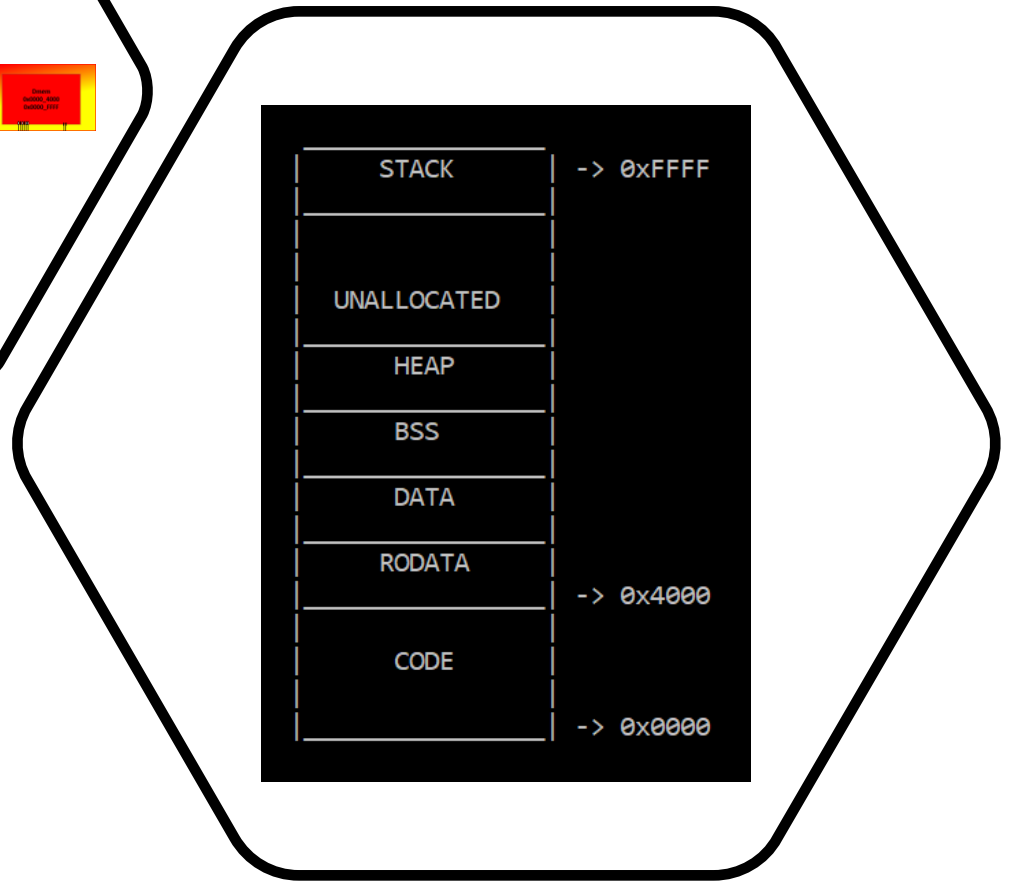
Architecture

RV32I - In order execution - 5 stage pipeline

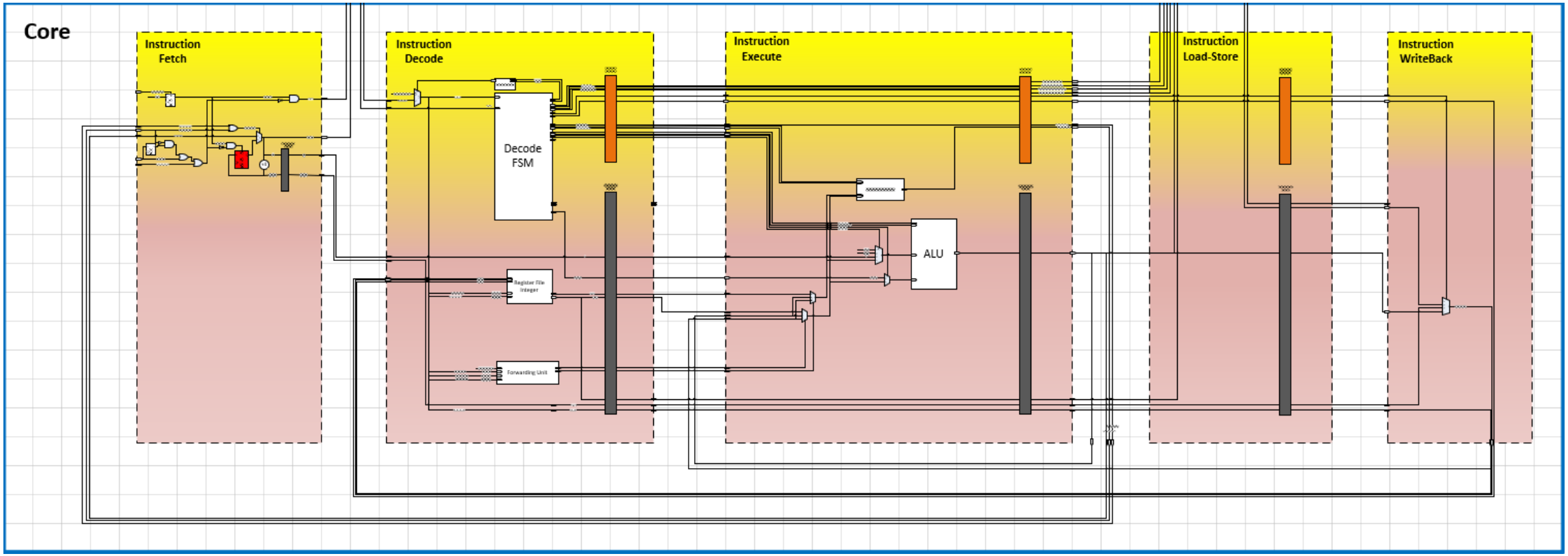


Memory





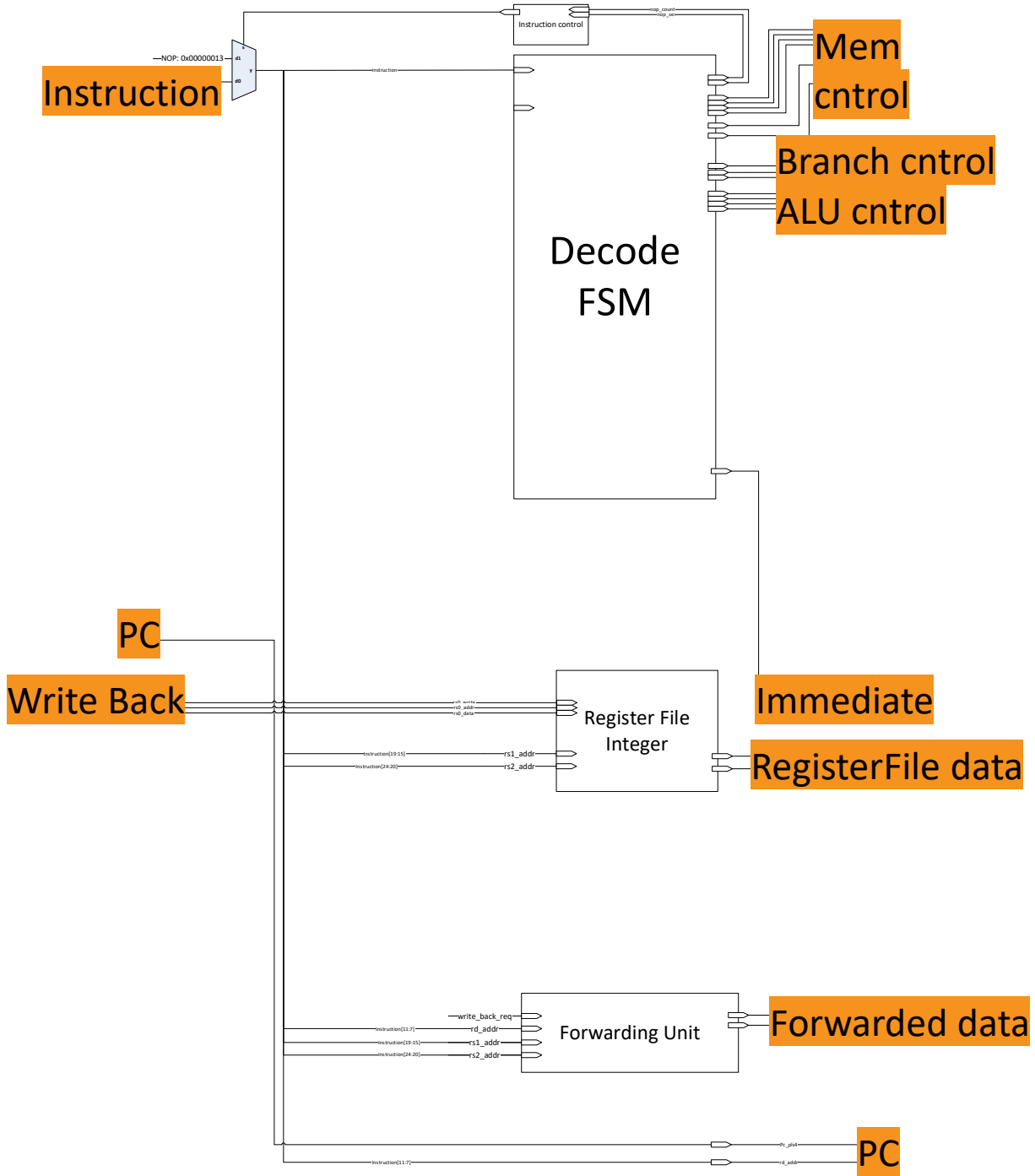
MEMORY BLOCK	SIZE	ADDRESS RANGE	ACCESS	PORT	ENDIANNESS
I-MEM	16Kbytes	0x0000-0x3FFF	Read only - executable	Single	Little
D-MEM	48Kbytes	0x4000-0xFFFF	Read/Write – non executable	Single	Little


Core
Instruction Fetch
Instruction Decode
Instruction Execute
Instruction Load-Store
Instruction WriteBack
Decode FSM
ALU
Register File Integer
Forwarding Unit

Core

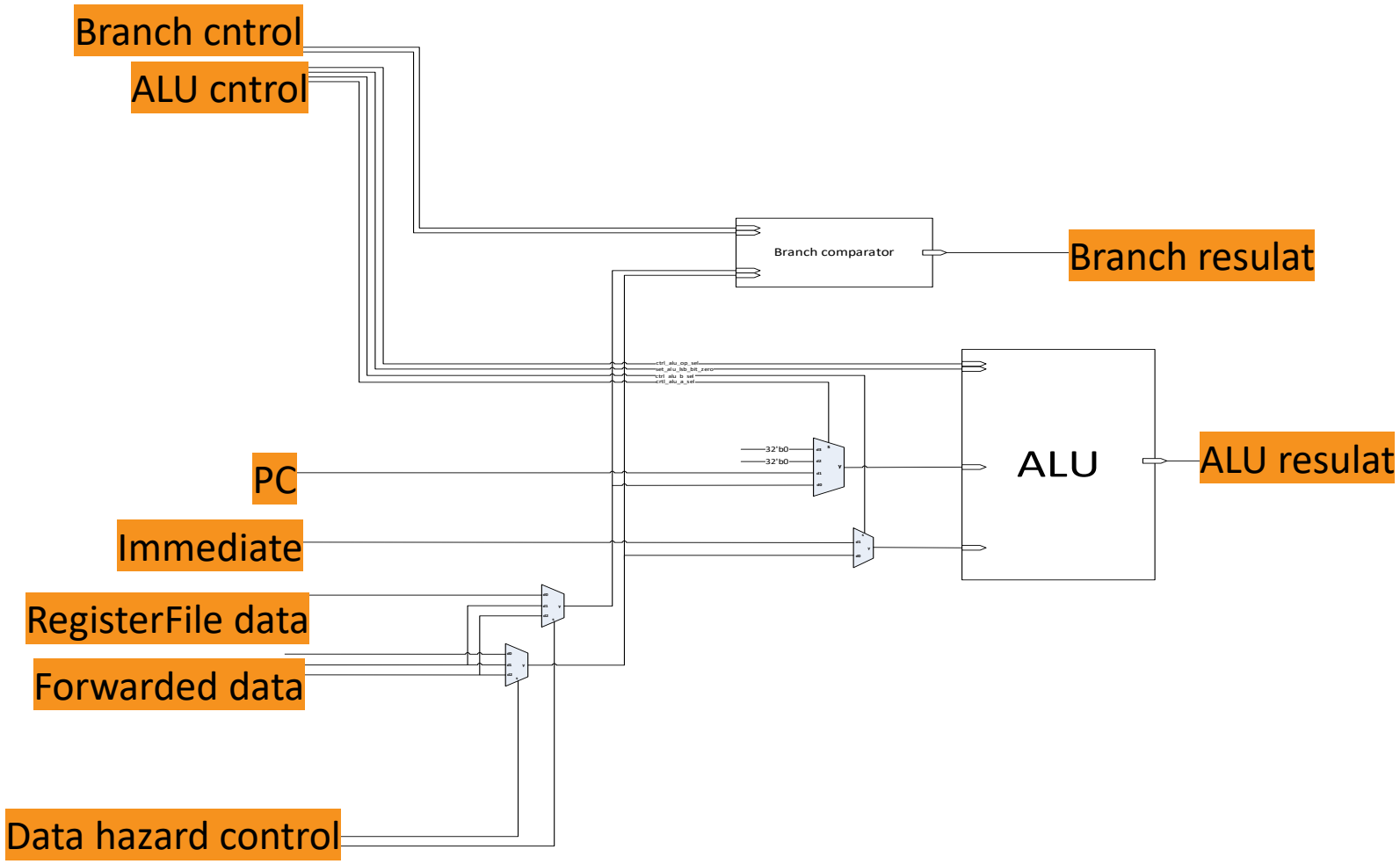
Decode pipeline

The Decode state decoded the 32-bit instruction into the core control signals and change the Core state to execute the instruction.



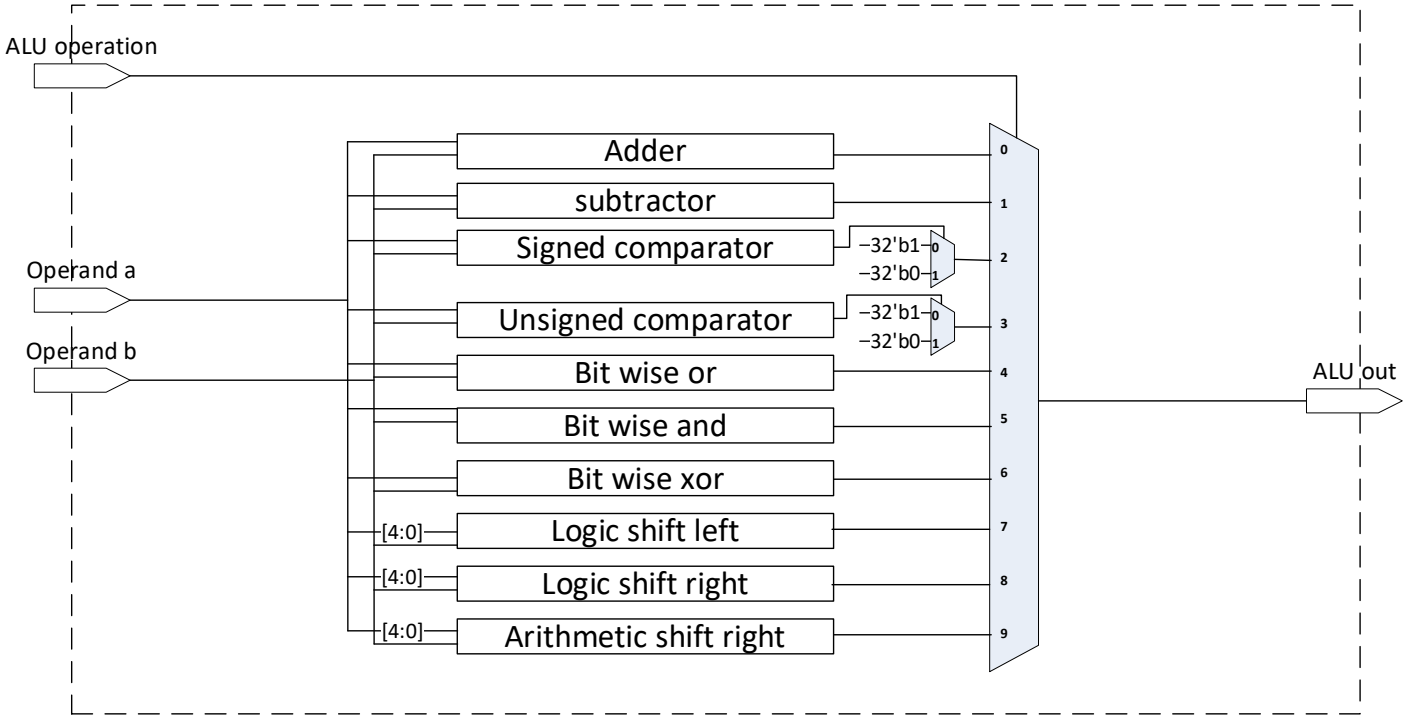
Execution pipeline

The Execution state execute the operation based on the instruction, calculate address for Load/Store instructions or decided if a branch operation should be taken.



Execution pipeline

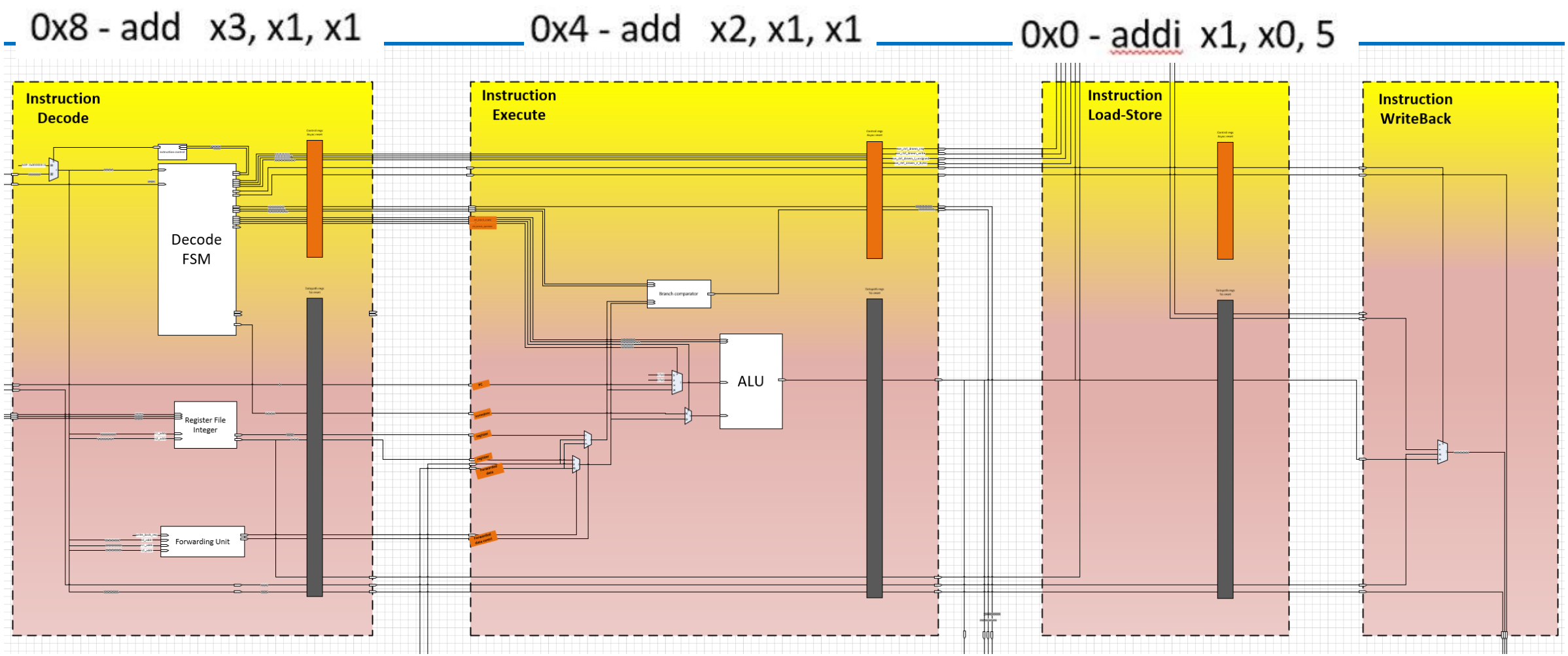
The Execution main component is the Arithmetic Logic Unit (ALU) which preforms the arithmetic operation for the desired instruction



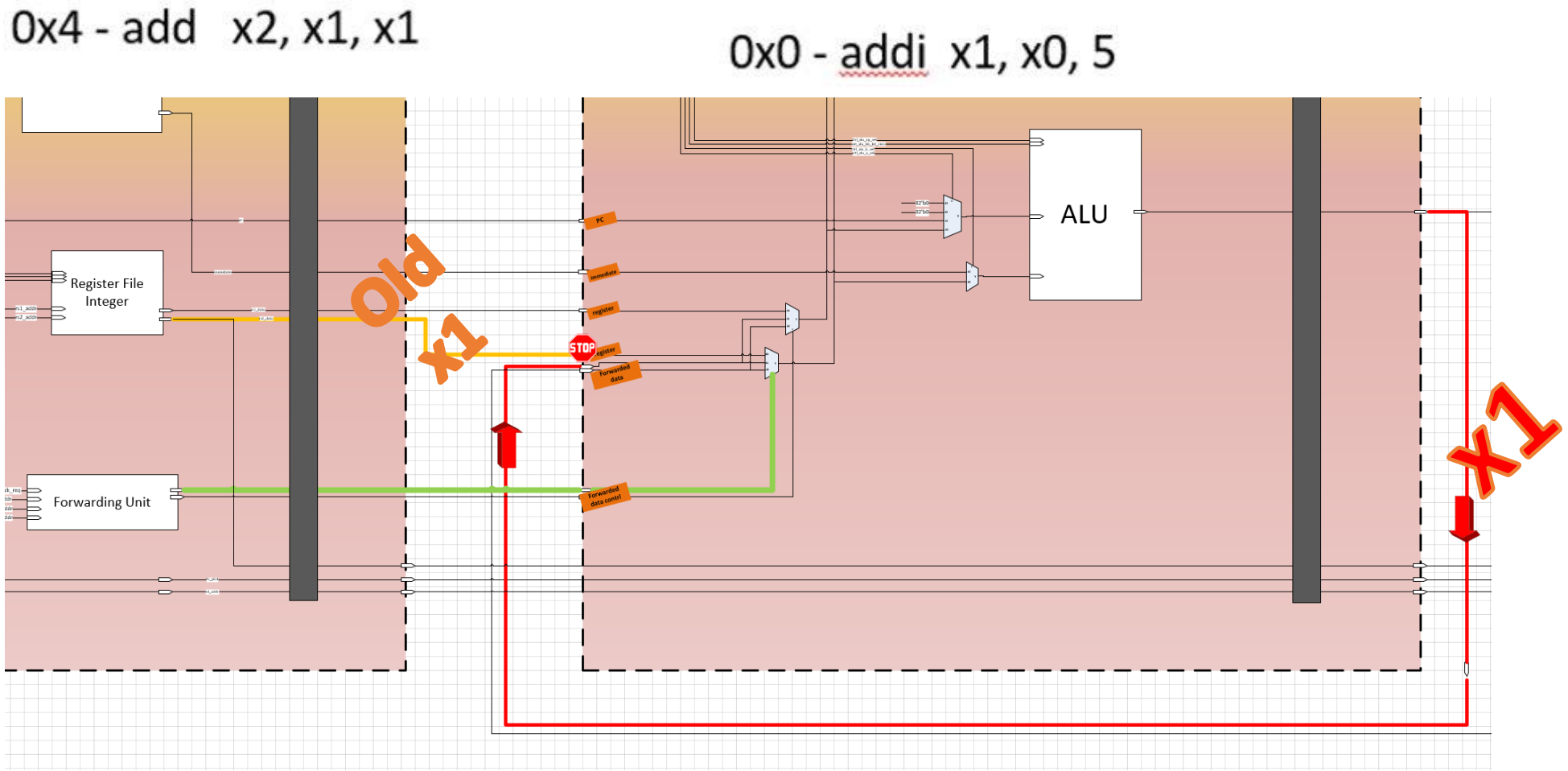
Data hazard

Data hazard can happen when new instruction need to use a data from a Register before the data is available in the register file

```
0x0 -   addi  x1, x0,  5
0x4 -   add   x2, x1, x1
0x8 -   add   x3, x1, x1
0xC -   NOP
```



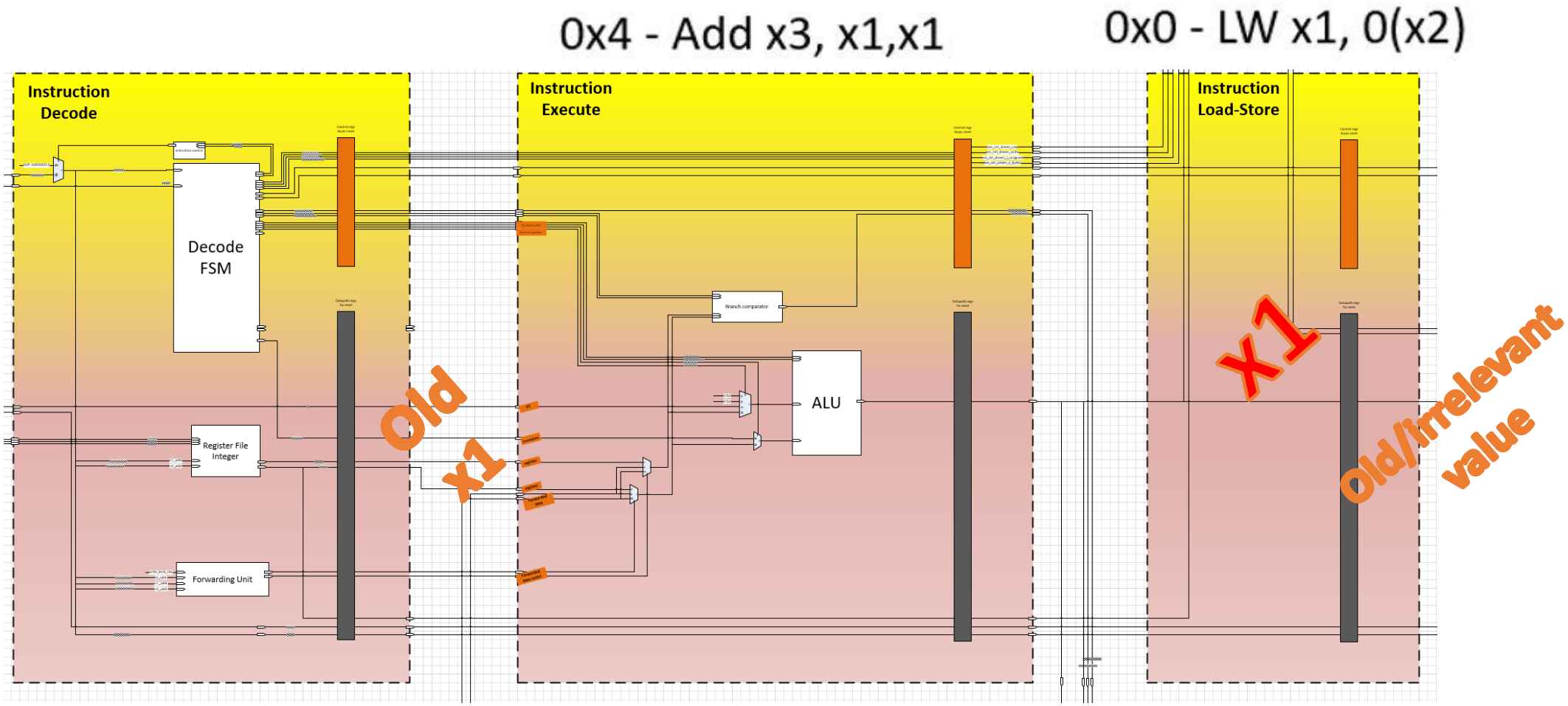
Data hazard – Forwarding unit



Load hazard

Load hazard can happen when new instruction need to use a data which loaded from the memory in the previous instruction

0x0 - LW x1, 0(x2)
0x4 - Add x3, x1,x1
0x8 - NOP
0xC - NOP



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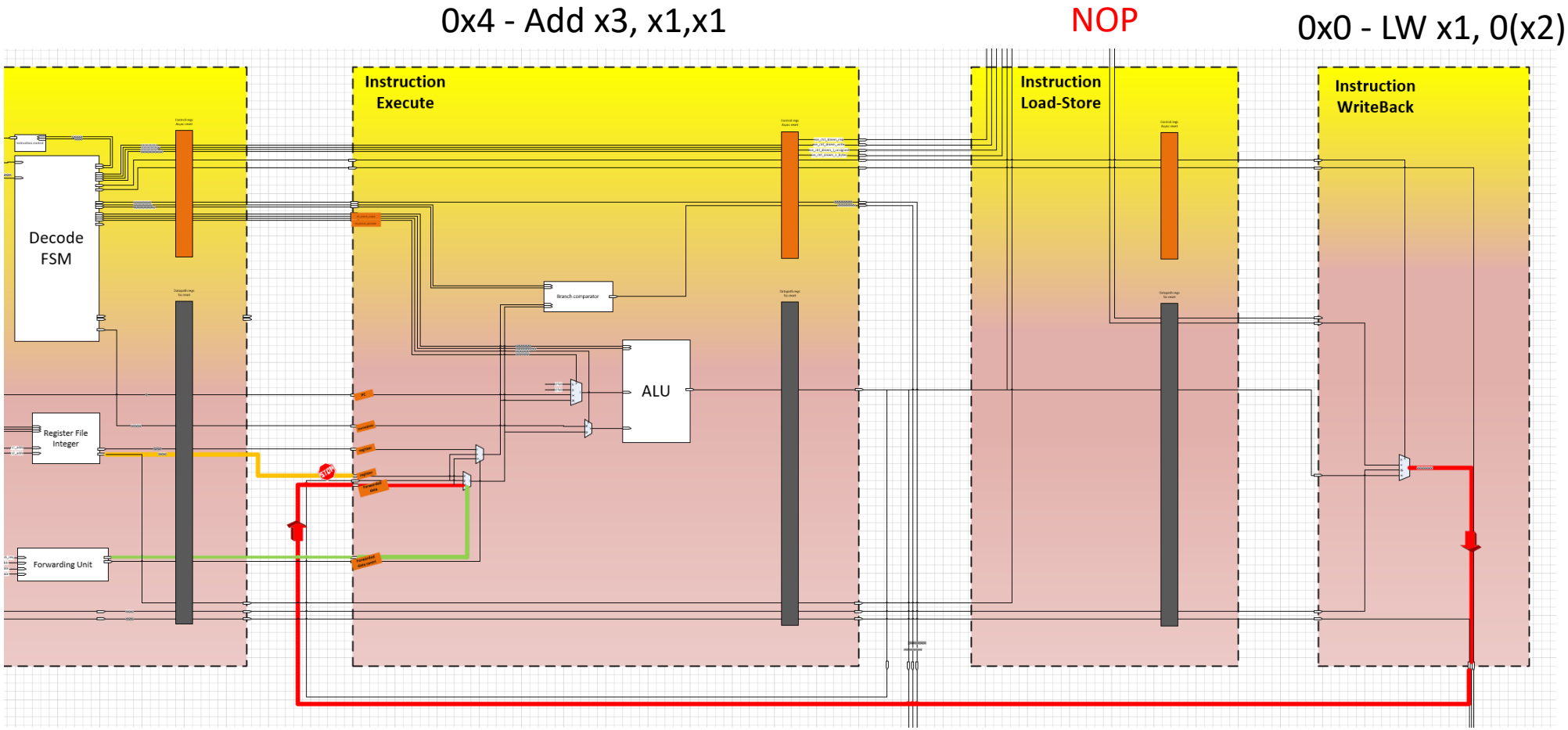
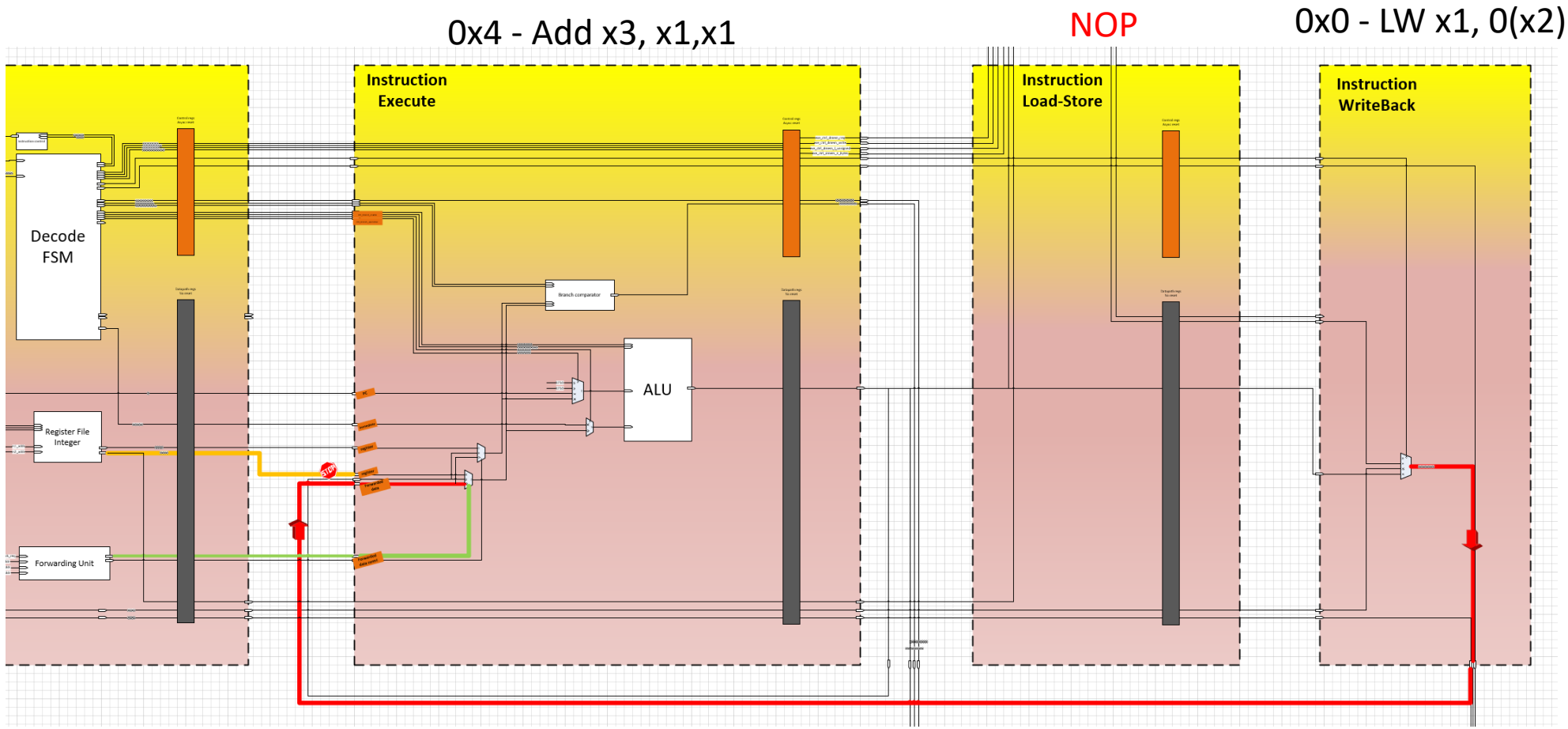


Control hazard

Load hazard can happen when we have a conditional branch instruction and we don’t know which instruction to fetch

0x0 – jump/Branch 0x10
0x4 - Add x3, x1,x1
0x8 - Add x4, x10, x10
0xC - Add x5, x11, x11
0x10 - Add x6, x12, x12



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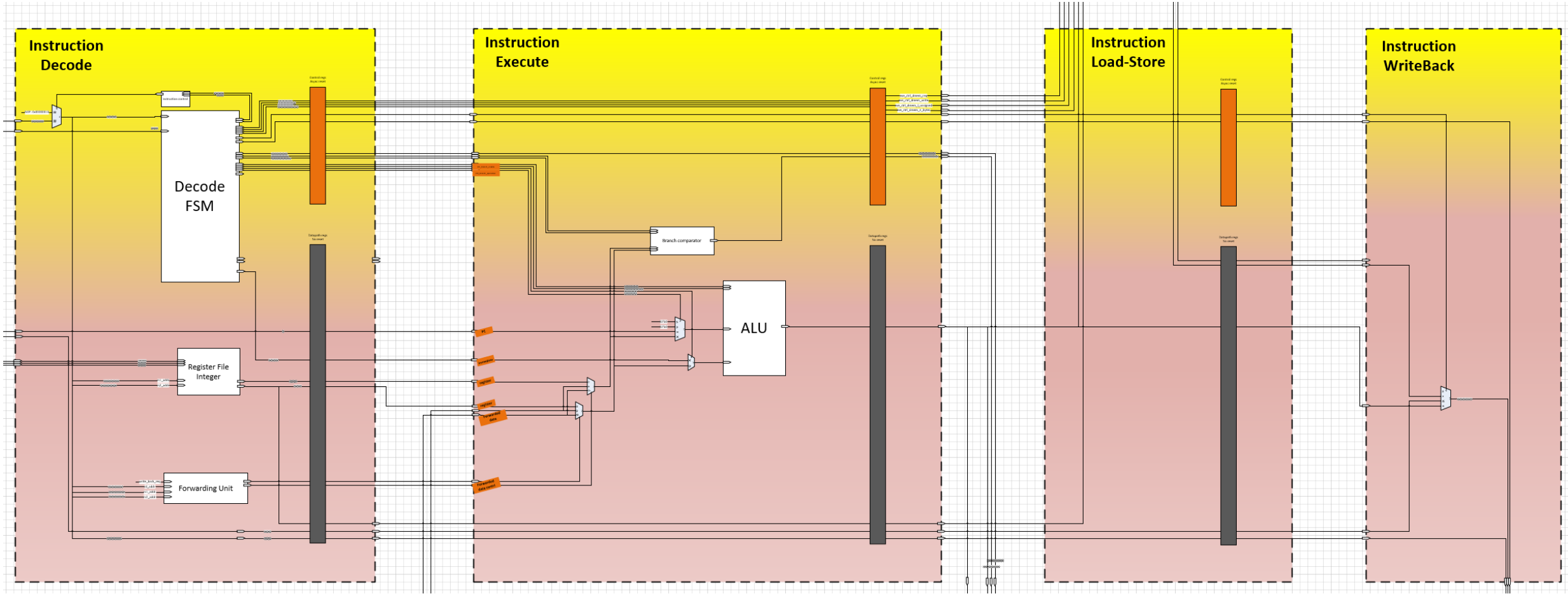

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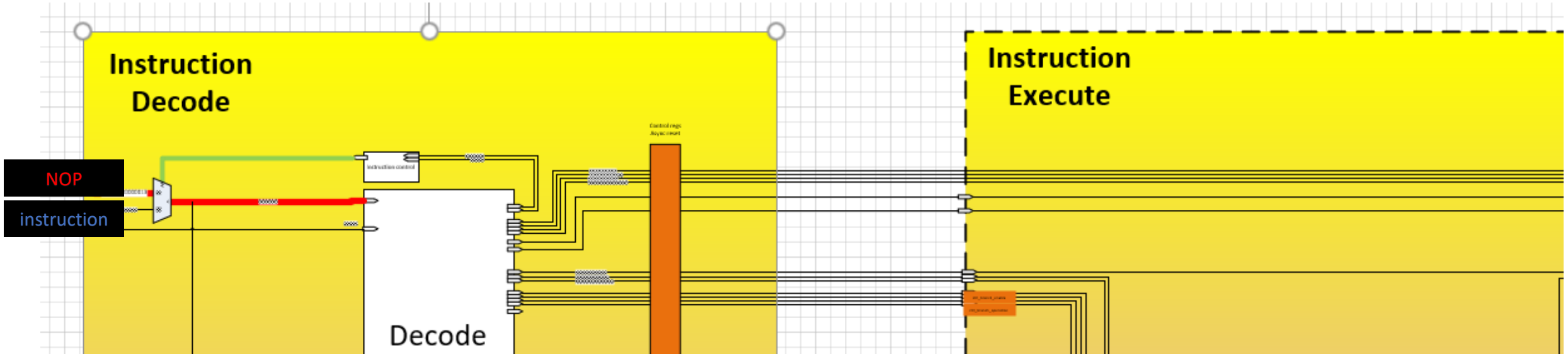

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NOP
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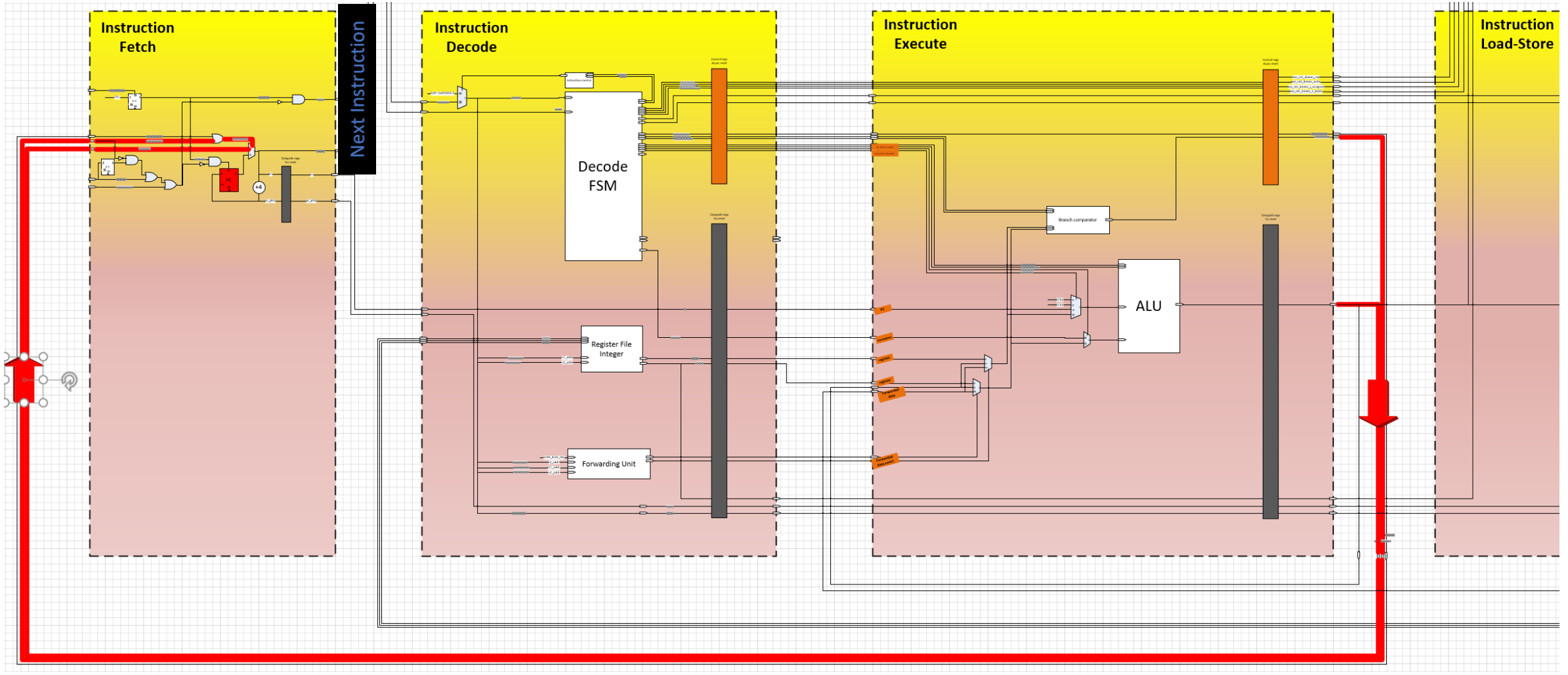
NOP NOP 0x0 – jump/Branch 0x10

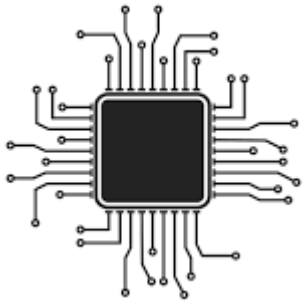


Performance

- $CPU_{time} = IC * CPI * \frac{1}{f}$
- Power ?
- Area ?

TEST	INSTRUCTIONS RETIRED	CYCLES	IPC	DESCRIPTION
Tower of Hanoi	28198	37924	0.743	N of disks = 10
Sudoku solver	3533	4909	0.720	Cube = 9x9
Fibonacci	470725	645863	0.728	Fib(20)
Binary search	652	751	0.868	N=200 elements

Validation plan



Design review

RTL simulations

System-level simulation

FPGA deployment

ISA simulations

Data memory image comparison

Validation trackers

Performance trackers

Demo

Alternatives…
RISC based Arch

PowerPC™

Apple-IBM-Motorolla

AVR®

Atmell
arduino

BLACKfin®

Analog Devices
2000

arm

Acorn RISC machines
1978

MIPS

1981-Stanford
Playstation-2
Wave computing

RISC-V in the press