1. Introduce

Bio-M001A is a Bio-module in healthcare; The Bio-module measures and transfers various types of bio-data including ECG, RESP, GSR, HR, PPG, HCM and BIA etc, integrated Bio-Processor with Analog Front-End to make an all-in-one health monitoring solution.

The algorithm core runs in Bio-Processor, including SPO2, motion recognition,dynamic heart rate monitoring, trend analysis of blood pressure, Emotional and mental stress etc.

The Bio-module integrates red (660 nm), green (520 nm) and infrared (940 nm) three-color LED and photodiode(PD) sensor to realize PPG-related applications; and supports four electrodes to achieve applications with human electrical activities and impedance activities; on-module 14-bit three-axis Gsensor for motion/sleep applications.

The Bio-module hardware interface supports SPI/I2C/UART optional, FPC connector reference DF37NB-30DS-0.4V.

APPLICATIONS

1. Fitness,wristband devices;
2. Healthcare devices;
3. Mobile devices and robots etc;

FEATURES

- Single lead ECG :
  - 3 electrodes with right leg driver;
  - Lead-off detect;

- Bio-impedance with 4 electrodes:
  - Built-in DAC and multi-frequency waveform generator;
  - Support RESP,BIA and GSR etc;

- PPG:
  - on-module red (660 nm), green (520 nm) and IR (940 nm) LED and PD;
  - Support HR,SPO2 and bio-assay etc;

- Electrodes mean interface:
  - Support electrodes as input keypad;
  - Support pair of electrodes as data channel: eg,USB/UART etc;
  - Support pair of electrodes as power charger channel;

- Gsensor:
  - Built-in 14 bits 3-axis Gsensor, range + 2G, + 4G, + 8g, + 16g;
  - Pedometer,Action recognition;

- Hardware interface:
  - Optional SPI/UART/I2C;
  - FPC connector DF37NB-30DS-0.4V,from hirose;

- Small size, suitable for wristband devices:
  - 22x26mm;

4. Hardware interface

4. 1 FPC Connector

Bio-M001A provides 30-pin FPC connector (reference DF37NB-30DS-0.4V) to access analog and digital data.

4. 1. 1 Pins map

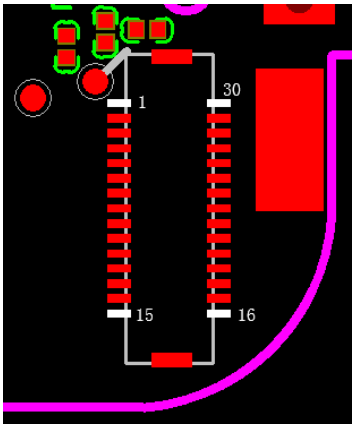


Figure 1

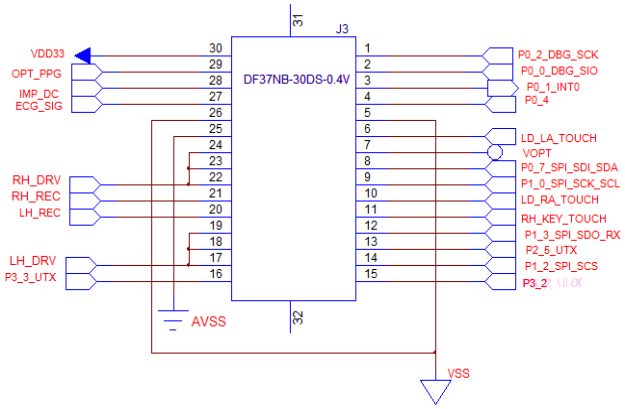


Figure 2

4．1．2　FPC Pins

Table 1:

Name	No.	Type	Function
P0_2	1	I/O	GP0.2; hardware intface switch
P0_0	2	I/O	GP0.0; hardware intface switch
P0_1_INT	3	I/O	GP0.1; INT Output, the rising edge active
P0_4	4	I/O	GP0.4; firmware upgrade mode switch
VSS	5	POWER	Ground
LD_LA_TOUCH	6	AO	Lead-off detection analog output from left arm
VOPT	7	POWER	Power supply driving PPG led
P0_7_SPI_SDI_SDA	8	I/O	GP0.7; SDI of slave spi; SDA of slave I2C
P1_0_SPI_SCK_SCL	9	I/O	GP1.0; SCK of slave spi; SCL of slave I2C
LD_RA_TOUCH	10	AO	Lead-off detection analog output0 from right arm
RH_KEY_TOUCH	11	AO	Lead-off detection analog output1 from right arm
P1_3_SPI_SDO_RX	12	I/O	GP1.3; SDO of slave spi; RX of UART
P2_5_UTX	13	I/O	GP2.5; TX of UART
P1_2_SPI_SCS	14	I/O	GP1.2; SCS of slave spi
P3_2	15	I/O	GP3.2
P3_3	16	I/O	GP3.3
LH_DRV	17	SO	Drive source about left hand, ECG RLD output
	18		
	19		
LH_REC	20	SI	Input about ECG/impedance from left hand
RH_REC	21	SI	Input about ECG/impedance from right hand
RH_DRV	22	SO	Drive source about right hand
	23		
	24		
AVSS	25	POWER	Analog ground
VSS	26	POWER	Ground
ECG_SIG	27	AO	ECG analog output
IMP_DC	28	AO	Body impedance analog DC output
OPT_PPG	29	AO	PPG analog output
VDD33	30	POWER	Power supply

Note：AO--Analog Output,SO--Source Output,SI--Source Input

4．1．3 Strapping Pins

Bio-M001A has three strapping pins ：

- P0_2
- P0_0
- P0_4

During reset, Bio-M001A interface and work mode are configured by sampling strapping pin voltage level. The final mode will determine the actual functions of the five pins of P0_7, P1_0, P1_3, P2_5 and P1_2.

The internal default of the module is weak pull-up, and we can complete pull-down by external resistor. After reset, the strapping pins work as the normal functions pins.. Refer to the following table:

Table 2 Hardware interface definition :

Hardware intface method					
pin	default	SPI	UART	I2C(Address=0x66)	I2C(Address=0x67)
P0_0	pull-up	1	0	1	0
P0_2	pull-up	1	0	0	1

Table 3 Work mode definition :

Work mode			
pin	default	Normal	Boot
P0_4	pull-up	1	0

4．2 Hardware interface

Standard I2C,SPI and UART interfaces are used to communicate with the Bio-module. Hardware interface definition is referred to table 2. Function map for pins is referred to table 4.

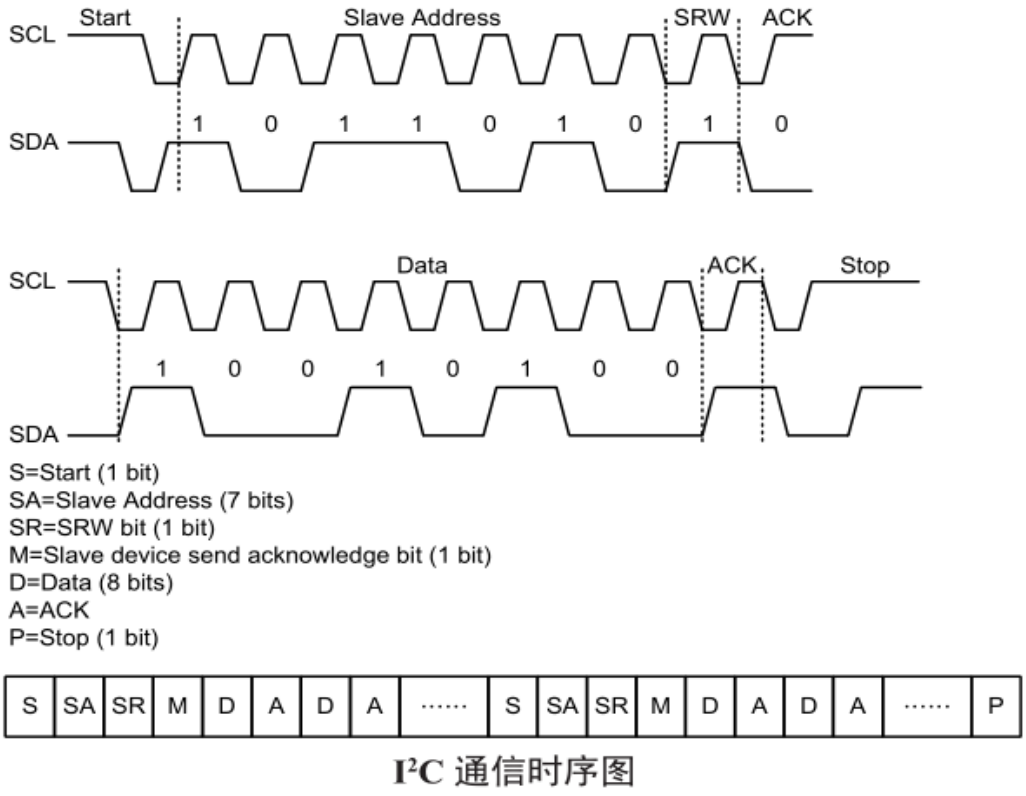
Table 4:

Hardware intface pins map					
intface	P0_7	P1_0	P1_2	P1_3	P2_5
SPI	SDI	SCK	SCS	SDO	x
I2C	SDA	SCL	x	x	x
UART	x	x	x	RX	TX

4．2．1 I2C Operation

Bio-M001A supports slave I2C，I2C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I2C device address of Bio-M001A is shown below Table 5. The LSB bit of the 7bits device address is configured via P0_0，P0_2 pins; Refer to table 2 for address configuration.

Figure 3



I²C 通信时序图

Table 5:

I2C Address							
SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	W/R
1	1	0	0	1	1	LSB	0/1

4．2．2 SPI Operation

Bio-M001A support 4-wires slave SPI;As shown in Figure 3，The falling edge of SCS, in conjunction with the rising edge of SCLK, determines the start of framing. Data is 8 bits，and MSB first mode.

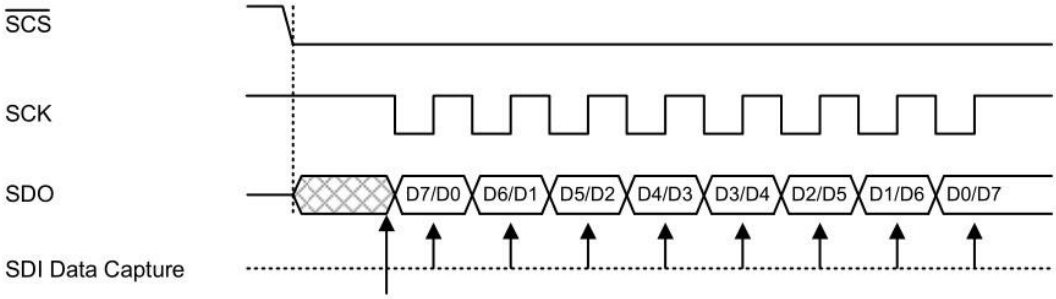


Figure 4

4．3 Sensors map

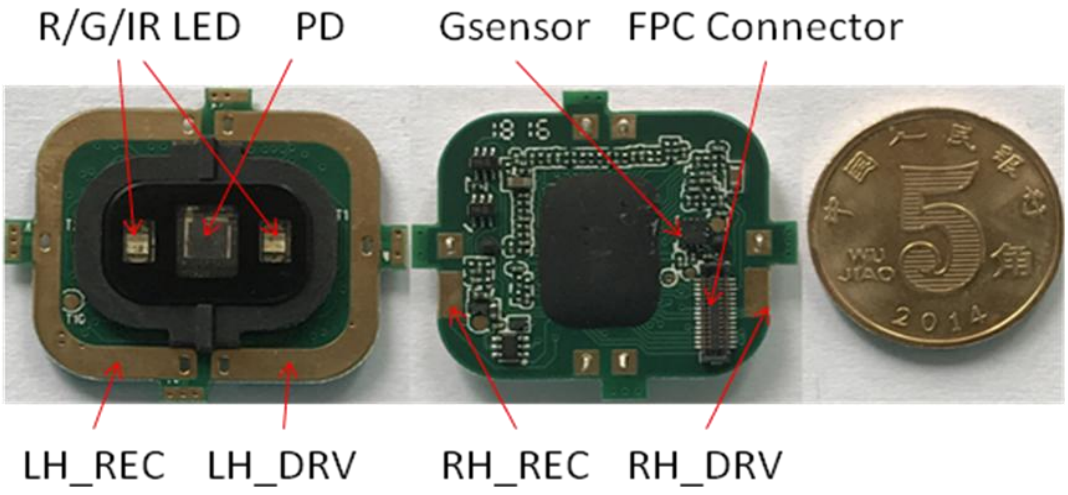
Bio-M001A integrates three major sensors ：

A． Optical transceiver sensor for collecting PPG signal. As shown in Fig. 5, R/G/IR LED is red, green and infrared light emitting area, and PD is photodiode sensitive area；

B． Electrode sensor for collecting electrical and impedance signals of human body. As shown in Fig. 5, xH_REC is connected with limb leads for sensing electrical and impedance activities, and xH_DRV is connected with driving electrode.

C． GSensor for feeling motion;

Figure 5



5 Registers

5．1 Registers map

Table 6 describes the list of registers about Bio-M001A.

Table 6:

Name	Addr	Type	Description	Default
Reg_INT_DATAL	0x00	R	Interrupt data low 8 bits	0x00
Reg_INT_DATAM	0x01	R	Interrupt data middle 8 bits	0x00
Reg_INT_DATAH	0x02	R	Interrupt data high 8 bits	0x00
Reg_INT_DATATYPE	0x03	R	Interrupt data type	0x00
Reg_DEVICE_ID	0x04	R	Device ID	0x21/0xA1
Reg_FIRMWARE_VER	0x05	R	Firmware version	0xXX
Reg_BL_VERSION	0x06	R	Boot loader version	0x01/x81
Reg_PSTATUS	0x07	R	Reserve	0x00
Reg_FUN_CMD0	0x08	R/W	Function CMD 0	0x00
Reg_MODE_CMD1	0x09	R/W	Mode and Function CMD 1	0x00
Reg_BL_DATA	0x0A	W	Upload CMD during upgrading	0x00

5．2 Registers Description

5．2．1 Reg_INT_DATAL （00H）

The register is updated when a new interrupt occurs, and the value is defined by the Reg_INT_DATATYPE field. During firmware update, the register content is response value for firmware upgrade command. The definitions are as follows:

Table 7:

Firmware upgrade response description		
RSP Name	RSP Value	Description
BL_RSP_OK	0x01	Response ok
BL_RSP_PARA_ERROR	0x02	Command parameter error
BL_RSP_CMD_ERROR	0x03	Command error
BL_RSP_ERASE_ERROR	0x04	FLASH erase error
BL_RSP_PROGRAM_ERROR	0x05	FLASH Programming error
BL_RSP_CRC_ERROR	0x06	CRC Check error
BL_RSP_VERIFY_ERROR	0x07	FLASH Verify error
BL_RSP_UNKNOW	0x08	Unknow error

5.2.2 Reg_INT_DATAM (01H)

The register is updated when a new interrupt occurs, and the value is defined by the Reg_INT_DATATYPE field.

5.2.3 Reg_INT_DATAH (02H)

The register is updated when a new interrupt occurs, and the value is defined by the Reg_INT_DATATYPE field.

5.2.4 Reg_INT_DATATYPE (03H)

When a new interrupt occurs, the register and 0x00H-0x02H registers will be updated. The high 4-bits(Data Type field) of the register indicates the interrupt data type, and please refer to table 9.

When the data type is set to a value associated with the embedded 24-bit analog-to-digital converter (AD) in Bio-M001A, the low 4-bits of the register are used as the AD Sample Sequence field to indicate the sequence number of the data sampled by AD; the sequence number is used to verify that data frames are continuous and that no packets are lost.

Table 9:

Data Type Map			
Data Type	Reg_INT_DATAL	Reg_INT_DATAM	Reg_INT_DATAH
0h	Low 8-bits AD data for Green/DC PPG	Middle 8-bits AD data for Green/DC PPG	High 8-bits AD data for Green/DC PPG
1h	Low 8-bits AD data for Red/DC PPG	Middle 8-bits AD data for Red/DC PPG	High 8-bits AD data for Red/DC PPG
2h	Low 8-bits AD data for IR/DC PPG	Middle 8-bits AD data for IR/DC PPG	High 8-bits AD data for IR/DC PPG
3h	Low 8-bits AD data for Impedance	High 8-bits AD data for Impedance	High 8-bits AD data for Impedance
4h	Low 8-bits AD data for GSR	Low 8-bits AD data for GSR	Low 8-bits AD data for GSR
5h	Reserve	Reserve	Reserve
6h	Reserve	Reserve	Reserve
7h	Low 8-bits AD data for Green/AC PPG	Middle 8-bits AD data for Green/AC PPG	High 8-bits AD data for Green/AC PPG
8h	Low 8-bits AD data for Red/AC PPG	Middle 8-bits AD data for Red/AC PPG	High 8-bits AD data for Red/AC PPG
9h	Low 8-bits AD data for IR/AC PPG	Middle 8-bits AD data for IR/AC PPG	High 8-bits AD data for IR/AC PPG
Ah	Low 8-bits AD data for RESP	Low 8-bits AD data for RESP	Low 8-bits AD data for RESP
Bh	Low 8-bits AD data for ECG	Low 8-bits AD data for ECG	Low 8-bits AD data for ECG
Ch	Reserve	Reserve	Reserve
Dh	GSensor	GSensor	GSensor
Eh	Reserve	Reserve	Reserve
Fh	Response for firmware upgrade	Reserve	Reserve

Table 8:

Reg_INT_DATATYPE							
Data Type				AD Sample Sequence			
0	0	0	0	0	0	0	0

5.2.5 Reg_DEVICE_ID (04H)

The low 7-bits of the register indicate device special identifier (0x21), the bit7 indicates current operation mode , 0 for Boot mode, 1 for normal mode.

Table 10:

Device ID							
MODE	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0/1	0	1	0	0	0	0	1

5.2.6 Reg_FIRMWARE_VER (05H)

This register indicates firmware version of device. The specific value can refer to released production version.

5.2.7 Reg_BL_VERSION (06H)

The low 7-bits of the register indicate boot loader version of device, the bit7 indicates current operation mode , 0 for Boot mode, 1 for normal mode.

Table 11:

Device ID							
MODE	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0/1	0	1	0	0	0	0	1

5.2.8 Reg_PSTATUS (07H)

The register is reserved.

5.2.9 Reg_FUN_CMD0 (08H)

This is a functional control register that operates in two ways; when the high 3-bits of register Reg_MODE_CMD1 is defined as FW Upgrade mode (see Table 14 and Table 16), the register content is firmware upgrade command, and the command definitions please refer to table 13;

If the high 3-bits of register Reg_MODE_CMD1 is not defined as FW Upgrade mode, then please refer to Table 12 for the register content; if the related bits are set to 1, the related functions can be enabled.

Please note: After writing this register, the register Reg_MODE_CMD1 (09H) must be followed to write, and the operation will be effective. For specific function commands, please refer to table 15.

Table 12:

Function CMD Map							
GSR	RESP	Impedance	Preserve	PPG_IR	PPG_GREEN	PPG_RED	ECG_EXT_AD
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0

Table 13:

Firmware upgrade command description		
BL CMD Name	CMD Value	Description
BL_CMD_ERASEAPP	0x62	FLASH Erase
BL_CMD_JMPAPP	0x63	Jump to APP
BL_CMD_APRDY	0x64	APP ready OK
BL_CMD_PROGRAM	0x6F	FLASH Programme

5. 2. 10 Reg_MODE_CMD1 (09H)

This is a mode and function control register, and a normal operation command consists of three parts: Function Mode + Function CMD + Start bit;

Mode are defined by high 3-bits of the register, as shown in Table 14 and Table 16;

When Start bit is set to 1, it means the current operation is started, otherwise it means stopped.

The function command includes Reg_FUN_CMD0 and the low 4 bits of this register. For specific function commands, please refer to table 15.

Table 15:

Function CMD description	
Function CMD	Description
ECG_EXT_AD	ECG, Using external AD sampling
PPG_RED	PPG with red led
PPG_GREEN	PPG with green led
PPG_IR	PPG with IR led
Impedance	Limb bio-impedance
RESP	Respiratory
GSR	Electrodermal activity
ECG_INT_AD	ECG, Using internal AD sampling
Preserve	Reserve

Table 14:

Function CMD1 Map							
Function Mode			Start	Preserve	Preserve	Preserve	ECG_INT_AD
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0

Table 16:

Function Mode Map				
Function Mode Value			Mode	Description
Bit7	Bit6	Bit5		
1	1	1	Halt mode	power saving mode
1	1	0	Obey mode	Passive measurement mode
1	0	1	Watch mode	Supervision mode
1	0	0	Calibration	Calibration mode
0	1	1	FW Upgrade	Firmware update mode

5. 2. 11 Reg_BL_DATA (0AH)

This register is used for large data block operation when Bio-M001A is upgrading firmware. The original binary data block of the firmware can be written directly to this register, and then the internal flash is programmed.

6 Firmware update

During power on, Bio-M001A will start according to the flow, as shown in Figure 6; and Bio-M001A can be entered into boot or app mode under certain setting.

During reset, the P0_4 Pin is pull-down, or send request during APP mode(Refer to 5. 2. 10), Bio-M001A will be entered into boot mode.

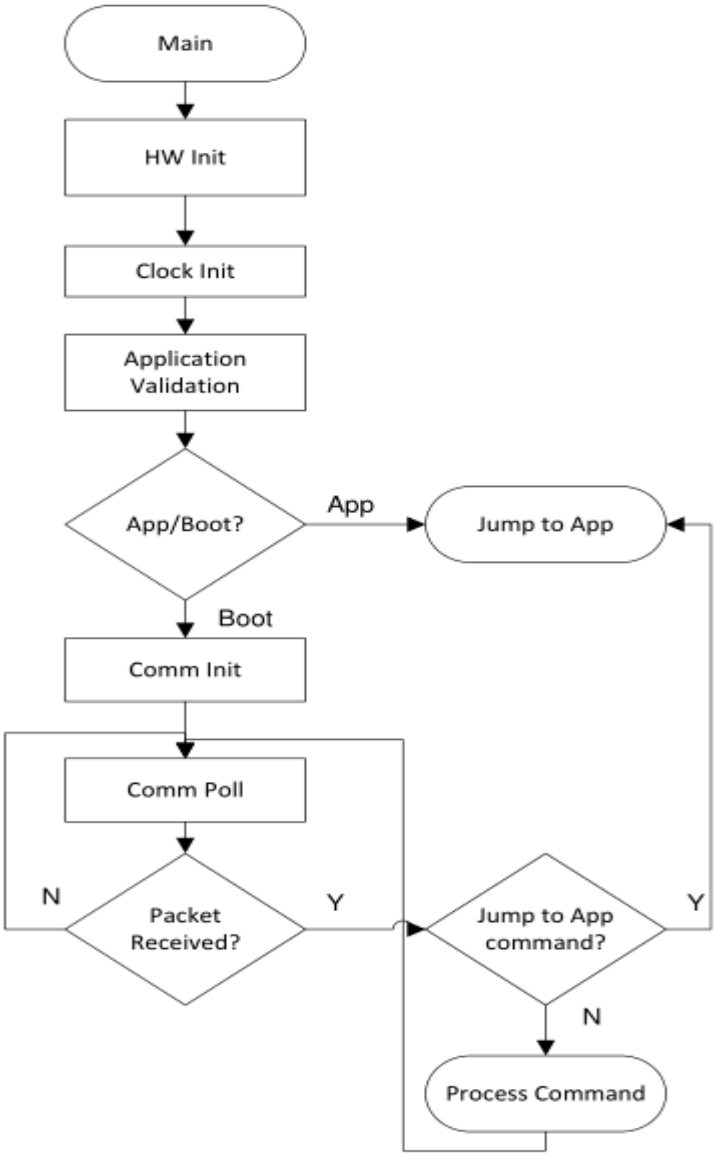

Main
HW Init
Clock Init
Application Validation
App/Boot?
App
Jump to App
Boot
Comm Init
Comm Poll
N
Packet Received?
Y
Jump to App command?
Y
N
Process Command

Figure 6