DLX Instruction Format

	I-type 6 5 5 16 op rs1 rs2 imm	R-type 6 5 5 5 11 op rs1 rs2 rd func	J-type 6 26 op offset
Load/Store			
Load	R(rs2) <- M[R(rs1)+imm] Ex. LH R3,4(R4)		
Store	M[R(rs1)+imm] <- R(rs2) Ex. SB 4(R4),R3		
ALU			
xxxI	R(rs2) <- R(rs1) op imm Ex. ADDI R7,R8,#3		
xxx		R(rd) <- R(rs1) func R(rs2) Ex. ADD R2,R3,R4 (op = 0)	
Jump			
J/JAL (PC-relative)			PC <- PC + offset / R31 <- PC; PC <- PC + offset Ex. J label / JAL label
JR/JALR	PC <- R(rs1) / R31 <- PC; PC <- R(rs1) Ex. JR R1 / JALR R1		
Branch (PC-relative)	if (R(rs1) op 0) PC <- PC + imm (op: == or !=) Ex. BEQZ R1, label		

Opcodes/Signal codes for DLX

/* Primary opcodes (opcode field) for instructions */

OP_J 2	OP_SUBUI 11	OP_SEQI 24	OP_LBU 36	OP_SEQUI 48
OP_JAL 3	OP_ANDI 12	OP_SNEI 25	OP_LHU 37	OP_SNEUI 49
OP_BEQZ 4	OP_ORI 13	OP_SLTI 26		OP_SLTUI 50
OP_BNEZ 5	OP_XORI 14	OP_SGTI 27		OP_SGTUI 51
	OP_LHI 15	OP_SLEI 28	OP_SB 40	OP_SLEUI 52
		OP_SGEI 29	OP_SH 41	OP_SGEUI 53
OP_ADDI 8		OP_LB 32	OP_SW 43	OP_SLLI 54
OP_ADDUI 9	OP_JR 18	OP_LH 33		OP_SRLI 55
OP_SUBI 10	OP_JALR 19	OP_LW 35		OP_SRAI 56

/* Secondary opcodes (**func** field) for ALU instructions (primary opcode = 0) */

OP_SLL 4		OP_SUBU 35	OP_SGT 43
OP_SRL 6		OP_AND 36	OP_SLE 44
OP_SRA 7		OP_OR 37	OP_SGE 45
OP_SLTU 18		OP_XOR 38	
OP_SGTU 19	OP_ADD 32	OP_SEQ 40	
OP_SLEU 20	OP_ADDU 33	OP_SNE 41	
OP_SGEU 21	OP_SUB 34	OP_SLT 42	

/* Control signal codes (**ALUop** signals) for ALU operations */

ADD 0	OR 5	SEQ 16	SGEU 23	ADDU 28
SUB 1	XOR 6	SNE 18	SGT 24	SUBU 29
PASS_S1 2	SLL 8	SLT 20	SGTU 25	
PASS_S2 3	SRL 10	SLTU 21	SLE 26	
AND 4	SRA 12	SGE 22	SLEU 27	

/* Control signal codes (**S2op** signals) for S2 bus operations in ALU */

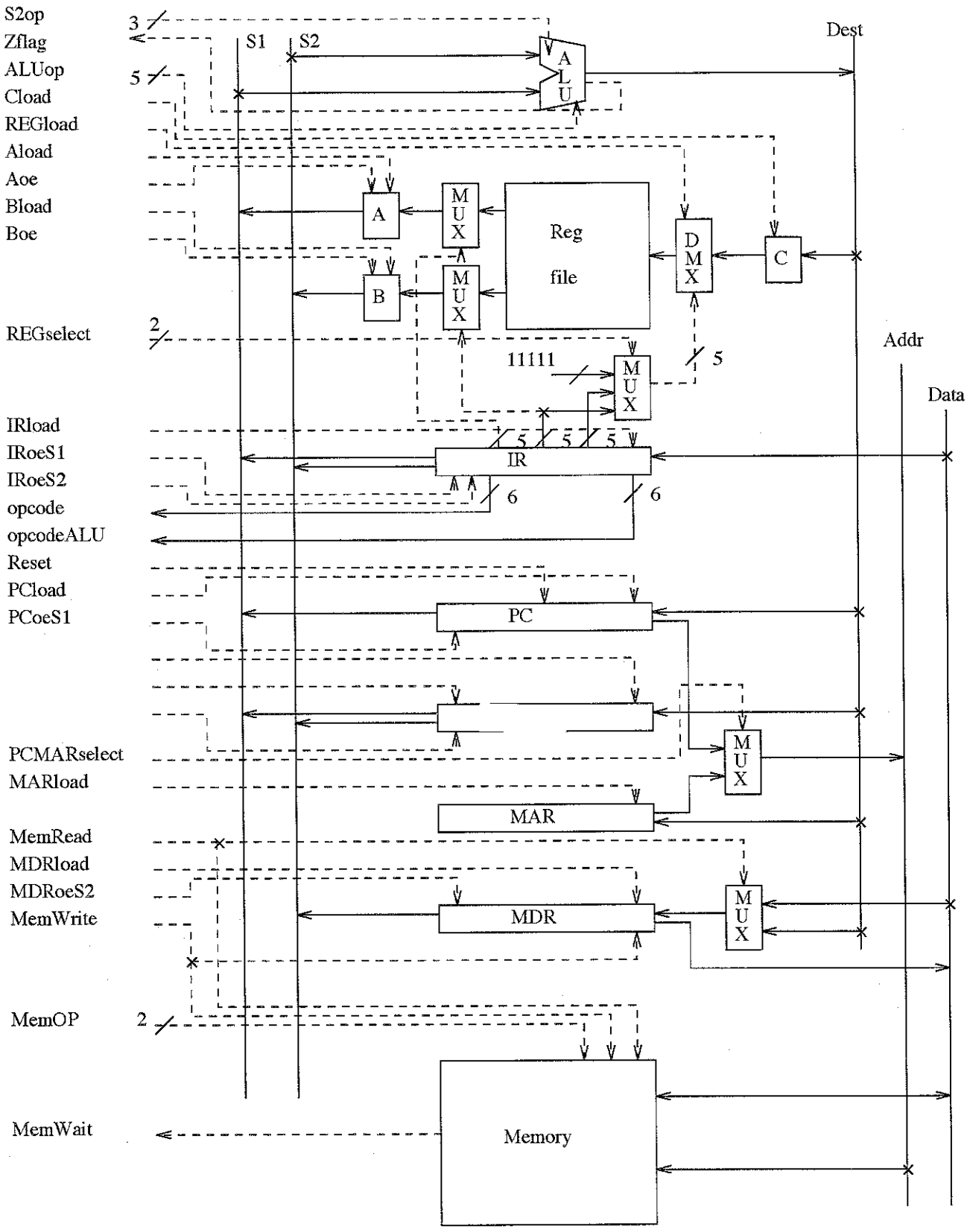
PASS 0	IMM8ZXT 2	IMM16ZXT 4	CONST16 6
IMM8SXT 1	IMM16SXT 3	IMM26SXT 5	CONST4 7

/* Control signal codes (**MemOP** signals) for Memory operations */

W_OP 0	HW_OP 1	B_OP 2

/* Control signal codes (**REGselect** signals) for selecting destination in register file */

rd 0	rs2 1	$31(11111_b)$ 2


S2op
Zflag
ALUop
Cload
REGload
Aload
Aoe
Bload
Boe
REGselect
IRload
IRoeS1
IRoeS2
opcode
opcodeALU
Reset
PCload
PCoeS1
PCMARselect
MARload
MemRead
MDRload
MDRoeS2
MemWrite
MemOP
MemWait
3
5
2
S1
S2
ALU
Dest
A
B
MUX
Reg
file
DMX
C
11111
5
Addr
Data
IR
6
PC
MAR
MDR
Memory