An FPGA Implementation of a Digital Storage Oscilloscope

Andrei Purcarus Ze Yu Yang

ECSE 487
McGill University

April 10, 2017

Table of Contents

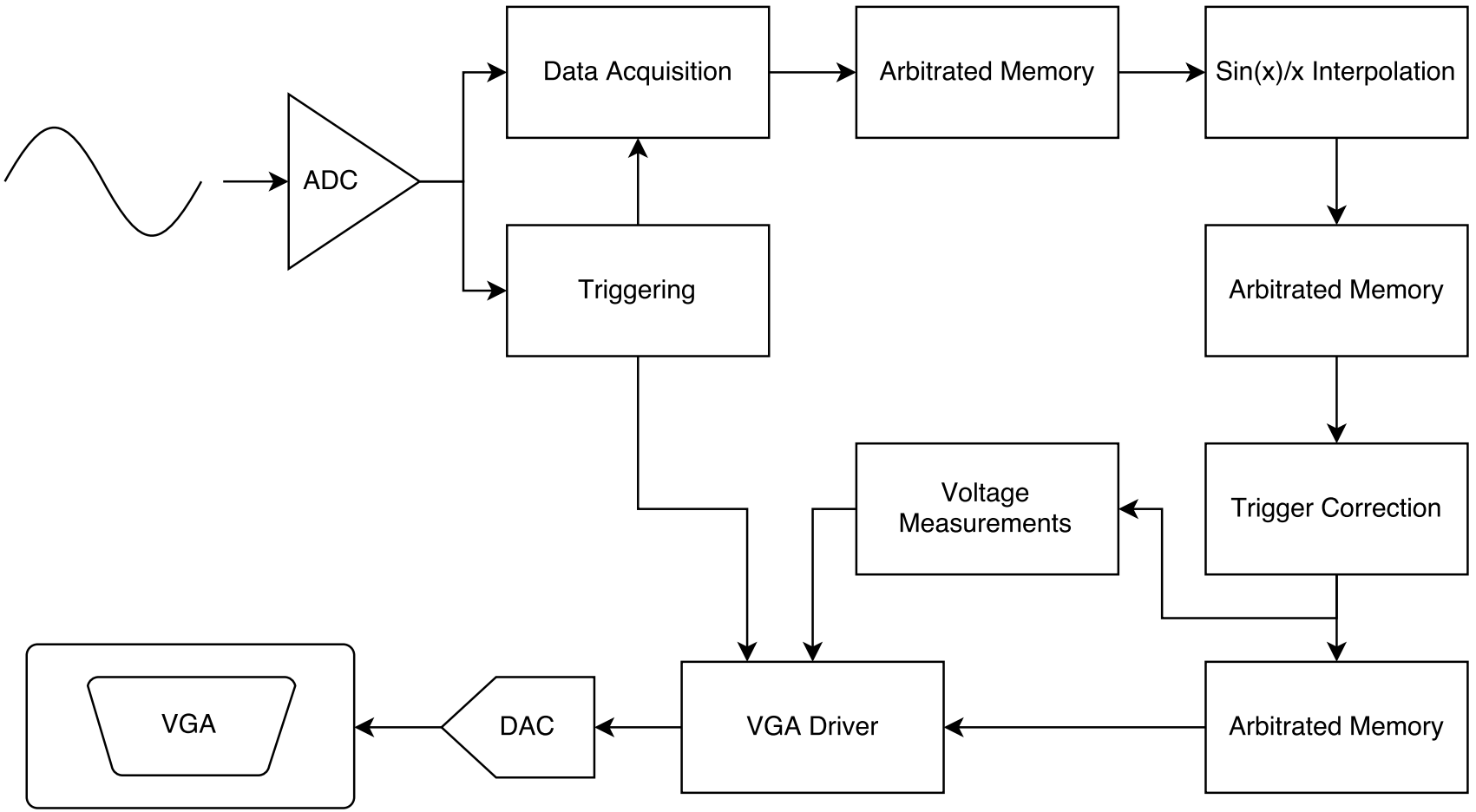
Table of Contents

Objectives

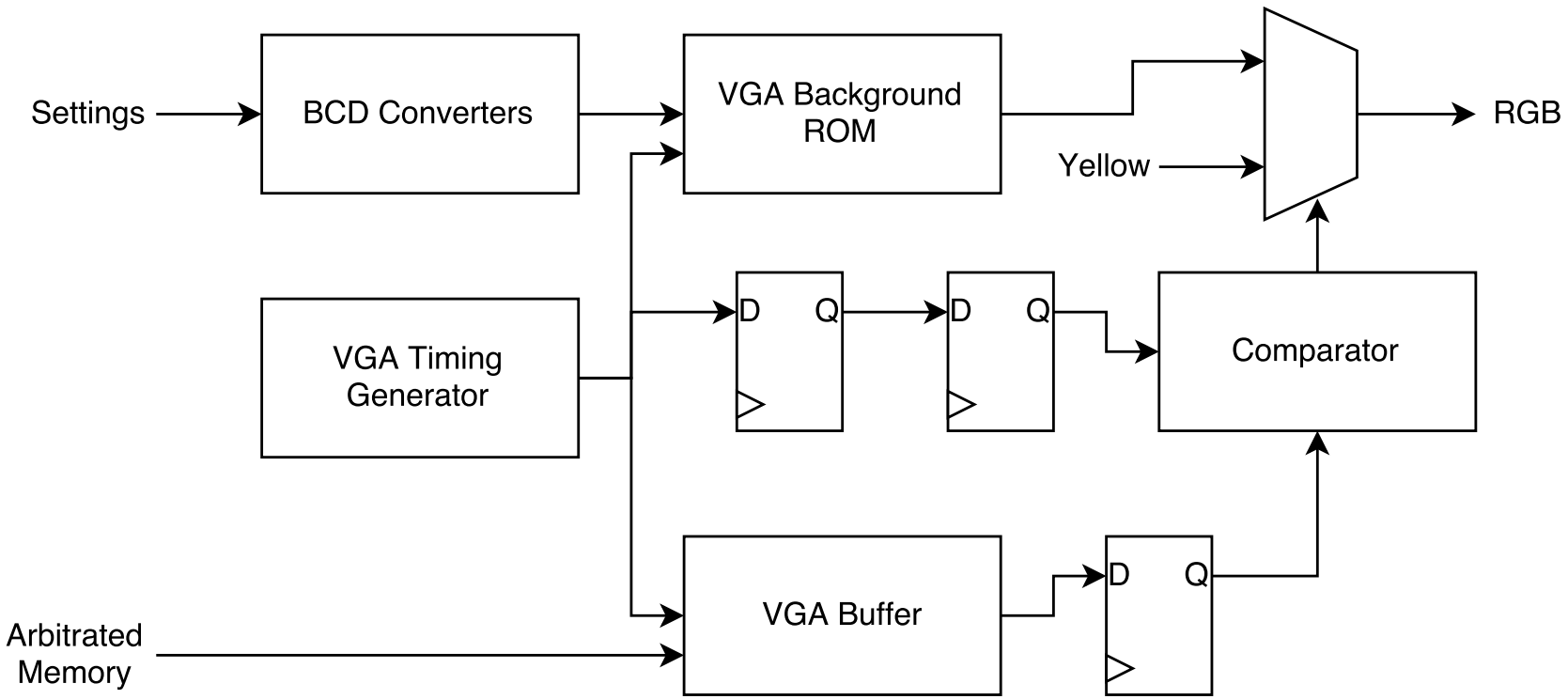
- Display of waveforms with frequencies from 1 kHz to 200 kHz
- Frequency measurements with an accuracy of 1 % + 10 Hz
- Voltage measurements with an accuracy of 1 % + 10 mV

Table of Contents

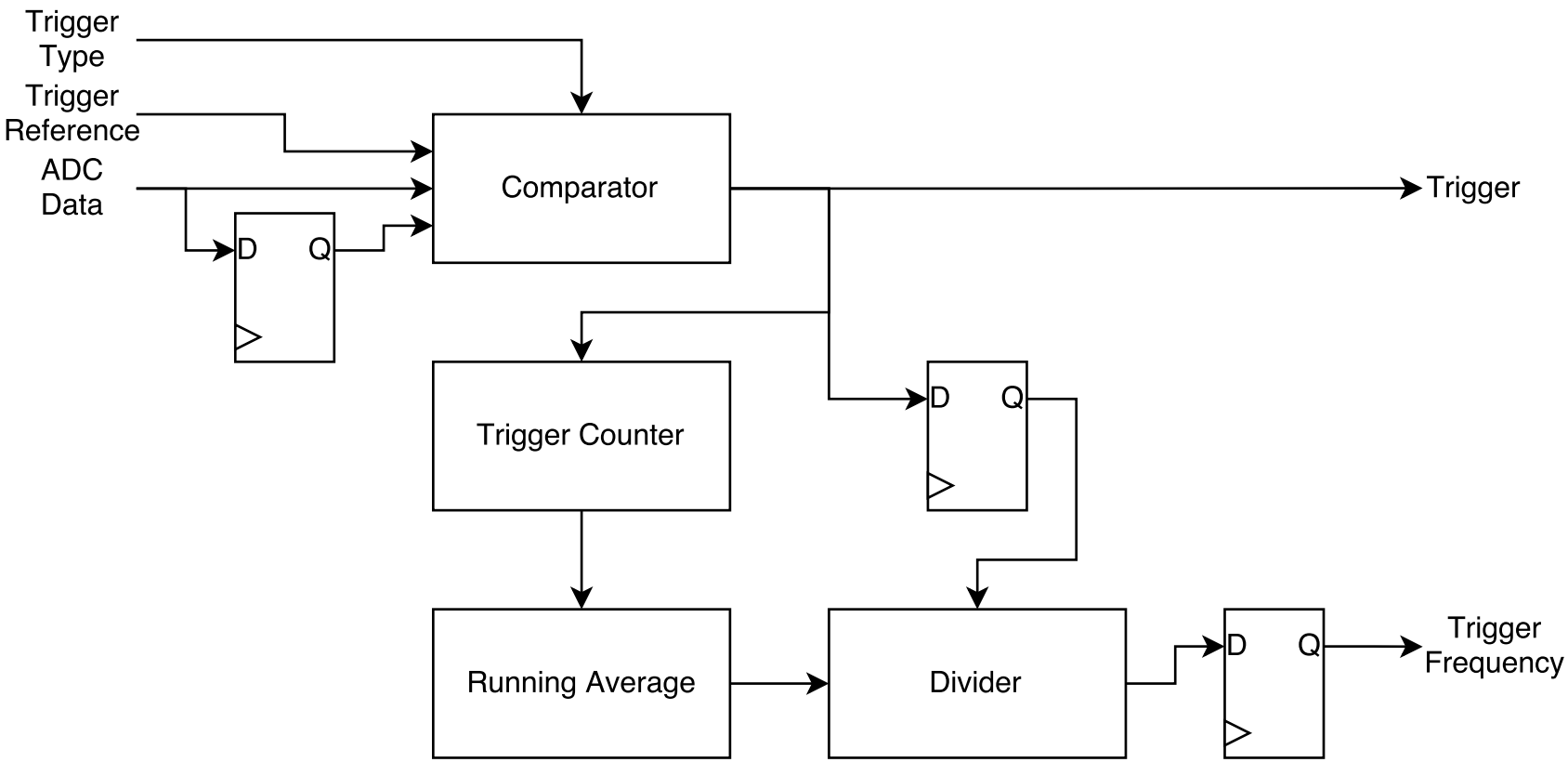
System


Data Acquisition
Arbitrated Memory
Sin(x)/x Interpolation
ADC
Triggering
Arbitrated Memory
Voltage Measurements
Trigger Correction
VGA
DAC
VGA Driver
Arbitrated Memory

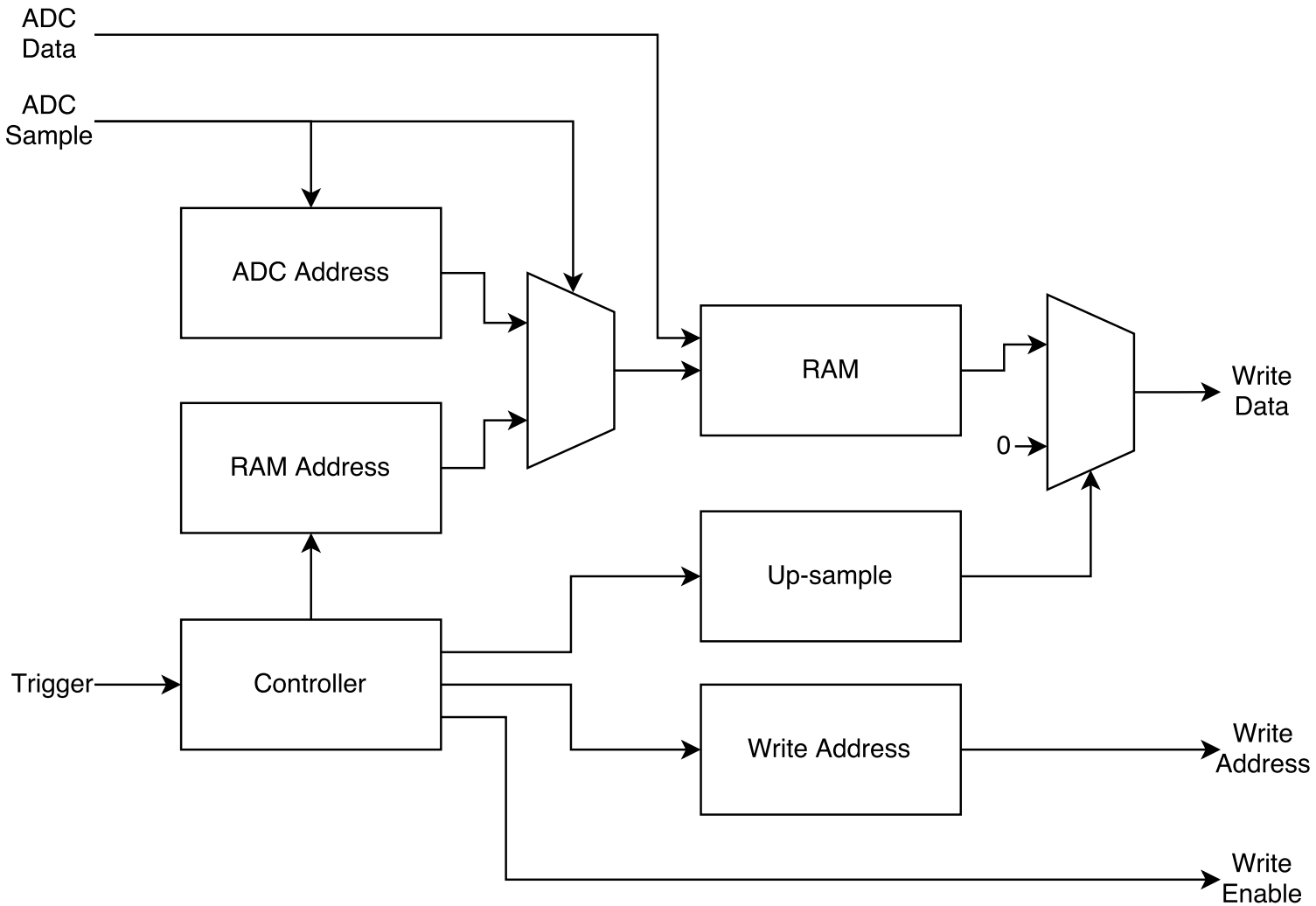
VGA Driver


Settings
BCD Converters
VGA Background ROM
Yellow
RGB
VGA Timing Generator
D
Q
D
Q
Comparator
Arbitrated Memory
VGA Buffer
D
Q

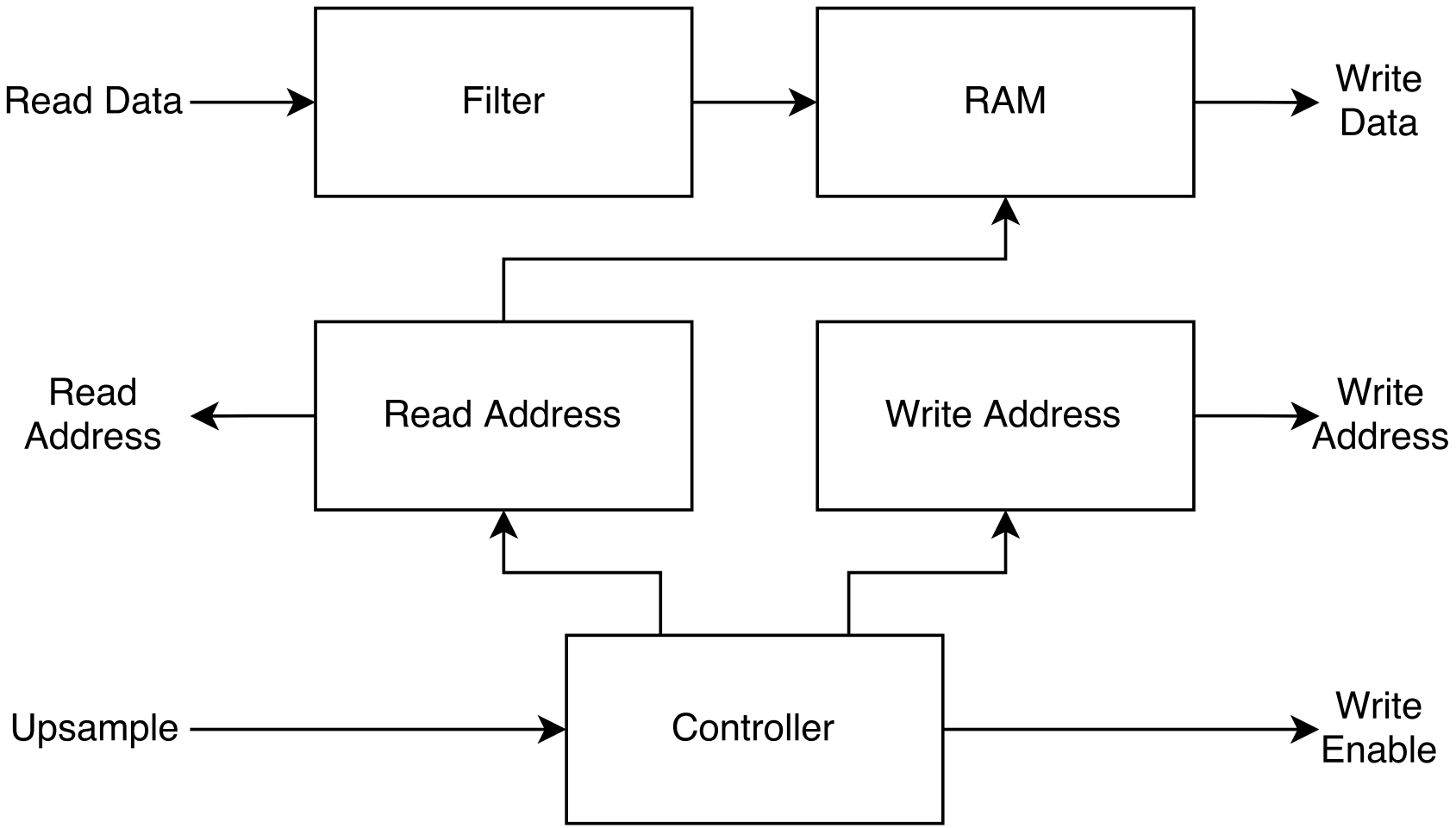
Triggering


Trigger Type
Trigger Reference
ADC Data
Comparator
Trigger
D
Q
Trigger Counter
D
Q
Running Average
Divider
D
Q
Trigger Frequency

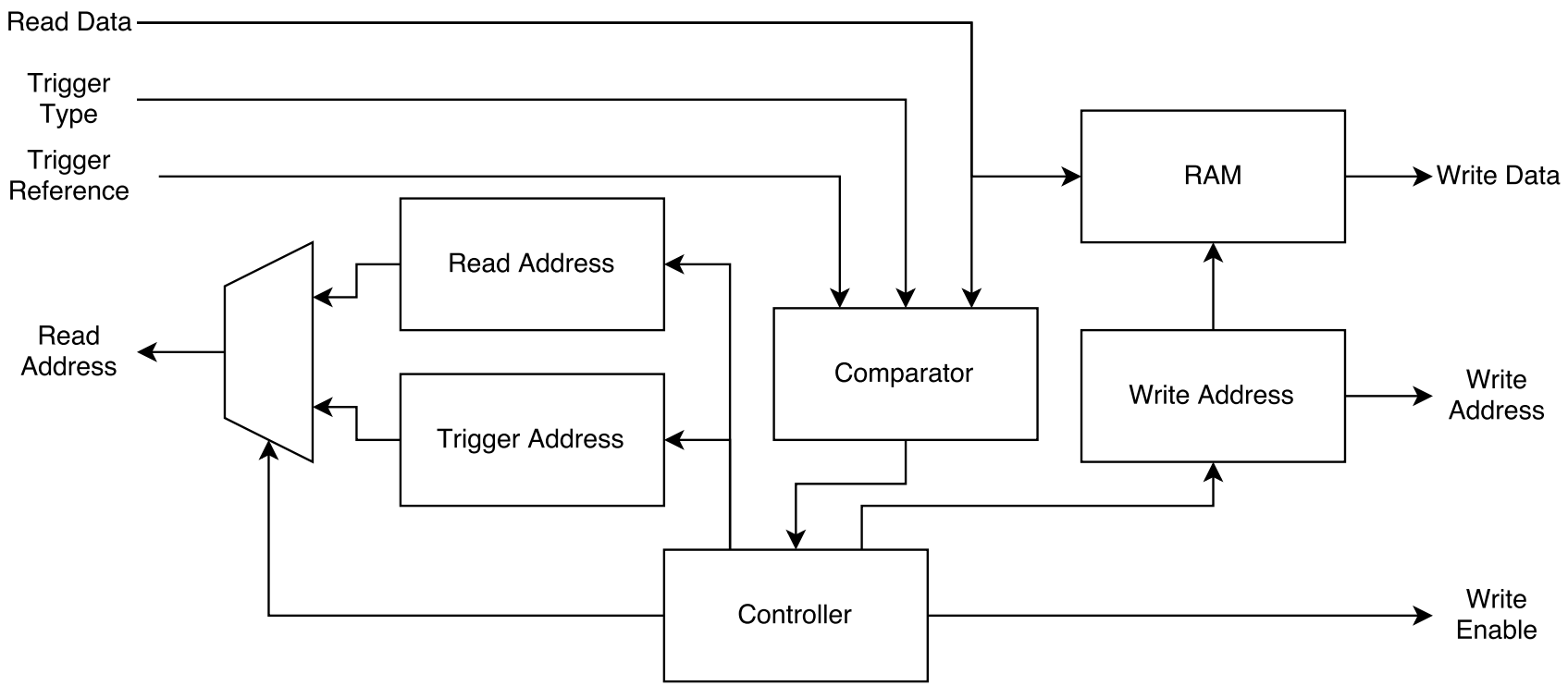
Data Acquisition



Sin(x)/x Interpolation



Trigger Correction



ADC Interface

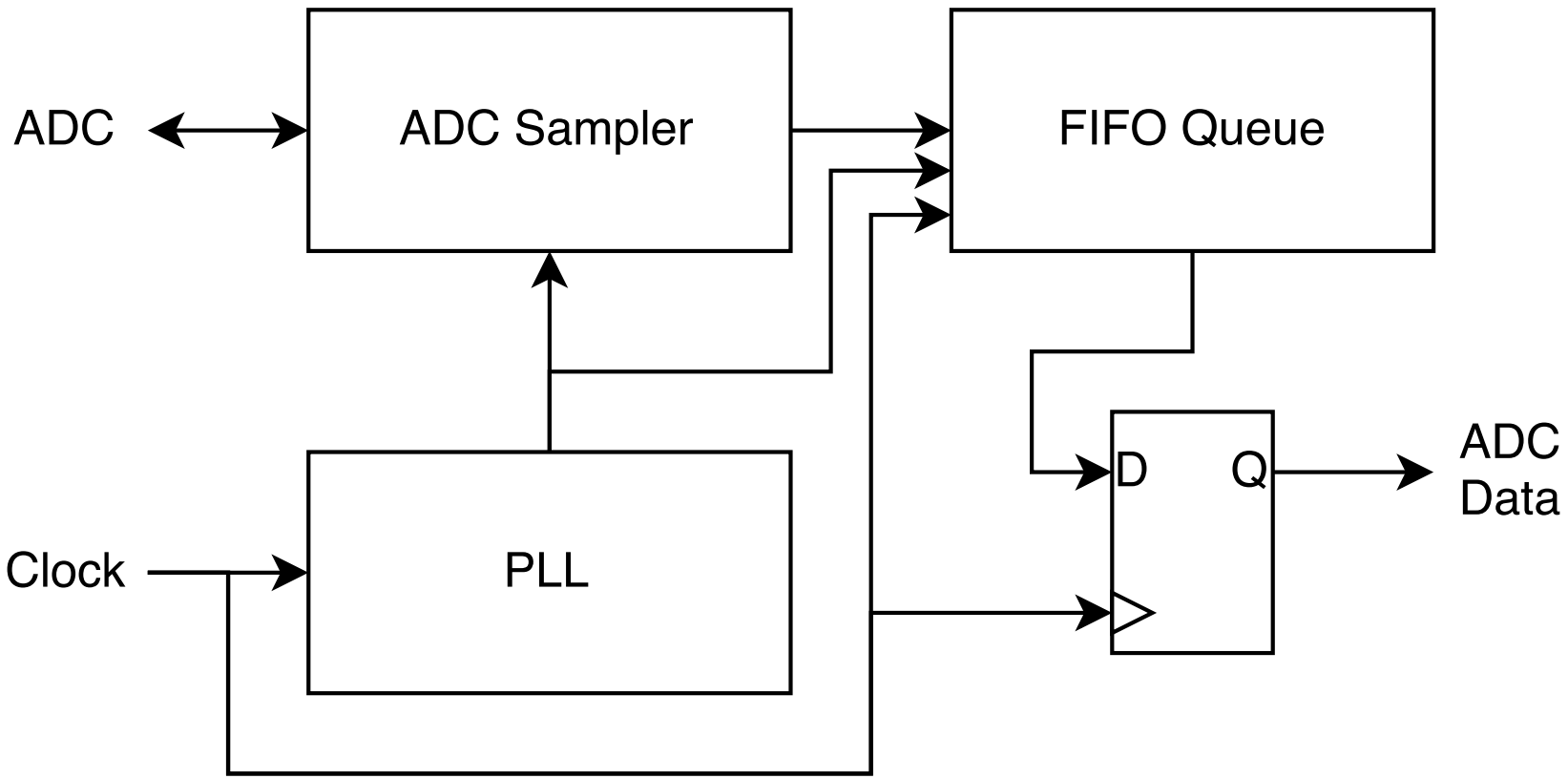
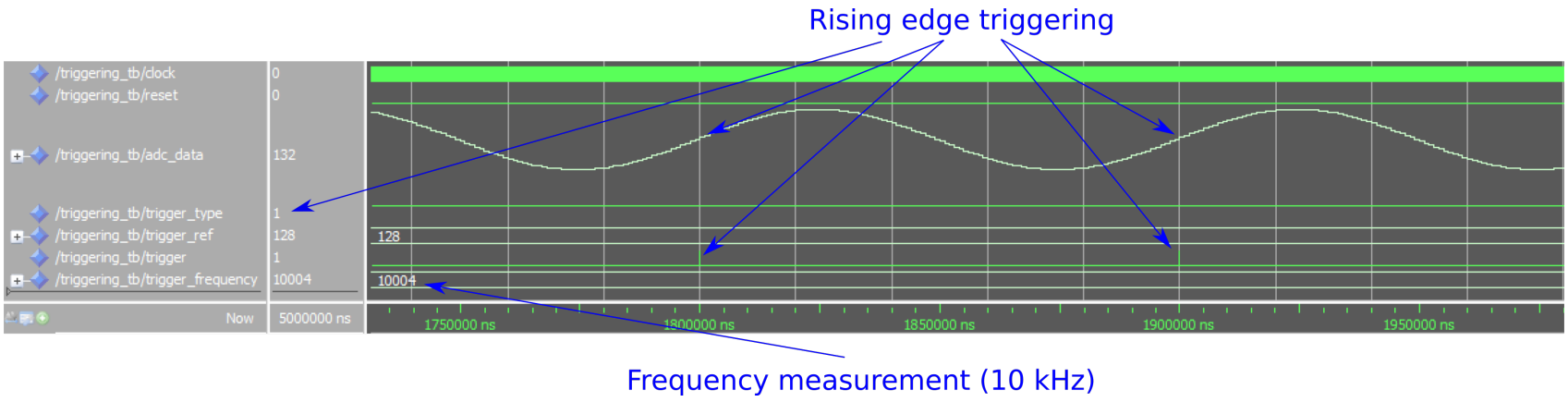
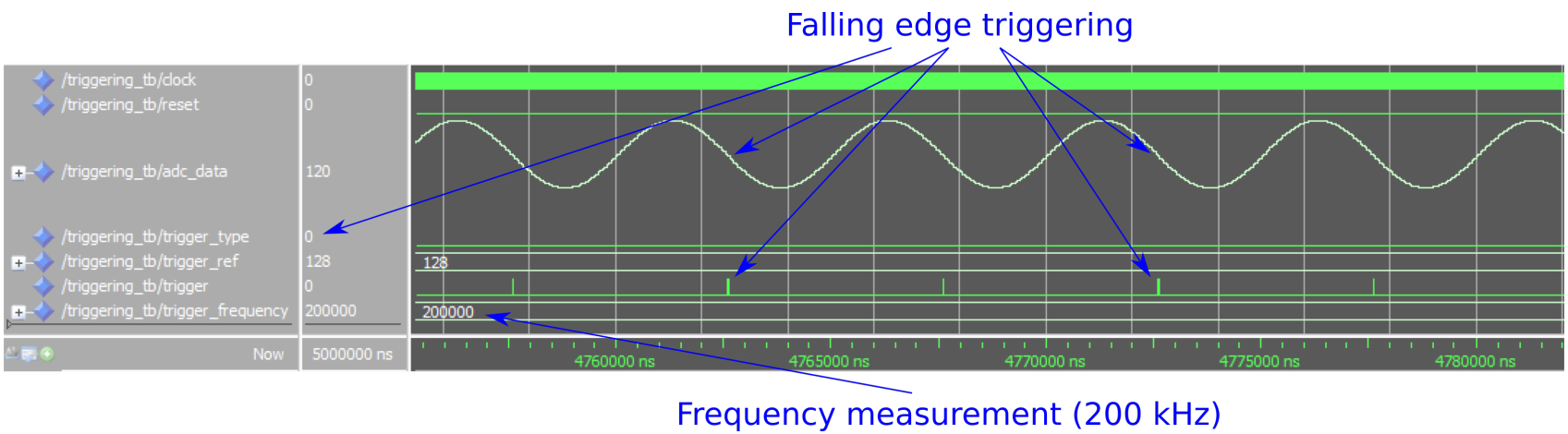


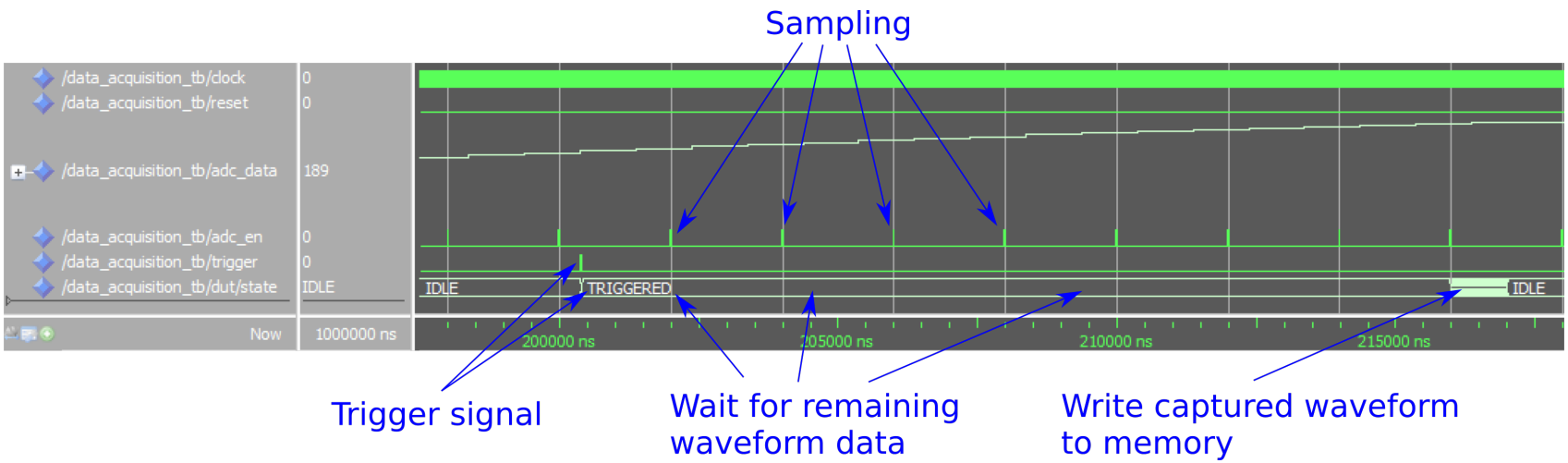
Table of Contents

Triggering

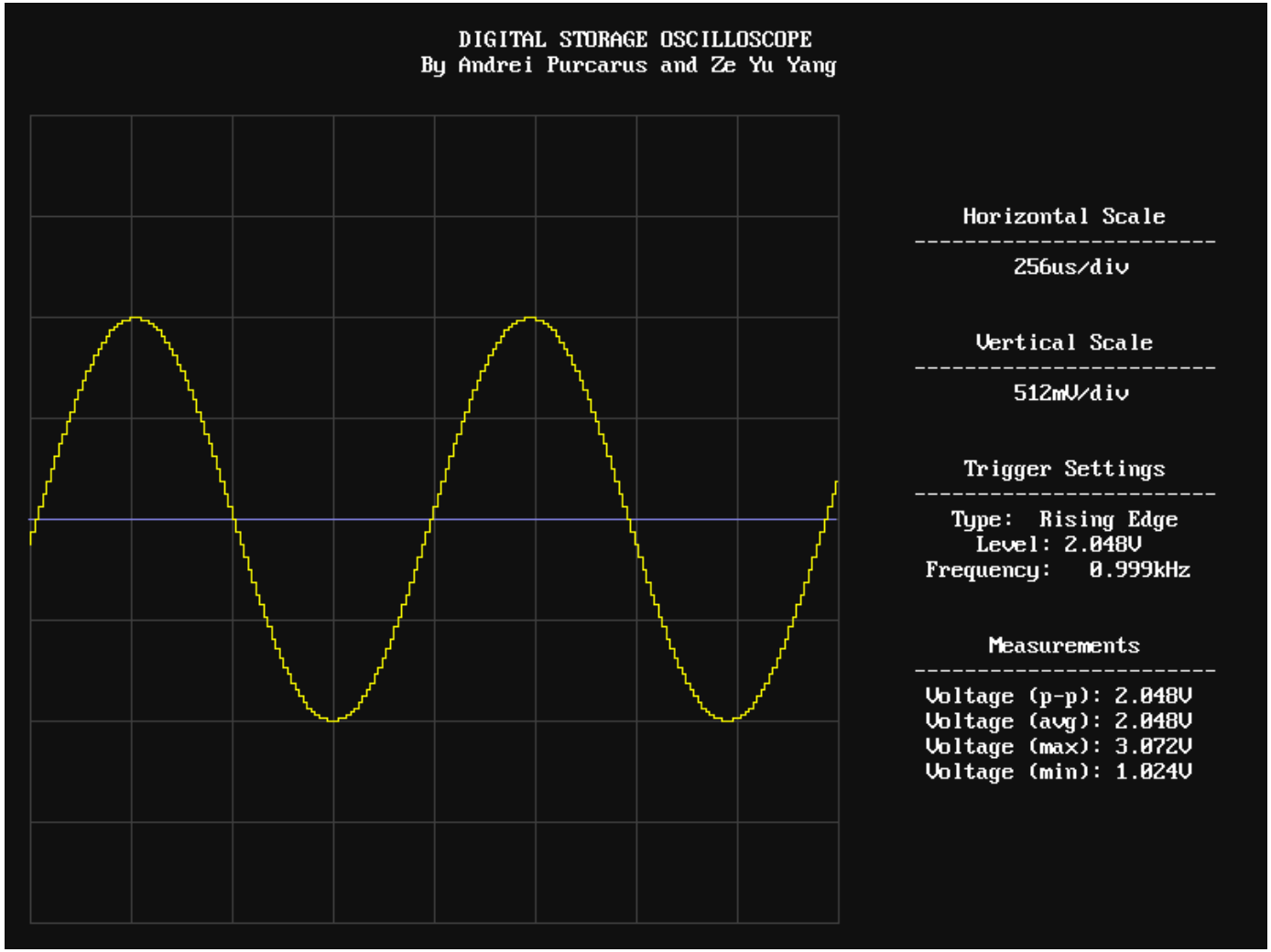

Rising edge triggering
/triggering_tb/clock
/triggering_tb/reset
/triggering_tb/adc_data
/triggering_tb/trigger_type
/triggering_tb/trigger_ref
/triggering_tb/trigger
/triggering_tb/trigger_frequency
0
0
132
1
128
1
10004
128
10004
Now
5000000 ns
1750000 ns
1800000 ns
1850000 ns
1900000 ns
1950000 ns
Frequency measurement (10 kHz)


Falling edge triggering
/triggering_tb/clock
/triggering_tb/reset
/triggering_tb/adc_data
/triggering_tb/trigger_type
/triggering_tb/trigger_ref
/triggering_tb/trigger
/triggering_tb/trigger_frequency
0
0
120
0
128
0
200000
128
200000
Now
5000000 ns
4760000 ns
4765000 ns
4770000 ns
4775000 ns
4780000 ns
Frequency measurement (200 kHz)

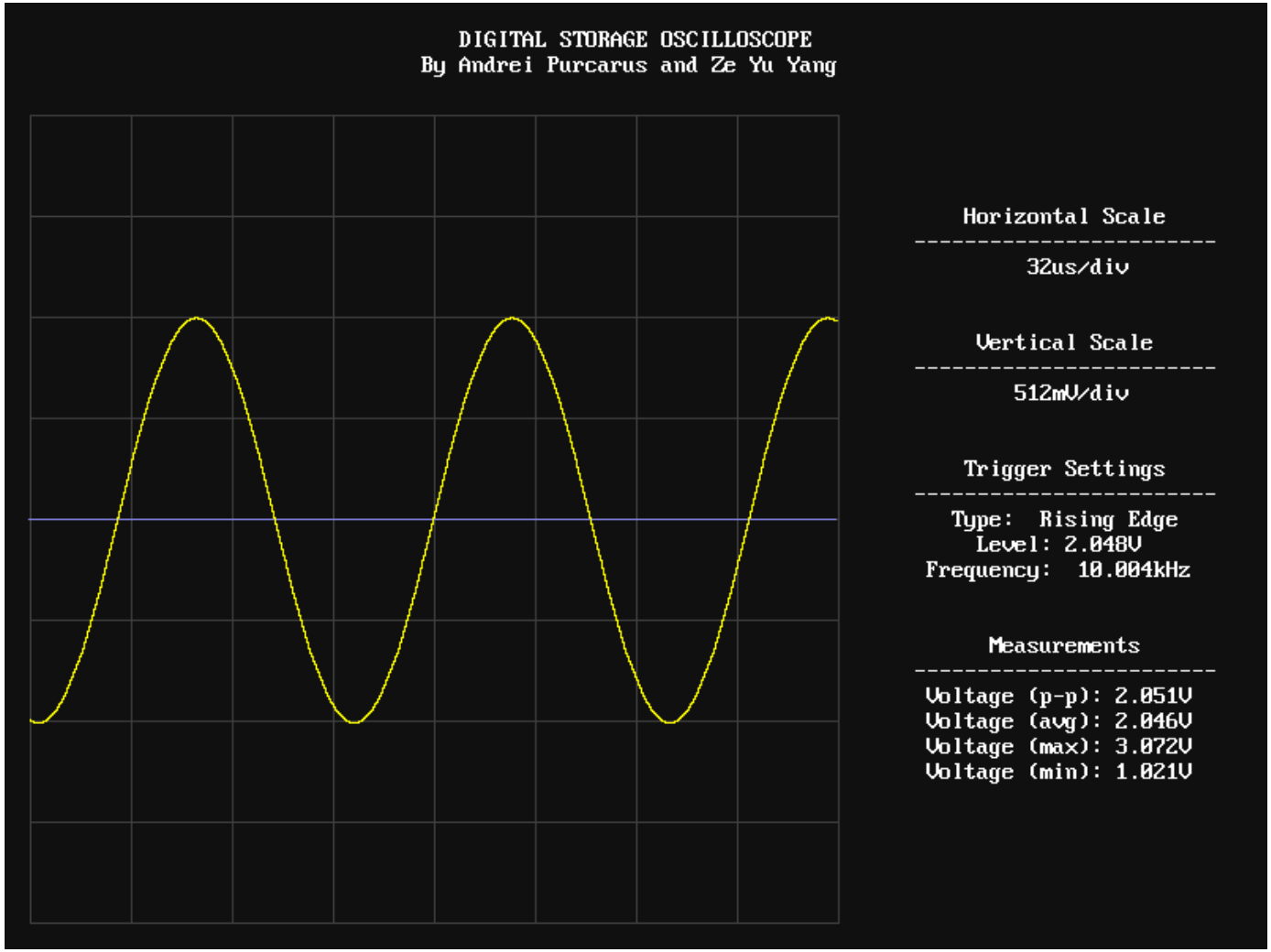
Data Acquisition



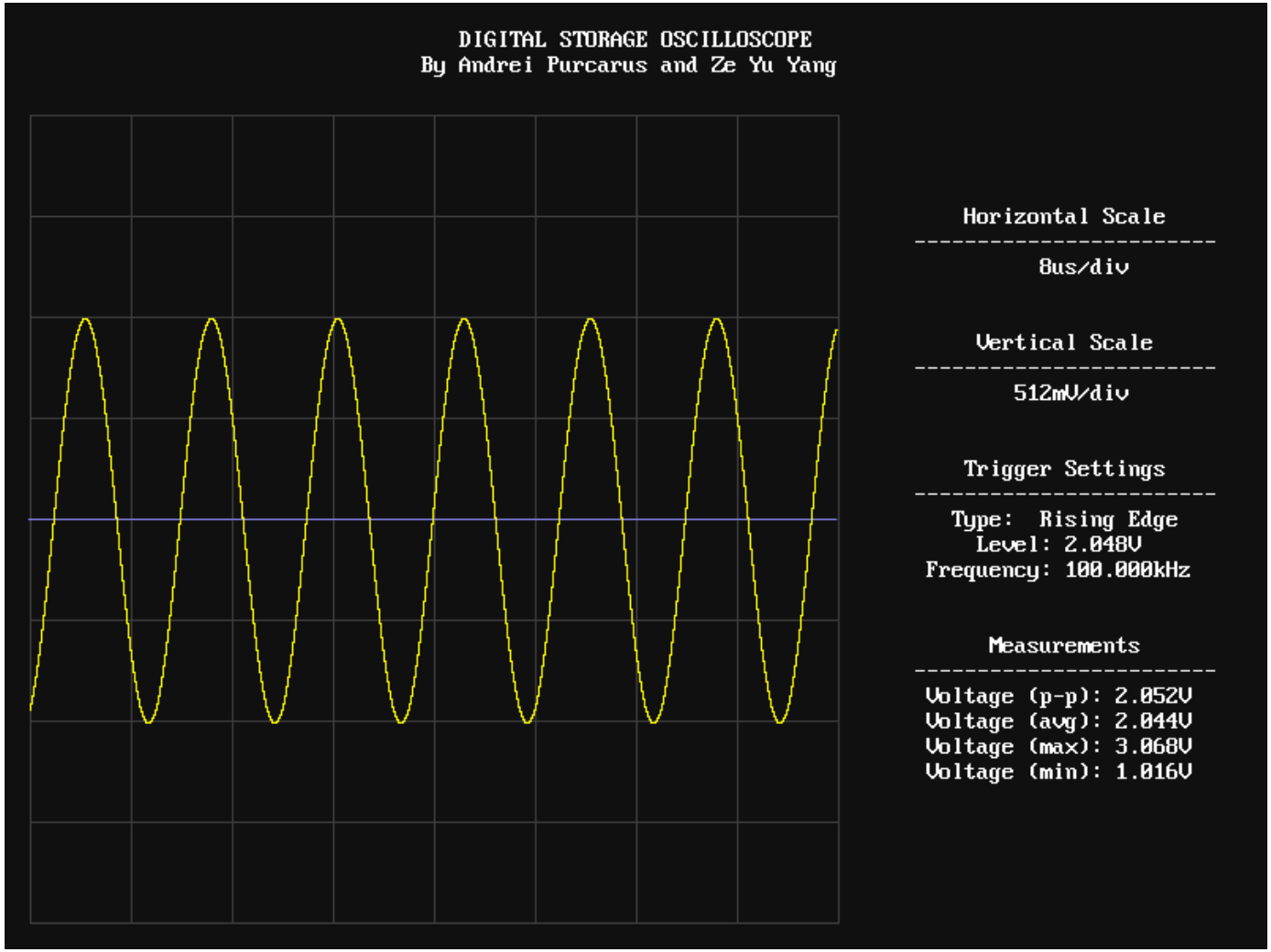
Oscilloscope



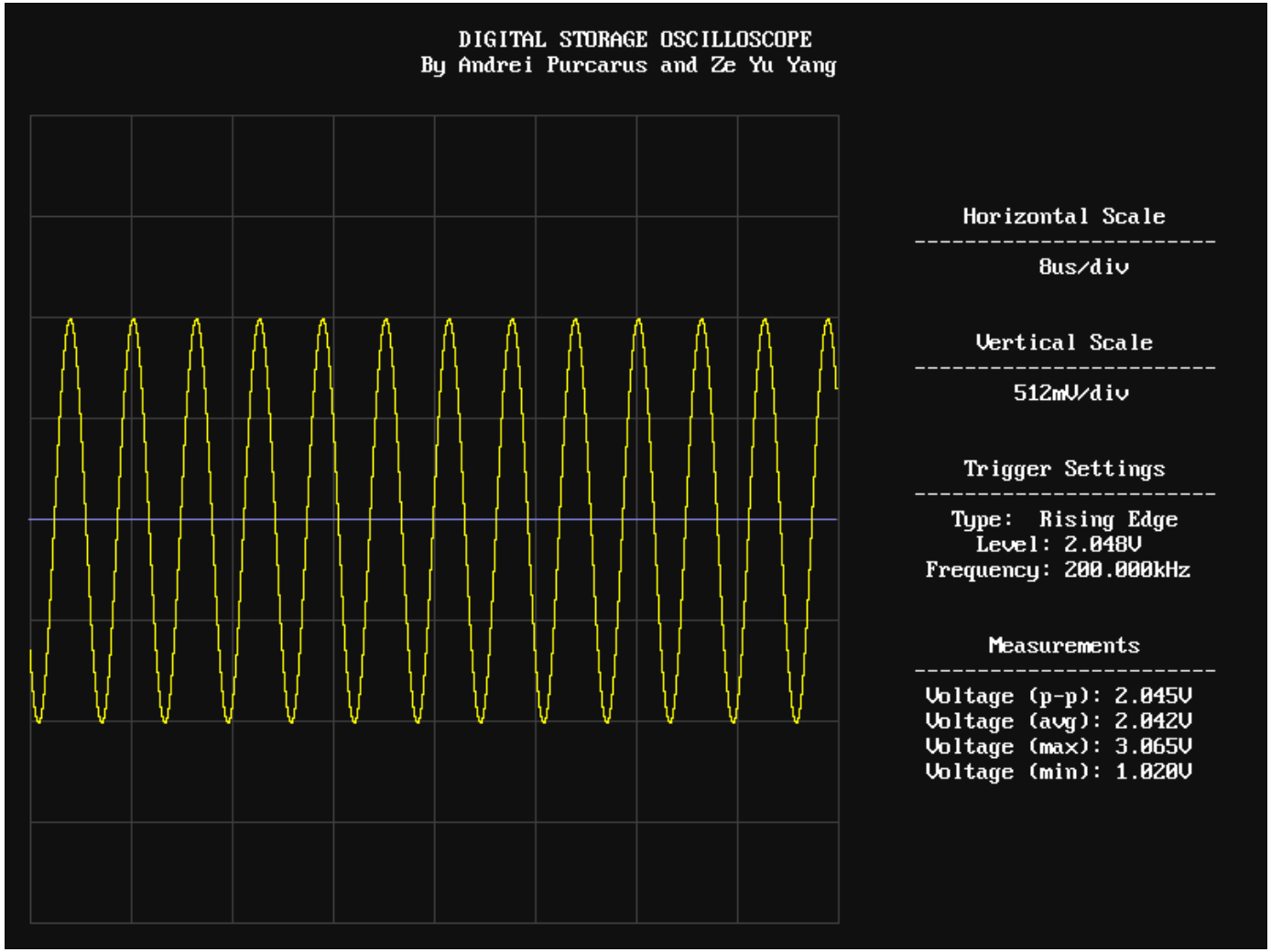
Oscilloscope



Oscilloscope



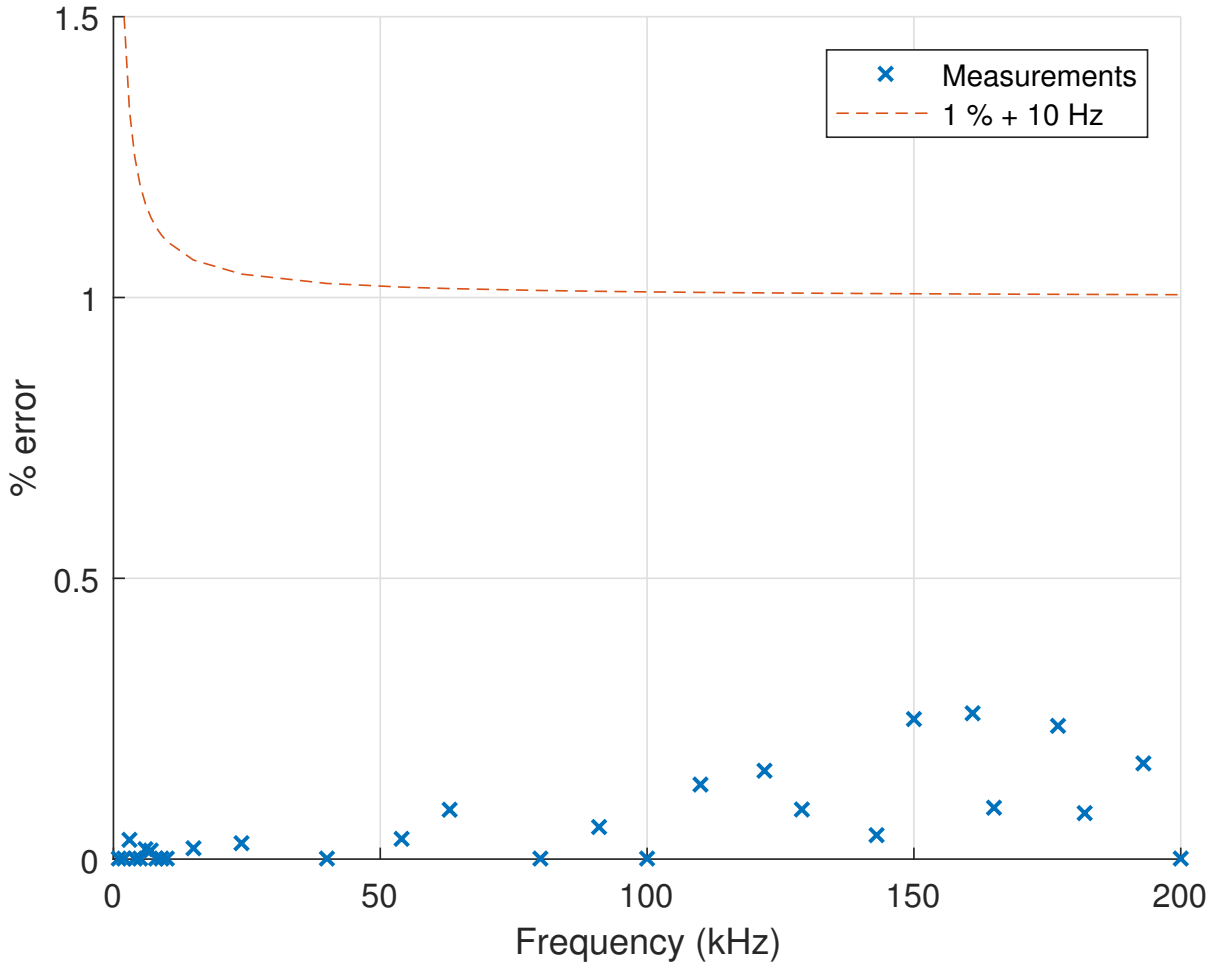
Oscilloscope



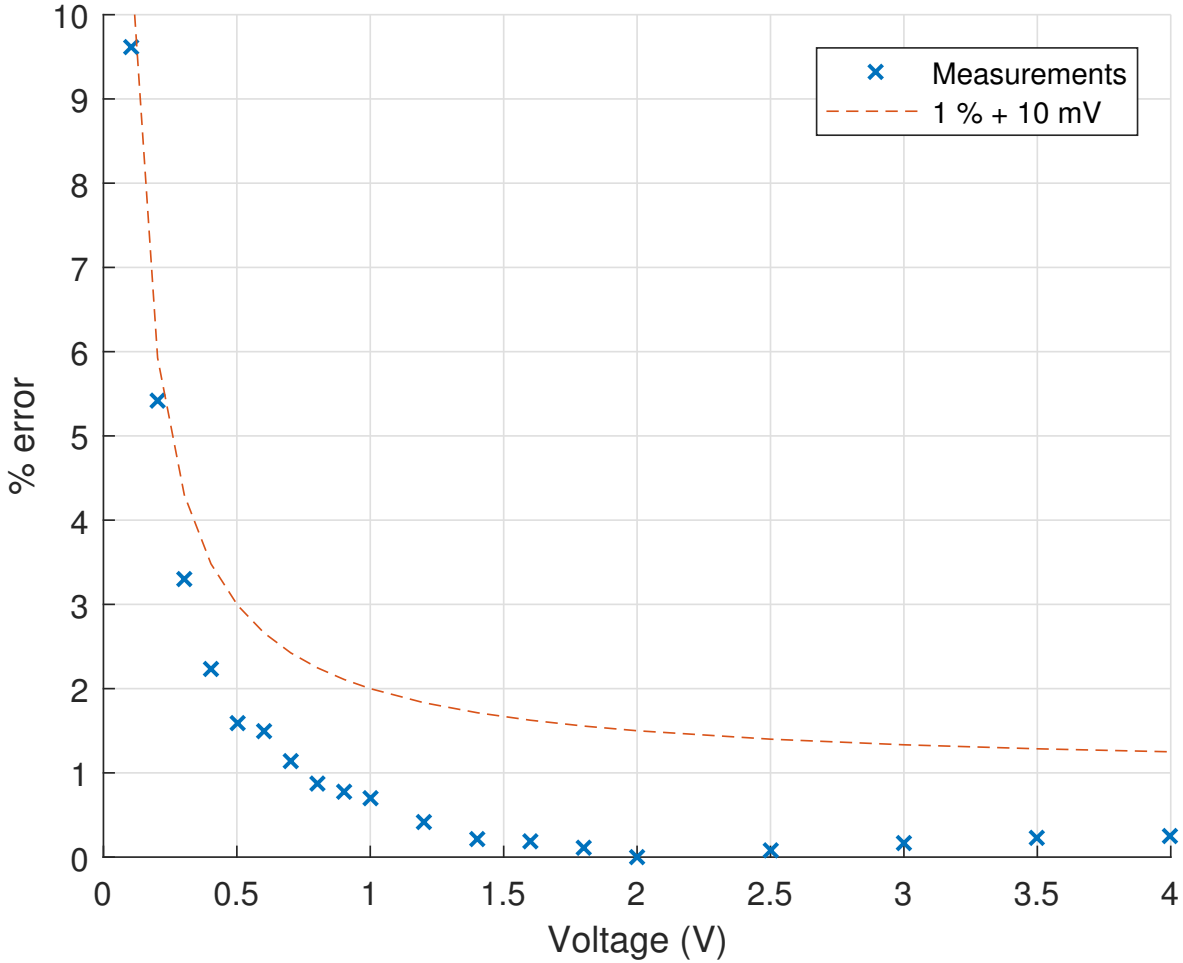
Synthesis

Family	Cyclone V
Device	5CSEMA5F31C6
Logic Utilization	19,901 / 32,070 (62 %)
Total Registers	23770
Total Block Memory Bits	246,832 / 4,065,280 (6 %)
Total DSP Blocks	87 / 87 (100 %)
Fmax	60.26 MHz
Setup Slack	3.405 ns
Hold Slack	0.016 ns

Frequency Measurement Error



Absolute Voltage Measurement Error



Relative Voltage Measurement Error