REPORT

Problem Statement : Design and Functional Simulation of Land rover FIGO FSM

Team Name : Adventurer

Team Size : 1

Team Member: Karthikeyan A

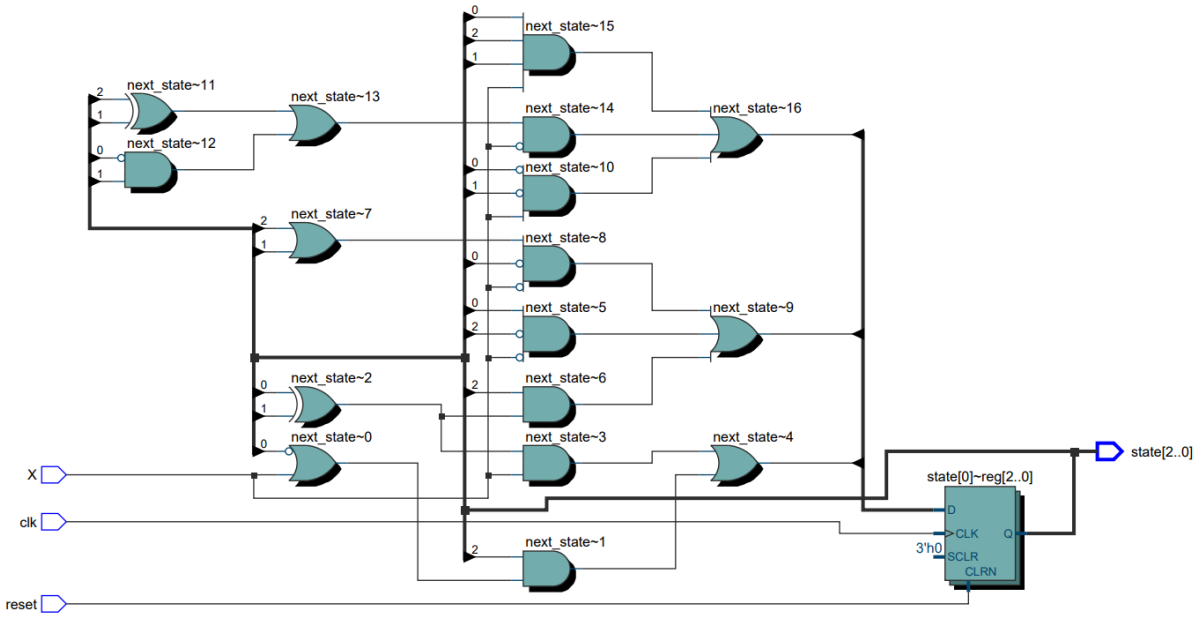
College Name : Sairam Group of Institutions

Topics

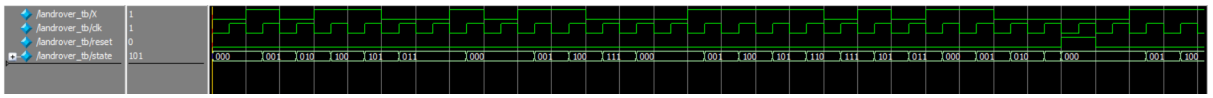
1. Tasks performed .
2. Tests carried out .

1. Tasks Performed

✅ Done Analysis & Elaboration and got a Logic Diagram.



✅Done Simulation.



✅ Done Pin Planning.

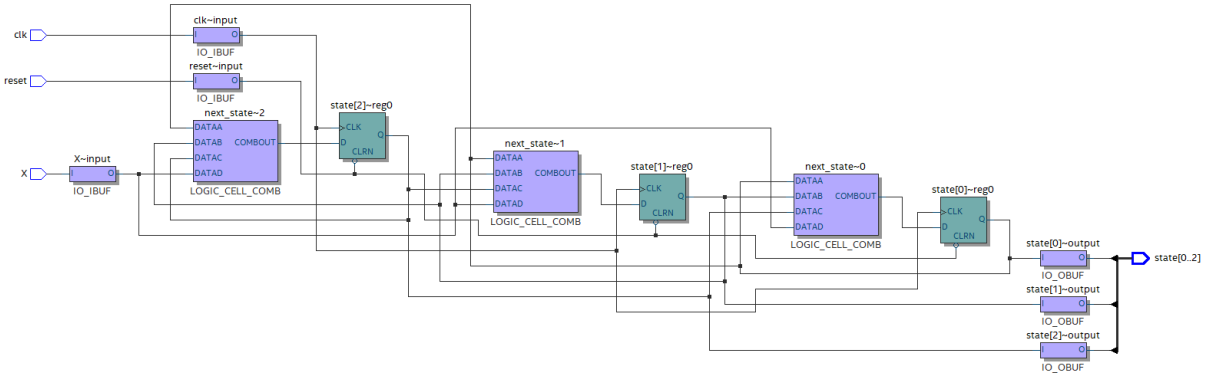
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Locatior	I/O Standard	Reserved	Current Streng	Slew Rate
X	Input	PIN_AB12	3A	B3A_N0	PIN_AK18	3.3-V LVTTL		16mA ...ault)	
clk	Input	PIN_AF14	3B	B3B_N0	PIN_AF14	3.3-V LVTTL		16mA ...ault)	
reset	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	3.3-V LVTTL		16mA ...ault)	
state[2]	Output	PIN_V16	4A	B4A_N0	PIN_V16	3.3-V LVTTL		16mA ...ault)	1 (default)
state[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	3.3-V LVTTL		16mA ...ault)	1 (default)
state[0]	Output	PIN_V17	4A	B4A_N0	PIN_V17	3.3-V LVTTL		16mA ...ault)	1 (default)

✅ Done Analysis & Synthesis.

summary

Analysis & Synthesis Status	Successful - Wed Jul 12 07:24:56 2023
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	landrover
Top-level Entity Name	landrover
Family	Cyclone V
Logic utilization (in ALMs)	N/A
Total registers	3
Total pins	6
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	0
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

✅ Got Post Mapping Diagram.



✅ Done Fitter Placement and Fitter Routing .

summary

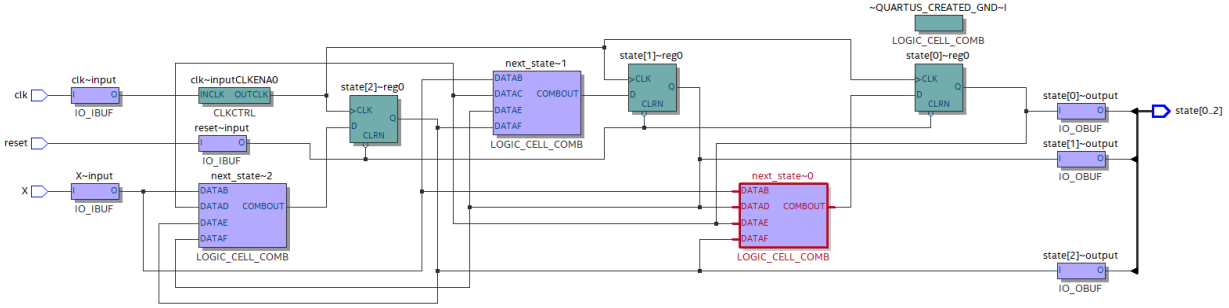
Fitter Status	Successful - Wed Jul 12 08:00:03 2023
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	landrover
Top-level Entity Name	landrover
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	2 / 32,070 (< 1 %)
Total registers	3
Total pins	6 / 457 (1 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total RAM Blocks	0 / 397 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

Resource usage summary

Fitter Resource Usage Summary		
Resource	Usage	%
Logic utilization (ALMs needed / total ALMs on device)	2 / 32,070	< 1 %
ALMs needed [=A-B+C]	2	
[A] ALMs used in final placement [=a+b+c+d]	3 / 32,070	< 1 %
[a] ALMs used for LUT logic and registers	2	
[b] ALMs used for LUT logic	1	
[c] ALMs used for registers	0	
[d] ALMs used for memory (up to half of total ALMs)	0	
[B] Estimate of ALMs recoverable by dense packing	1 / 32,070	< 1 %
[C] Estimate of ALMs unavailable [=a+b+c+d]	0 / 32,070	0 %
[a] Due to location constrained logic	0	
[b] Due to LAB-wide signal conflicts	0	
[c] Due to LAB input limits	0	
[d] Due to virtual I/Os	0	
Difficulty packing design	Low	
Total LABs: partially or completely used	2 / 3,207	< 1 %
-- Logic LABs	2	
-- Memory LABs (up to half of total LABs)	0	
Combinational ALUT usage for logic	4	
-- 7 input functions	0	
-- 6 input functions	0	
-- 5 input functions	0	
-- 4 input functions	3	
-- <=3 input functions	1	
Combinational ALUT usage for route-throughs	0	

Dedicated logic registers	3	
-- By type:		
-- Primary logic registers	3 / 64,140	< 1 %
-- Secondary logic registers	0 / 64,140	0 %
-- By function:		
-- Design implementation registers	3	
-- Routing optimization registers	0	
Virtual pins	0	
I/O pins	6 / 457	1 %
-- Clock pins	1 / 8	13 %
-- Dedicated input pins	0 / 21	0 %
Hard processor system peripheral utilization		
-- Boot from FPGA	0 / 1 (0 %)	
-- Clock resets	0 / 1 (0 %)	
-- Cross trigger	0 / 1 (0 %)	
-- S2F AXI	0 / 1 (0 %)	
-- F2S AXI	0 / 1 (0 %)	
-- AXI Lightweight	0 / 1 (0 %)	
-- SDRAM	0 / 1 (0 %)	
-- Interrupts	0 / 1 (0 %)	
-- JTAG	0 / 1 (0 %)	
-- Loan I/O	0 / 1 (0 %)	
-- MPU event standby	0 / 1 (0 %)	
-- MPU general purpose	0 / 1 (0 %)	
-- STM event	0 / 1 (0 %)	
-- TPIU trace	0 / 1 (0 %)	
-- DMA	0 / 1 (0 %)	
-- CAN	0 / 2 (0 %)	
-- EMAC	0 / 2 (0 %)	

✅ Got Post Fitting Diagram.



✅ Done Power Analysis.

Power Analyzer Status	Successful - Wed Jul 12 08:25:53 2023
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	landrover
Top-level Entity Name	landrover
Family	Cyclone V
Device	5CSEMA5F31C6
Power Models	Final
Total Thermal Power Dissipation	420.13 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	411.23 mW
I/O Thermal Power Dissipation	8.90 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

✅ Generated SOF file using Assembler.

Assembler Status	Successful - Wed Jul 12 08:45:13 2023
Revision Name	landrover
Top-level Entity Name	landrover
Family	Cyclone V
Device	5CSEMA5F31C6

2. Tests Carried Out

For testing using simulation,we have to check for each state what happens if 1 is input and what happens if 0 is input, if both the input makes the corresponding transitions then we can say that the FSM is working fine.

```
X = 0;    // initially x is zero and state is at 000.
clk = 0;
reset = 0;

#10 X = 1;  // state goes to 001 or Room 1
#10 X = 0;  // state goes to 010 or Room 2
```

```
#10 X = 1; // state goes to 100 or Room 4
#10 X = 1; // state goes to 101 or Room 5
#10 X = 0; // state goes to 011 or Room 3
#10 X = 0; // state stays at 011 or Room 3
#10 X = 1; // state goes to 000 or Room 0
#10 X = 0; // state stays at 000 or Room 0
#10 X = 1; // state goes to 001 or Room 1
#10 X = 1; // state goes to 100 or Room 4
#10 X = 0; // state goes to 111 or Room 7
#10 X = 0; // state goes to 000 or Room 0
#10 X = 0; // state stays at 000 or Room 0
#10 X = 1; // state goes to 001 or Room 1
#10 X = 1; // state goes to 100 or Room 4
#10 X = 1; // state goes to 101 or Room 5
#10 X = 1; // state goes to 110 or Room 6
#10 X = 0; // state goes to 111 or Room 7
#10 X = 1; // state goes to 101 or Room 5
#10 X = 0; // state goes to 011 or Room 3
#10 X = 1; // state goes to 000 or Room 0
#10 X = 1; // state goes to 001 or Room 1
#10 X = 0; // state goes to 010 or Room 2
#10 X = 0; // state goes to 011 or Room 3
#10 reset = 1; // state goes to 000 or Room 0
#10 reset = 0; // state stays at 000 or Room 0
#10 X = 1; // state goes to 001 or Room 1
#10 X = 1; // state goes to 100 or Room 4
#10 X = 1; // state goes to 101 or Room 5
```

Challenges still facing:

- Can’t generate state machine diagram .
  (suspecting my design and feels like i have to do with if else or switch case to decide state transitions)
- Can’t see output in labsland board .
  (didn’t know why i can’t see output, i tried changing many pins still i couldn’t figure out where is the problem)