**Laboratoire d'Architecture des Processeurs**
IN-F Ecublens
CH-1015 Lausanne
http://lap.epfl.ch

**Semester or Diploma Project**
Summer 2016

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

# Pyramic array
# An FPGA based platform for many-channel audio acquisition

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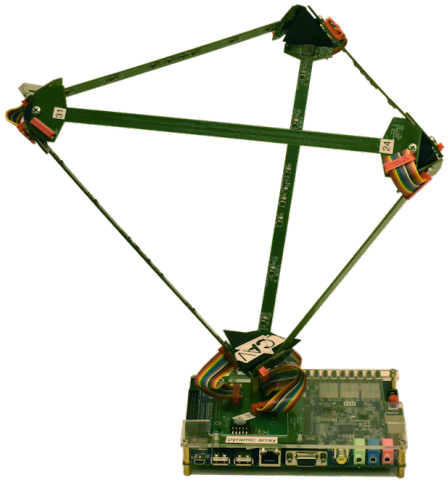
## Introduction



Localizing and separating sound sources are crucial preprocessing step for many speech recognition applications.

This work presents the design, test and operation of the Pyramic array, a 48-channels microphone array for real-time audio processing applications. The proposed design is based on a new generation of digital micro electromechanical (MEMS) microphones which are distributed on the edges of a tetrahedron. The Pyramic array interfaces with an Altera's Cyclone V device that features an field-programmable gate array (FPGA) and a Hard Processor System (HPS) in the same die.

## Goals

The aim of the project is to build and design a novel 48 microphones modular array architecture called Pyramic. The system should send the multi-channel audio samples through a parallel SPI master to a host Altera's Cyclone V device, which combines a Field Programmable Gate Array (FPGA) and an ARM-9 Hardcore Processor (HPS). The data should be processed in real-time by a cascade of FIR filters hardware accelerators, implementing a delay-and-sum beamformer. The ARM-9 processor should run on a Linux based OS and controls the acquisition. Moreover, the system should be accessible by Ethernet connection. Finally, Direction of Arrival (DoA) algorithms willl be tested offline in order to evaluate the reliability of the acquired audio data.

## Summary

The Pyramic array is a 48 microphone channels modular array suitable to perform echo-localization, beamforming and source separation algorithms. It is a modular system composed of six linear microphone arrays of eight microphones each arranged as a tetrahedron. The idea was originated at LCAV and the hardware was designed at LAP in EPFL. This project presents the design of an SPI interface with an FPGA host from Altera's Cyclone V device. The data is sent from six daisy-ADCs which are daisy-chained by pairs, each of the ADCs sends synchronous data from eight microphone channels sampled at 48 kHz and 16 bits.

A Hard Processor System (HPS) featuring an ARM-9 processor configures, controls and receives the samples from the FPGA part. The samples are stored in a DDR3 memory, a microSD card and sent to a host computer through scp communication. The system runs on a Linux operating system. This work introduces the implementation and design of all the communication between the different system blocks, as some offline results of Direction of Arrival algorithms tested at LCAV.

## Future work

The next students should benchmark the performance of the Pyramic array by conducting further tests of the correct behaviour of the array. A first approach would be to run advanced software applications in the device and compare their performance with the ones in a conventional CPU. Then, after identifiying which software parts add the biggest overhead, hardware accelerators can be implemented after identifying which part of the software code are slower. A comparison between hardware resources and processing speed could be interesting as well. Finally, more measurements with the Pyramic array to process the data with offline algorithms might help to understand better the Pyramic array behaviour.

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*And what about next research on this project…*

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