Laboratoire d'Architecture des Processeurs
IN-F Ecublens
CH-1015 Lausanne
http://lap.epfl.ch

Semester or Diploma Project
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ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Extension board for CycloneV
Multi microphone acquisition - Signal Analysis
Extending the Pyramic Array

Corentin Ferry

Optional Semester Project

Description of the project

This project is common between LAP and LCAV.

The Pyramic architecture is a flexible 48-microphone array mounted on a powerful FPGA-SoC system. It allows to do massively multi-channel audio processing in real-time. Currently, the acquisition and transfer to shared memory with the ARM CPU is operational.

We would like to extend the system to allow simultaneous recording and playback, either in real-time where the input is processed, either in the FPGA or the ARM processor, and sent to the output CODEC, or recording a sound played through the output CODEC.

Two possible paths can be followed. One is to implement a beamforming (filter-and-sum) architecture with reconfigurable weights in the FPGA. This would allow to have very easy control of the timings for the processing. The second path is to do the processing in the CPU and rely on hardware accelerator in the FPGA to speed up the processing. These accelerators could be ad-hoc for the algorithms, or some basic block such as matrix-matrix multiplication, Gaussian elimination and FFT.

Goals

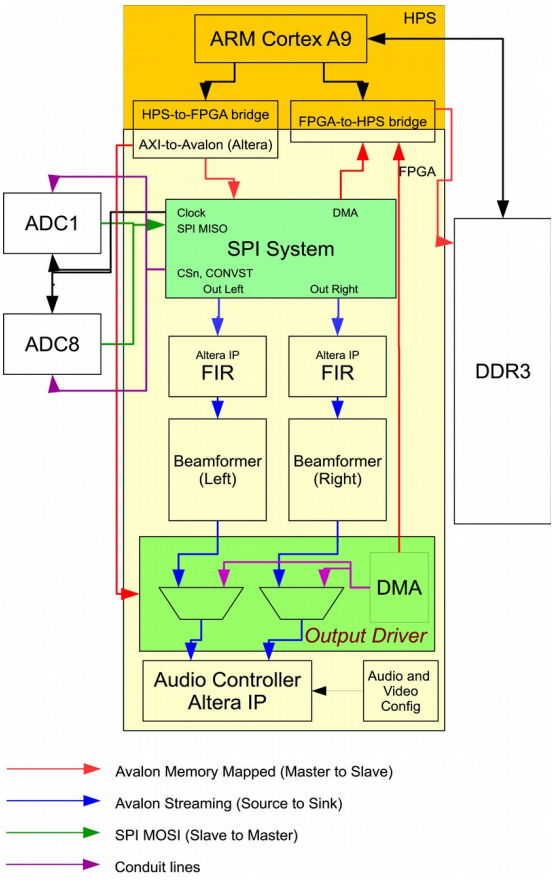
The final goal is to implement either direction of arrival, or beamforming algorithm and demonstrate it in a live real-time experiment.

The current design doesn't allow outputting sound either through the beamformer, which is not completely implemented, and doesn't permit the ARM system (Hardware Processor System, HPS) to output sound. On the hardware side, the goal of the project is to implement such an output. Also, we should complete the beamformer so that both paths described in the project description can be taken.

On the software side, the project should yield a library that permits access to the Pyramic array without Quartus.

Summary

We modified the design from the original Pyramic array to allow a regular capture with an exact sampling frequency of 48000 Hz. Moreover, we implemented fully the second path, that allows audio data to go through the HPS and then into the audio controller accessible via the FPGA. We also created a library that interfaces the HPS and FPGA systems, and allows controlling the Pyramic array.



The block schematic figure gives shows the modified or added parts in the FPGA design.