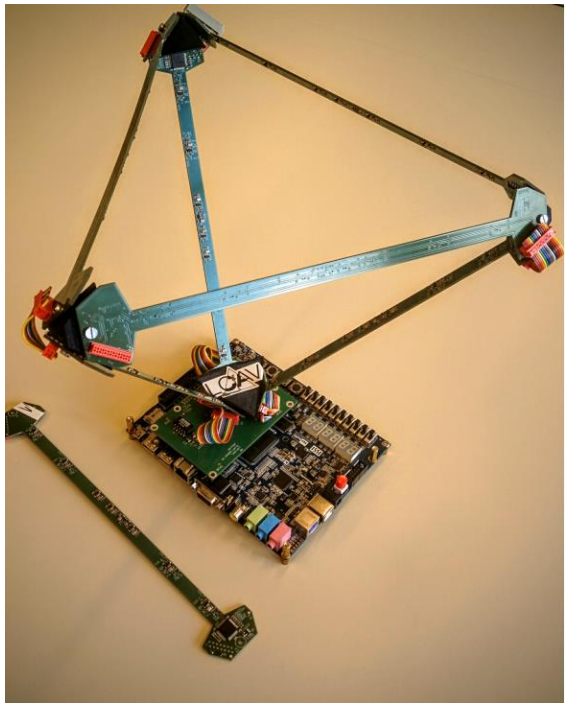
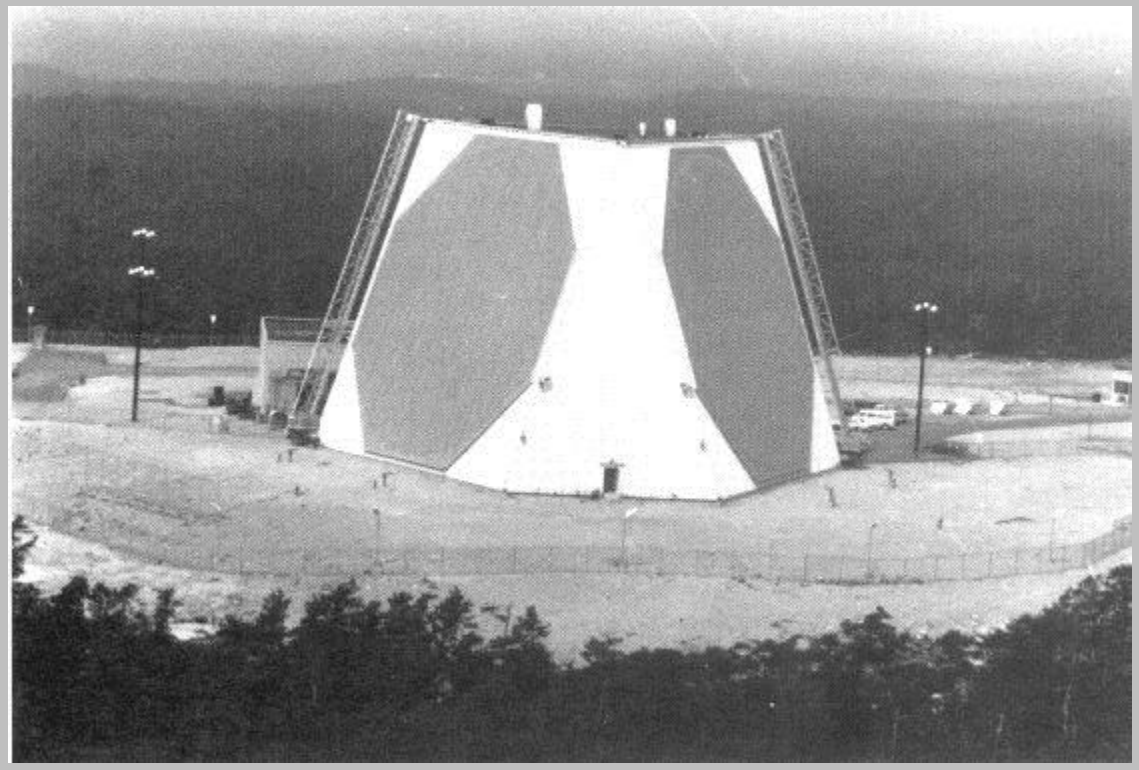
Pyramic array
An FPGA based platform for many-channel audio acquisition

Juan Azcarreta Ortiz



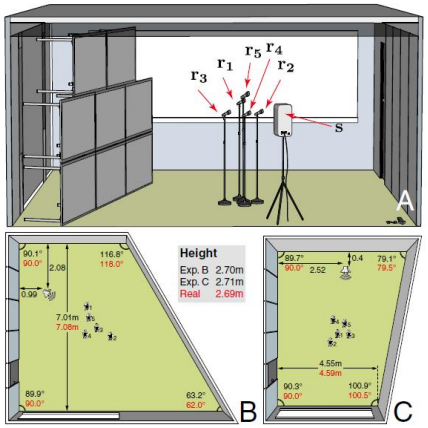
Supervised by
René Beuchat (LAP)
Robin Scheibler (LCAV)
Ramón Bragos (UPC)

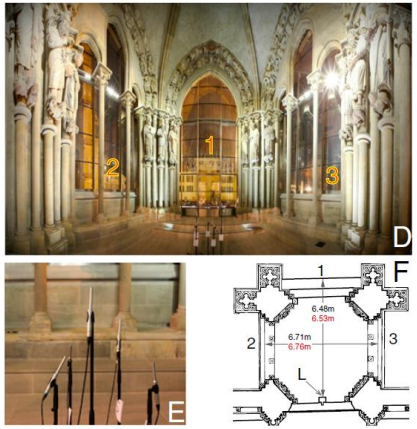
AN/FPS-115 PAVE PAWS radars

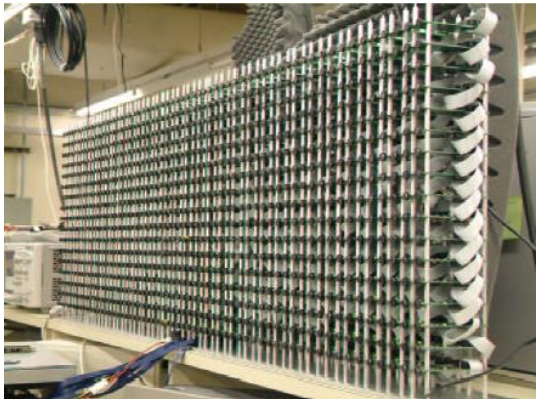


Microphone arrays

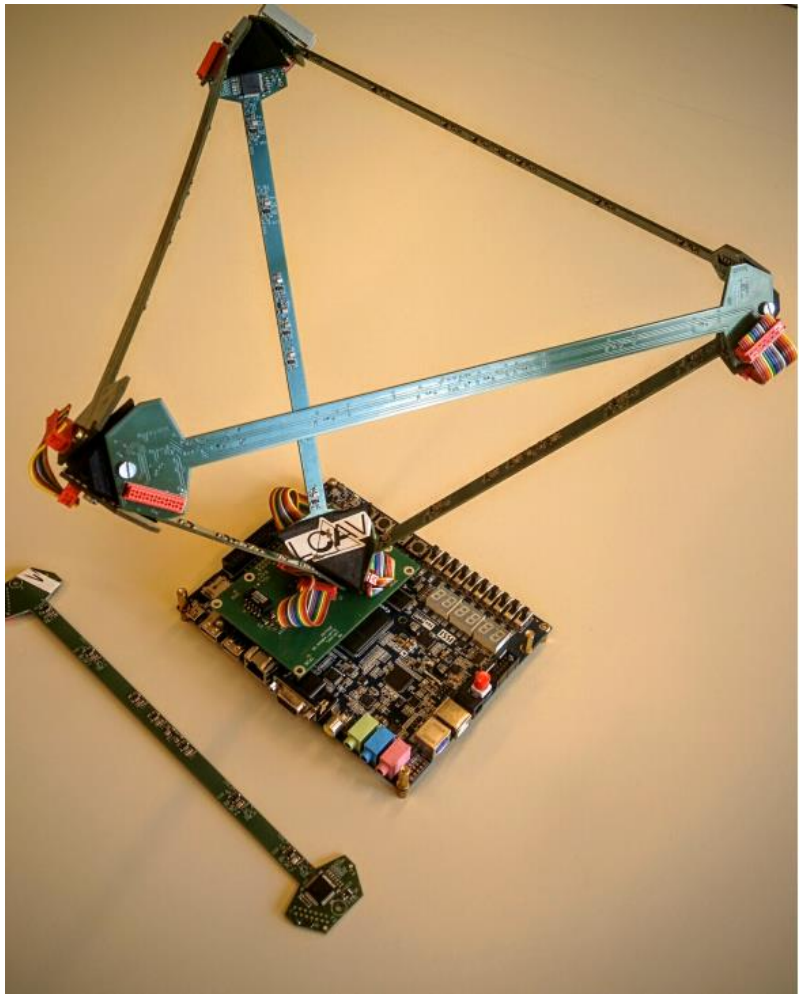
Alfred M. Mayer		MIT
2 microphones	Beamformer, indoor-localization, source separation..	1024 microphones

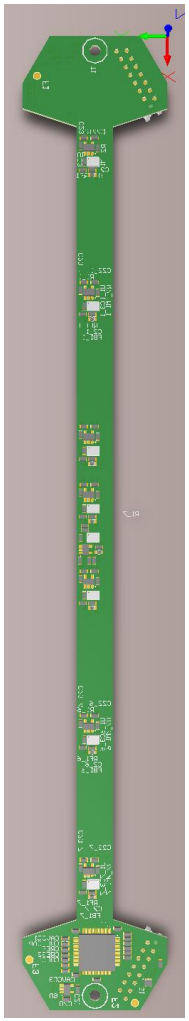




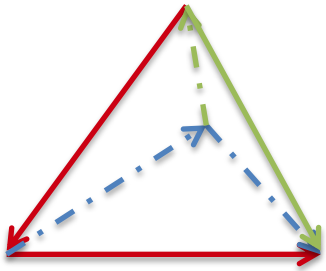


Pyramic array

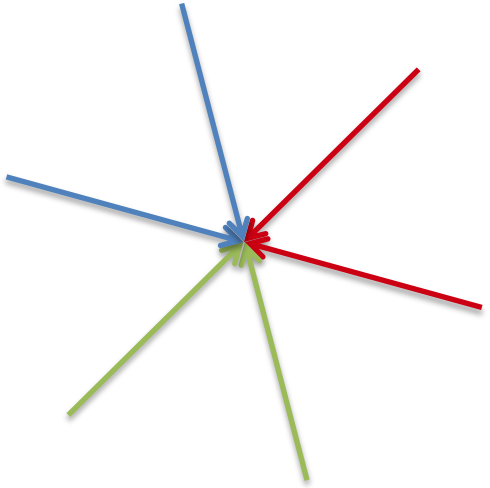




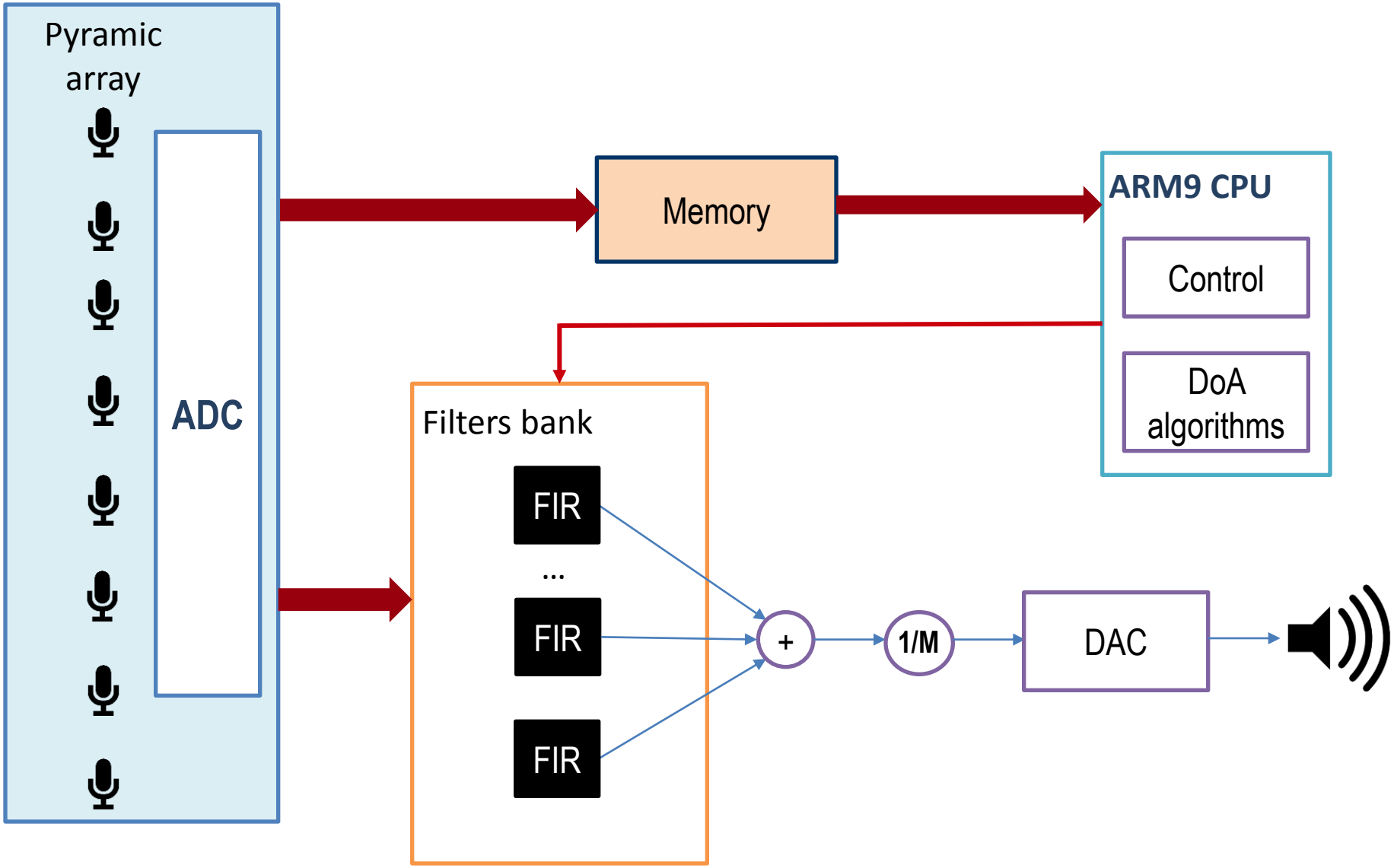
Tetrahedron configuration



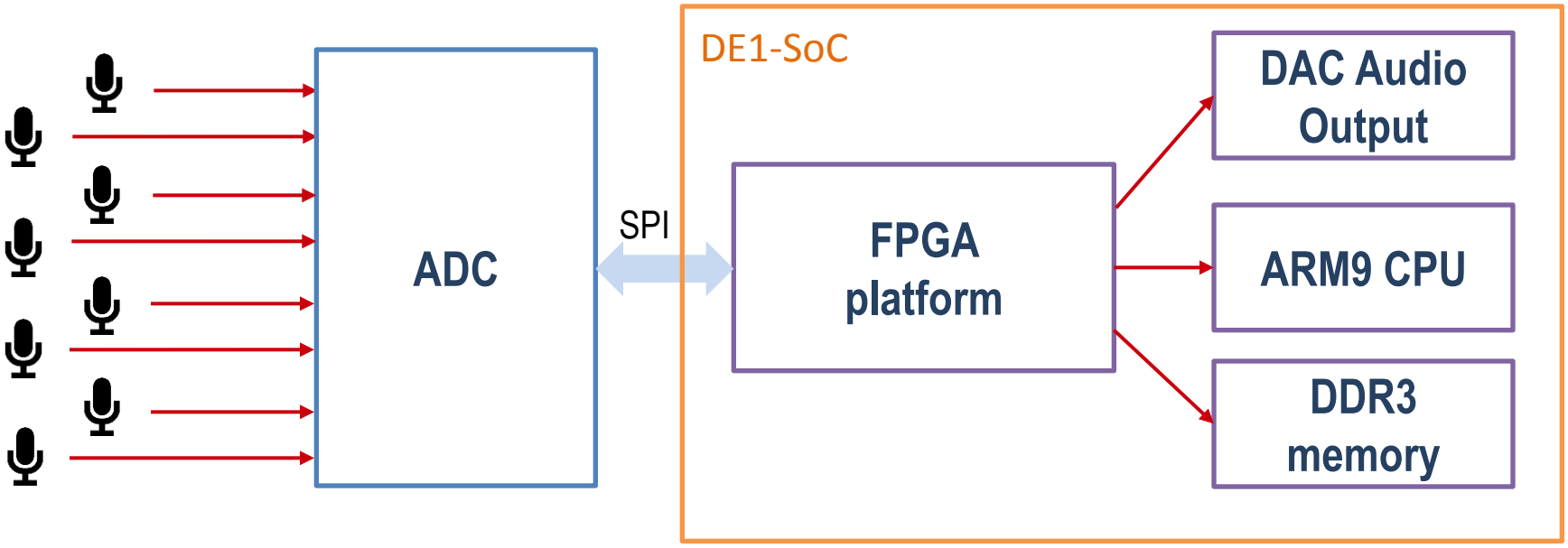
Star configuration

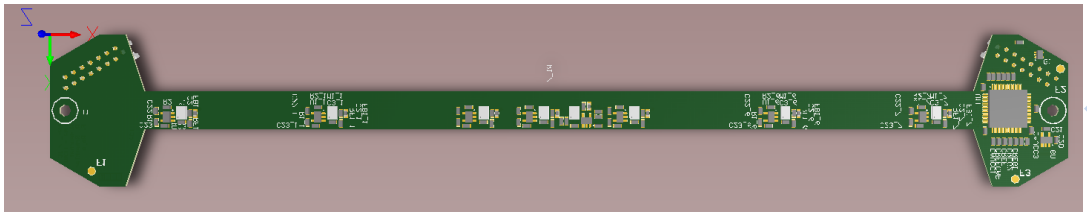


Objectives

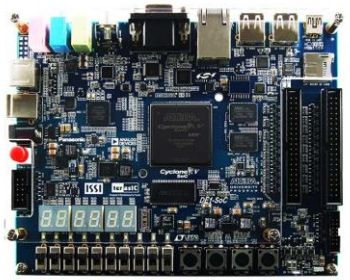

Pyramic array
ADC
Memory
ARM9 CPU
Control
DoA algorithms
Filters bank
FIR
...
FIR
FIR
+
1/M
DAC

Objectives: implementation

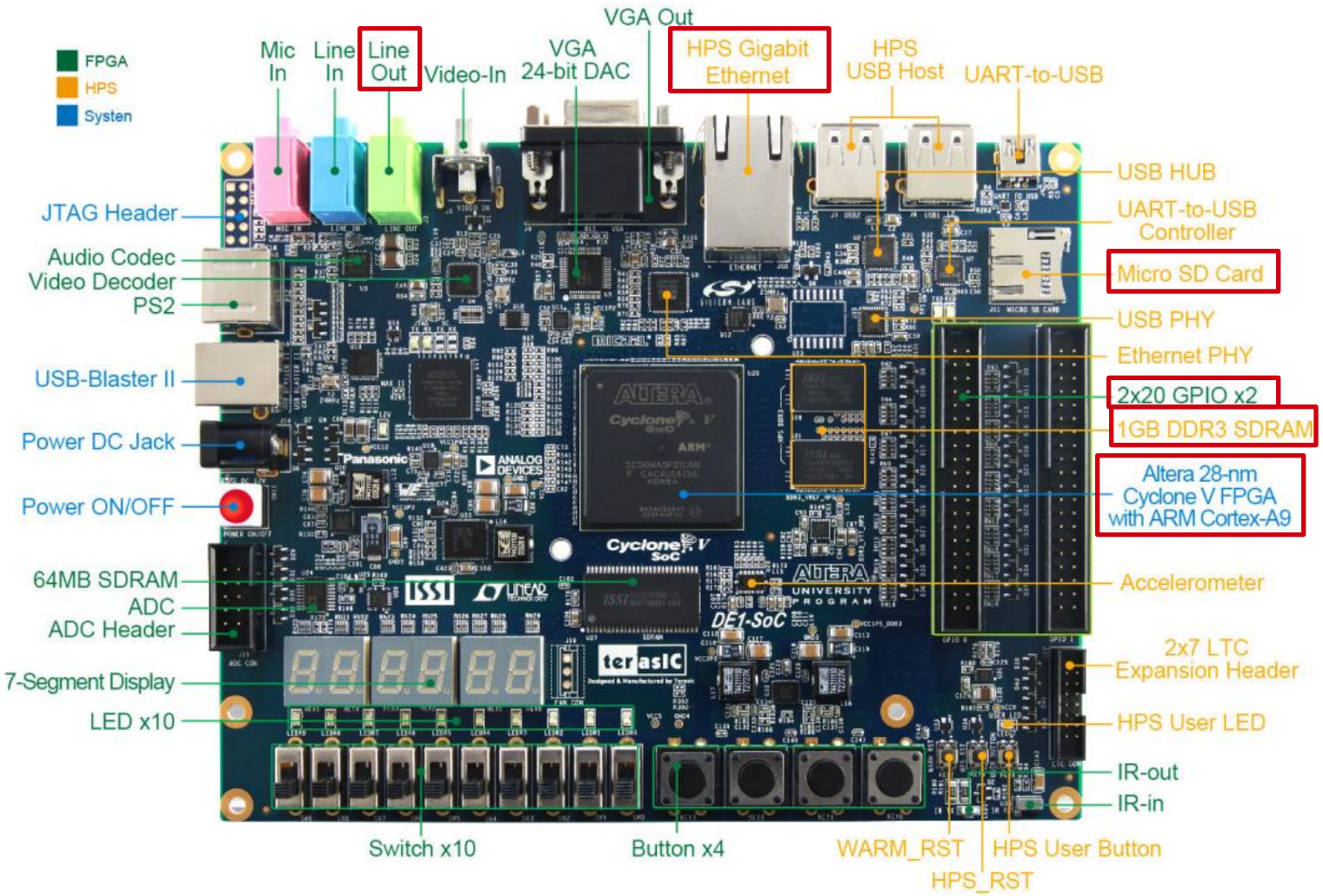




SPI



Terasic DE1-SoC

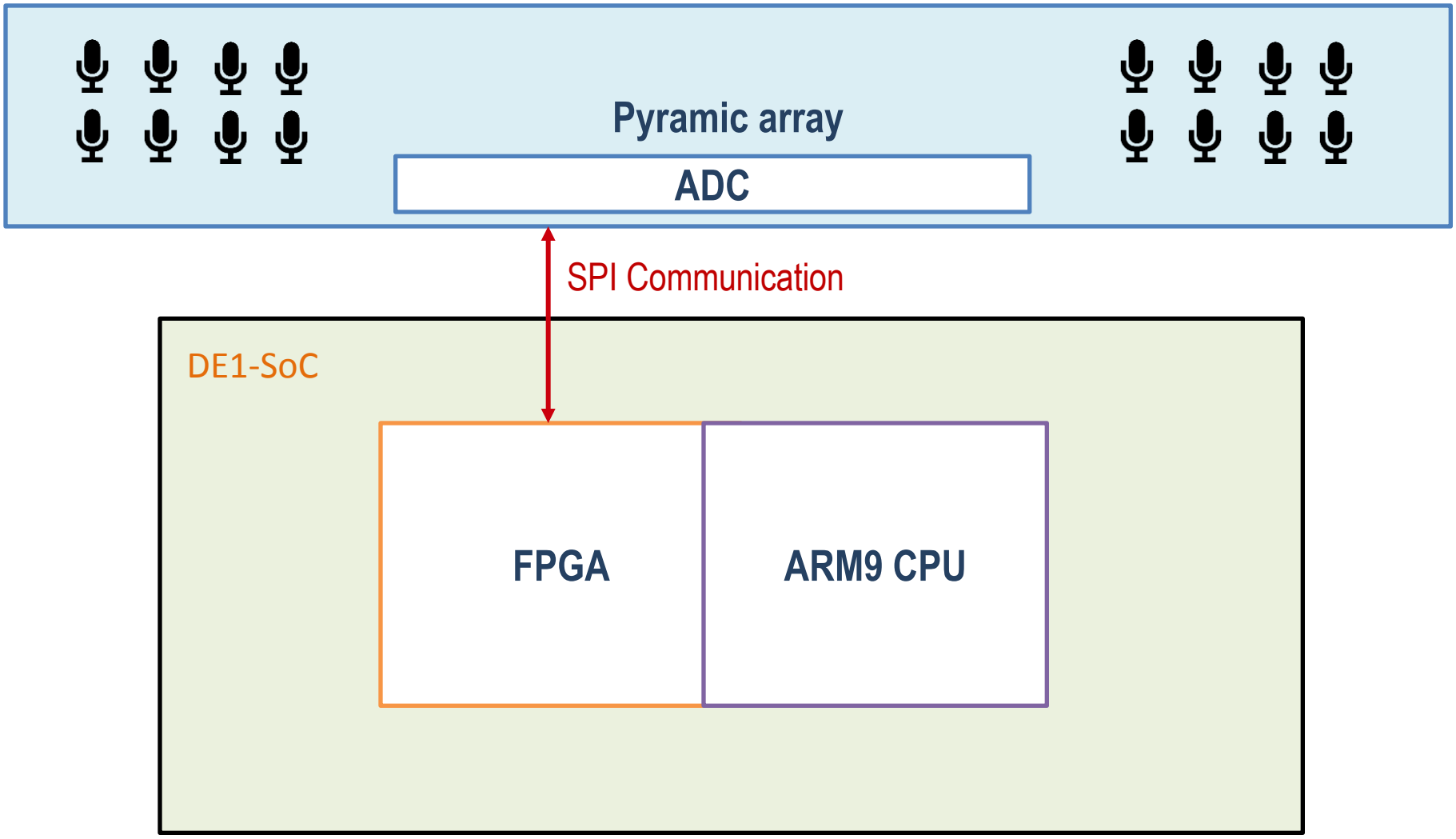


Objectives

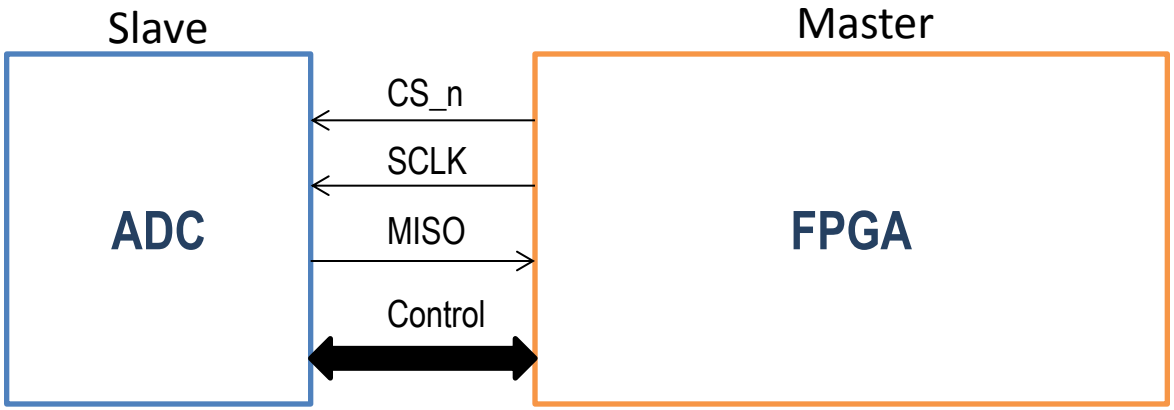
Outline

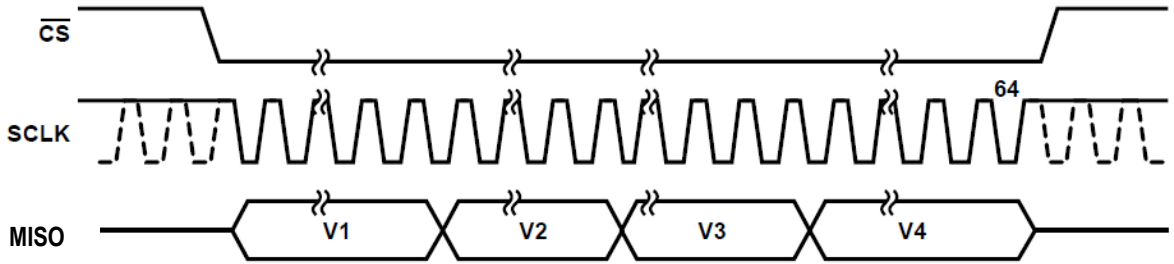
1. SPI Communication System
2. DDR3 memory storage
3. Real-time Filter-and-Sum beamforming
4. Experiment
5. Live demo

System Overview

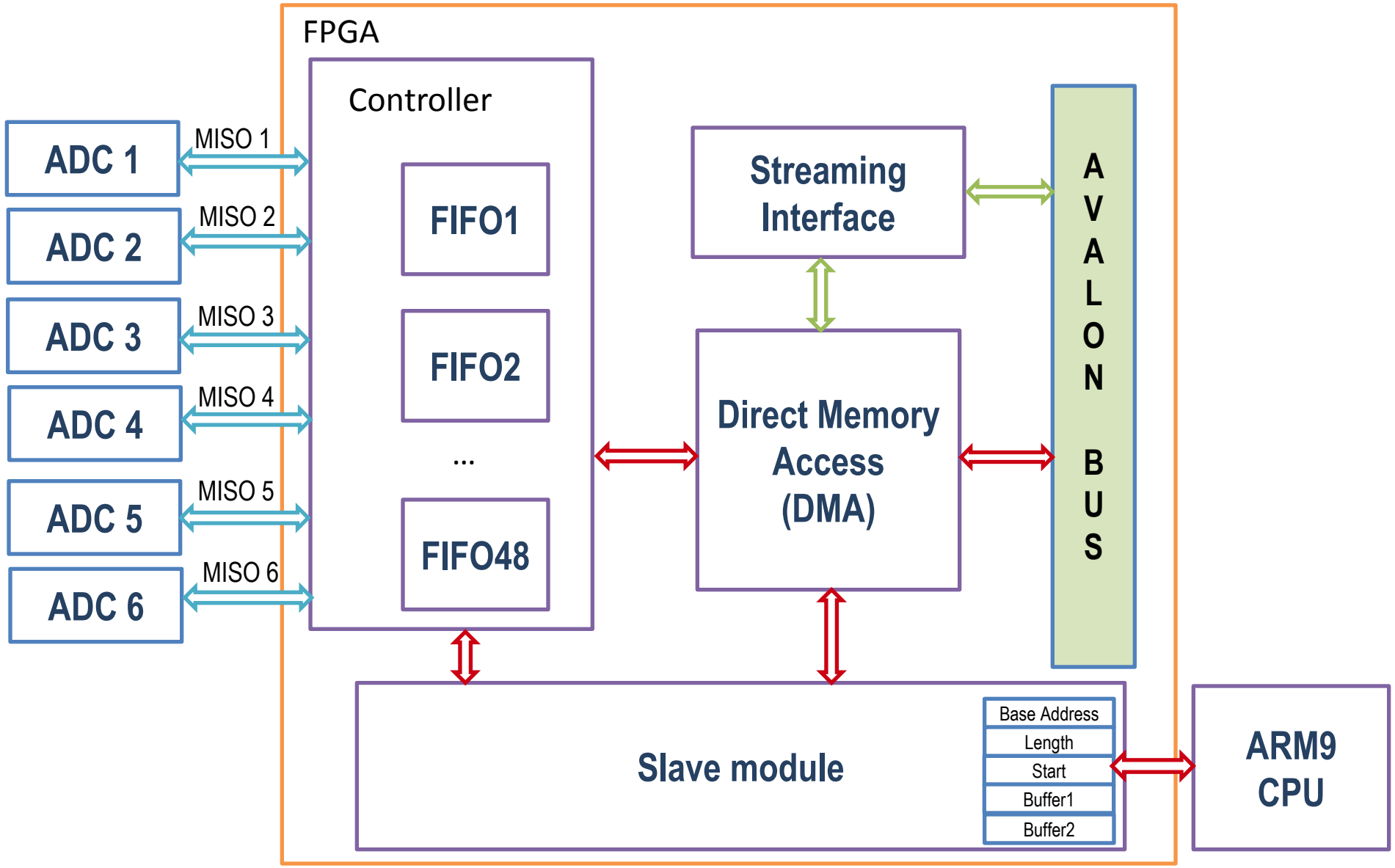


FPGA Design: SPI Communication

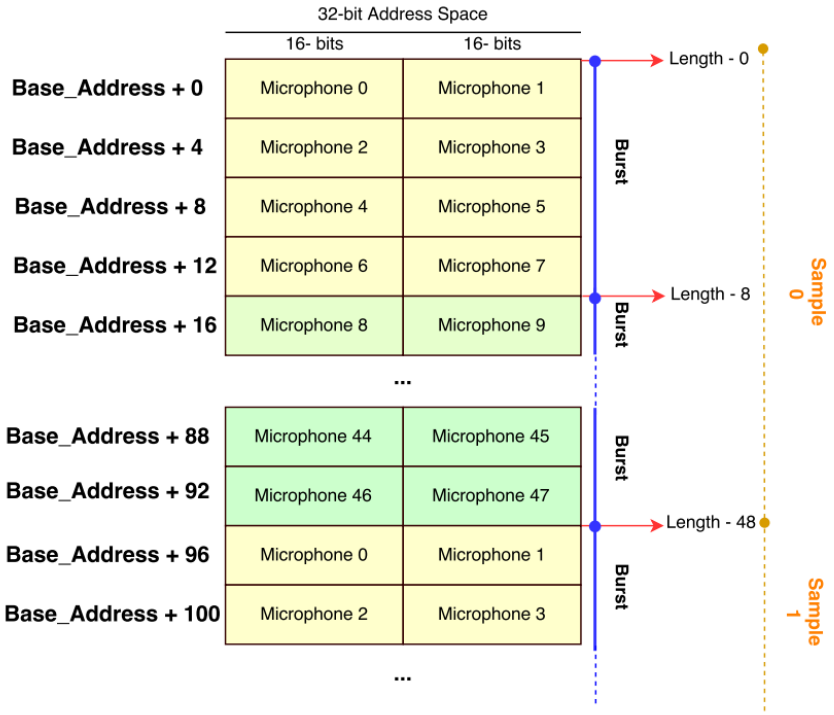


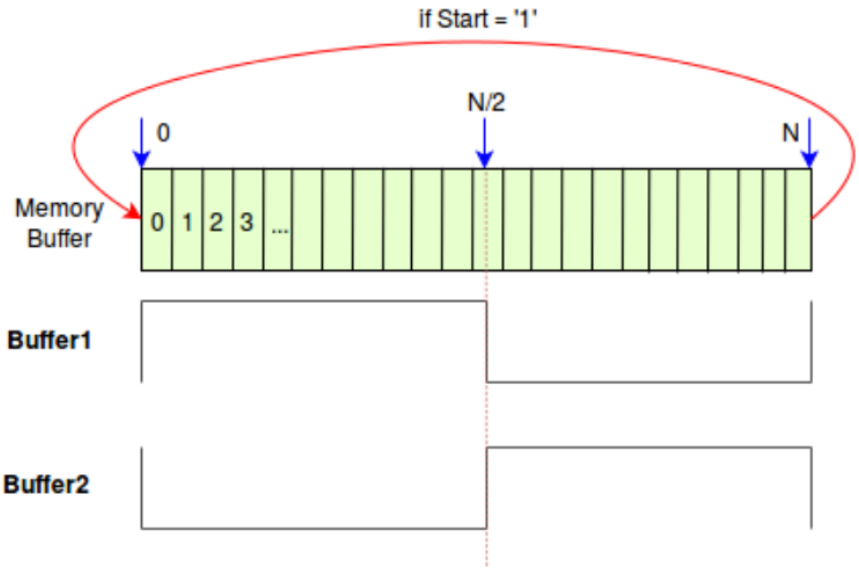


FPGA Design: SPI Communication

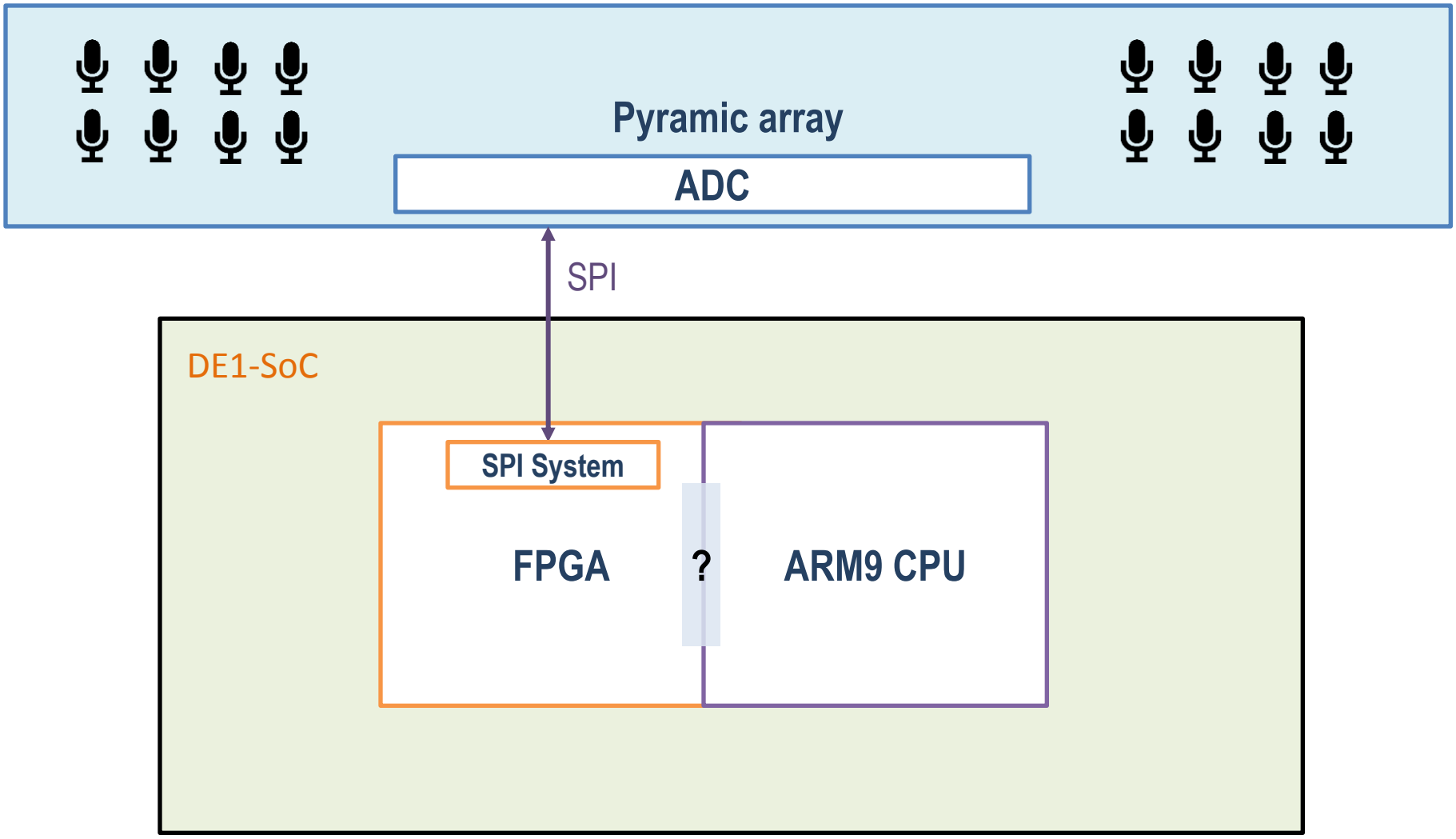


SPI Communication memory

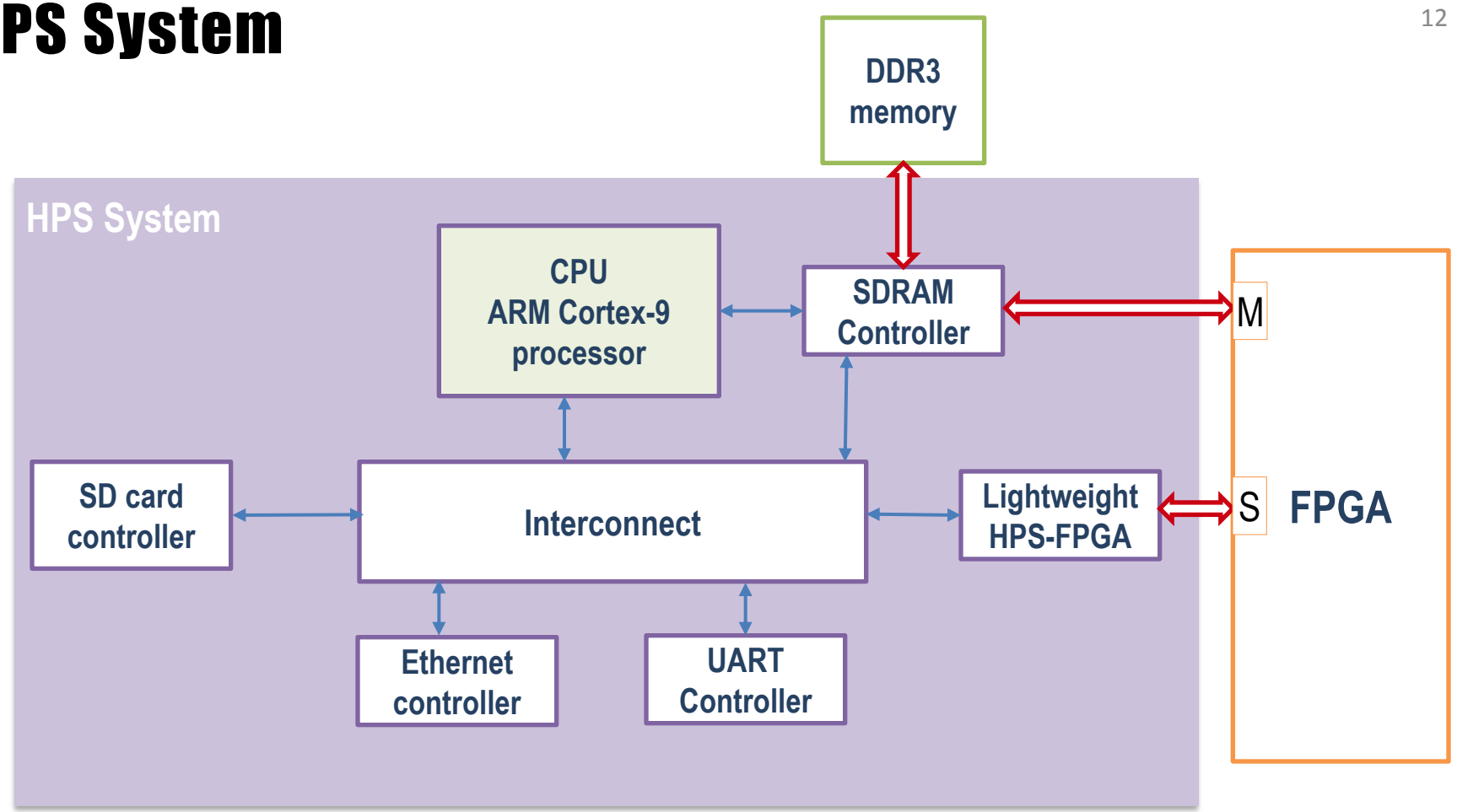




System Overview

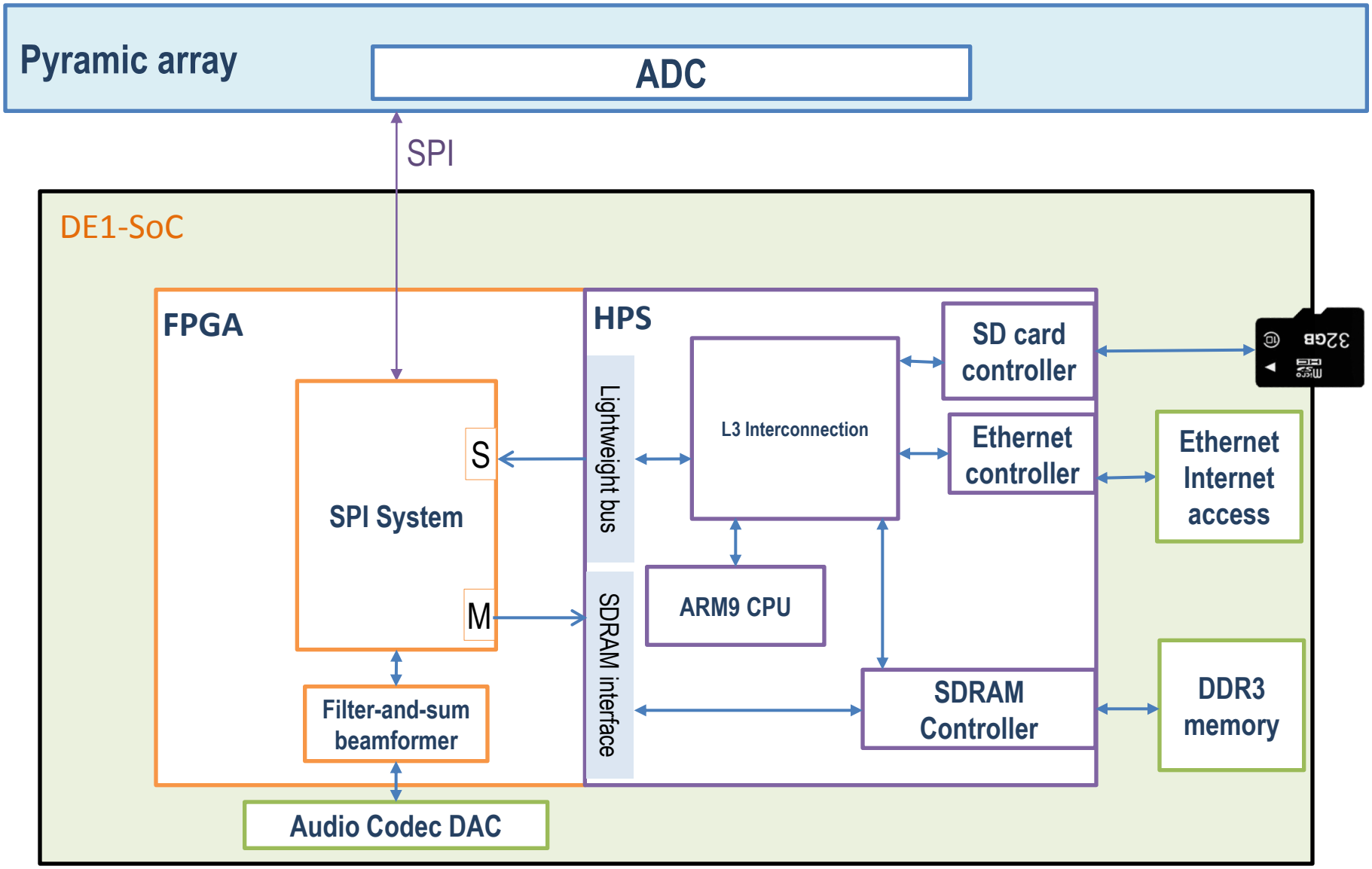


HPS System

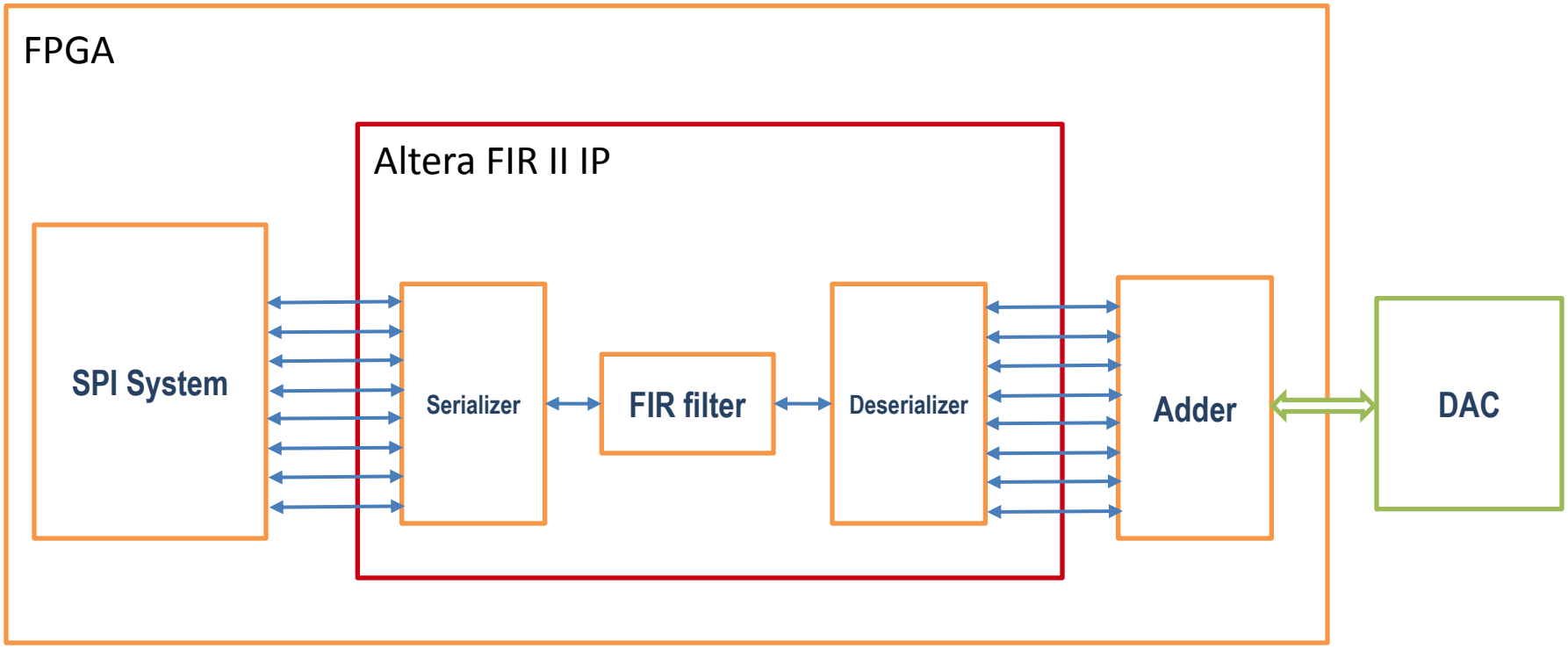


- ARM processor runs applications on Linux OS
- Ethernet connection for Internet access
- FPGA is configured from image stored on microSD card at power up time

System Overview



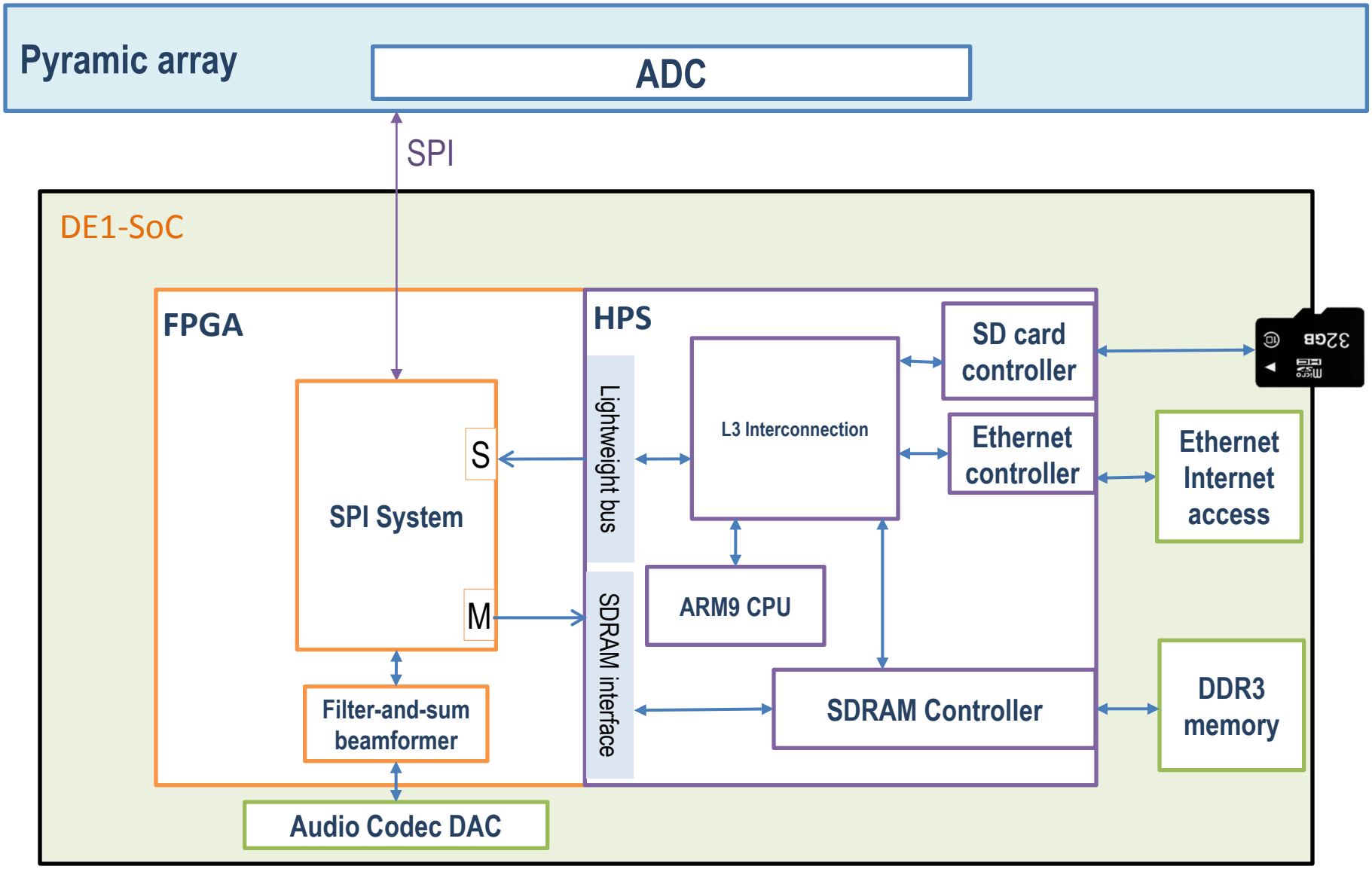
FPGA Design: Filter-and-sum beamformer



- Real-time delay-and-sum beamformer
- Serializer reduces hardware resources

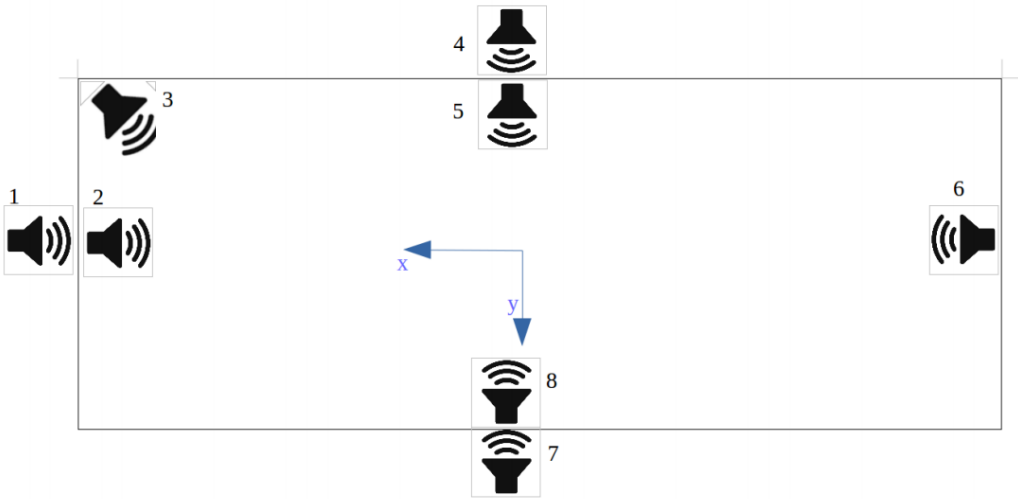
$$TDM = \frac{f_{clk}}{f_s} = \frac{50\ MHz}{48\ kHz} = 1024$$

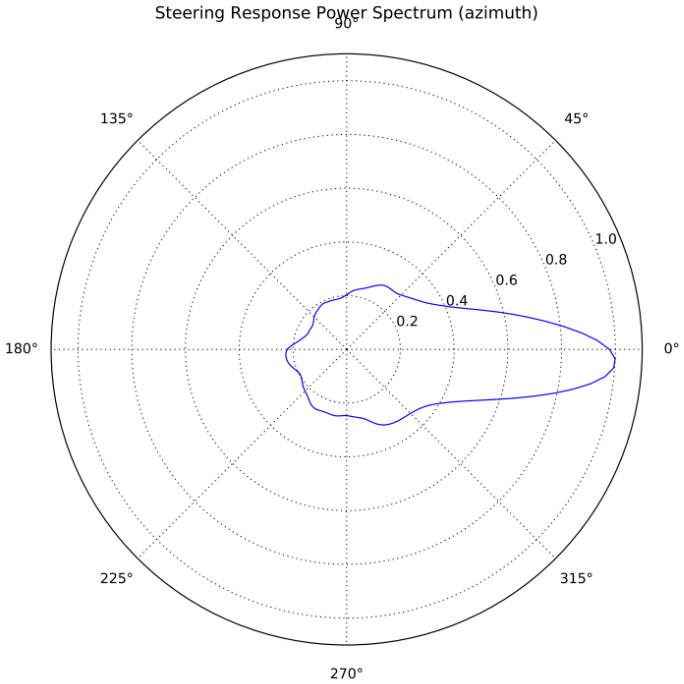
System Overview



Experiment

- SRP Phat: Steered-response power algorithm [1] for speech signals.
- Tested at *INR019* in EPFL.

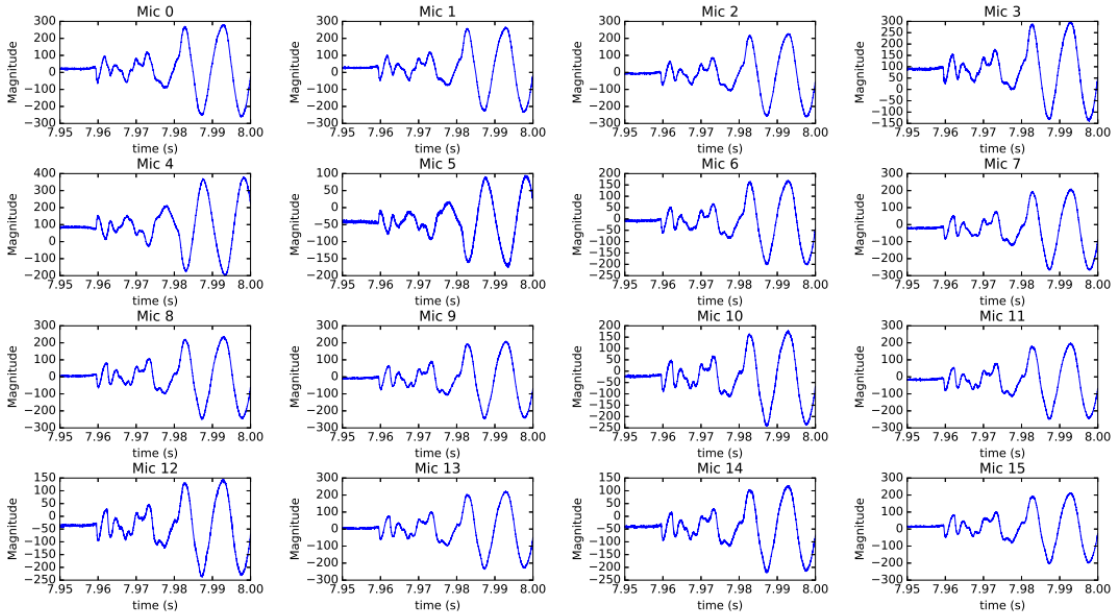




[1] J. H. DiBiade, 'A high-accuracy, low-latency technique for talker localiztion in reverberant environments using microphone arrays,' Ph.D. dissertation, Providence, RI, 2000.

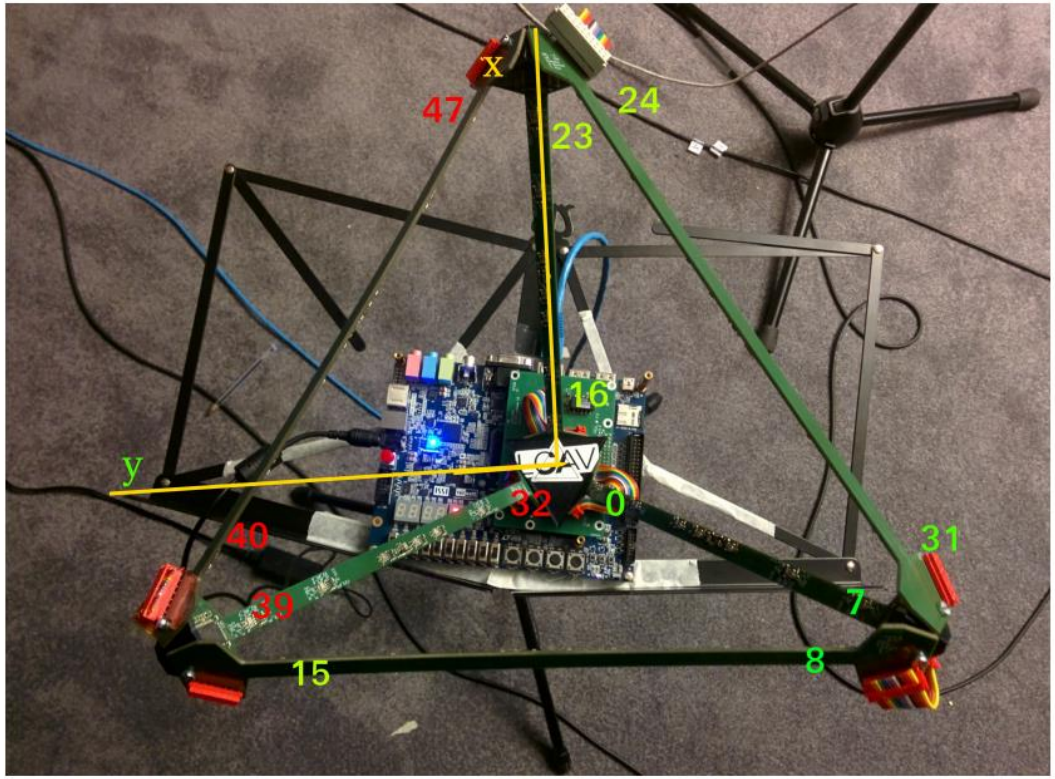
Further work

- Build advanced applications for the Pyramic array.
- Characterize the microphones' response.
- Design FPGA based hardware accelerators.
- Resolve output overflow when using the FIR filters bank
- Build reconfigurable FIR filters



DEMO

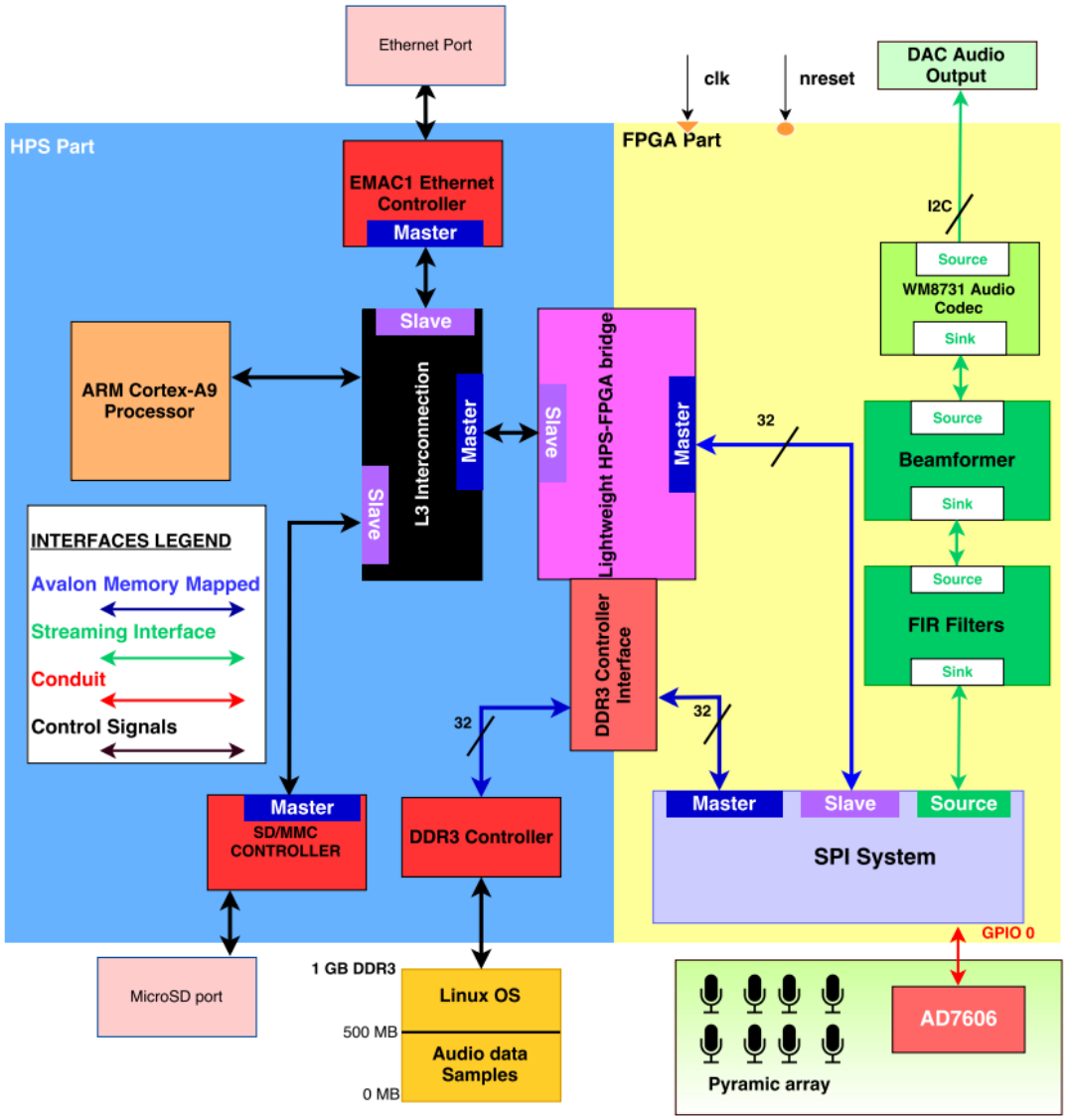
- SRP algorithm parameters
  - Frequency range: 100 Hz to 7 kHz
  - Far-field model
  - Hop size: 1024



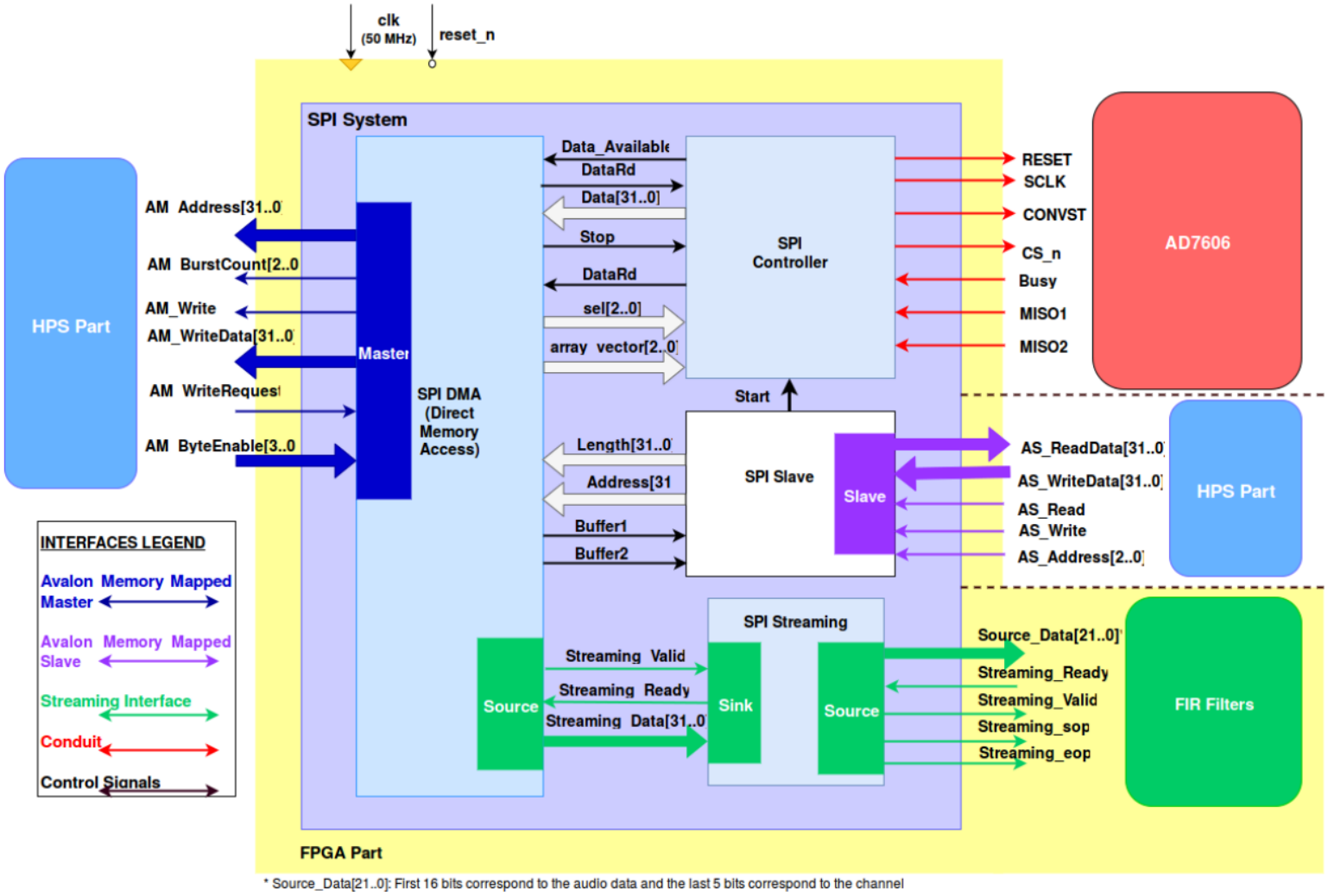
Thanks for your attention

Appendix : Summary

- SPI Communication with the Pyramic array
- Filters-beamforming
- microSD card
  - Powers on the system
  - Configures the FPGA
- Ethernet controller: Internet sharing
- ARM Cortex-A9 processor
  - Runs on Linux OS

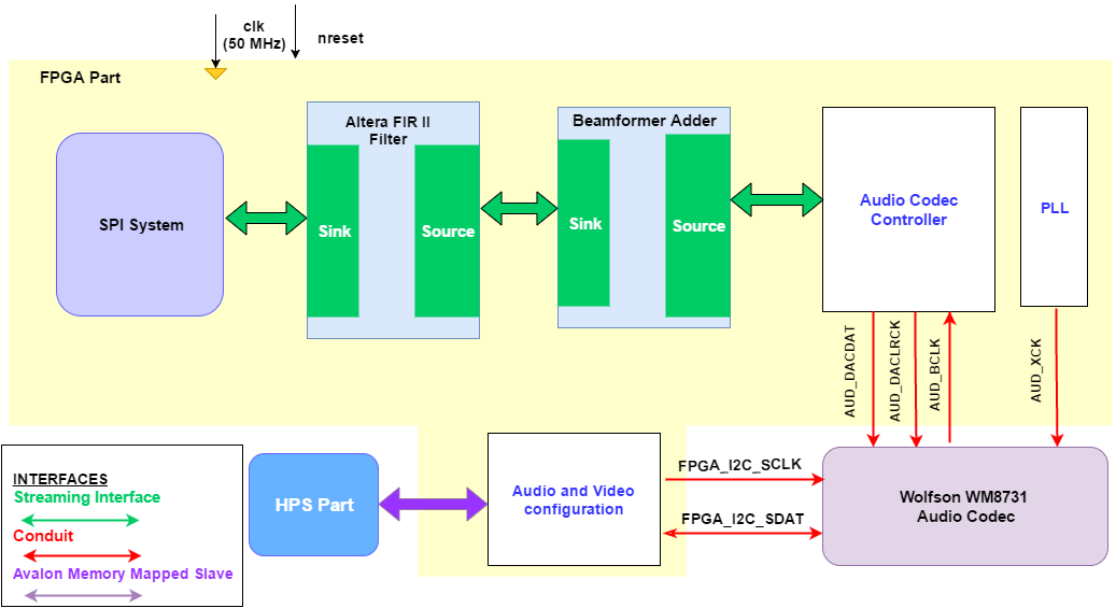


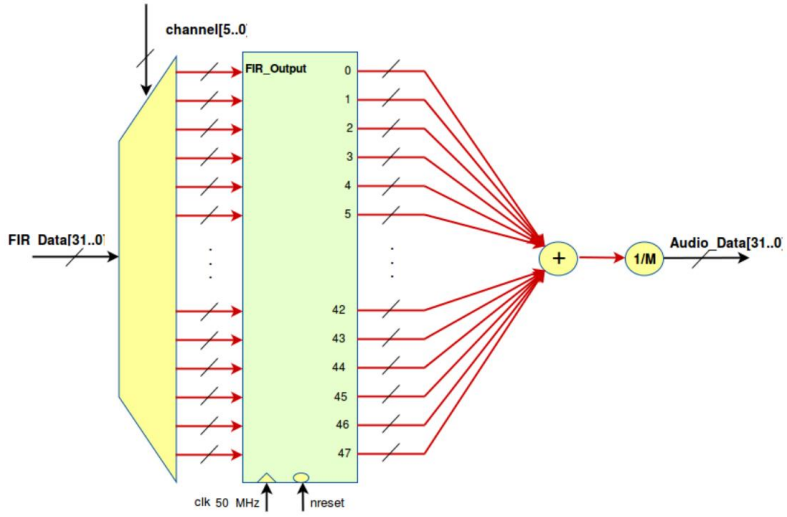
Appendix: SPI Communication

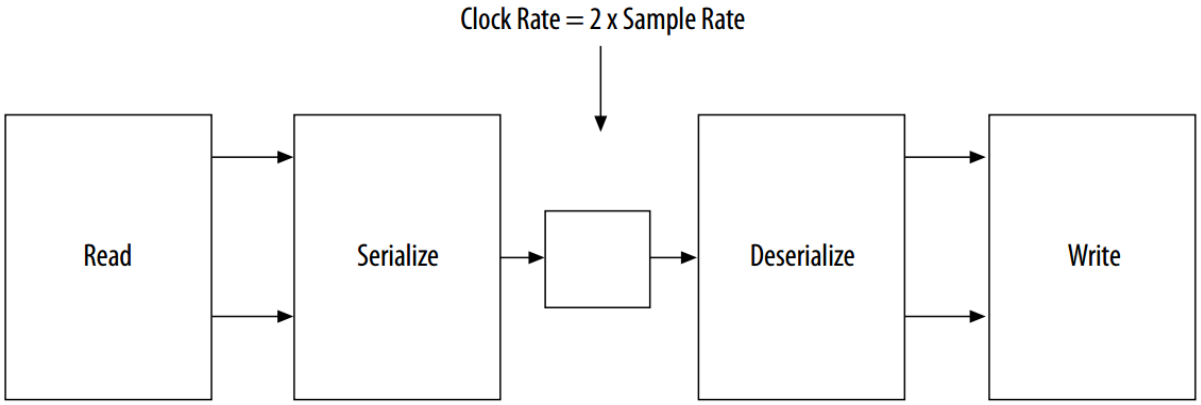


* Source_Data[21..0]: First 16 bits correspond to the audio data and the last 5 bits correspond to the channel

Appendix: Delay-and-sum beamformer







Appendix: HPS System