表 1: 8086 寄存器

Category	**Bits**	**Register Names**
General	16	AX(Accumulator), BX(Base), CX(Count), DX(Data)
	8	AH, AL, BH, BL, CH, CL, DH, DL
Pointer	16	SP(Stack Pointer), BP(Base Pointer)
Segment	16	CS(Code Segment), DS(Data Segment), SS(Stack Segment), ES(Extra Segment)
Instruction	16	IP(Instruction Pointer)
Flag	16	FR(Flag Register)

表 2: 8086 接脚

Signal	**Description**	0	1
ALE	Address Latch Enabled		Latched
$\overline{\text{BHE}}$	Bank High Enabled	$AD_8 \sim AD_{15}$ Enabled	$AD_8 \sim AD_{15}$ Disabled
DT/$\overline{\text{R}}$	direction of Data Transfer	sending data	receiving data
$\overline{\text{DEN}}$	Data transceiver ENabled	enabled	disabled
$\overline{\text{WR}}$	WRiting to Mem/IO	writing	
$\overline{\text{RD}}$	ReaDing from mem/IO	reading	
M/$\overline{\text{IO}}$	CPU accessing Memory / IO	IO	Memory
INTR	INTerrupt Request, maskable by clearing IF		Requesting
$\overline{\text{INTA}}$	INTerrupt Acknowledge		Acknowledge
NMI	Non-Maskable Interrupt, CPU is interrupted after finishing the current instruction; cannot be masked by software		will be interrupted
HOLD	HOLD the bus request		hold
HOLDA	HoLD request acknowledge		hold req ack
$\overline{\text{TEST}}$	for debug	test	
READY	mem/IO is READY for transfer		ready
RESET	reset the CPU, IP, DS, SS, ES and 6 inst in instruction queue are cleared		CS=0FFFFH

8086 16-bit, 20-bit address.
8088 16-bit internal, 8-bit external.
只有两段:
BIU (Bus Interface Unit) 连接内存与外设。
EU (Execution Unit) 执行之前获取的指令。
双工作模式
最小模式 MN/$\overline{\text{MX}} = 1$ 单 CPU。
最大模式 MN/$\overline{\text{MX}} = 0$ 多 CPU(8086+8087)，8288控制芯片。