Chapter9. Processor Modes & Thumb Code

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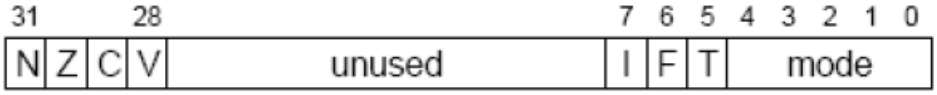
NOTE TAKING AREA

Processor modes

Current program status register (cpsr) uses 12 bits out of 32: 4 bits for condition codes or flags (N, Z, C, V), 5 bits for mode (User, FIQ, IRQ, SVC, Abort, Undef, System), 2 bits I and F to disable interrupts, 1 thumb bit T.



User:	10000
FIQ:	10001
IRQ:	10010
SVC:	10011
Abort:	10111
Undef:	11011
System:	11111

Saved program status register (spsr): 5 registers, from old mode to new mode.

7 processor modes of ARM: user, FIQ, IRQ, supervisor, abort, undef, system.

- Supervisor mode is entered on **reset** or **software interrupt (SWI, supervisor call) instruction is executed**.
- Abort mode is used when a **memory access violation** occurs.
- Undef mode is entered when the instruction decoder encounters **machine code for which there is no instruction**.
- System mode is a **privileged mode** used for the operating system.

Exception vectors

When an interrupt occurs the program counter (r15) is reloaded with the exception vector value.

IRQ 0x00000018 and FIQ 0x0000001C, initially 0x00000000.

Action upon an exception:

1. The cpsr is copied into relevant spsr.
2. Processor switches mode, and change mode bit in cpsr.
3. If appropriate, interrupts are disabled by setting bits in cpsr.
4. Return address is stored in link register.
5. Program counter is reloaded with the relevant vector address.

Thumb instruction set

Thumb instructions are 16 bit compressed ARM instructions.

The register range **from 0 to 7**, the immediate value range **from 0 to 255**.

Immediate value cannot be rotated.

Always been **non-conditional** and **set flags**.

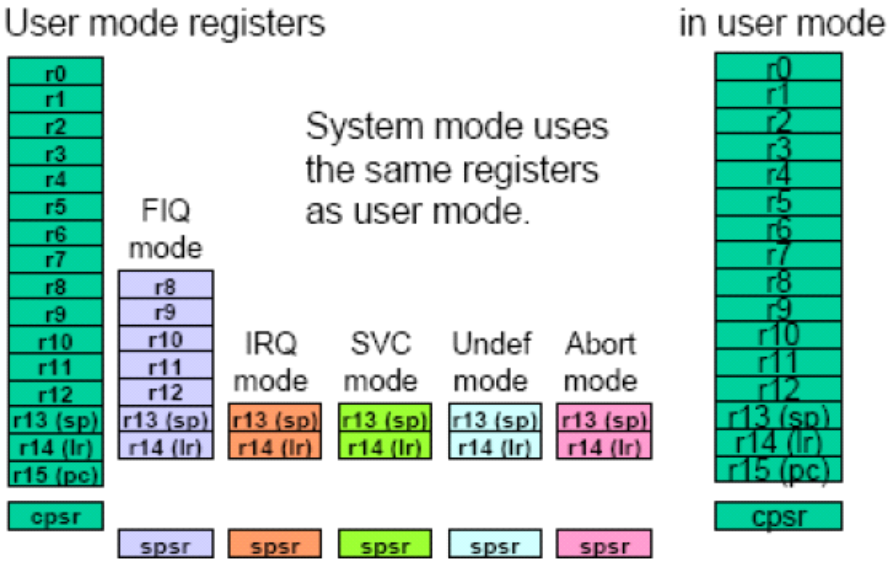
Thumb de-compressor: used to execute Thumb code (T bit set in cpsr).

Split 32 bit word into 2*16 bit Thumb code, and map Thumb code into ARM code, each instruction in 1 clock cycle.

ARM codes are faster in 32 bit processor, while Thumb codes are faster in 16 bit.

CUE COLUMN

Different registers in each mode



Each mode replaces corresponding registers, and copy spsr.

Vector table

Exception	Mode	vector address
Reset	SVC	0x00000000
Undefined instruction	Undef	0x00000004
Software interrupt (SWI)	SVC	0x00000008
Prefetch abort (instruction fetch memory fault)	Abort	0x0000000C
Data abort (data access memory fault)	Abort	0x00000010
IRQ (normal interrupts)	IRQ	0x00000018
FIQ (fast interrupts)	FIQ	0x0000001C

Example of Thumb code

0x402E for logical AND: r5 AND r6, and result in r6, $AND\ r6, r5$.

Machine code: 0100000000101110

Note only two registers allowed;

registers must be in range r0 to r7;

always unconditional;

always sets the flags.

0x3136 for adding 54 to r1 and result in r1, $ADD\ r1, \#0x36$.

Machine code: 0011000100110110

Only one register allowed which must be in range r0 to r7;

immediate value must be in range from 0 to 255 (can not be rotated);

always unconditional;

always sets the flags.

SUMMARIES

1. Processor modes: cpsr and spsr, 7 system modes.
2. Exception vectors.
3. Thumb instruction set and Thumb de-compressor.