# Contents



# VHDL Package

```
-- -------------------------------------------------------------
--
-- File Name: hdlsrc\untitled\vhdl_approximate_tanh_design_fixpt_slcfg.vhd
-- Created: 2021-08-24 11:43:20
--
-- Generated by MATLAB 9.8 and HDL Coder 3.16
--
-- -------------------------------------------------------------


-- -------------------------------------------------------------
--
-- Module: vhdl_approximate_tanh_design_fixpt_slcfg
-- Source Path: untitled/vhdl_approximate_tanh_design_fixpt_slcfg
-- Hierarchy Level: 1
--
-- -------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;
USE work.untitled_pkg.ALL;

ENTITY vhdl_approximate_tanh_design_fixpt_slcfg IS
  PORT( x                                 :   IN
vector_of_std_logic_vector14(0 TO 125);  -- sfix14_En10 [126]
        y_out                             :   OUT
vector_of_std_logic_vector14(0 TO 125)  -- sfix14_En13 [126]
        );
END vhdl_approximate_tanh_design_fixpt_slcfg;


ARCHITECTURE rtl OF vhdl_approximate_tanh_design_fixpt_slcfg IS

  -- Constants
  CONSTANT One                            : real :=
    2.0;  -- double
  CONSTANT C_divbyzero_p                  : real :=
    1.0E+308;  -- double
```

```
  -- Functions
  -- HDLCODER_TO_SIGNED
  FUNCTION hdlcoder_to_signed(arg: real; width: integer) RETURN signed IS
  BEGIN
    RETURN to_signed(integer(arg), width);
  END FUNCTION;


  -- Signals
  SIGNAL x_signed                         : vector_of_signed14(0 TO 125);  --
sfix14_En10 [126]
  SIGNAL y_out_tmp                        : vector_of_signed14(0 TO 125);  --
sfix14_En13 [126]

BEGIN
  outputgen1: FOR k1 IN 0 TO 125 GENERATE
    x_signed(k1) <= signed(x(k1));
  END GENERATE;

  vhdl_approximate_tanh_design_fixpt_slcfg_1_output : PROCESS (x_signed)
    VARIABLE y : vector_of_signed32(0 TO 125);
    VARIABLE y_0 : vector_of_signed32(0 TO 125);
    VARIABLE b : vector_of_signed32(0 TO 125);
    VARIABLE z1 : vector_of_signed32(0 TO 125);
    VARIABLE tmp : signed(31 DOWNTO 0);
    VARIABLE cast : vector_of_real(0 TO 125);
    VARIABLE div_temp : vector_of_real(0 TO 125);
    VARIABLE mul_temp : vector_of_signed29(0 TO 125);
    VARIABLE cast_0 : vector_of_signed28(0 TO 125);
    VARIABLE cast_1 : vector_of_signed28(0 TO 125);
    VARIABLE cast_2 : vector_of_unsigned32(0 TO 125);
    VARIABLE sll_temp : vector_of_unsigned32(0 TO 125);
    VARIABLE add_temp : vector_of_signed33(0 TO 125);
    VARIABLE sub_temp : vector_of_signed33(0 TO 125);
    VARIABLE cast_3 : vector_of_signed32(0 TO 125);
  BEGIN
    tmp := to_signed(16#00000000#, 32);
    --HDL code generation from MATLAB function:
sf_gateway_vhdl_approximate_tanh_design_fixpt_slcfg
    --MATLAB Function 'vhdl_approximate_tanh_design_fixpt_slcfg'
    --
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    --
%
    --           Generated by MATLAB 9.8 and Fixed-Point Designer 7.0
%
    --
%
    --
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    FOR k IN 0 TO 125 LOOP
      mul_temp(k) := to_signed(16#2E00#, 15) * x_signed(k);
      cast_0(k) := mul_temp(k)(27 DOWNTO 0);
      cast_1(k) := resize(cast_0(k)(27 DOWNTO 22), 28);
```

```
      y(k) := resize(cast_1(k), 32);
      IF y(k) > to_signed(16#0000001E#, 32) THEN
        tmp := to_signed(16#7FFFFFFF#, 32);
      ELSE
        IF y(k)(31) = '1' THEN
          cast_2(k) := X"00000000";
        ELSE
          cast_2(k) := unsigned(y(k));
        END IF;
        sll_temp(k) := to_unsigned(16#00000001#, 32) sll
to_integer(cast_2(k));
        IF sll_temp(k)(31) /= '0' THEN
          tmp := X"7FFFFFFF";
        ELSE
          tmp := signed(sll_temp(k));
        END IF;
      END IF;
      y_0(k) := tmp;
      add_temp(k) := resize(y_0(k), 33) + to_signed(1, 33);
      IF (add_temp(k)(32) = '0') AND (add_temp(k)(31) /= '0') THEN
        b(k) := X"7FFFFFFF";
      ELSIF (add_temp(k)(32) = '1') AND (add_temp(k)(31) /= '1') THEN
        b(k) := X"80000000";
      ELSE
        b(k) := add_temp(k)(31 DOWNTO 0);
      END IF;
      cast(k) := real(to_integer(b(k)));
      IF cast(k) = 0.0 THEN
        div_temp(k) := C_divbyzero_p;
      ELSE
        div_temp(k) := One / cast(k);
      END IF;
      z1(k) := hdlcoder_to_signed(div_temp(k), 32);
      sub_temp(k) := to_signed(1, 33) - resize(z1(k), 33);
      IF (sub_temp(k)(32) = '0') AND (sub_temp(k)(31) /= '0') THEN
        cast_3(k) := X"7FFFFFFF";
      ELSIF (sub_temp(k)(32) = '1') AND (sub_temp(k)(31) /= '1') THEN
        cast_3(k) := X"80000000";
      ELSE
        cast_3(k) := sub_temp(k)(31 DOWNTO 0);
      END IF;
      y_out_tmp(k) <= signed'(cast_3(k)(0) & '0' & '0' & '0' & '0' & '0' &
'0' & '0' & '0' & '0' & '0' & '0' & '0' & '0');
    END LOOP;

  END PROCESS vhdl_approximate_tanh_design_fixpt_slcfg_1_output;


  outputgen: FOR k1 IN 0 TO 125 GENERATE
    y_out(k1) <= std_logic_vector(y_out_tmp(k1));
  END GENERATE;

END rtl;


-- -------------------------------------------------------------
```

```
--
-- File Name: hdlsrc\untitled\untitled_pkg.vhd
-- Created: 2021-08-24 11:43:20
--
-- Generated by MATLAB 9.8 and HDL Coder 3.16
--
-- -------------------------------------------------------------


LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

PACKAGE untitled_pkg IS
  TYPE vector_of_std_logic_vector14 IS ARRAY (NATURAL RANGE <>) OF
std_logic_vector(13 DOWNTO 0);
  TYPE vector_of_signed14 IS ARRAY (NATURAL RANGE <>) OF signed(13 DOWNTO 0);
  TYPE vector_of_signed32 IS ARRAY (NATURAL RANGE <>) OF signed(31 DOWNTO 0);
  TYPE vector_of_real IS ARRAY (NATURAL RANGE <>) OF real;
  TYPE vector_of_signed29 IS ARRAY (NATURAL RANGE <>) OF signed(28 DOWNTO 0);
  TYPE vector_of_signed28 IS ARRAY (NATURAL RANGE <>) OF signed(27 DOWNTO 0);
  TYPE vector_of_unsigned32 IS ARRAY (NATURAL RANGE <>) OF unsigned(31 DOWNTO
0);
  TYPE vector_of_signed33 IS ARRAY (NATURAL RANGE <>) OF signed(32 DOWNTO 0);
END untitled_pkg;
```

## VHDL Source

```
-- -------------------------------------------------------------
--
-- File Name: hdlsrc\untitled\untitled.vhd
-- Created: 2021-08-24 11:43:20
--
-- Generated by MATLAB 9.8 and HDL Coder 3.16
--
--
-- -------------------------------------------------------------
-- Rate and Clocking Details
-- -------------------------------------------------------------
-- Model base rate: 0.2
-- Target subsystem base rate: 0.2
--
-- -------------------------------------------------------------


-- -------------------------------------------------------------
--
-- Module: untitled
-- Source Path: untitled
-- Hierarchy Level: 0
--
-- -------------------------------------------------------------
LIBRARY IEEE;
```

```
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;
USE work.untitled_pkg.ALL;

ENTITY untitled IS
  PORT( in1                                     :   IN
vector_of_std_logic_vector14(0 TO 125);  -- sfix14_En10 [126]
        out1                                    :   OUT
vector_of_std_logic_vector14(0 TO 125)  -- sfix14_En13 [126]
        );
END untitled;


ARCHITECTURE rtl OF untitled IS

  -- Component Declarations
  COMPONENT vhdl_approximate_tanh_design_fixpt_slcfg
    PORT( x                                     :   IN
vector_of_std_logic_vector14(0 TO 125);  -- sfix14_En10 [126]
          y_out                                 :   OUT
vector_of_std_logic_vector14(0 TO 125)  -- sfix14_En13 [126]
          );
  END COMPONENT;

  -- Component Configuration Statements
  FOR ALL : vhdl_approximate_tanh_design_fixpt_slcfg
    USE ENTITY work.vhdl_approximate_tanh_design_fixpt_slcfg(rtl);

  -- Signals
  SIGNAL y_out                                  : vector_of_std_logic_vector14(0 TO
125);  -- ufix14 [126]

BEGIN
  u_vhdl_approximate_tanh_design_fixpt_slcfg :
vhdl_approximate_tanh_design_fixpt_slcfg
    PORT MAP( x => in1,  -- sfix14_En10 [126]
              y_out => y_out  -- sfix14_En13 [126]
              );

  out1 <= y_out;

END rtl;
```

## Design

```
function [y_out] = vhdl_approximate_tanh_design( x )
    y_out = 1-(2./(power(2,((4-1-(1/4)+(1/8))*x))+1));
end
```

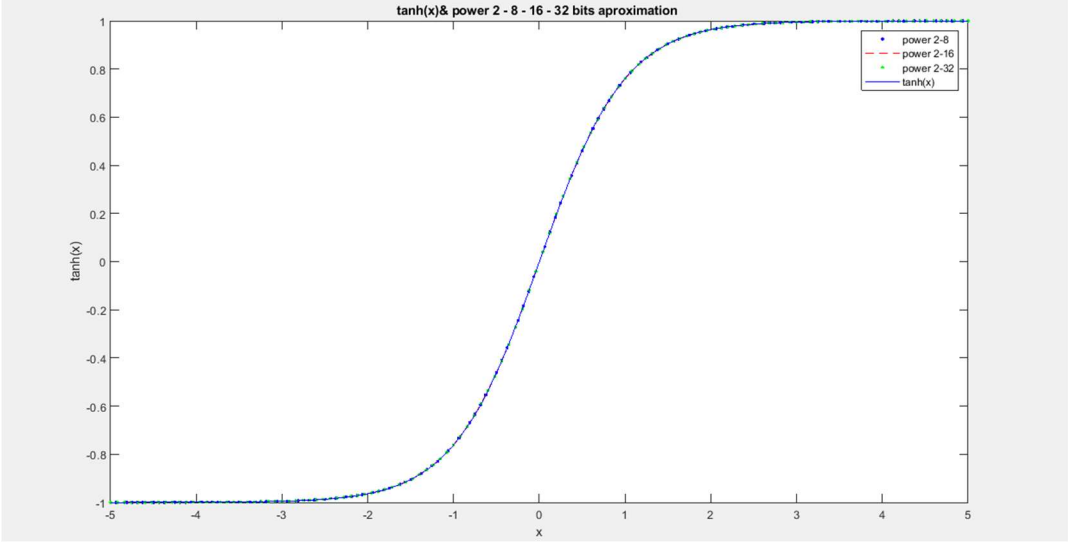
## Test Bunch

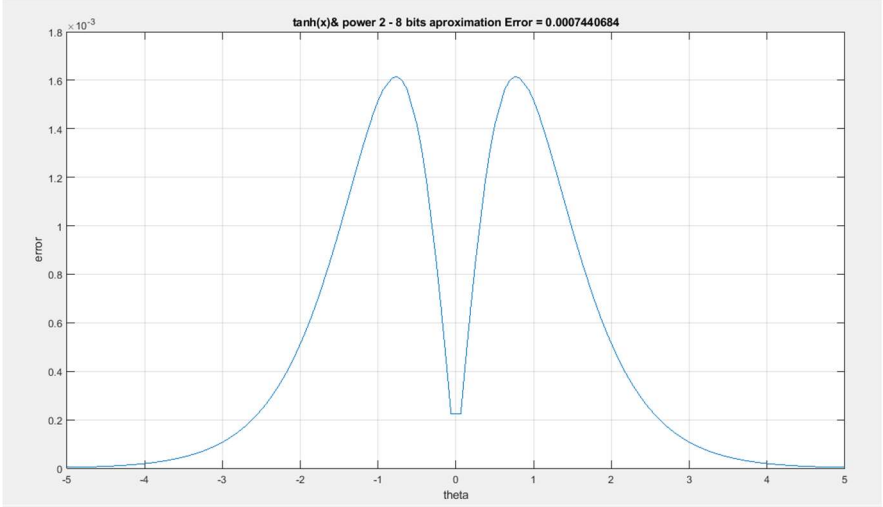
```
% C:\Program
Files\Polyspace\R2020a\toolbox\hdlcoder\hdlcoderdemos\matlabhdlcoderdemos
% https://www.mathworks.com/company/newsletters/articles/best-practices-for-
converting-matlab-code-to-fixed-point.html
% https://www.mathworks.com/help/fixedpoint/ug/functions-supported-for-code-
acceleration-and-code-generation-from-matlab.html
function vhdl_approximate_tanh_tb
  % Test inputs
  x_8  = fi(-5:0.08:5,1,8);
  x_16 = fi(-5:0.08:5,1,16);
  x_32 = fi(-5:0.08:5,1,32);
  % Run
 y = tanh( double(x_8) );
 y_power2_8 = vhdl_approximate_tanh_design( double( x_8));    % 8 bits
 %y_power2_16 = vhdl_approximate_tanh_design( double( x_16));    % 16 bits
 %y_power2_32 = vhdl_approximate_tanh_design( double( x_32));    % 32 bits

  figure;
  plot(x_8,y_power2_8,'r.',x_8,y,'b'),legend('power 2-8','power 2-16', 'power
2-32', 'tanh(x)');

%   plot(x_8,y_power2_8,'r.',x_16,y_power2_16,'r--', x_32,y_power2_32,'g.'
,x_8,y,'b'),legend('power 2-8','power 2-16', 'power 2-32', 'tanh(x)');
  title("tanh(x)& power 2 - 8 - 16 - 32 bits aproximation " );
  xlabel('x');
  ylabel('tanh(x)');


  error8_ = RMSE(y_power2_8,y);
  formatSpec = '%.10f';
  error8_=num2str(error8_,formatSpec);
  disp("error 8 bits:" + error8_);

  figure;
  err = abs(y - double(y_power2_8));
  plot(x_8, err);
  xlabel('theta');
  ylabel('error');
  title("tanh(x)& power 2 - 8 bits aproximation Error = " + error8_);
  grid on;

%   y_16 = tanh( double(x_16) );
%   error16_ = RMSE(y_power2_16,y_16);
%   formatSpec = '%.10f';
%   error16_=num2str(error16_,formatSpec);
%   disp("error 16 bits:" + error16_);
%
%   figure;
%   err = abs(y_16 - double(y_power2_16));
%   plot(x_16, err);
%   xlabel('theta');
%   ylabel('error');
%   title("tanh(x)& power 2 - 16 bits aproximation Error = " + error16_);
%   grid on;
```

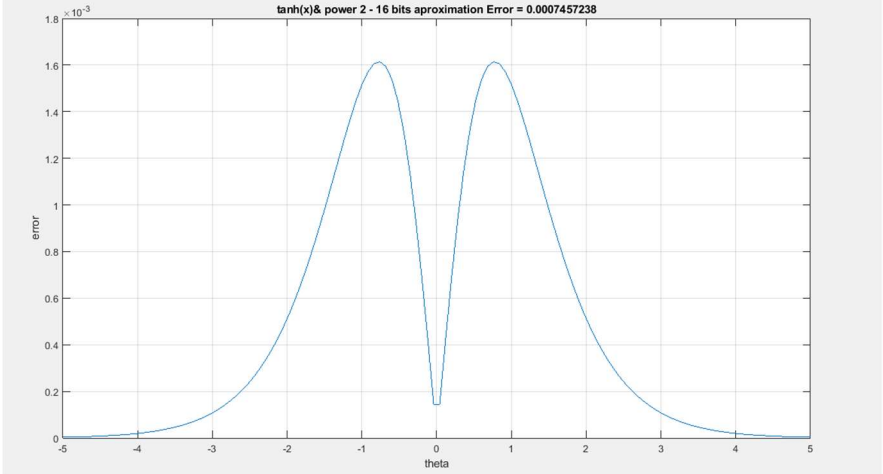
```
%
%    y_32 = tanh( double(x_32) );
%    error32_ = RMSE(y_power2_32,y_32);
%    formatSpec = '%.10f';
%    error32_=num2str(error32_,formatSpec);
%    disp("error 32 bits:" + error32_);
%
%    figure;
%    err_32 = abs(y_32 - double(y_power2_32));
%    plot(x_32, err_32);
%    xlabel('theta');
%    ylabel('error');
%    title("tanh(x)& power 2 - 32 bits aproximation Error = " + error32_);
%    grid on;

end
```

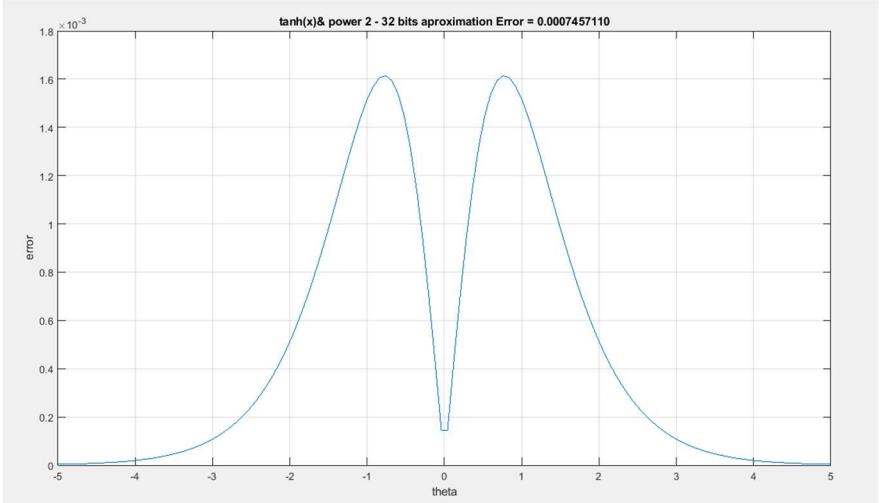
## Plots

```
4    function vhdl_approximate_tanh_tb
5      % Test inputs
6 -    x_8  = fi(-5:0.08:5,1,8);
7 -    x_16 = fi(-5:0.08:5,1,16);
8 -    x_32 = fi(-5:0.08:5,1,32);
9      % Run
10 -   y = tanh( double(x_8) );
11 -   y_power2_8 = vhdl_approximate_tanh_design( double( x_8));   % 8 bits
12 -   y_power2_16 = vhdl_approximate_tanh_design( double( x_16));   % 16 bits
13 -   y_power2_32 = vhdl_approximate_tanh_design( double( x_32));   % 32 bits
14
15 -    figure;
16 -    plot(x_8,y_power2_8,'r.',x_16,y_power2_16,'r--', x_32,y_power2_32,'g.' ,x_8,y,'b'),legend(
17 -    title("tanh(x)& power 2 - 8 - 16 - 32 bits aproximation " );
18 -    xlabel('x');
```




tanh(x)& power 2 - 8 bits aproximation Error = 0.0007440684
×10^-3
error
theta


tanh(x)& power 2 - 16 bits aproximation Error = 0.0007457238
×10^-3
error
theta


tanh(x)& power 2 - 32 bits aproximation Error = 0.0007457110
×10^-3
error
theta

vhdl_approximate_tanh_tb.m | vhdl_approximate_tanh_design.m

```
function [y_out] = vhdl_approximate_tanh_design( x )
    y_out = 1-(2./(power(2,((4-1-(1/4)+(1/8))*x))+1));
end
```

Command Window

```
Warning: An error occurred while reading the desktop configuration file.
Using the default configuration.
>> vhdl_approximate_tanh_tb
error 8 bits:0.0007440684
error 16 bits:0.0007457238
error 32 bits:0.0007457110
>>
```

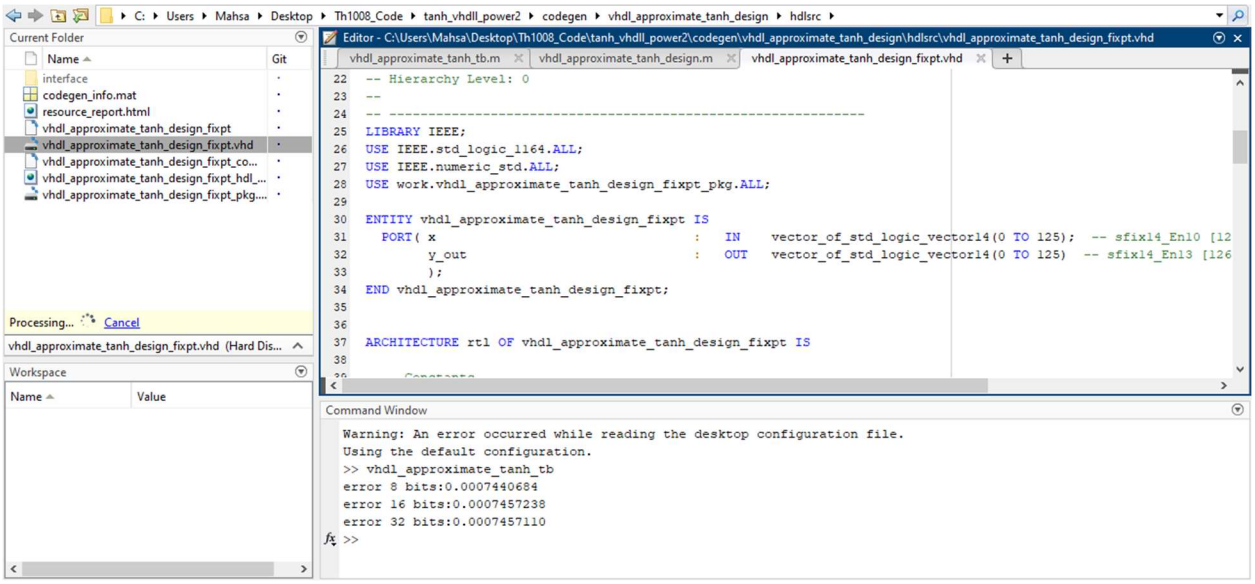
vhdl_approximate_tanh_tb.m | vhdl_approximate_tanh_design.m

```
% C:\Program Files\Polyspace\R2020a\toolbox\hdlcoder\hdlcoderdemos\matlabhdlcoderdemos
% https://www.mathworks.com/company/newsletters/articles/best-practices-for-converting-matlab-code-to-fixed
% https://www.mathworks.com/help/fixedpoint/ug/functions-supported-for-code-acceleration-and-code-generatic
function vhdl_approximate_tanh_tb
    % Test inputs
    x_8  = fi(-5:0.08:5,1,8);
    x_16 = fi(-5:0.08:5,1,16);
    x_32 = fi(-5:0.08:5,1,32);
    % Run
   y = tanh( double(x_8) );
   y_power2_8 = vhdl_approximate_tanh_design( double( x_8));   % 8 bits
   y_power2_16 = vhdl_approximate_tanh_design( double( x_16));   % 16 bits
   y_power2_32 = vhdl_approximate_tanh_design( double( x_32));   % 32 bits

    figure;
    plot(x_8,y_power2_8,'r.',x_16,y_power2_16,'r--', x_32,y_power2_32,'g.' ,x_8,y,'b'),legend('power 2-8','pc
    title("tanh(x)& power 2 - 8 - 16 - 32 bits aproximation " );
```

Command Window

```
Warning: An error occurred while reading the desktop configuration file.
Using the default configuration.
>> vhdl_approximate_tanh_tb
error 8 bits:0.0007440684
error 16 bits:0.0007457238
error 32 bits:0.0007457110
>>
```

UTF-8 | vhdl_approximate_tanh_tb | Ln 5 Col 16


C: ▸ Users ▸ Mahsa ▸ Desktop ▸ Th1008_Code ▸ tanh_vhdll_power2 ▸ codegen ▸ vhdl_approximate_tanh_design ▸ hdlsrc ▸
Current Folder
Name
Git
interface
codegen_info.mat
resource_report.html
vhdl_approximate_tanh_design_fixpt
vhdl_approximate_tanh_design_fixpt.vhd
vhdl_approximate_tanh_design_fixpt_co...
vhdl_approximate_tanh_design_fixpt_hdl_...
vhdl_approximate_tanh_design_fixpt_pkg....
Processing... Cancel
vhdl_approximate_tanh_design_fixpt.vhd (Hard Dis...
Workspace
Name
Value
Editor - C:\Users\Mahsa\Desktop\Th1008_Code\tanh_vhdll_power2\codegen\vhdl_approximate_tanh_design\hdlsrc\vhdl_approximate_tanh_design_fixpt.vhd
vhdl_approximate_tanh_tb.m
vhdl_approximate_tanh_design.m
vhdl_approximate_tanh_design_fixpt.vhd
22 -- Hierarchy Level: 0
23 --
24 -- ------------------------------------------------------------
25 LIBRARY IEEE;
26 USE IEEE.std_logic_1164.ALL;
27 USE IEEE.numeric_std.ALL;
28 USE work.vhdl_approximate_tanh_design_fixpt_pkg.ALL;
29
30 ENTITY vhdl_approximate_tanh_design_fixpt IS
31 PORT( x : IN vector_of_std_logic_vector14(0 TO 125); -- sfix14_En10 [12
32 y_out : OUT vector_of_std_logic_vector14(0 TO 125) -- sfix14_En13 [126
33 );
34 END vhdl_approximate_tanh_design_fixpt;
35
36
37 ARCHITECTURE rtl OF vhdl_approximate_tanh_design_fixpt IS
38
Command Window
Warning: An error occurred while reading the desktop configuration file.
Using the default configuration.
>> vhdl_approximate_tanh_tb
error 8 bits:0.0007440684
error 16 bits:0.0007457238
error 32 bits:0.0007457110
>>

Web Browser - HDL Resource Utilization Report for 'vhdl_approximate_tanh_design_fixpt'

HDL Resource Utilization Report for 'vhdl_approximate_tanh_design_fixpt'

Location: file:///C:/Users/Mahsa/Desktop/Th1008_Code/tanh_vhdll_power2/codege

## Summary

| | |
|---|---|
| Multipliers | 126 |
| Adders/Subtractors | 252 |
| Registers | 0 |
| Total 1 Bit Registers | 0 |
| RAMs | 0 |
| Multiplexers | 630 |
| I/O Bits | 3528 |
| Shifters | 126 |

### Multipliers (126)

- 15x14-bit Multipliers : 126

### Adders/Subtractors (252)

- 33x33-bit Adders : 126
- 33x33-bit Subtractors : 126

### Multiplexers (630)

- 32-bit 2-to-1 Multiplexer : 126
- 32-bit 3-to-1 Multiplexer : 378
- real 2-to-1 Multiplexer : 126

### Shift operators (126)

- Static Left Shift operators : 126

### I/O Bits (3528)

#### Input Bits (1764)

- x : 1764 bits