Contents

Design

```
function []=tanh_RALUT()
    problem = FunctionApproximation.Problem('tanh');
    problem.InputTypes =  numerictype(1,8);
    problem.InputLowerBounds = -5;
    problem.InputUpperBounds = 5;
    problem.OutputType = numerictype(1,8,7);

    %Range Addressable Look Up Table
    %Optimization to be Range Addressable Look Up
    problem.Options.BreakpointSpecification='EvenPow2Spacing';
    problem.Options.WordLengths=8; %[8, 16, 32]
    problem.Options.Display=0;
    problem.Options.Interpolation = "Flat";
%     problem.Options.HDL-Optimized = 1;
    problem.Options.SaturateToOutputType = 1; %Whether to automatically
saturate the range of the output of the function to approximate to the range
of the output data type, specified as a numeric or logical 1 (true) or 0
(false).
%     problem.Options.UseParallel=1;
    problem.Options.OnCurveTableValues=0;

    solution = solve(problem);
    compare(solution);
    approximate(solution);
    memory = totalmemoryusage(solution);
    disp(memory);

end
%
https://www.mathworks.com/help/fixedpoint/ref/functionapproximation.options-
class.html
```

VHDL Package

```
-- ------------------------------------------------------------
```

```
--
-- File Name:
hdlsrc\Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9\Approximate_id
_0af2ac3f3b928182f3ff557fc379a1d7491938e9_pkg.vhd
-- Created: 2021-08-24 10:29:19
--
-- Generated by MATLAB 9.8 and HDL Coder 3.16
--
-- -------------------------------------------------------------


LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

PACKAGE Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9_pkg IS
  TYPE vector_of_signed8 IS ARRAY (NATURAL RANGE <>) OF signed(7 DOWNTO 0);
END Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9_pkg;
```

VHDL Approximation

```
-- -------------------------------------------------------------
--
-- File Name:
hdlsrc\Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9\Approximate_id
_0af2ac3f3b928182f3ff557fc379a1d7491938e9_pkg.vhd
-- Created: 2021-08-24 10:29:19
--
-- Generated by MATLAB 9.8 and HDL Coder 3.16
--
-- -------------------------------------------------------------


LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

PACKAGE Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9_pkg IS
  TYPE vector_of_signed8 IS ARRAY (NATURAL RANGE <>) OF signed(7 DOWNTO 0);
END Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9_pkg;
```

VHDL Source

```
-- -------------------------------------------------------------
--
-- File Name:
hdlsrc\Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9\Source.vhd
-- Created: 2021-08-24 10:29:18
```

```
--
-- Generated by MATLAB 9.8 and HDL Coder 3.16
--
-- -------------------------------------------------------------


-- -------------------------------------------------------------
--
-- Module: Source
-- Source Path:
Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9/Source
-- Hierarchy Level: 1
--
-- Simulink subsystem description for
Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9/Source:
--
-- This block was created using function approximation.
--
-- -------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;
USE work.Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9_pkg.ALL;

ENTITY Source IS
  PORT( clk                               :   IN    std_logic;
        enb                               :   IN    std_logic;
        In1                               :   IN    std_logic_vector(7 DOWNTO
0);  -- sfix8_En4
        Out1                              :   OUT   std_logic_vector(7 DOWNTO
0)  -- sfix8_En7
        );
END Source;


ARCHITECTURE rtl OF Source IS

  -- Constants
  CONSTANT LUT_data                       : vector_of_signed8(0 TO 158) :=
    (to_signed(-16#80#, 8), to_signed(-16#80#, 8), to_signed(-16#80#, 8),
to_signed(-16#80#, 8),
     to_signed(-16#80#, 8), to_signed(-16#80#, 8), to_signed(-16#80#, 8),
to_signed(-16#80#, 8),
     to_signed(-16#80#, 8), to_signed(-16#80#, 8), to_signed(-16#80#, 8),
to_signed(-16#80#, 8),
     to_signed(-16#80#, 8), to_signed(-16#80#, 8), to_signed(-16#80#, 8),
to_signed(-16#80#, 8),
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to_signed(-16#80#, 8),
     to_signed(-16#80#, 8), to_signed(-16#80#, 8), to_signed(-16#80#, 8),
to_signed(-16#80#, 8),
     to_signed(-16#80#, 8), to_signed(-16#80#, 8), to_signed(-16#80#, 8),
to_signed(-16#80#, 8),
     to_signed(-16#80#, 8), to_signed(-16#80#, 8), to_signed(-16#80#, 8),
to_signed(-16#7F#, 8),
```
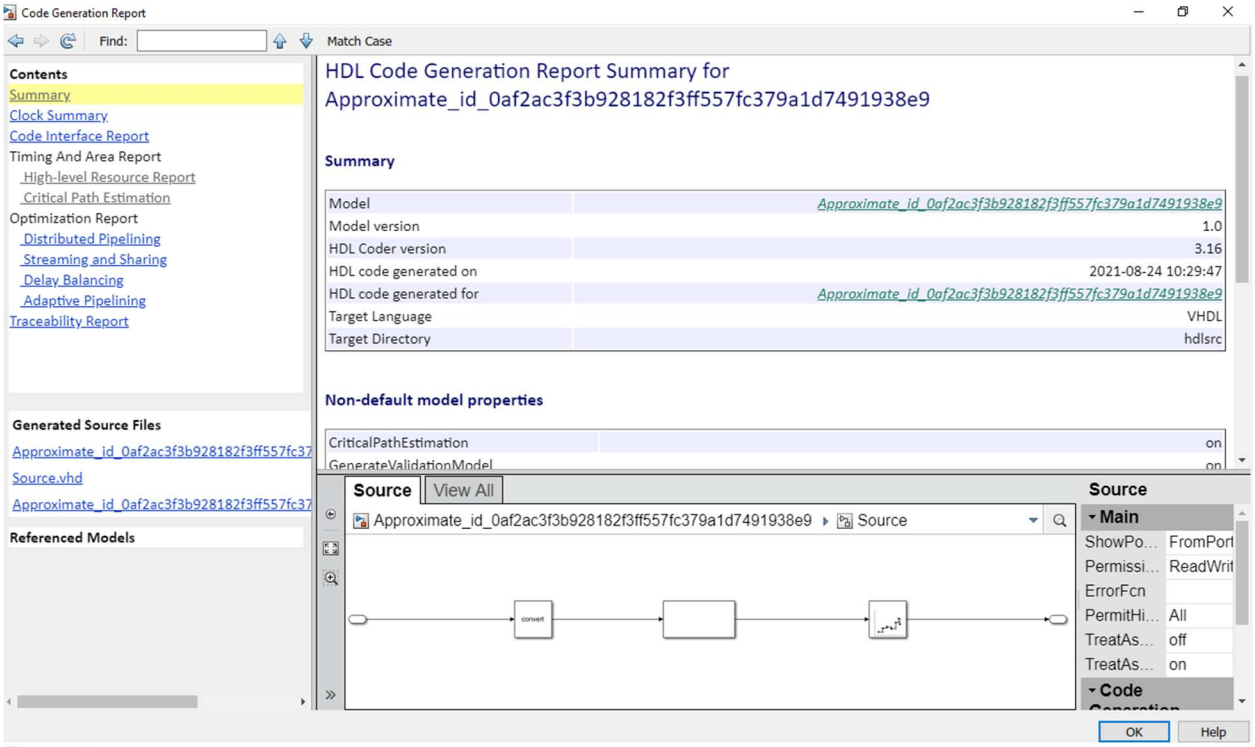
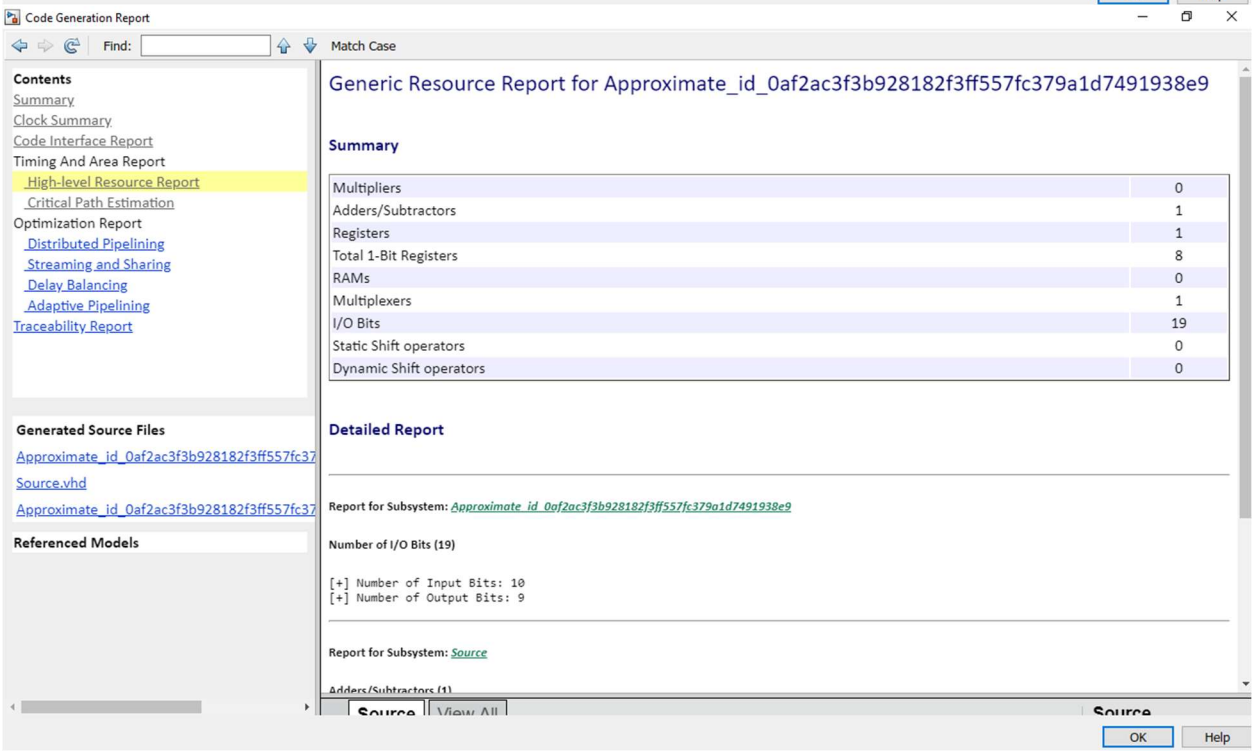
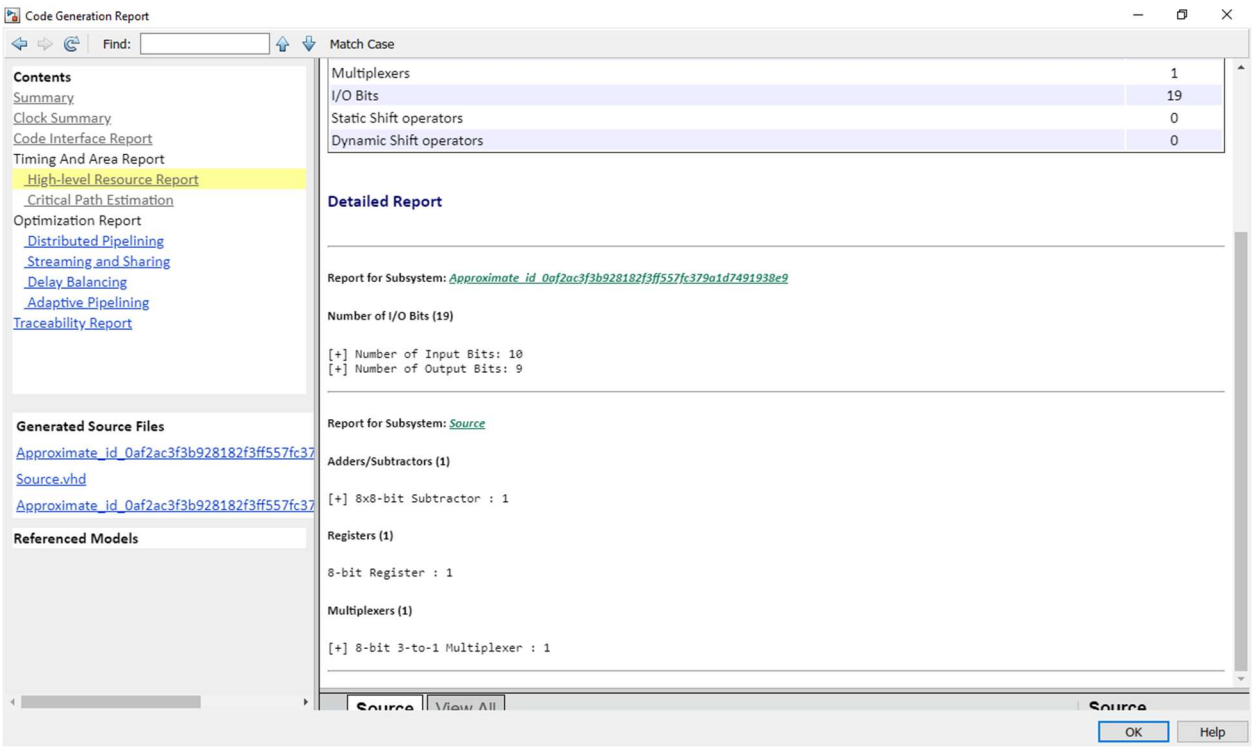

```
     to_signed(-16#7F#, 8), to_signed(-16#7F#, 8), to_signed(-16#7F#, 8),
to_signed(-16#7F#, 8),
     to_signed(-16#7F#, 8), to_signed(-16#7F#, 8), to_signed(-16#7F#, 8),
to_signed(-16#7E#, 8),
     to_signed(-16#7E#, 8), to_signed(-16#7E#, 8), to_signed(-16#7E#, 8),
to_signed(-16#7E#, 8),
     to_signed(-16#7D#, 8), to_signed(-16#7D#, 8), to_signed(-16#7C#, 8),
to_signed(-16#7C#, 8),
     to_signed(-16#7B#, 8), to_signed(-16#7B#, 8), to_signed(-16#7A#, 8),
to_signed(-16#79#, 8),
     to_signed(-16#78#, 8), to_signed(-16#78#, 8), to_signed(-16#76#, 8),
to_signed(-16#75#, 8),
     to_signed(-16#74#, 8), to_signed(-16#72#, 8), to_signed(-16#71#, 8),
to_signed(-16#6F#, 8),
     to_signed(-16#6D#, 8), to_signed(-16#6A#, 8), to_signed(-16#68#, 8),
to_signed(-16#65#, 8),
     to_signed(-16#61#, 8), to_signed(-16#5E#, 8), to_signed(-16#5A#, 8),
to_signed(-16#56#, 8),
     to_signed(-16#51#, 8), to_signed(-16#4C#, 8), to_signed(-16#47#, 8),
to_signed(-16#41#, 8),
     to_signed(-16#3B#, 8), to_signed(-16#35#, 8), to_signed(-16#2E#, 8),
to_signed(-16#27#, 8),
     to_signed(-16#1F#, 8), to_signed(-16#18#, 8), to_signed(-16#10#, 8),
to_signed(-16#08#, 8),
     to_signed(16#00#, 8), to_signed(16#08#, 8), to_signed(16#10#, 8),
to_signed(16#18#, 8), to_signed(16#1F#, 8),
     to_signed(16#27#, 8), to_signed(16#2E#, 8), to_signed(16#35#, 8),
to_signed(16#3B#, 8), to_signed(16#41#, 8),
     to_signed(16#47#, 8), to_signed(16#4C#, 8), to_signed(16#51#, 8),
to_signed(16#56#, 8), to_signed(16#5A#, 8),
     to_signed(16#5E#, 8), to_signed(16#61#, 8), to_signed(16#65#, 8),
to_signed(16#68#, 8), to_signed(16#6A#, 8),
     to_signed(16#6D#, 8), to_signed(16#6F#, 8), to_signed(16#71#, 8),
to_signed(16#72#, 8), to_signed(16#74#, 8),
     to_signed(16#75#, 8), to_signed(16#76#, 8), to_signed(16#78#, 8),
to_signed(16#78#, 8), to_signed(16#79#, 8),
     to_signed(16#7A#, 8), to_signed(16#7B#, 8), to_signed(16#7B#, 8),
to_signed(16#7C#, 8), to_signed(16#7C#, 8),
     to_signed(16#7D#, 8), to_signed(16#7D#, 8), to_signed(16#7E#, 8),
to_signed(16#7E#, 8), to_signed(16#7E#, 8),
     to_signed(16#7E#, 8), to_signed(16#7E#, 8), to_signed(16#7F#, 8),
to_signed(16#7F#, 8), to_signed(16#7F#, 8),
     to_signed(16#7F#, 8), to_signed(16#7F#, 8), to_signed(16#7F#, 8),
to_signed(16#7F#, 8), to_signed(16#7F#, 8),
     to_signed(16#7F#, 8), to_signed(16#7F#, 8), to_signed(16#7F#, 8),
to_signed(16#7F#, 8), to_signed(16#7F#, 8),
     to_signed(16#7F#, 8), to_signed(16#7F#, 8), to_signed(16#7F#, 8),
to_signed(16#7F#, 8), to_signed(16#7F#, 8),
     to_signed(16#7F#, 8), to_signed(16#7F#, 8), to_signed(16#7F#, 8),
to_signed(16#7F#, 8), to_signed(16#7F#, 8),
     to_signed(16#7F#, 8), to_signed(16#7F#, 8), to_signed(16#7F#, 8),
to_signed(16#7F#, 8), to_signed(16#7F#, 8),
     to_signed(16#7F#, 8), to_signed(16#7F#, 8), to_signed(16#7F#, 8),
to_signed(16#7F#, 8), to_signed(16#7F#, 8),
     to_signed(16#7F#, 8), to_signed(16#7F#, 8), to_signed(16#7F#, 8),
to_signed(16#7F#, 8));  -- sfix8 [159]
```

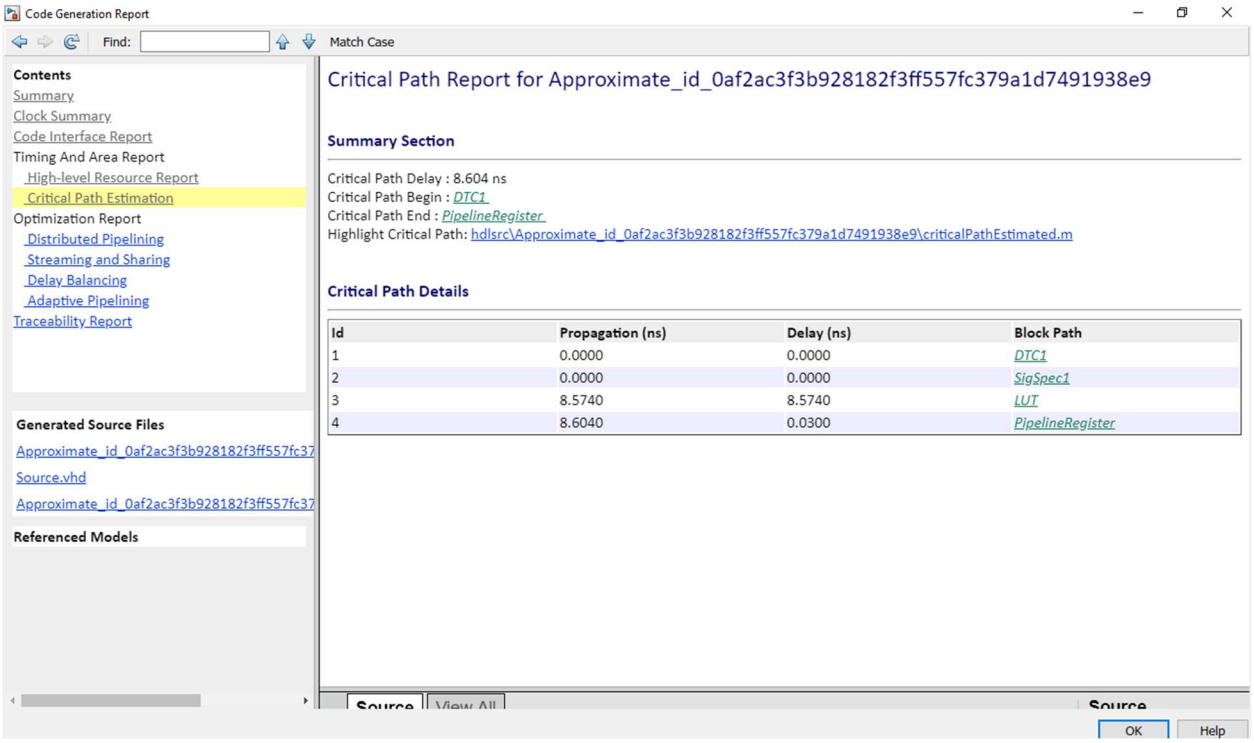
```
  -- Signals
  SIGNAL In1_signed                       : signed(7 DOWNTO 0);  -- sfix8_En4
  SIGNAL LUT_k                            : unsigned(7 DOWNTO 0);  -- ufix8
  SIGNAL LUT_sub_temp                     : signed(7 DOWNTO 0);  -- sfix8
  SIGNAL LUT_out1                         : signed(7 DOWNTO 0);  -- sfix8_En7
  SIGNAL LUT_out1_1                       : signed(7 DOWNTO 0) :=
to_signed(16#00#, 8);  -- sfix8_En7

BEGIN
  In1_signed <= signed(In1);

  LUT_sub_temp <= In1_signed - to_signed(-16#50#, 8);

  LUT_k <= to_unsigned(16#00#, 8) WHEN In1_signed <= to_signed(-16#50#, 8)
ELSE
      to_unsigned(16#9E#, 8) WHEN In1_signed >= to_signed(16#4E#, 8) ELSE
      unsigned(LUT_sub_temp);
  LUT_out1 <= LUT_data(to_integer(LUT_k));

  PipelineRegister_process : PROCESS (clk)
  BEGIN
    IF clk'EVENT AND clk = '1' THEN
      IF enb = '1' THEN
        LUT_out1_1 <= LUT_out1;
      END IF;
    END IF;
  END PROCESS PipelineRegister_process;


  Out1 <= std_logic_vector(LUT_out1_1);

END rtl;
```

Plots


Code Generation Report
Find:
Match Case
Contents
Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
Approximate_id_0af2ac3f3b928182f3ff557fc37
Source.vhd
Approximate_id_0af2ac3f3b928182f3ff557fc37
Referenced Models
HDL Code Generation Report Summary for
Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Summary
Model
Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Model version
1.0
HDL Coder version
3.16
HDL code generated on
2021-08-24 10:29:47
HDL code generated for
Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Target Language
VHDL
Target Directory
hdlsrc
Non-default model properties
CriticalPathEstimation
on
Source
View All
Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Source
convert
Source
Main
ShowPo...
FromPort
Permissi...
ReadWrit
ErrorFcn
PermitHi...
All
TreatAs...
off
TreatAs...
on
Code
OK
Help


Code Generation Report
Find:
Match Case
Contents
Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
Approximate_id_0af2ac3f3b928182f3ff557fc37
Source.vhd
Approximate_id_0af2ac3f3b928182f3ff557fc37
Referenced Models
Generic Resource Report for Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Summary
Multipliers
0
Adders/Subtractors
1
Registers
1
Total 1-Bit Registers
8
RAMs
0
Multiplexers
1
I/O Bits
19
Static Shift operators
0
Dynamic Shift operators
0
Detailed Report
Report for Subsystem: Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Number of I/O Bits (19)
[+] Number of Input Bits: 10
[+] Number of Output Bits: 9
Report for Subsystem: Source
Adders/Subtractors (1)
Source
View All
Source
OK
Help


Code Generation Report
Find:
Match Case
Contents
Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
Approximate_id_0af2ac3f3b928182f3ff557fc37
Source.vhd
Approximate_id_0af2ac3f3b928182f3ff557fc37
Referenced Models
Multiplexers 1
I/O Bits 19
Static Shift operators 0
Dynamic Shift operators 0
Detailed Report
Report for Subsystem: Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Number of I/O Bits (19)
[+] Number of Input Bits: 10
[+] Number of Output Bits: 9
Report for Subsystem: Source
Adders/Subtractors (1)
[+] 8x8-bit Subtractor : 1
Registers (1)
8-bit Register : 1
Multiplexers (1)
[+] 8-bit 3-to-1 Multiplexer : 1
Source
View All
Source
OK
Help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Clock Summary
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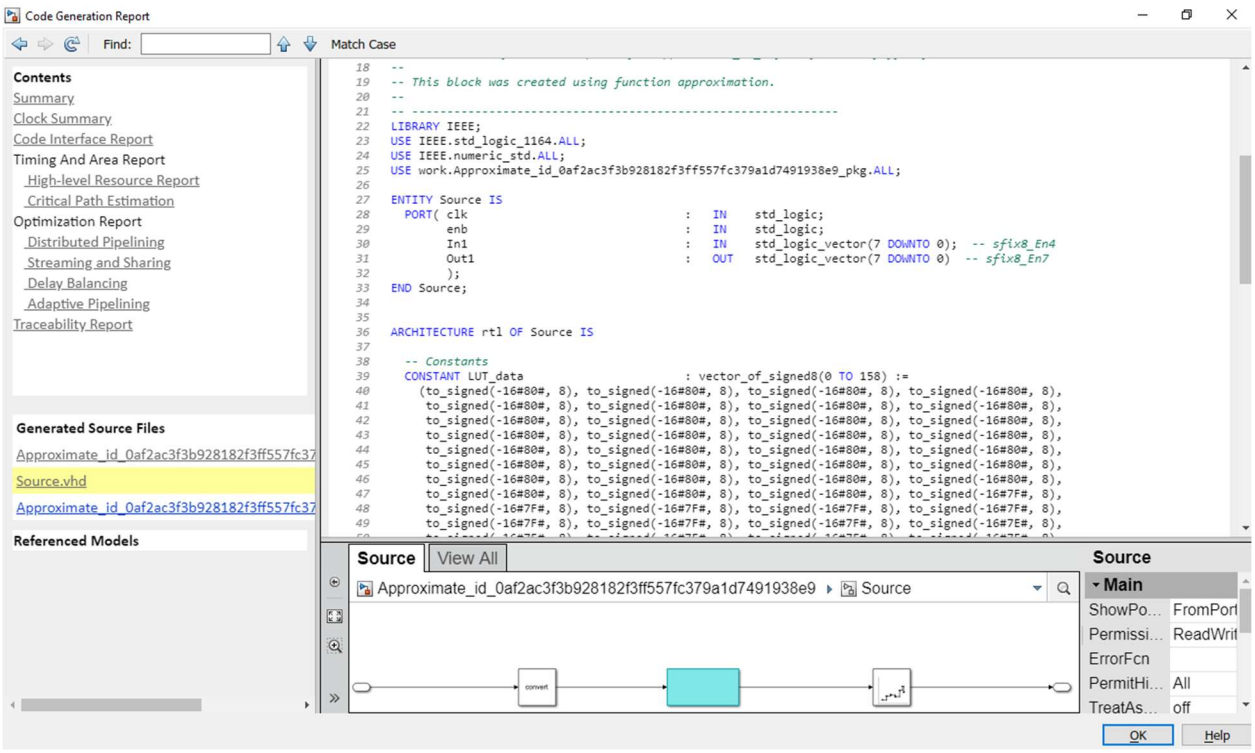
Traceability Report
Generated Source Files
Approximate_id_0af2ac3f3b928182f3ff557fc37
Source.vhd
Approximate_id_0af2ac3f3b928182f3ff557fc37
Referenced Models
Critical Path Report for Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Summary Section
Critical Path Delay : 8.604 ns
Critical Path Begin : DTC1
Critical Path End : PipelineRegister
Highlight Critical Path: hdlsrc\Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9\criticalPathEstimated.m
Critical Path Details
Id Propagation (ns) Delay (ns) Block Path
1 0.0000 0.0000 DTC1
2 0.0000 0.0000 SigSpec1
3 8.5740 8.5740 LUT
4 8.6040 0.0300 PipelineRegister
Source
View All
Source
OK
Help


Code Generation Report
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Timing And Area Report
High-level Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
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Traceability Report
Generated Source Files
Approximate_id_0af2ac3f3b928182f3ff557fc37
Source.vhd
Approximate_id_0af2ac3f3b928182f3ff557fc37
Referenced Models
-- This block was created using function approximation.
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;
USE work.Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9_pkg.ALL;
ENTITY Source IS
PORT(clk : IN std_logic;
enb : IN std_logic;
In1 : IN std_logic_vector(7 DOWNTO 0); -- sfix8_En4
Out1 : OUT std_logic_vector(7 DOWNTO 0) -- sfix8_En7
);
END Source;
ARCHITECTURE rtl OF Source IS
-- Constants
CONSTANT LUT_data : vector_of_signed8(0 TO 158) :=
Source
View All
Approximate_id_0af2ac3f3b928182f3ff557fc379a1d7491938e9
Source
convert
Source
Main
ShowPo...
FromPort
Permissi...
ReadWrit
ErrorFcn
PermitHi...
All
TreatAs...
off
OK
Help