Contents

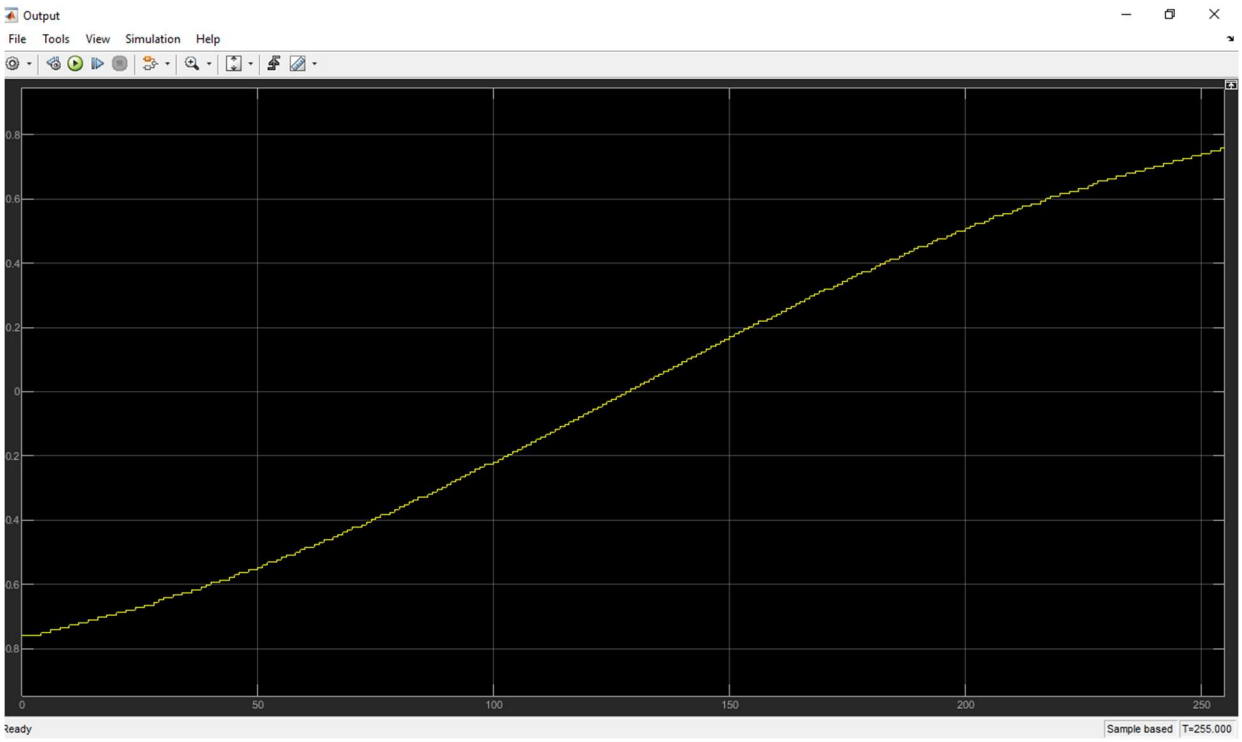
VHDL

```
-- -------------------------------------------------------------
--
-- File Name:
hdlsrc\ModelWithApproximation_20210821T210314460\ModelWithApproximation_20210
821T210314460.vhd
-- Created: 2021-08-21 21:51:33
--
-- Generated by MATLAB 9.8 and HDL Coder 3.16
--
--
-- -------------------------------------------------------------
-- Rate and Clocking Details
-- -------------------------------------------------------------
-- Model base rate: 1
-- Target subsystem base rate: 1
--
-- -------------------------------------------------------------



-- -------------------------------------------------------------
--
-- Module: ModelWithApproximation_20210821T210314460
-- Source Path: ModelWithApproximation_20210821T210314460
-- Hierarchy Level: 0
--
-- -------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

ENTITY ModelWithApproximation_20210821T210314460 IS
END ModelWithApproximation_20210821T210314460;


ARCHITECTURE rtl OF ModelWithApproximation_20210821T210314460 IS

BEGIN
  -- Open scope to see simulation results


END rtl;
```

Design

```
function []=tanh_lookup()
    problem = FunctionApproximation.Problem('tanh');
    problem.InputTypes =  numerictype(1,8,7);
    problem.InputLowerBounds = -5;
    problem.InputUpperBounds = 5;
    problem.OutputType = numerictype(1,8,7);
    problem.Options.BreakpointSpecification='EvenSpacing';
    problem.Options.WordLengths=8; %[8, 16, 32]
    problem.Options.OnCurveTableValues=1;
    solution = solve(problem);
    compare(solution);
    approximate(solution);
    memory = totalmemoryusage(solution);
    disp(memory);
end
```

Plots



tanh_lookup.m

```
function []=tanh_lookup()
    problem = FunctionApproximation.Problem('tanh');
    problem.InputTypes =  numerictype(1,8,7);
    problem.InputLowerBounds = -5;
    problem.InputUpperBounds = 5;
    problem.OutputType = numerictype(1,8,7);
    problem.Options.BreakpointSpecification='EvenSpacing';
    problem.Options.WordLengths=8; %[8, 16, 32]
    problem.Options.OnCurveTableValues=0;
    solution = solve(problem);
    compare(solution);
    approximate(solution);
end
```

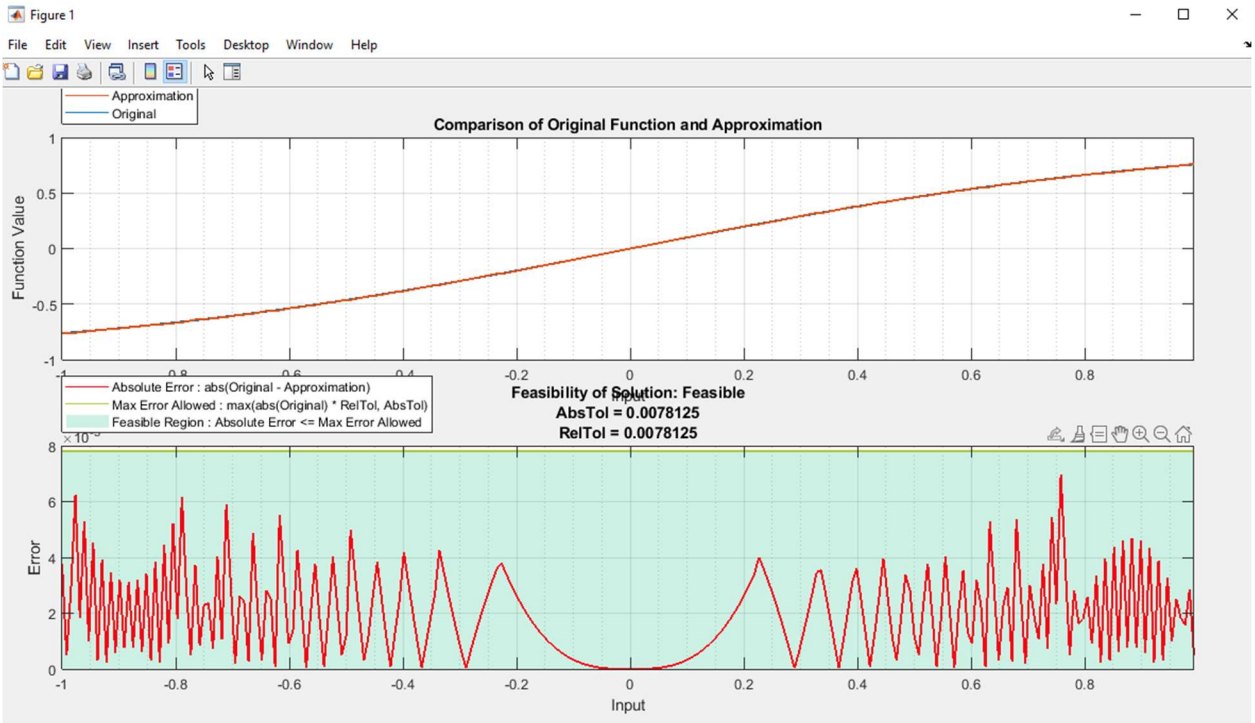
Command Window

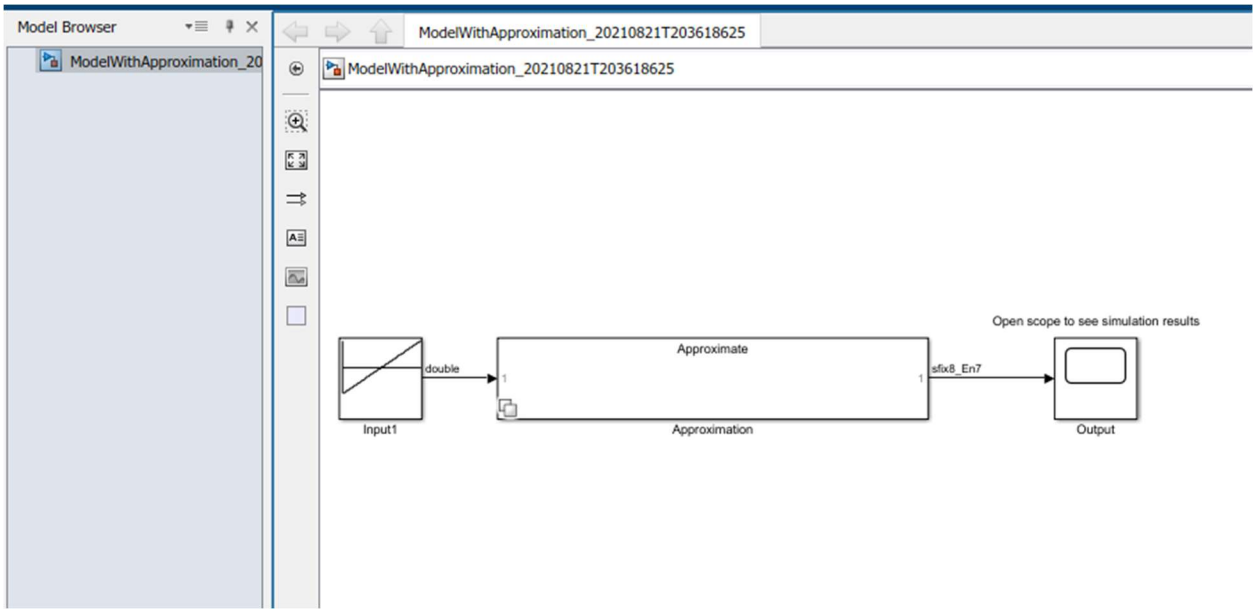
ID	Memory (bits)	Feasible	Table Size	Breakpoints WLs	TableData WL	BreakpointSpecification	Error(Max,Current)
10	432	0	52	8	8	EvenSpacing	7.812500e-03, 1.088633e-02
11	704	0	86	8	8	EvenSpacing	7.812500e-03, 1.123616e-02
12	80	0	8	8	8	EvenSpacing	7.812500e-03, 1.764247e-02
13	72	0	7	8	8	EvenSpacing	7.812500e-03, 1.796145e-02
14	1040	1	128	8	8	EvenPow2Spacing	7.812500e-03, 6.974172e-03

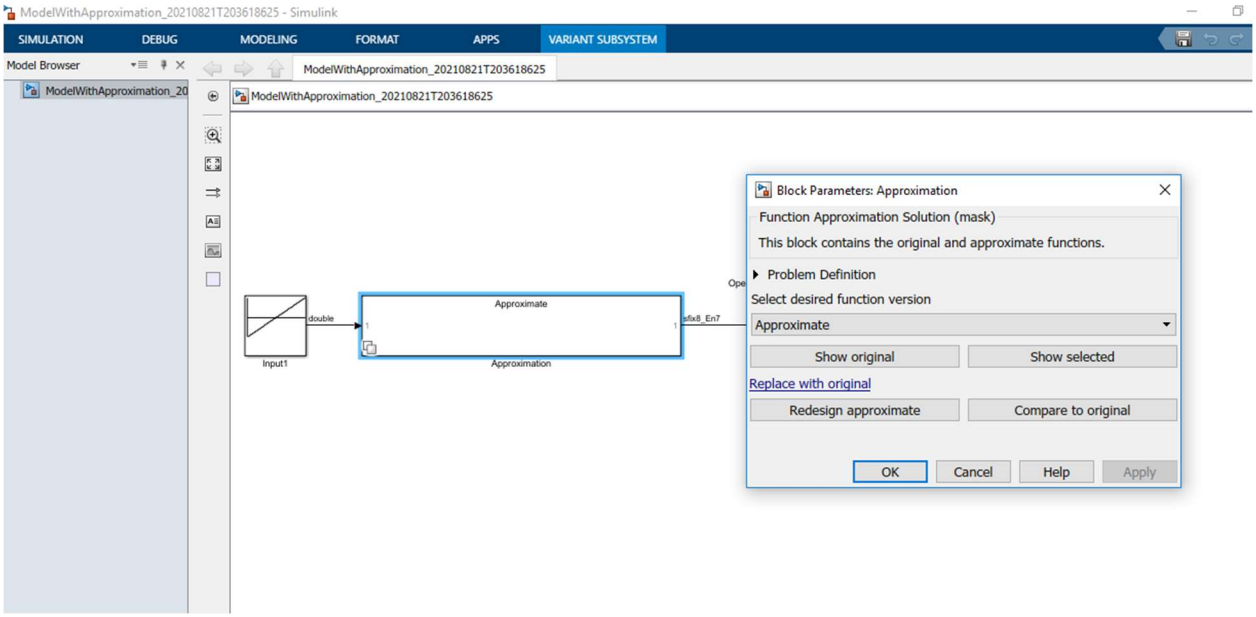
Best Solution

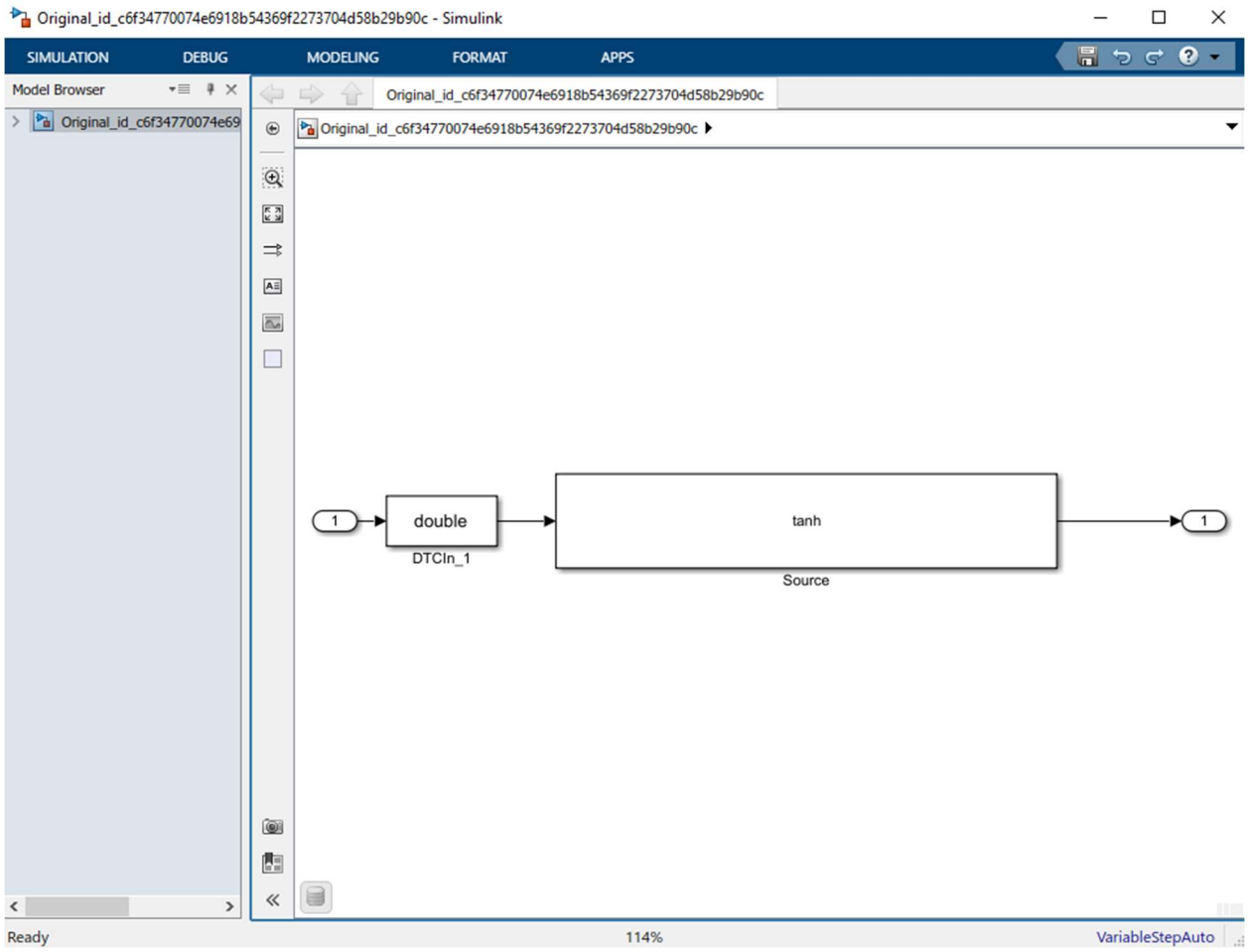
ID	Memory (bits)	Feasible	Table Size	Breakpoints WLs	TableData WL	BreakpointSpecification	Error(Max,Current)
14	1040	1	128	8	8	EvenPow2Spacing	7.812500e-03, 6.974172e-03

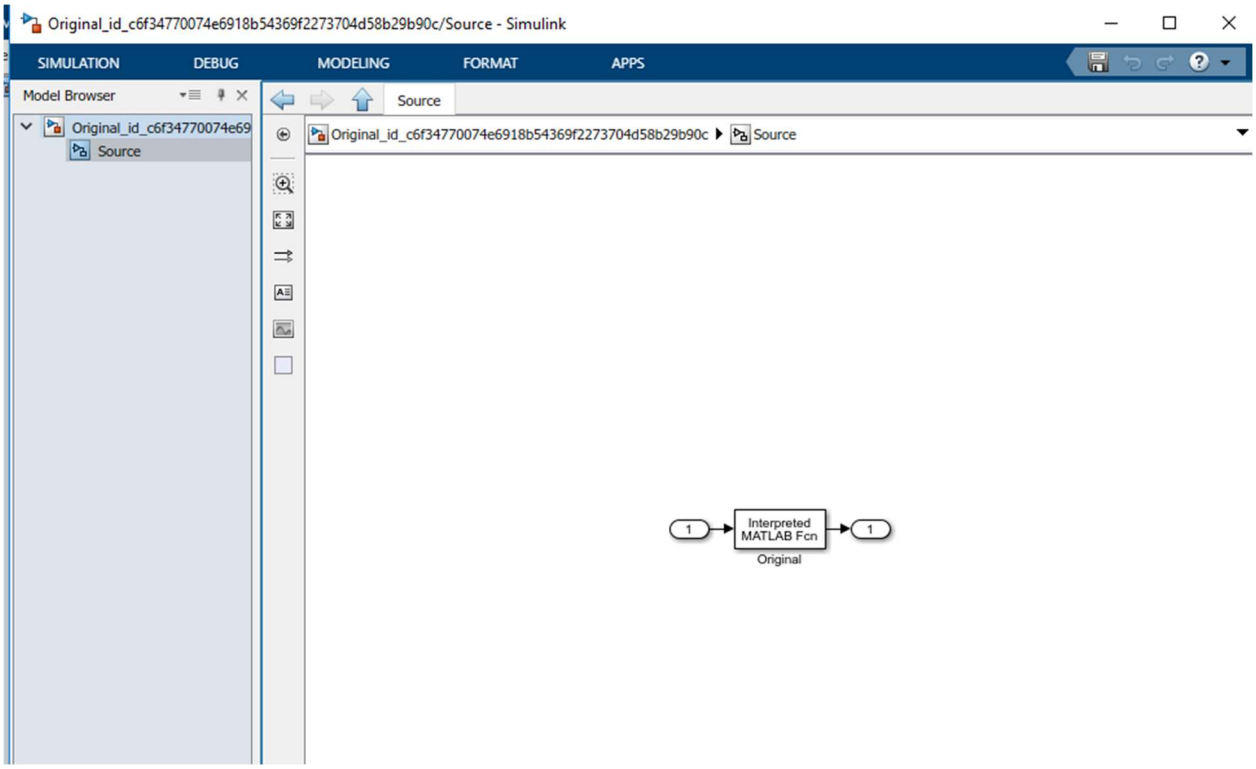
fx >>

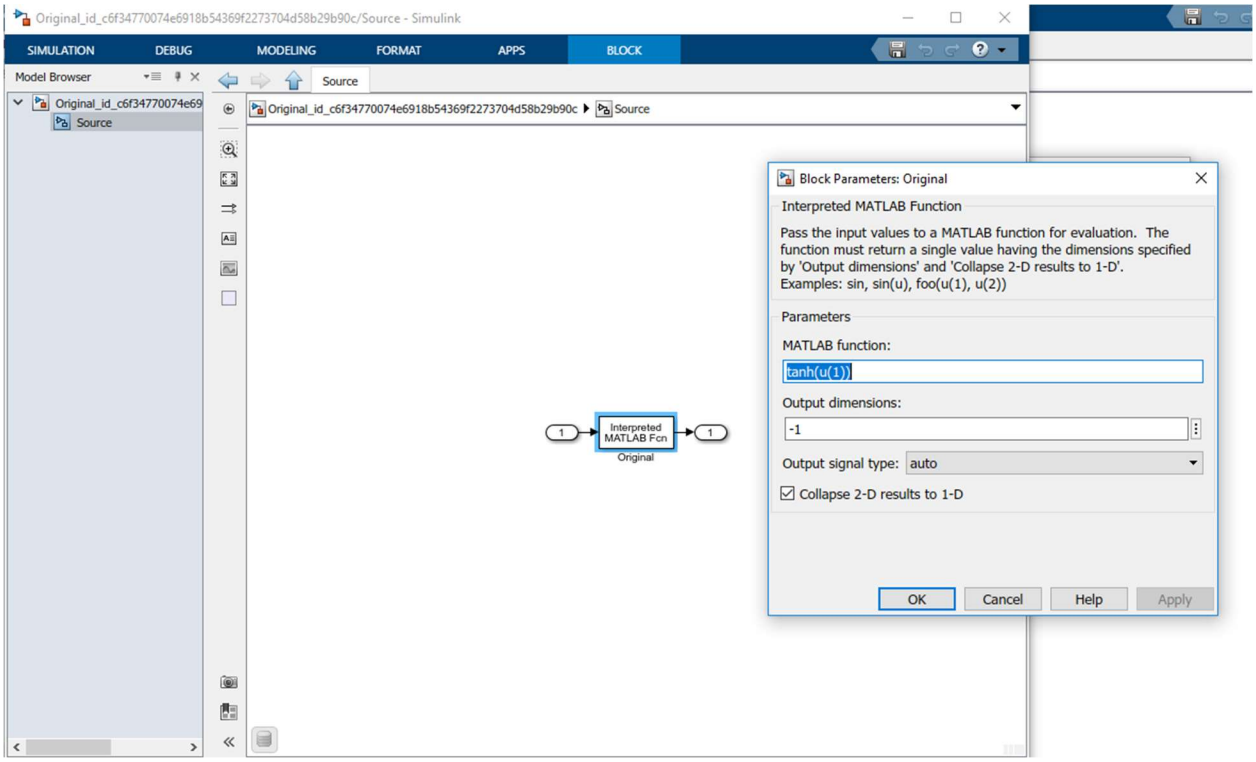


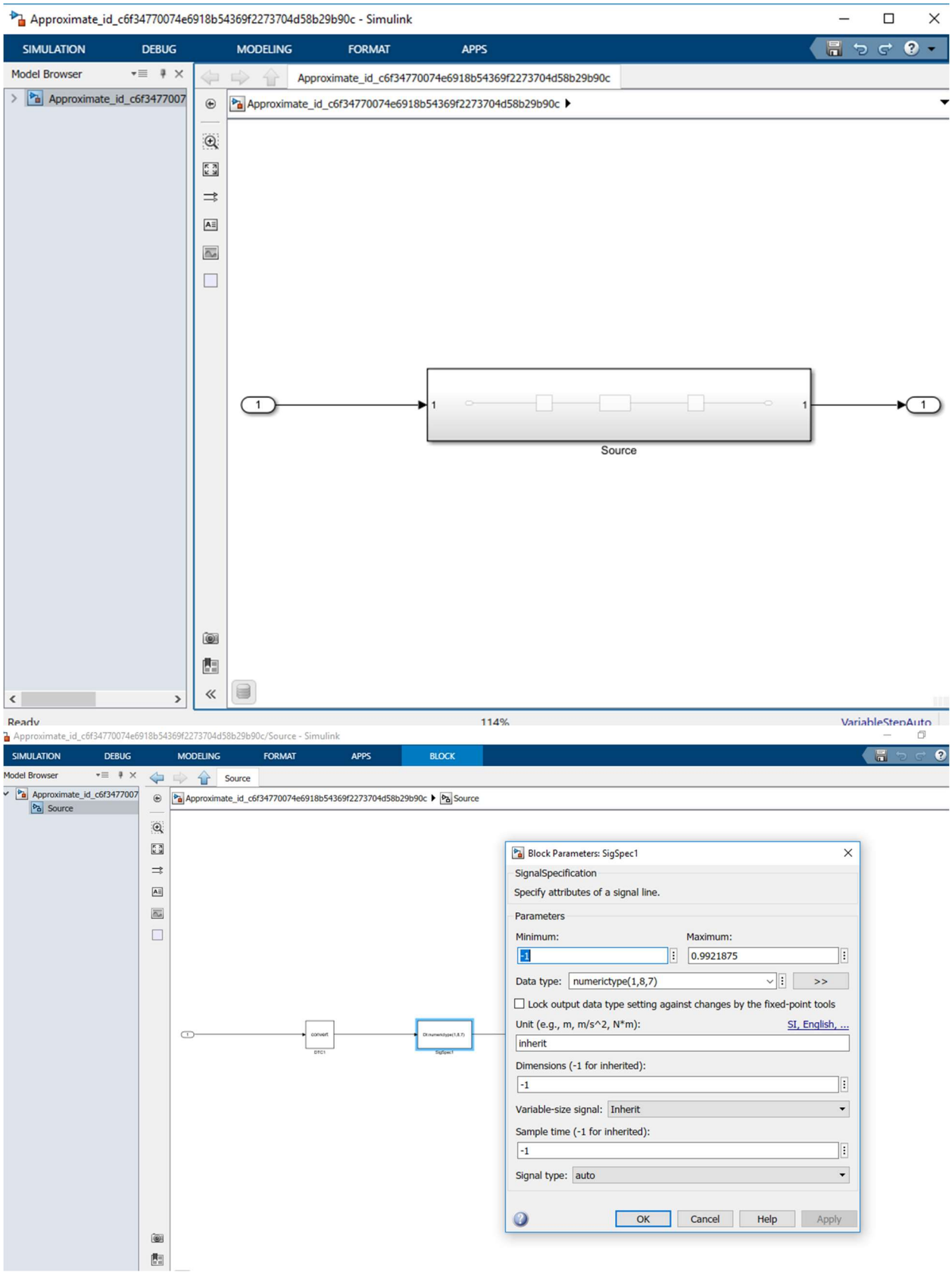

Model Browser
ModelWithApproximation_20
ModelWithApproximation_20210821T203618625
ModelWithApproximation_20210821T203618625
Open scope to see simulation results
Approximate
double
sfix8_En7
Input1
Approximation
Output

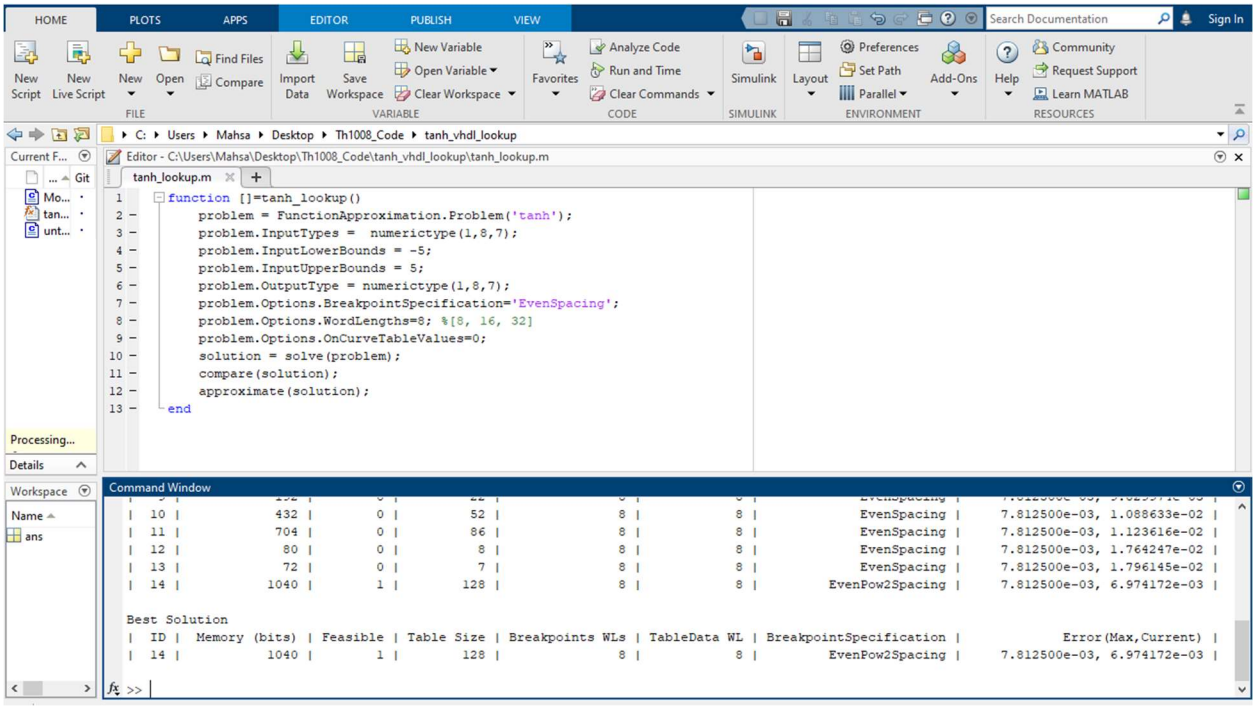

ModelWithApproximation_20210821T203618625 - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
VARIANT SUBSYSTEM
Model Browser
ModelWithApproximation_20
ModelWithApproximation_20210821T203618625
ModelWithApproximation_20210821T203618625
Approximate
double
sfix8_En7
Input1
Approximation
Block Parameters: Approximation
Function Approximation Solution (mask)
This block contains the original and approximate functions.
Problem Definition
Select desired function version
Approximate
Show original
Show selected
Replace with original
Redesign approximate
Compare to original
OK
Cancel
Help
Apply

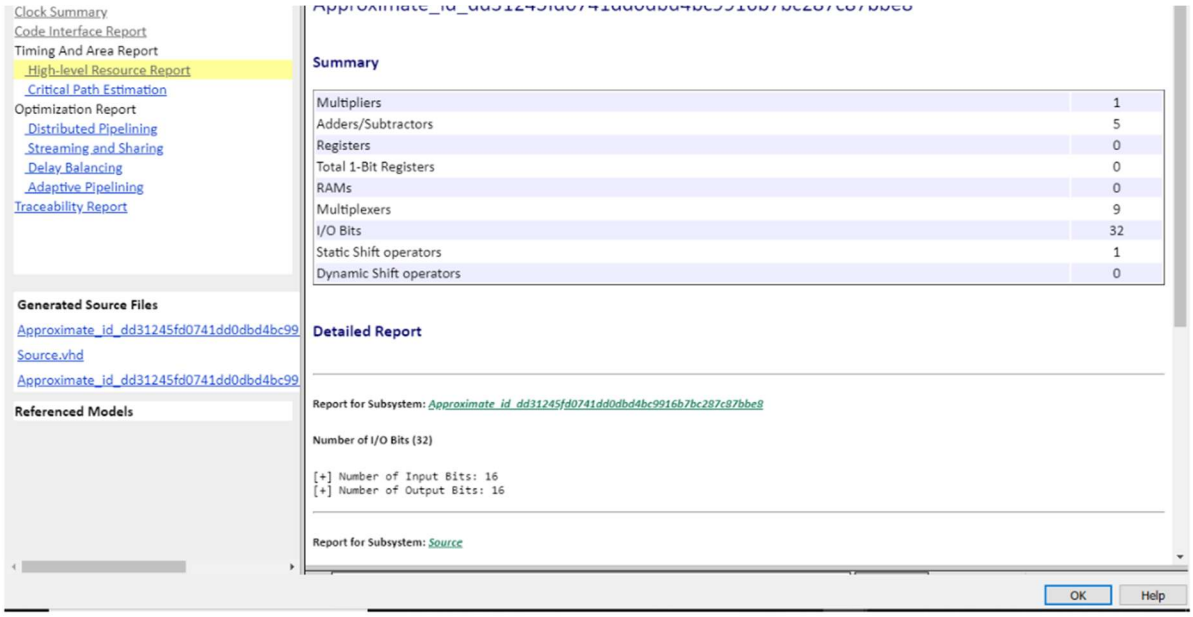

Original_id_c6f34770074e6918b54369f2273704d58b29b90c - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
Model Browser
Original_id_c6f34770074e69
Original_id_c6f34770074e6918b54369f2273704d58b29b90c
Original_id_c6f34770074e6918b54369f2273704d58b29b90c
1
double
DTCIn_1
tanh
Source
1
Ready
114%
VariableStepAuto

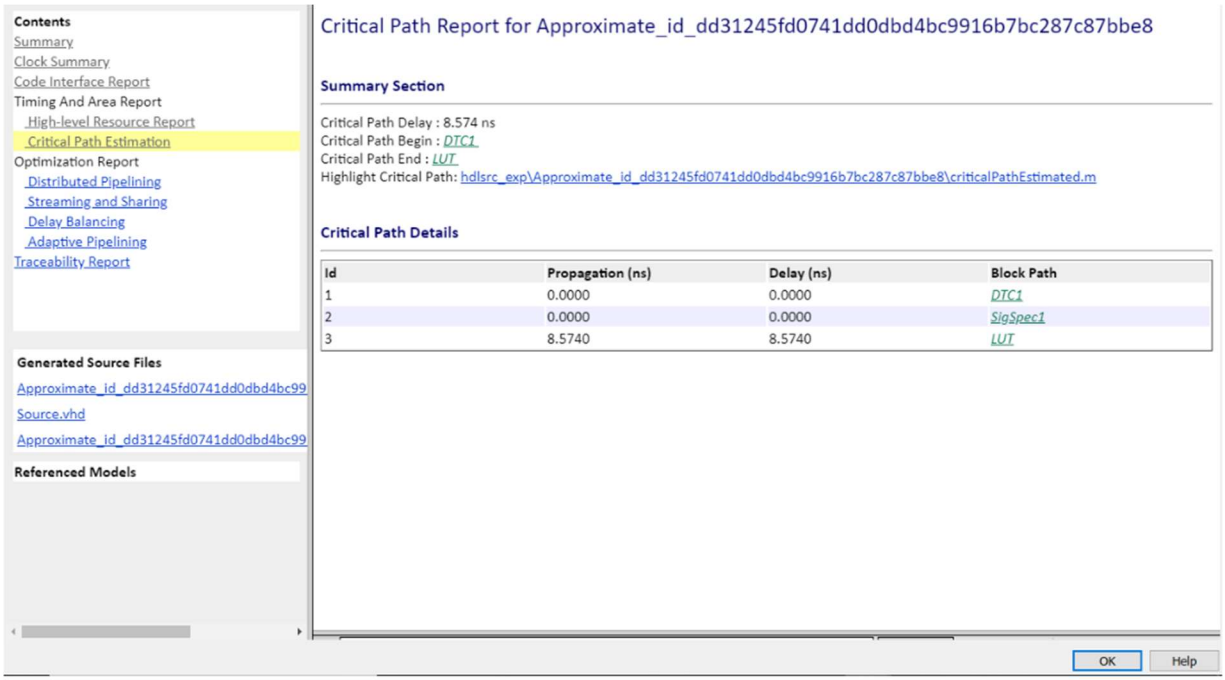

Original_id_c6f34770074e6918b54369f2273704d58b29b90c/Source - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
Model Browser
Original_id_c6f34770074e69
Source
Original_id_c6f34770074e6918b54369f2273704d58b29b90c
Source
1
Interpreted MATLAB Fcn
1
Original

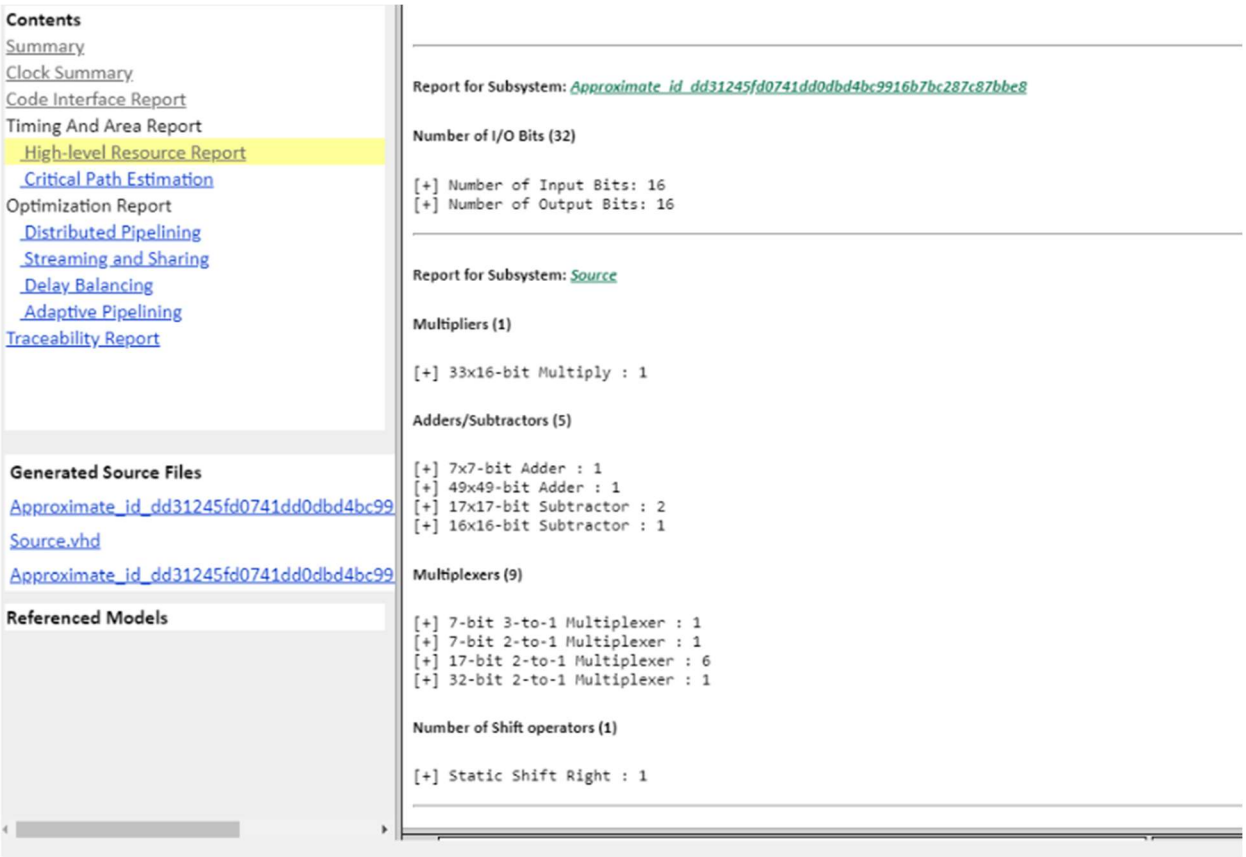

Original_id_c6f34770074e6918b54369f2273704d58b29b90c/Source - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
BLOCK
Model Browser
Original_id_c6f34770074e69
Source
Original_id_c6f34770074e6918b54369f2273704d58b29b90c
Source
1
Interpreted MATLAB Fcn
1
Original
Block Parameters: Original
Interpreted MATLAB Function
Pass the input values to a MATLAB function for evaluation. The function must return a single value having the dimensions specified by 'Output dimensions' and 'Collapse 2-D results to 1-D'.
Examples: sin, sin(u), foo(u(1), u(2))
Parameters
MATLAB function:
tanh(u(1))
Output dimensions:
-1
Output signal type:
auto
Collapse 2-D results to 1-D
OK
Cancel
Help
Apply


Approximate_id_c6f34770074e6918b54369f2273704d58b29b90c - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
Model Browser
Approximate_id_c6f3477007
Approximate_id_c6f34770074e6918b54369f2273704d58b29b90c
Approximate_id_c6f34770074e6918b54369f2273704d58b29b90c
1
1
1
1
Source
Ready
114%
VariableStepAuto
Approximate_id_c6f34770074e6918b54369f2273704d58b29b90c/Source - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
BLOCK
Model Browser
Approximate_id_c6f3477007
Source
Source
Approximate_id_c6f34770074e6918b54369f2273704d58b29b90c
Source
Block Parameters: SigSpec1
SignalSpecification
Specify attributes of a signal line.
Parameters
Minimum:
Maximum:
-1
0.9921875
Data type:
numerictype(1,8,7)
>>
Lock output data type setting against changes by the fixed-point tools
Unit (e.g., m, m/s^2, N*m):
SI, English, ...
inherit
Dimensions (-1 for inherited):
-1
Variable-size signal:
Inherit
Sample time (-1 for inherited):
-1
Signal type:
auto
OK
Cancel
Help
Apply


HOME
PLOTS
APPS
EDITOR
PUBLISH
VIEW
Search Documentation
Sign In
New Script
New Live Script
New
Open
Find Files
Compare
Import Data
Save Workspace
New Variable
Open Variable
Clear Workspace
Favorites
Analyze Code
Run and Time
Clear Commands
Simulink
Layout
Preferences
Set Path
Parallel
Add-Ons
Help
Community
Request Support
Learn MATLAB
FILE
VARIABLE
CODE
SIMULINK
ENVIRONMENT
RESOURCES
C: ▸ Users ▸ Mahsa ▸ Desktop ▸ Th1008_Code ▸ tanh_vhdl_lookup
Editor - C:\Users\Mahsa\Desktop\Th1008_Code\tanh_vhdl_lookup\tanh_lookup.m
tanh_lookup.m
1 function []=tanh_lookup()
2 problem = FunctionApproximation.Problem('tanh');
3 problem.InputTypes = numerictype(1,8,7);
4 problem.InputLowerBounds = -5;
5 problem.InputUpperBounds = 5;
6 problem.OutputType = numerictype(1,8,7);
7 problem.Options.BreakpointSpecification='EvenSpacing';
8 problem.Options.WordLengths=8; %[8, 16, 32]
9 problem.Options.OnCurveTableValues=0;
10 solution = solve(problem);
11 compare(solution);
12 approximate(solution);
13 end
Processing...
Details
Workspace
Name
ans
Command Window
10	432	0	52	8	8	EvenSpacing	7.812500e-03, 1.088633e-02
11	704	0	86	8	8	EvenSpacing	7.812500e-03, 1.123616e-02
12	80	0	8	8	8	EvenSpacing	7.812500e-03, 1.764247e-02
13	72	0	7	8	8	EvenSpacing	7.812500e-03, 1.796145e-02
14	1040	1	128	8	8	EvenPow2Spacing	7.812500e-03, 6.974172e-03
Best Solution
ID	Memory (bits)	Feasible	Table Size	Breakpoints WLs	TableData WL	BreakpointSpecification	Error(Max,Current)
14	1040	1	128	8	8	EvenPow2Spacing	7.812500e-03, 6.974172e-03
>>


Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
Approximate_id_dd31245fd0741dd0dbd4bc99
Source.vhd
Approximate_id_dd31245fd0741dd0dbd4bc99
Referenced Models
Summary
Multipliers 1
Adders/Subtractors 5
Registers 0
Total 1-Bit Registers 0
RAMs 0
Multiplexers 9
I/O Bits 32
Static Shift operators 1
Dynamic Shift operators 0
Detailed Report
Report for Subsystem: Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
Number of I/O Bits (32)
[+] Number of Input Bits: 16
[+] Number of Output Bits: 16
Report for Subsystem: Source
OK
Help


Contents
Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
Approximate_id_dd31245fd0741dd0dbd4bc99
Source.vhd
Approximate_id_dd31245fd0741dd0dbd4bc99
Referenced Models
Critical Path Report for Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
Summary Section
Critical Path Delay : 8.574 ns
Critical Path Begin : DTC1
Critical Path End : LUT
Highlight Critical Path: hdlsrc_exp\Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8\criticalPathEstimated.m
Critical Path Details
Id
Propagation (ns)
Delay (ns)
Block Path
1
0.0000
0.0000
DTC1
2
0.0000
0.0000
SigSpec1
3
8.5740
8.5740
LUT
OK
Help


Contents
Summary
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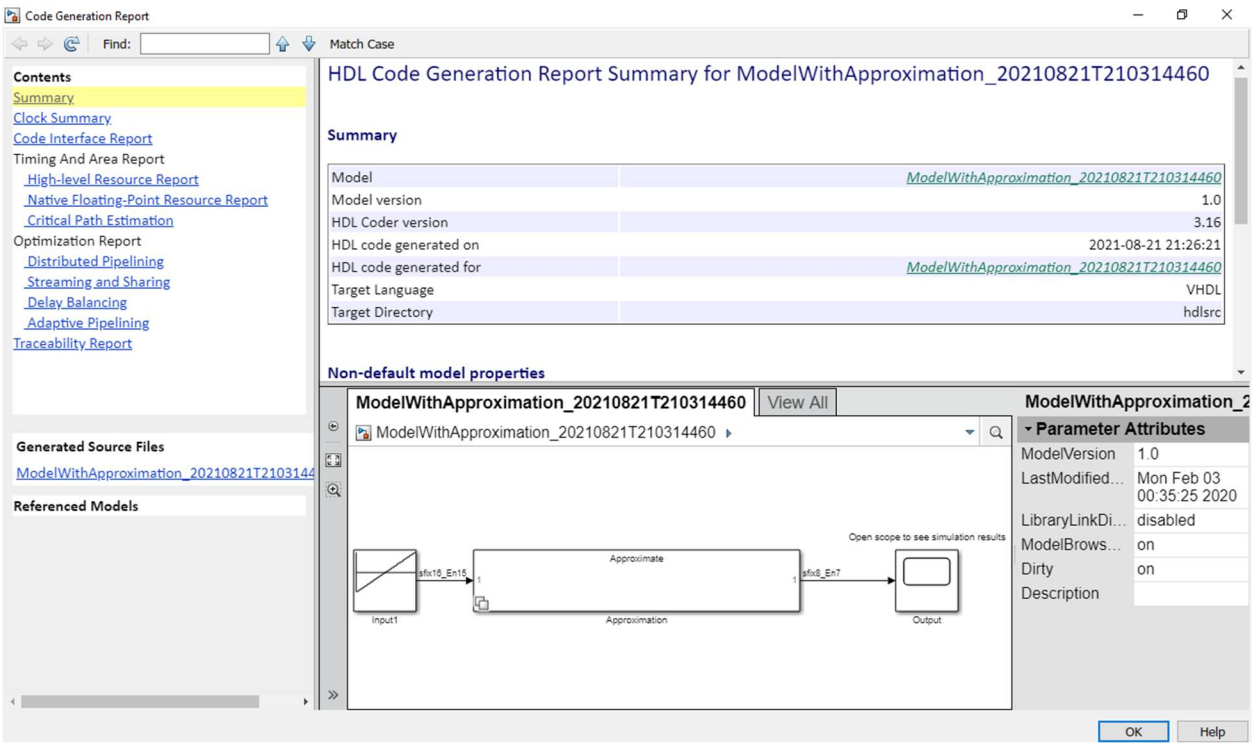
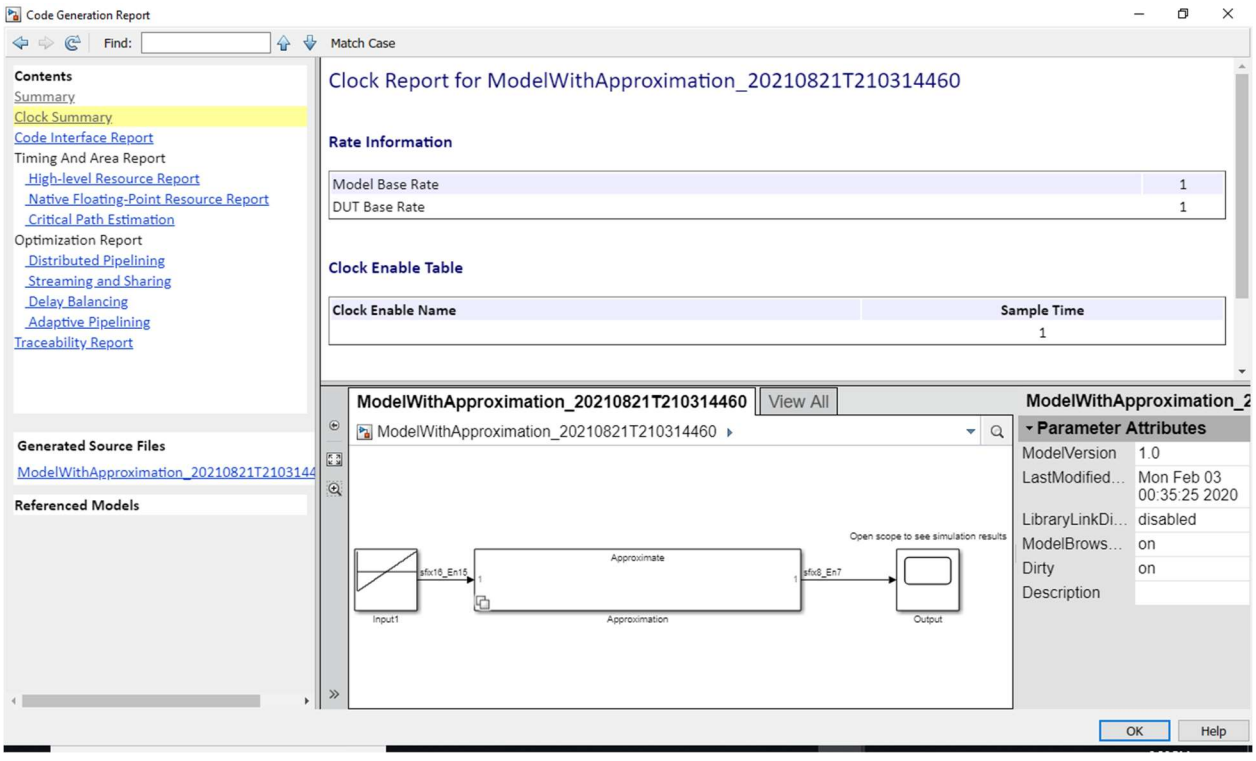
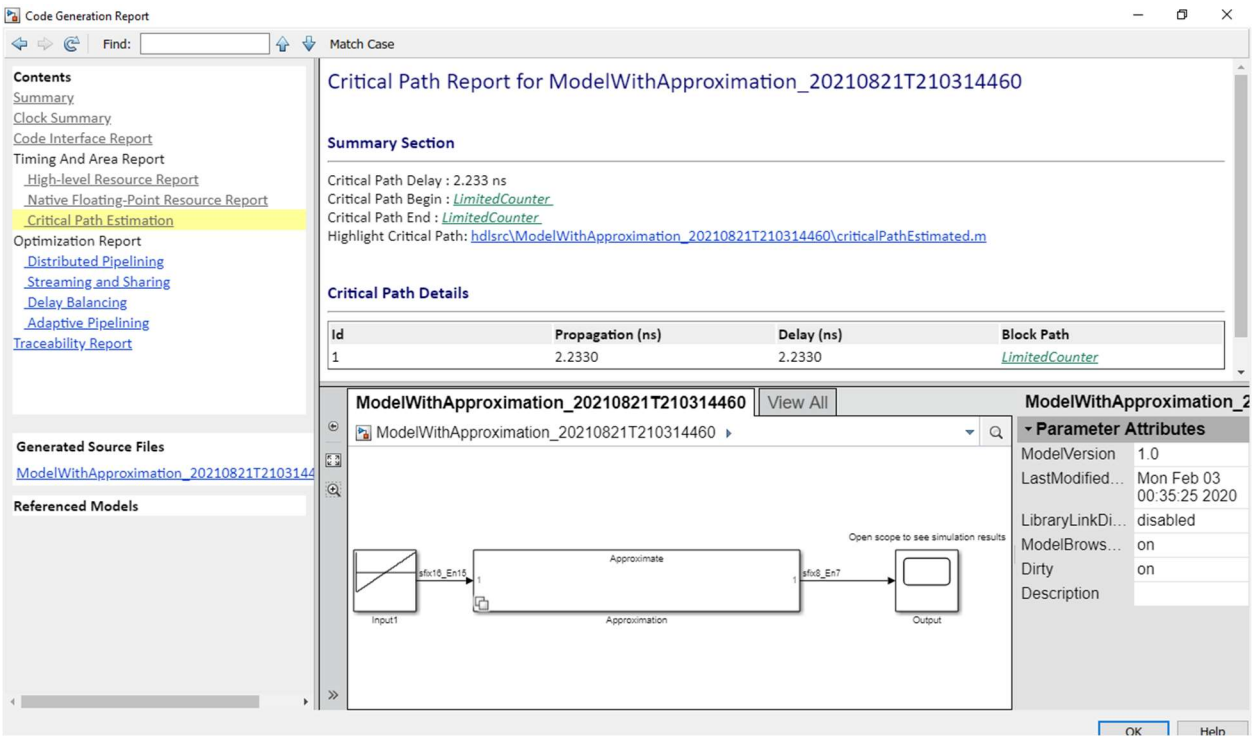
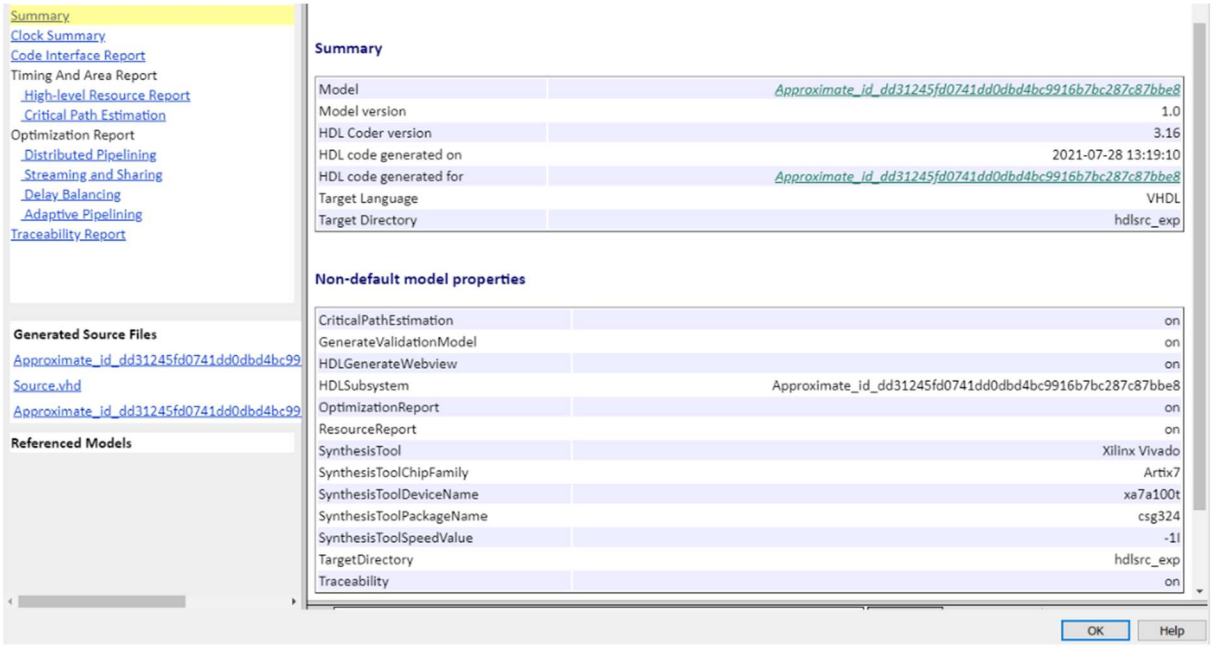
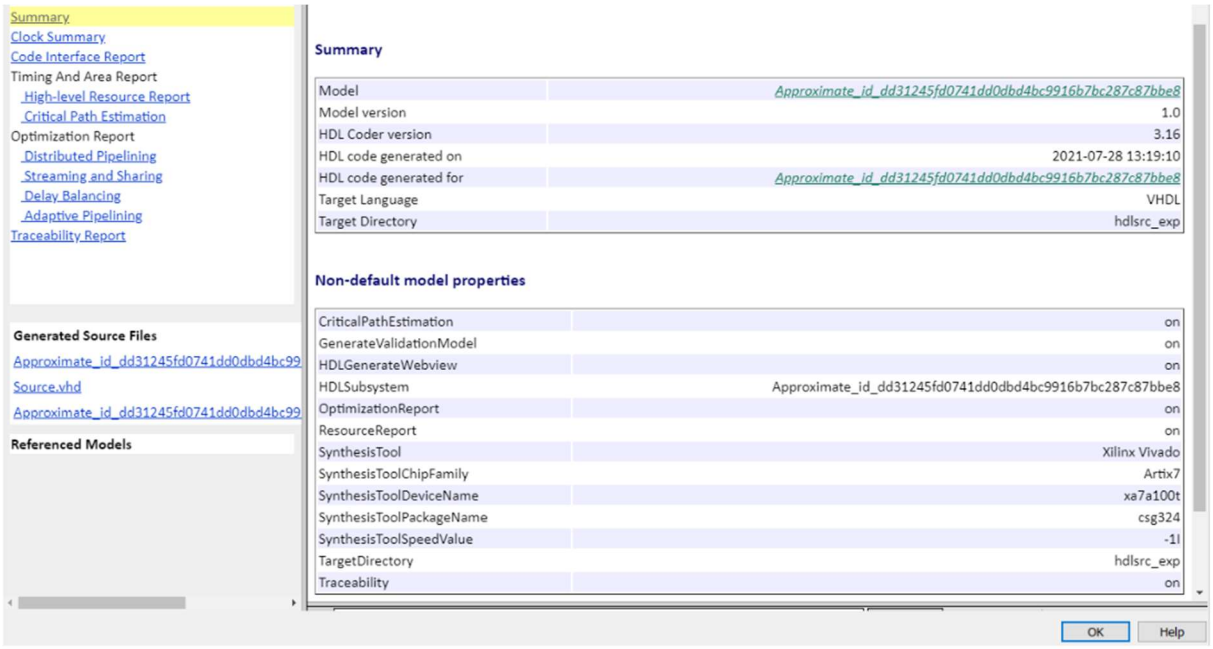
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
Approximate_id_dd31245fd0741dd0dbd4bc99
Source.vhd
Approximate_id_dd31245fd0741dd0dbd4bc99
Referenced Models
Report for Subsystem: Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
Number of I/O Bits (32)
[+] Number of Input Bits: 16
[+] Number of Output Bits: 16
Report for Subsystem: Source
Multipliers (1)
[+] 33x16-bit Multiply : 1
Adders/Subtractors (5)
[+] 7x7-bit Adder : 1
[+] 49x49-bit Adder : 1
[+] 17x17-bit Subtractor : 2
[+] 16x16-bit Subtractor : 1
Multiplexers (9)
[+] 7-bit 3-to-1 Multiplexer : 1
[+] 7-bit 2-to-1 Multiplexer : 1
[+] 17-bit 2-to-1 Multiplexer : 6
[+] 32-bit 2-to-1 Multiplexer : 1
Number of Shift operators (1)
[+] Static Shift Right : 1

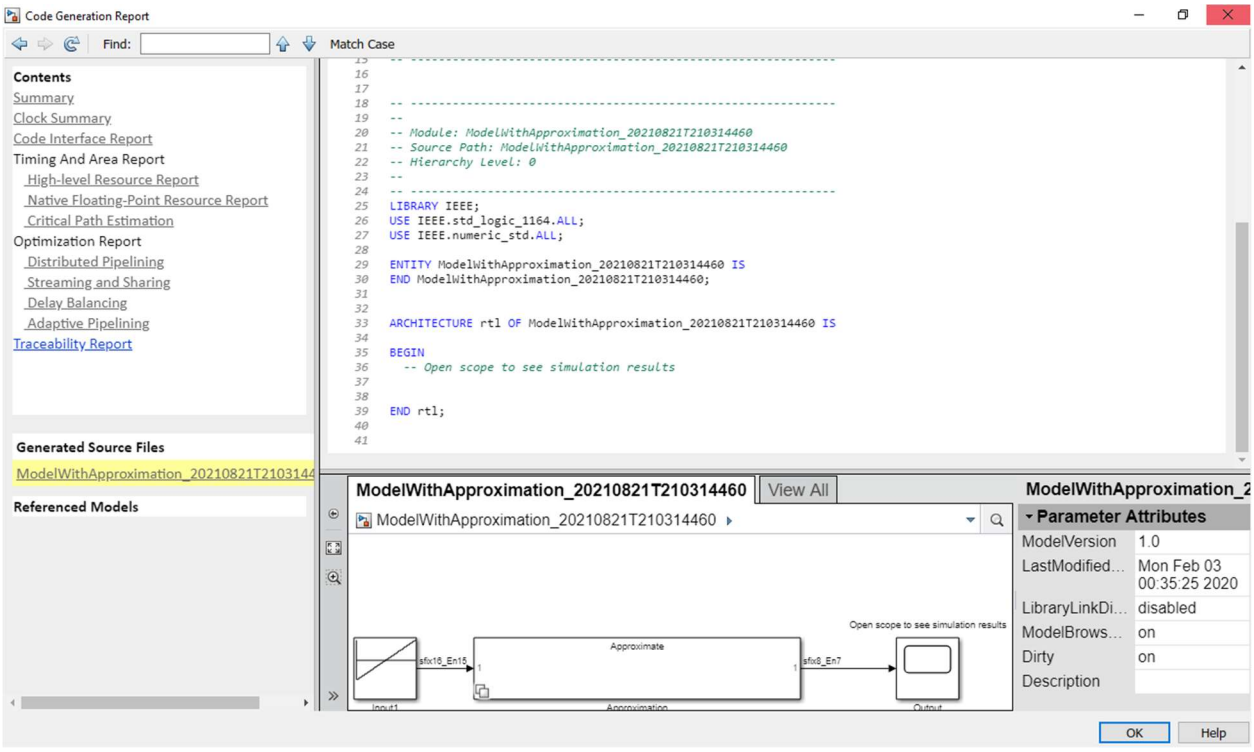

Code Generation Report
Find:
Match Case
Contents
Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Native Floating-Point Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
ModelWithApproximation_20210821T2103144
Referenced Models
HDL Code Generation Report Summary for ModelWithApproximation_20210821T210314460
Summary
Model
ModelWithApproximation_20210821T210314460
Model version
1.0
HDL Coder version
3.16
HDL code generated on
2021-08-21 21:26:21
HDL code generated for
ModelWithApproximation_20210821T210314460
Target Language
VHDL
Target Directory
hdlsrc
Non-default model properties
ModelWithApproximation_20210821T210314460
View All
ModelWithApproximation_20210821T210314460
Open scope to see simulation results
sfix16_En15
Approximate
sfix8_En7
Input1
Approximation
Output
ModelWithApproximation_2
Parameter Attributes
ModelVersion
1.0
LastModified...
Mon Feb 03 00:35:25 2020
LibraryLinkDi...
disabled
ModelBrows...
on
Dirty
on
Description
OK
Help


Code Generation Report
Find:
Match Case
Contents
Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Native Floating-Point Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
ModelWithApproximation_20210821T2103144
Referenced Models
Clock Report for ModelWithApproximation_20210821T210314460
Rate Information
Model Base Rate
1
DUT Base Rate
1
Clock Enable Table
Clock Enable Name
Sample Time
1
ModelWithApproximation_20210821T210314460
View All
ModelWithApproximation_20210821T210314460
Open scope to see simulation results
sfix16_En15
Approximate
sfix8_En7
Input1
Approximation
Output
ModelWithApproximation_2
Parameter Attributes
ModelVersion
1.0
LastModified...
Mon Feb 03 00:35:25 2020
LibraryLinkDi...
disabled
ModelBrows...
on
Dirty
on
Description
OK
Help


Code Generation Report
Find:
Match Case
Contents
Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Native Floating-Point Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
ModelWithApproximation_20210821T2103144
Referenced Models
Critical Path Report for ModelWithApproximation_20210821T210314460
Summary Section
Critical Path Delay : 2.233 ns
Critical Path Begin : LimitedCounter
Critical Path End : LimitedCounter
Highlight Critical Path: hdlsrc\ModelWithApproximation_20210821T210314460\criticalPathEstimated.m
Critical Path Details
Id
Propagation (ns)
Delay (ns)
Block Path
1
2.2330
2.2330
LimitedCounter
ModelWithApproximation_20210821T210314460
View All
ModelWithApproximation_20210821T210314460
Open scope to see simulation results
Approximate
sfix16_En15
sfix8_En7
Input1
Approximation
Output
ModelWithApproximation_2
Parameter Attributes
ModelVersion
1.0
LastModified...
Mon Feb 03 00:35:25 2020
LibraryLinkDi...
disabled
ModelBrows...
on
Dirty
on
Description
OK
Help


Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
Approximate_id_dd31245fd0741dd0dbd4bc99
Source.vhd
Approximate_id_dd31245fd0741dd0dbd4bc99
Referenced Models
Summary
Model
Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
Model version
1.0
HDL Coder version
3.16
HDL code generated on
2021-07-28 13:19:10
HDL code generated for
Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
Target Language
VHDL
Target Directory
hdlsrc_exp
Non-default model properties
CriticalPathEstimation
on
GenerateValidationModel
on
HDLGenerateWebview
on
HDLSubsystem
Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
OptimizationReport
on
ResourceReport
on
SynthesisTool
Xilinx Vivado
SynthesisToolChipFamily
Artix7
SynthesisToolDeviceName
xa7a100t
SynthesisToolPackageName
csg324
SynthesisToolSpeedValue
-1l
TargetDirectory
hdlsrc_exp
Traceability
on
OK
Help


Summary
Clock Summary
Code Interface Report
Timing And Area Report
High-level Resource Report
Critical Path Estimation
Optimization Report
Distributed Pipelining
Streaming and Sharing
Delay Balancing
Adaptive Pipelining
Traceability Report
Generated Source Files
Approximate_id_dd31245fd0741dd0dbd4bc99
Source.vhd
Approximate_id_dd31245fd0741dd0dbd4bc99
Referenced Models
Summary
Model
Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
Model version
1.0
HDL Coder version
3.16
HDL code generated on
2021-07-28 13:19:10
HDL code generated for
Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
Target Language
VHDL
Target Directory
hdlsrc_exp
Non-default model properties
CriticalPathEstimation
on
GenerateValidationModel
on
HDLGenerateWebview
on
HDLSubsystem
Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
OptimizationReport
on
ResourceReport
on
SynthesisTool
Xilinx Vivado
SynthesisToolChipFamily
Artix7
SynthesisToolDeviceName
xa7a100t
SynthesisToolPackageName
csg324
SynthesisToolSpeedValue
-1l
TargetDirectory
hdlsrc_exp
Traceability
on
OK
Help


Code Generation Report
Find:
Match Case
Contents
Summary
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Optimization Report
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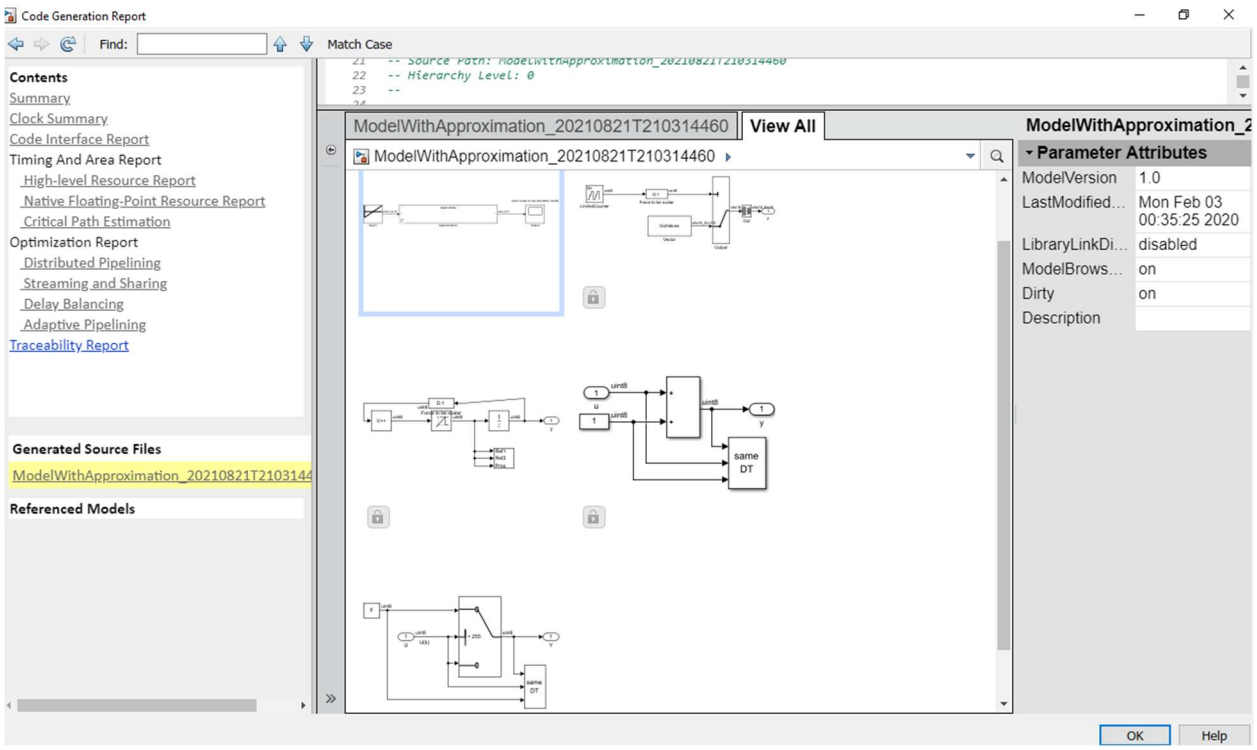
Adaptive Pipelining
Traceability Report
Generated Source Files
ModelWithApproximation_20210821T2103144
Referenced Models
-- Module: ModelWithApproximation_20210821T210314460
-- Source Path: ModelWithApproximation_20210821T210314460
-- Hierarchy Level: 0
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;
ENTITY ModelWithApproximation_20210821T210314460 IS
END ModelWithApproximation_20210821T210314460;
ARCHITECTURE rtl OF ModelWithApproximation_20210821T210314460 IS
BEGIN
-- Open scope to see simulation results
END rtl;
ModelWithApproximation_20210821T210314460
View All
ModelWithApproximation_20210821T210314460
Open scope to see simulation results
sfix16_En15
Approximate
sfix8_En7
Input1
Approximation
Output
ModelWithApproximation_2
Parameter Attributes
ModelVersion
1.0
LastModified...
Mon Feb 03 00:35:25 2020
LibraryLinkDi...
disabled
ModelBrows...
on
Dirty
on
Description
OK
Help


Code Generation Report
Find:
Match Case
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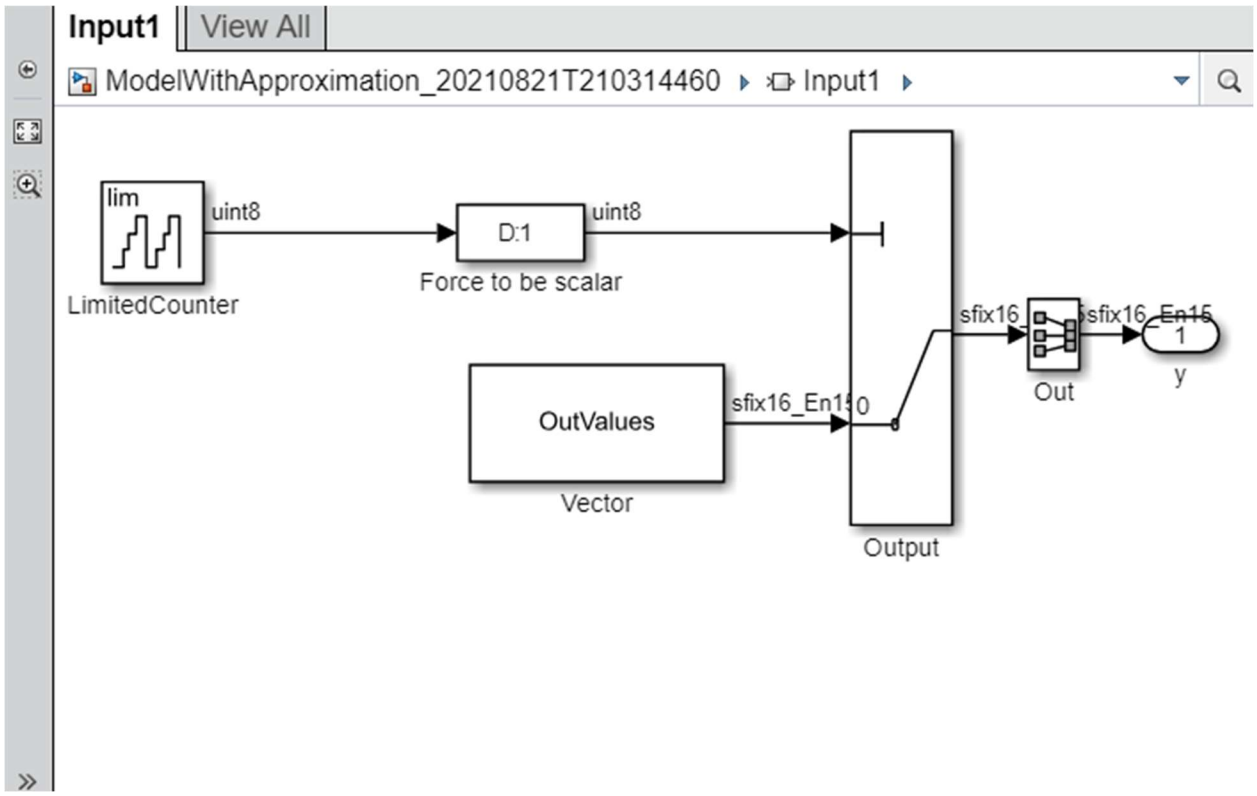
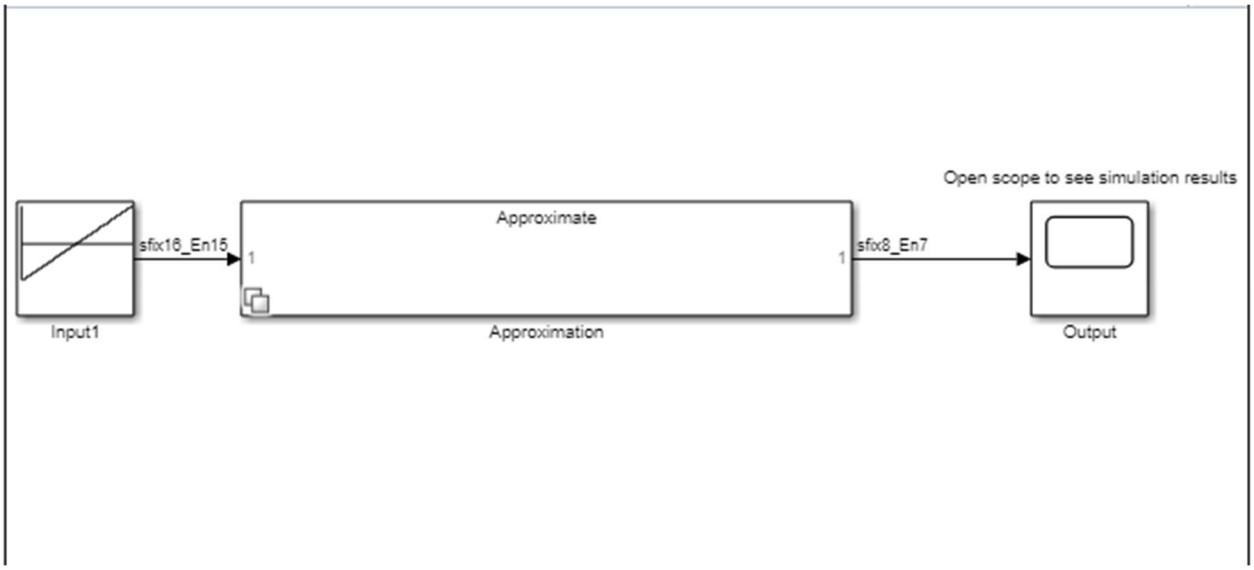
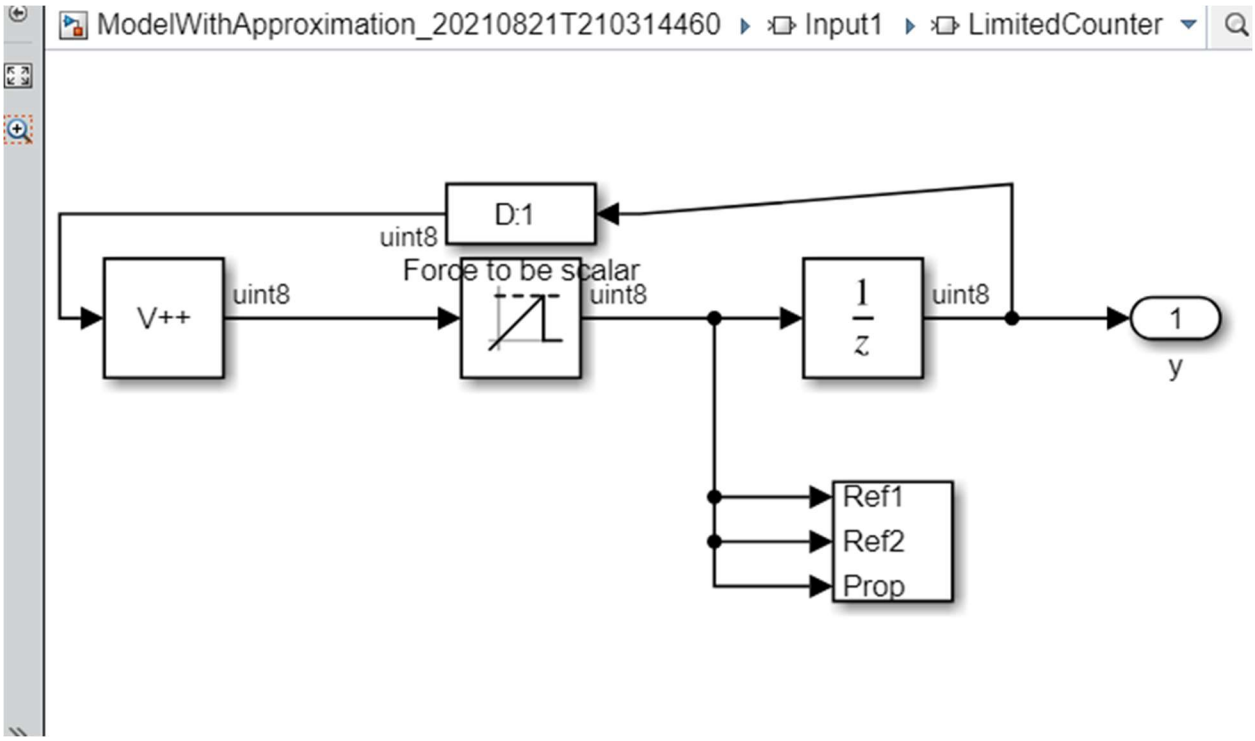
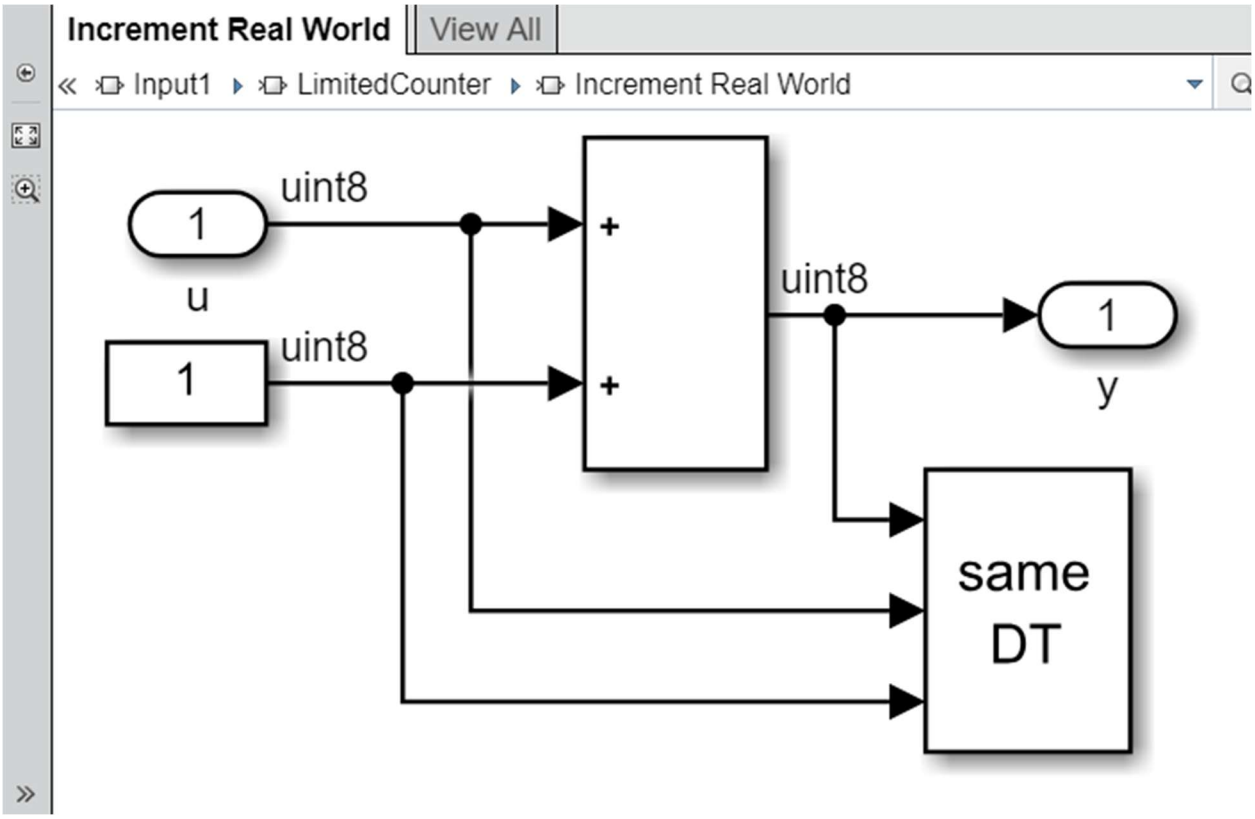
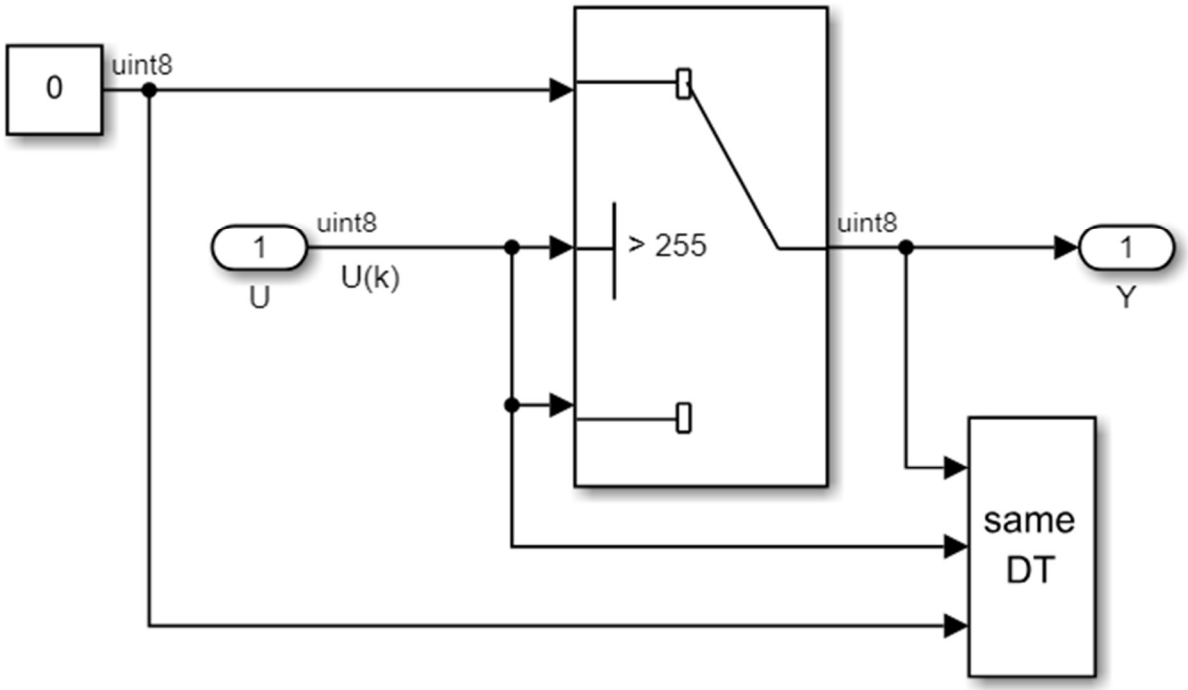
Generated Source Files
ModelWithApproximation_20210821T2103144
Referenced Models
-- Source Path: ModelWithApproximation_20210821T210314460
-- Hierarchy Level: 0
--
ModelWithApproximation_20210821T210314460
View All
ModelWithApproximation_20210821T210314460
same DT
ModelWithApproximation_2
Parameter Attributes
ModelVersion 1.0
LastModified... Mon Feb 03 00:35:25 2020
LibraryLinkDi... disabled
ModelBrows... on
Dirty on
Description
OK
Help

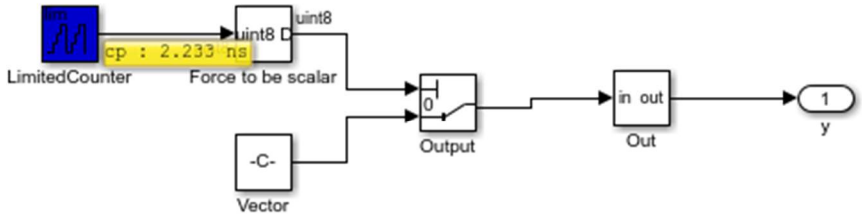

Input1
View All
ModelWithApproximation_20210821T210314460
Input1
lim
uint8
LimitedCounter
D:1
Force to be scalar
uint8
OutValues
Vector
sfix16_En15
sfix16
Out
sfix16_En15
1
y
Output

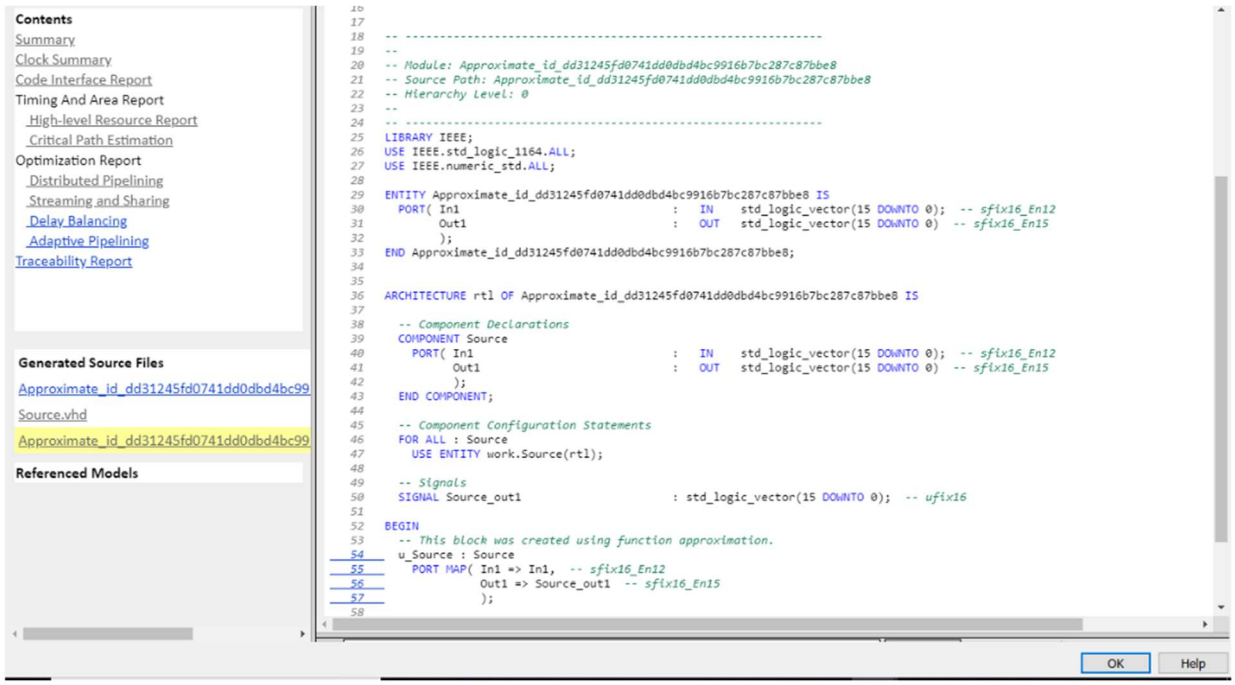

Open scope to see simulation results
Approximate
sfix16_En15
1
1
sfix8_En7
Input1
Approximation
Output


ModelWithApproximation_20210821T210314460
Input1
LimitedCounter
D:1
uint8
Force to be scalar
V++
uint8
uint8
uint8
1
z
1
y
Ref1
Ref2
Prop


Increment Real World
View All
Input1
LimitedCounter
Increment Real World
1
u
uint8
1
uint8
+
+
uint8
1
y
same
DT


0
uint8
1
U
uint8
U(k)
> 255
uint8
1
Y
same
DT





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Generated Source Files

Approximate_id_dd31245fd0741dd0dbd4bc99
Source.vhd
Approximate_id_dd31245fd0741dd0dbd4bc99

Referenced Models

```
16
17
18  -- -------------------------------------------------------------
19  --
20  -- Module: Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
21  -- Source Path: Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8
22  -- Hierarchy Level: 0
23  --
24  -- -------------------------------------------------------------
25  LIBRARY IEEE;
26  USE IEEE.std_logic_1164.ALL;
27  USE IEEE.numeric_std.ALL;
28
29  ENTITY Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8 IS
30    PORT( In1                             :   IN    std_logic_vector(15 DOWNTO 0);  -- sfix16_En12
31          Out1                            :   OUT   std_logic_vector(15 DOWNTO 0)  -- sfix16_En15
32          );
33  END Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8;
34
35
36  ARCHITECTURE rtl OF Approximate_id_dd31245fd0741dd0dbd4bc9916b7bc287c87bbe8 IS
37
38    -- Component Declarations
39    COMPONENT Source
40      PORT( In1                           :   IN    std_logic_vector(15 DOWNTO 0);  -- sfix16_En12
41            Out1                          :   OUT   std_logic_vector(15 DOWNTO 0)  -- sfix16_En15
42            );
43    END COMPONENT;
44
45    -- Component Configuration Statements
46    FOR ALL : Source
47      USE ENTITY work.Source(rtl);
48
49    -- Signals
50    SIGNAL Source_out1                    : std_logic_vector(15 DOWNTO 0);  -- ufix16
51
52  BEGIN
53    -- This block was created using function approximation.
54    u_Source : Source
55      PORT MAP( In1 => In1,  -- sfix16_En12
56                Out1 => Source_out1  -- sfix16_En15
57                );
58
```

OK Help