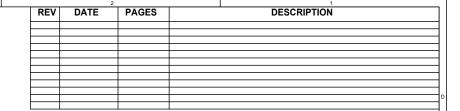
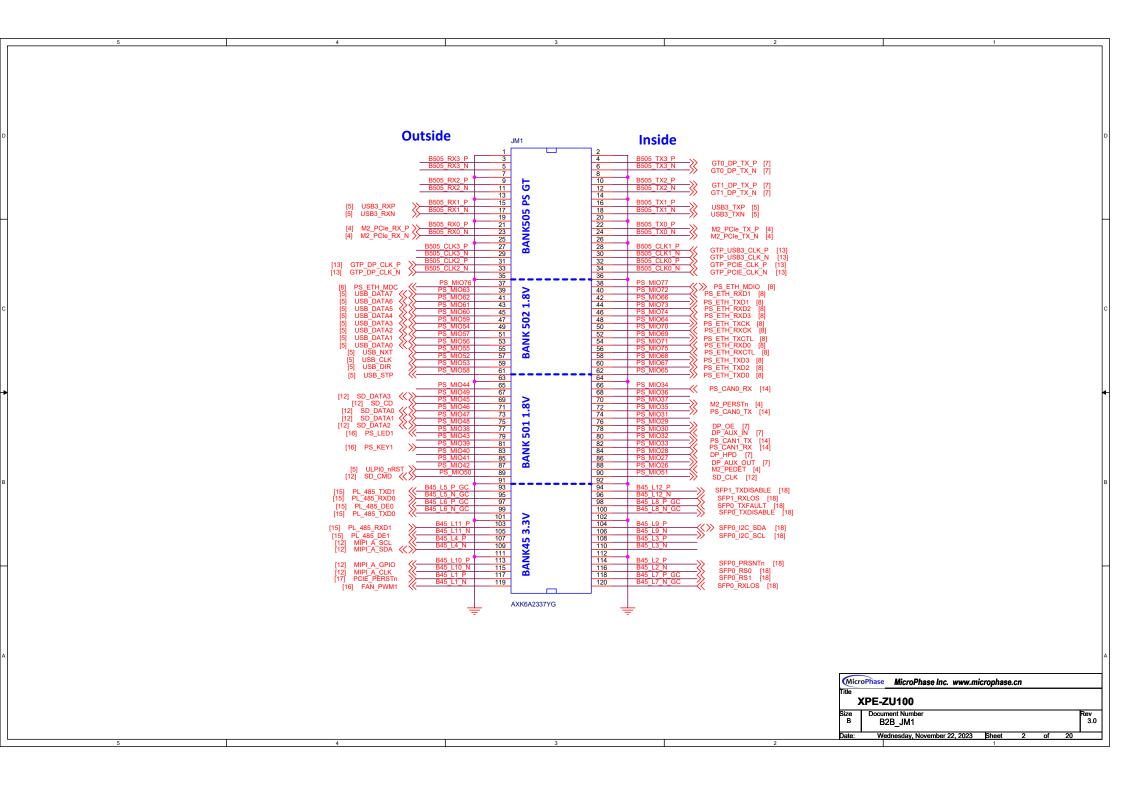
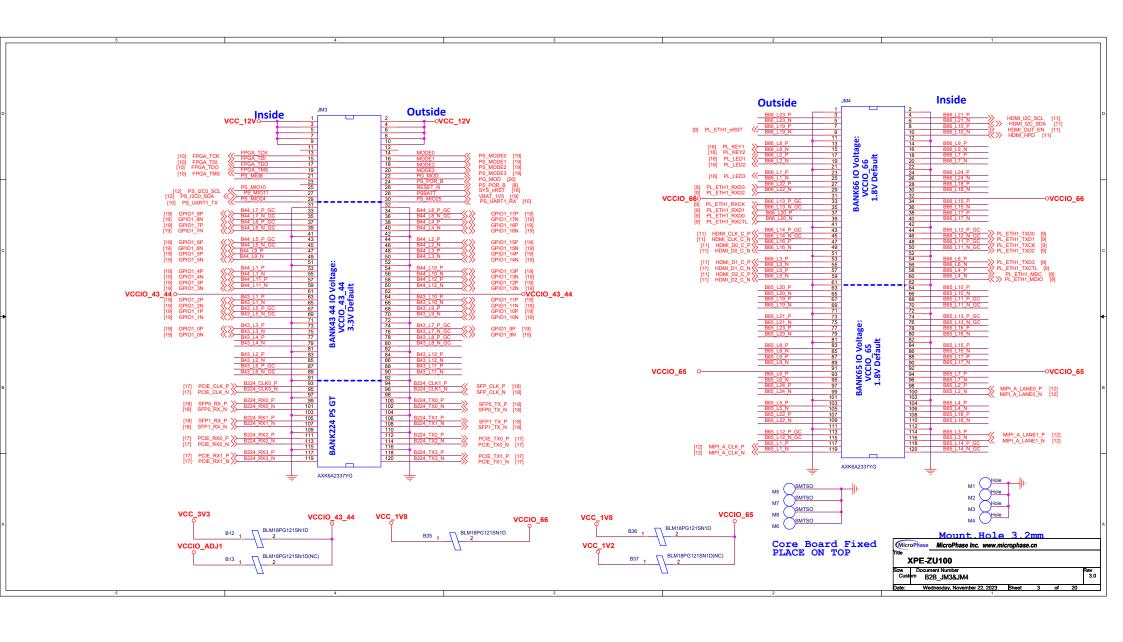
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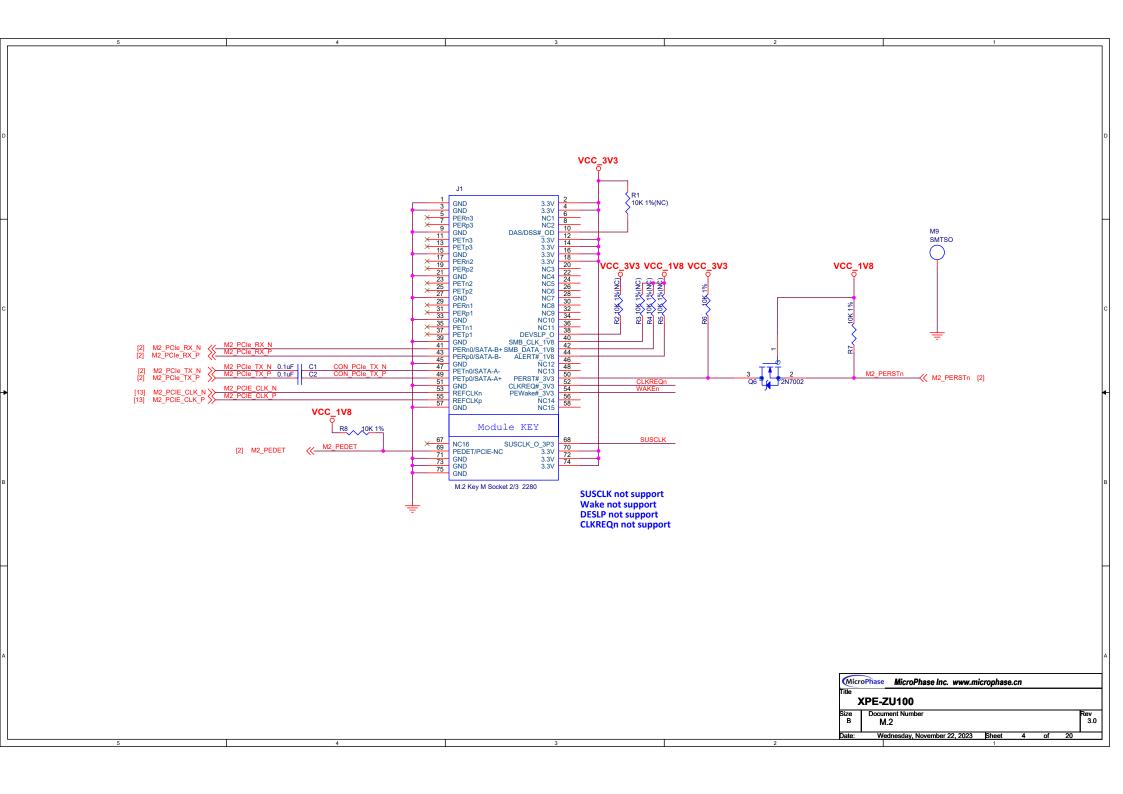


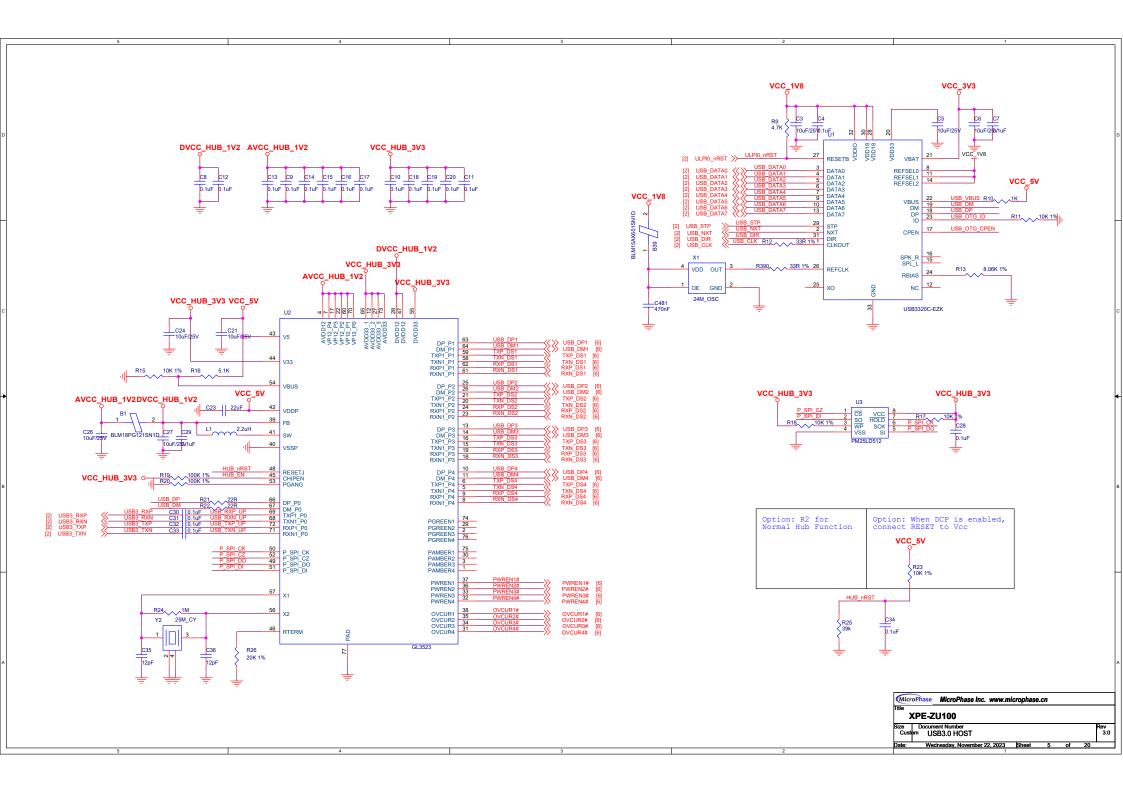
PAGE	DESCRIPTION	1
1	Title, Notes, Block Diagram, Revision History	I
2	B2B JM1	I
3	B2B JM3&JM4	I
4	M.2 Socket	I
5	USB3.0 HOST	I
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8	PS ETH0	I
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12	SD&MIPI&TP&EEPROM	ľ
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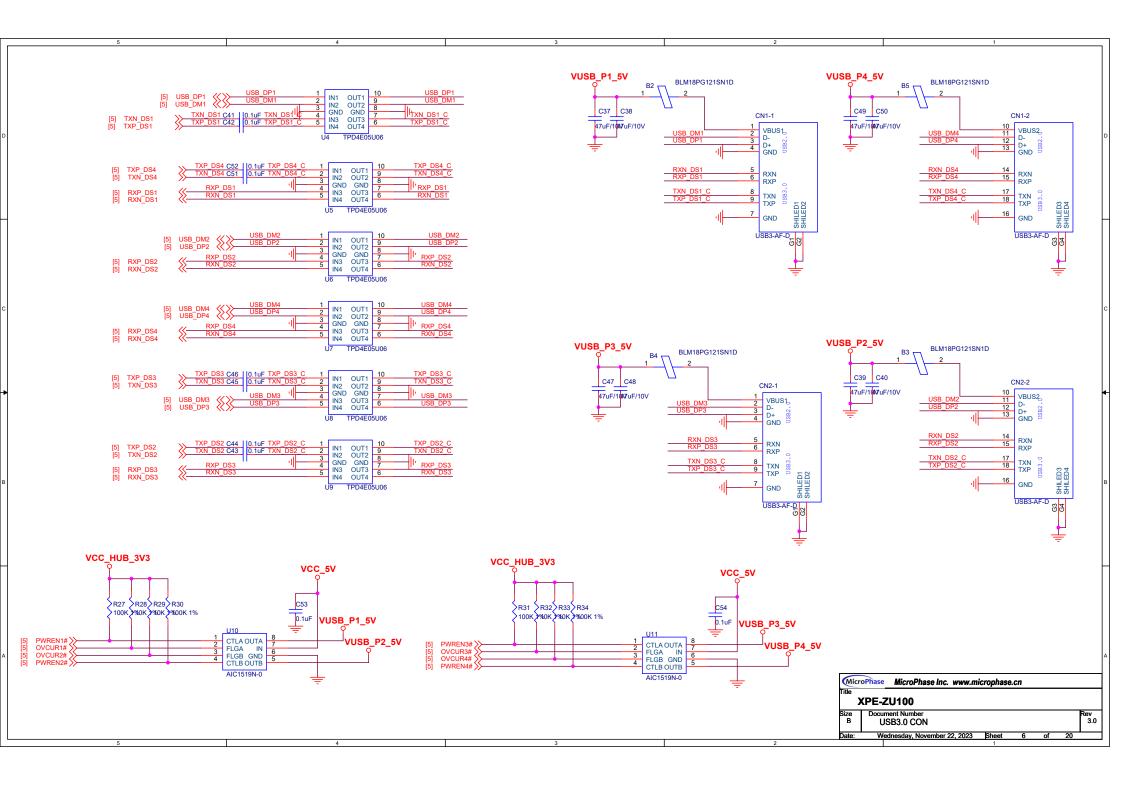
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Title										
2	KPE-Z	U100								
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В	Blo	ock Diagram						3.0		
Date:	Wed	Inesday, November 22	2, 2023	Sheet	1	of	20			
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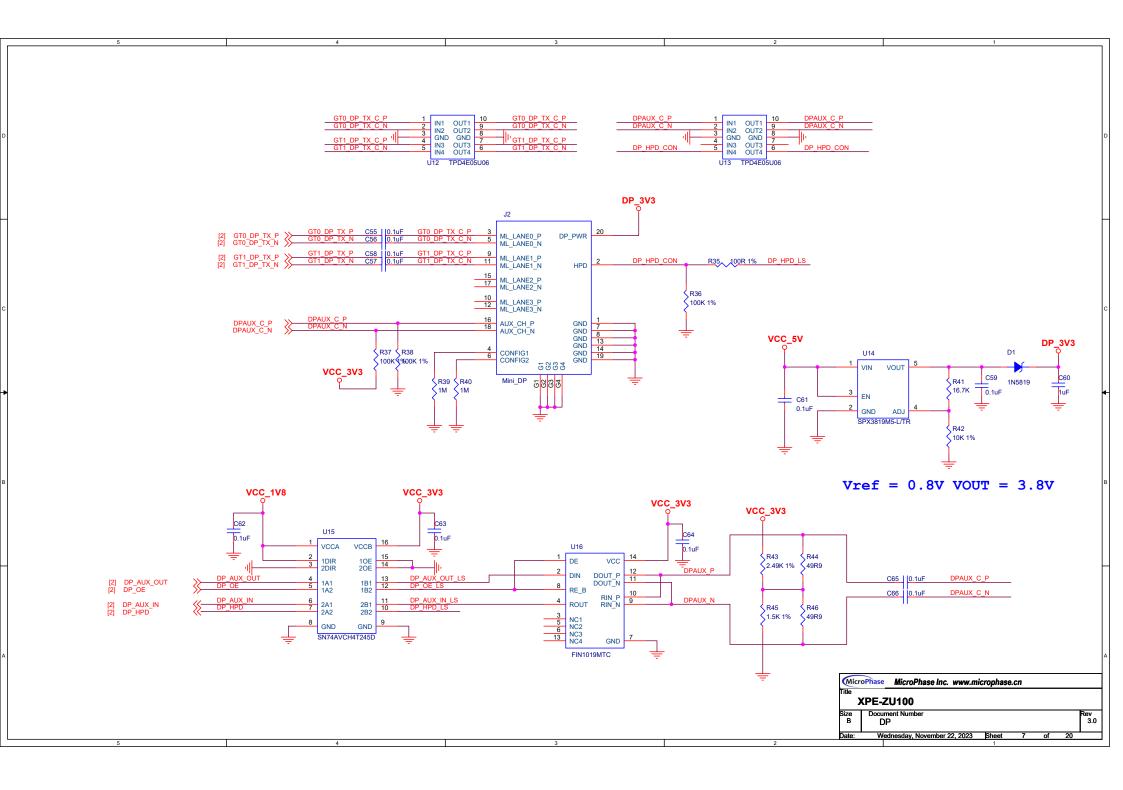


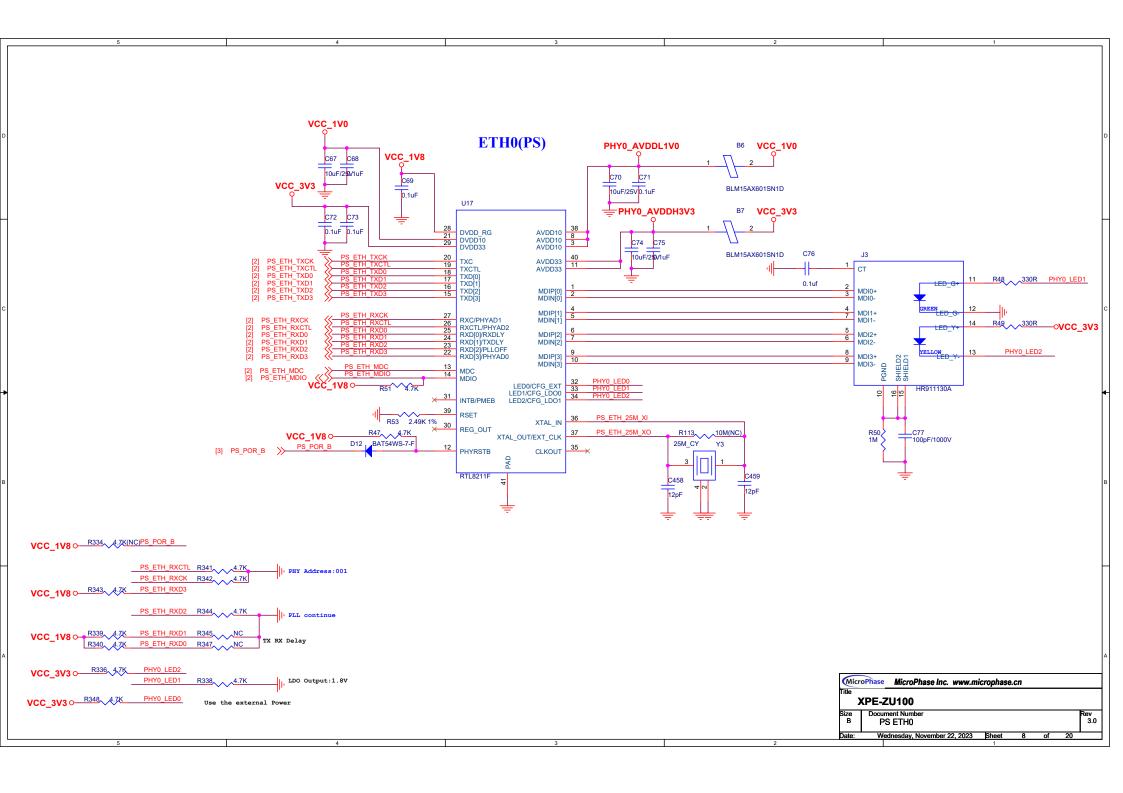


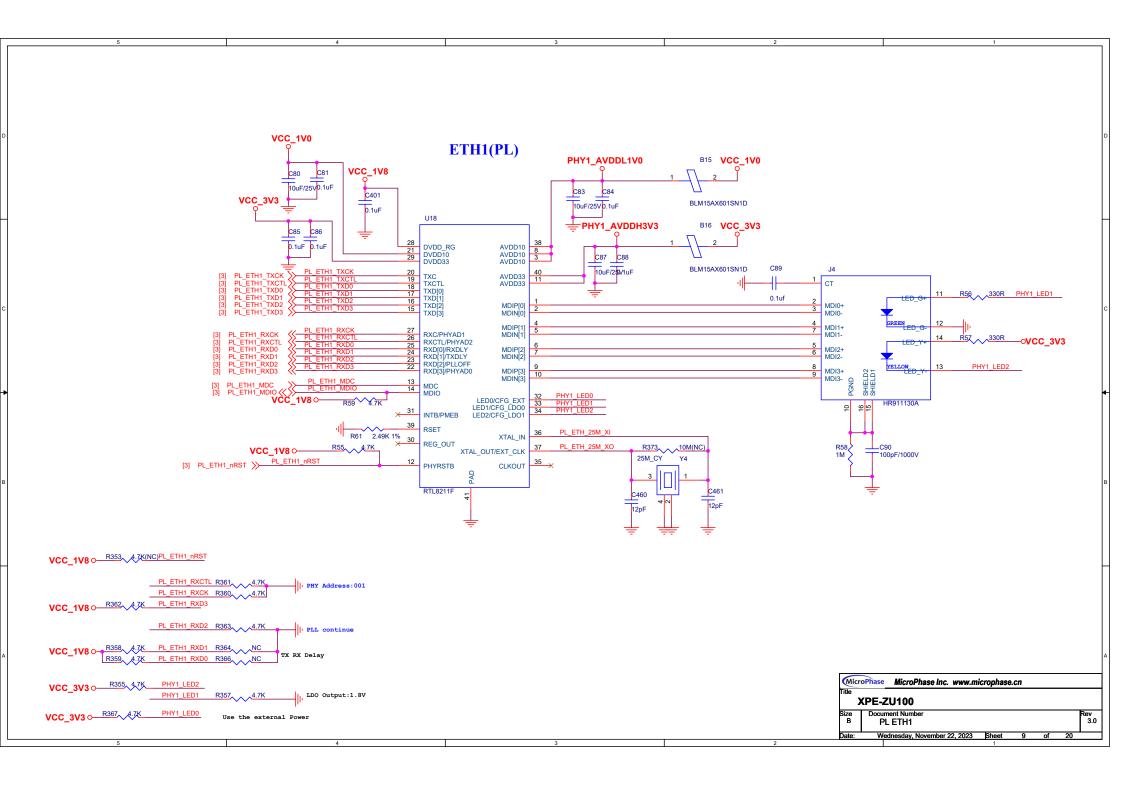


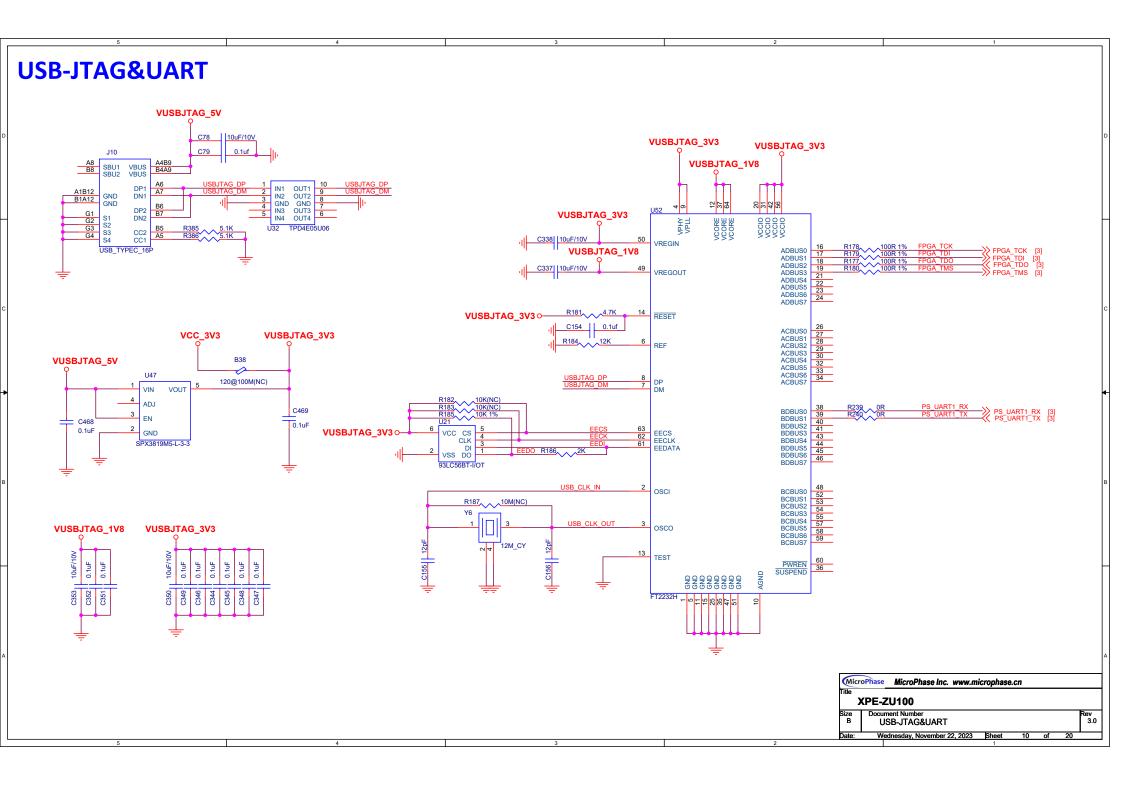


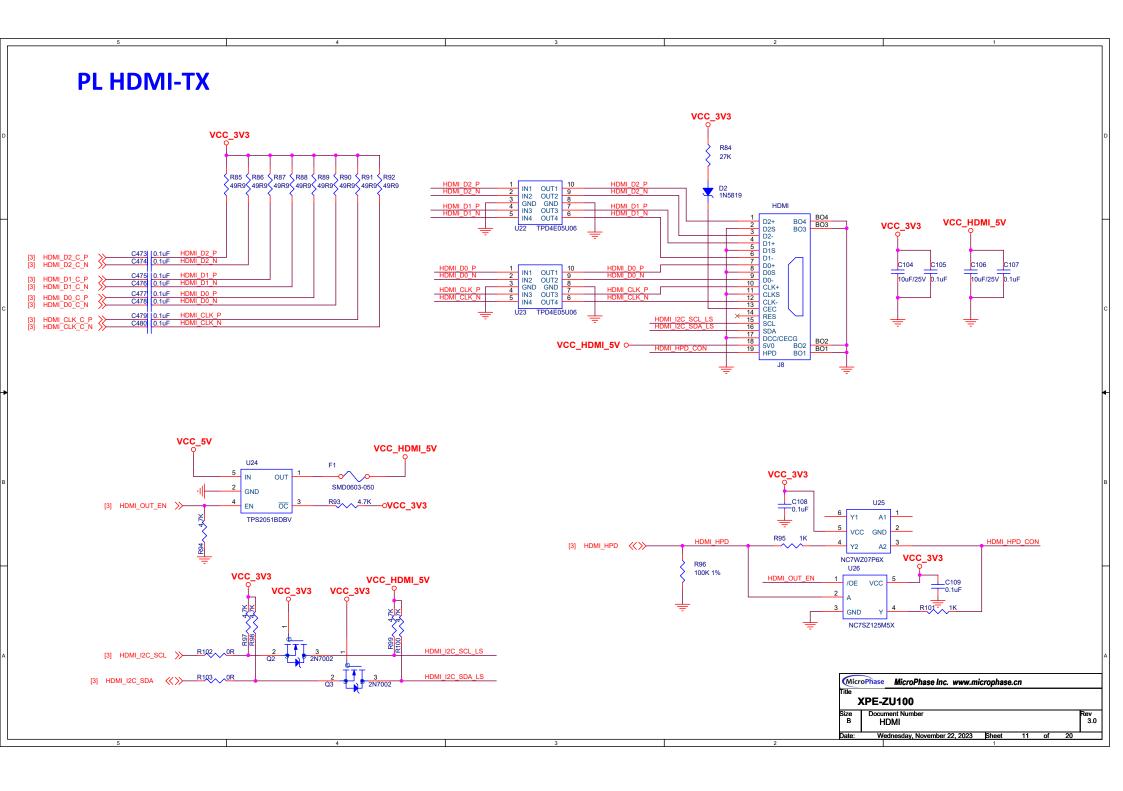


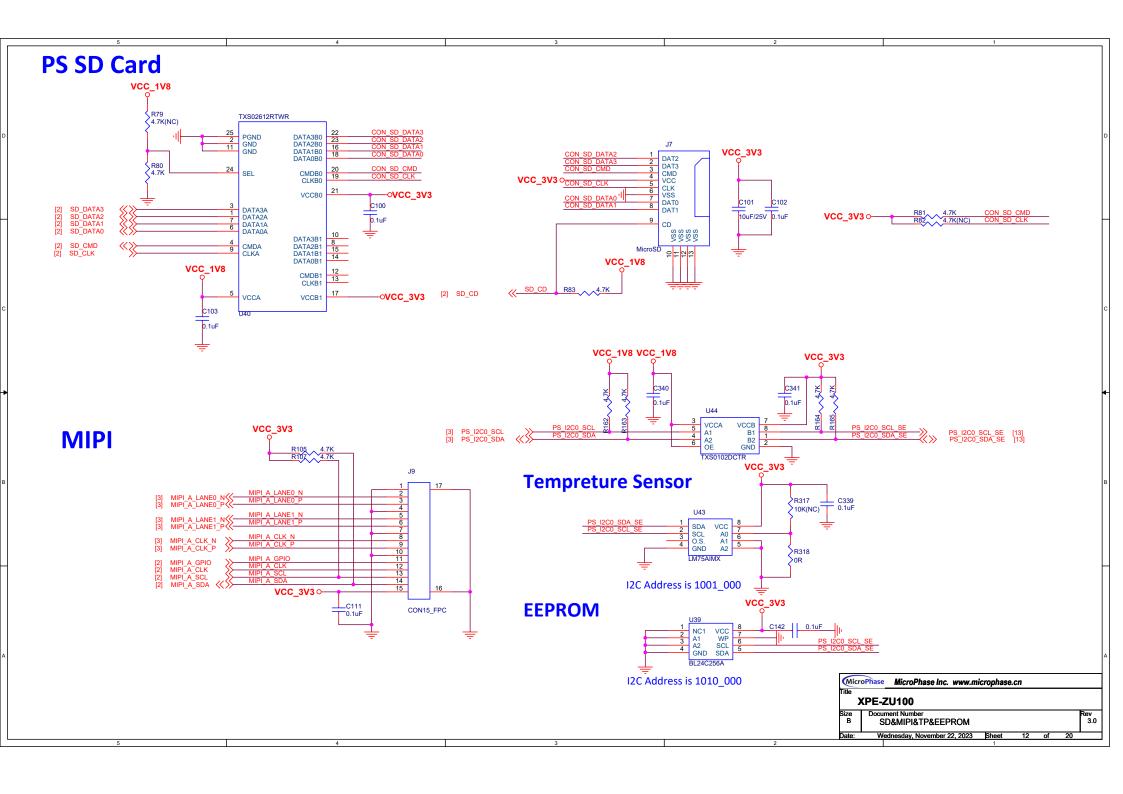


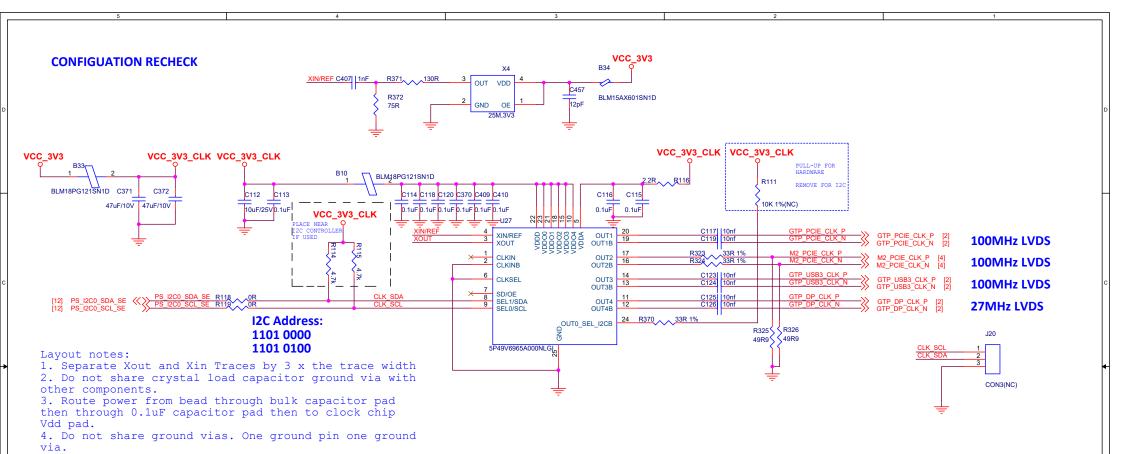






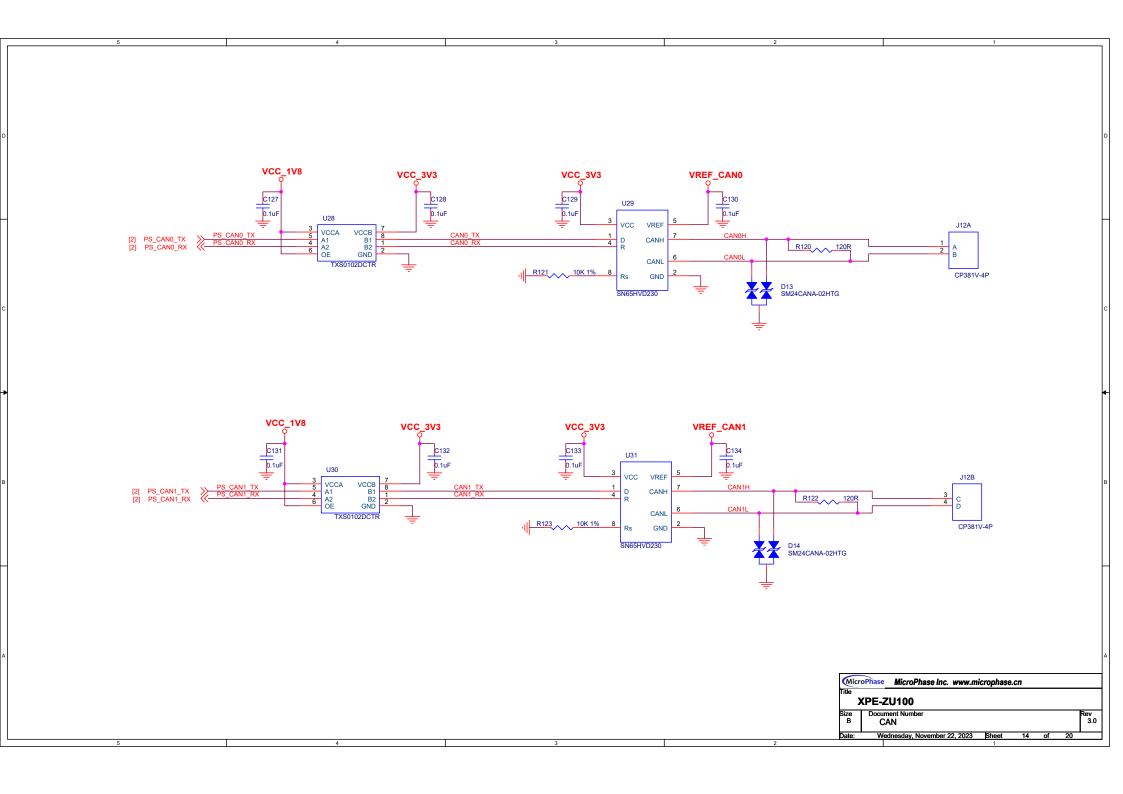


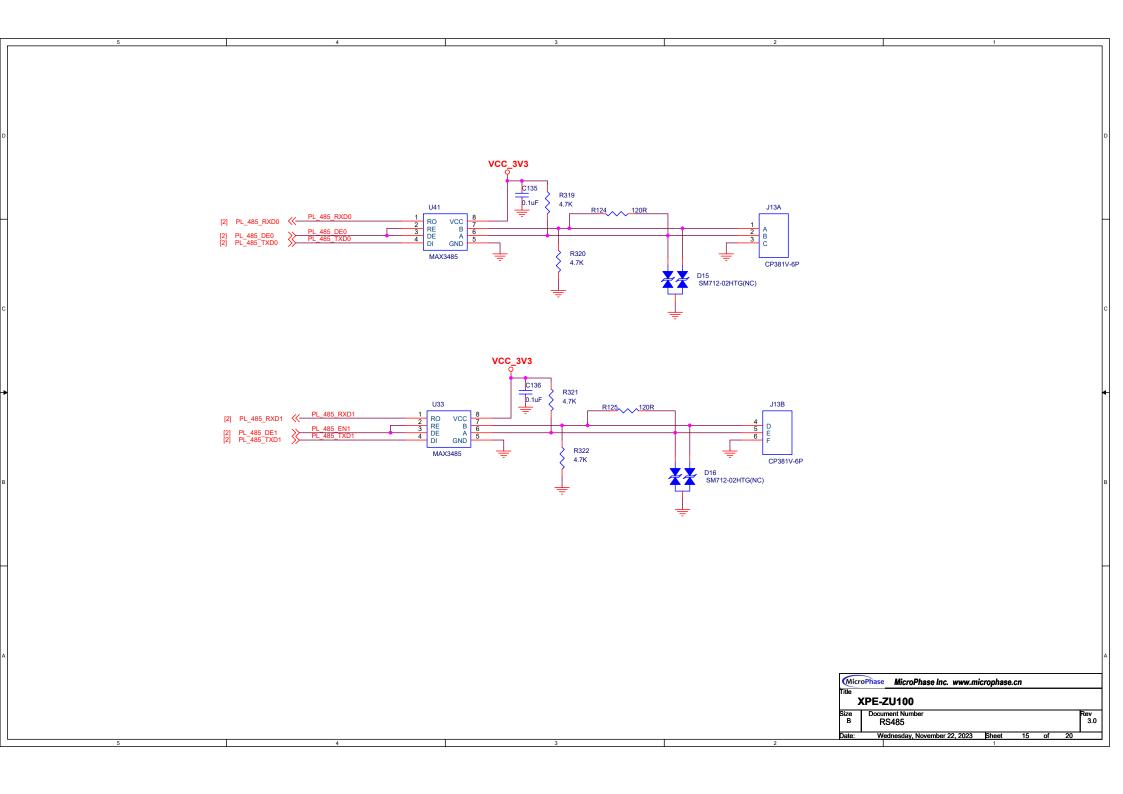


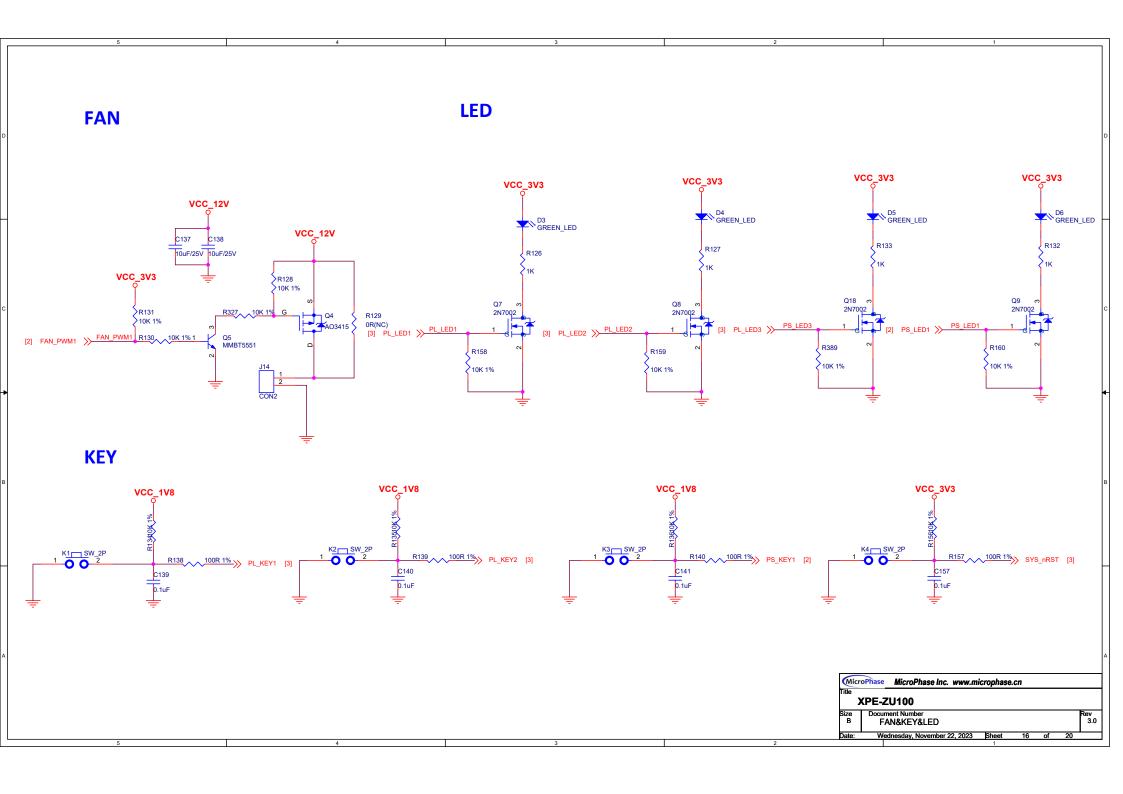


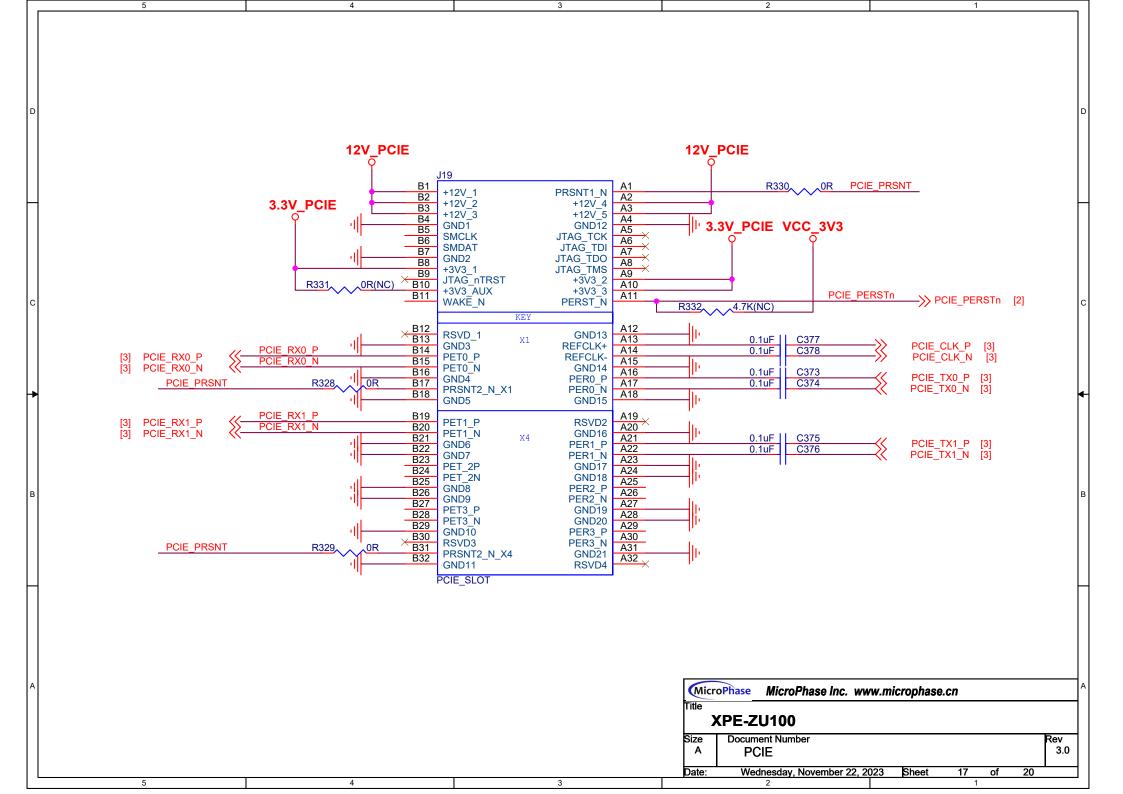
OUT0_SEL_I2CB at POR	SEL1	SEL0	I ² C Access	REG0:7	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	Х	Х	Yes	1	I ² C defaults
0	X	Х	Yes	0	0

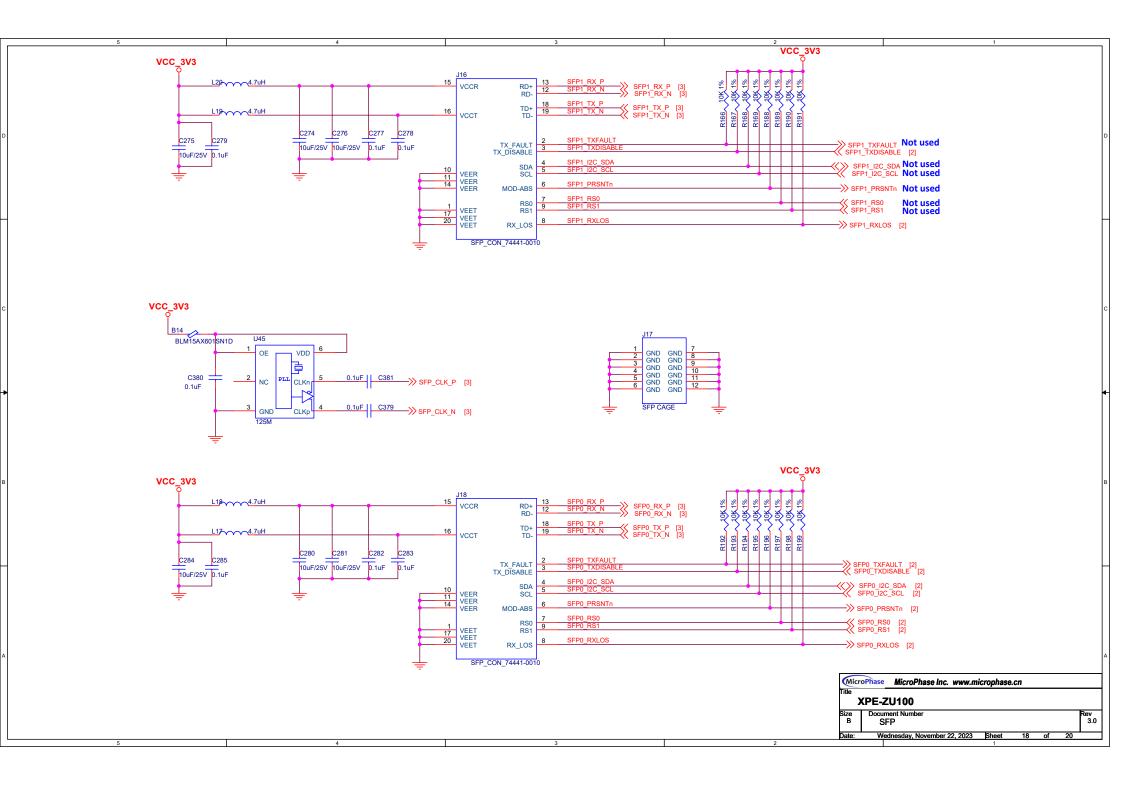
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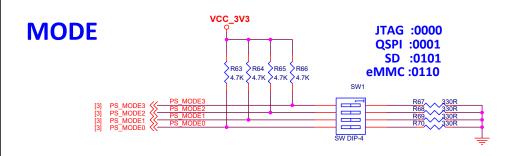




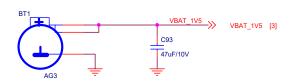




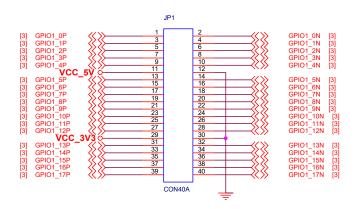




RTC



GPIO



Boot Mode	Mode Pins [3:0]	MIO Location	Non- Secure	Secure	Signed	Mode	Description	
JTAG	0x0	JTAG	Yes	No	No	Slave	Dedicated PS interface.	
QSPI24	0x1	MIO[12:0]	Yes	Yes	Yes	Master	24-bit addressing. Supports single and dual parallel configurations. Stack and dual stack is not supported.	
QSPI32	0x2	MIO[12:0]	Yes	Yes	Yes	Master	32-bit addressing. Supports single and dual parallel configurations. Stack and dual stack is not supported.	
SD0	0x3	MIO[25:13]	Yes	Yes	Yes	Master	Supports SD 2.0.	
NAND	0x4	MIO[25:09]	Yes	Yes	Yes	Master	Requires 8-bit data bus width	
SD1	0x5	MIO[51:38]	Yes	Yes	Yes	Master	Supports SD 2.0.	
eMMC_18	0x6	MIO[22:13]	Yes	Yes	Yes	Master	Supports eMMC 4.5 at 1.8V.	
USB 0	0111b	MIO[52:63]	Yes	Yes	Yes	Slave	Supports USB 2.0 and USB 3.0.	
PJTAG_0	0x8	MIO[29:26]	Yes	No	No	Slave	PS JTAG connection 0 option.	
PJTAG_1	0x9	MIO[15:12]	Yes	No	No	Slave	PS JTAG connection 1 option.	
SD1-LS	0xE	MIO[51:39]	Yes	Yes	Yes	Master	Supports SD 3.0 with a required SD 3.0 compliant level shifter.	

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Size B	Document Number MODE & RTC & GPIO	Rev 3.0					
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