

PE500 Block Diagram

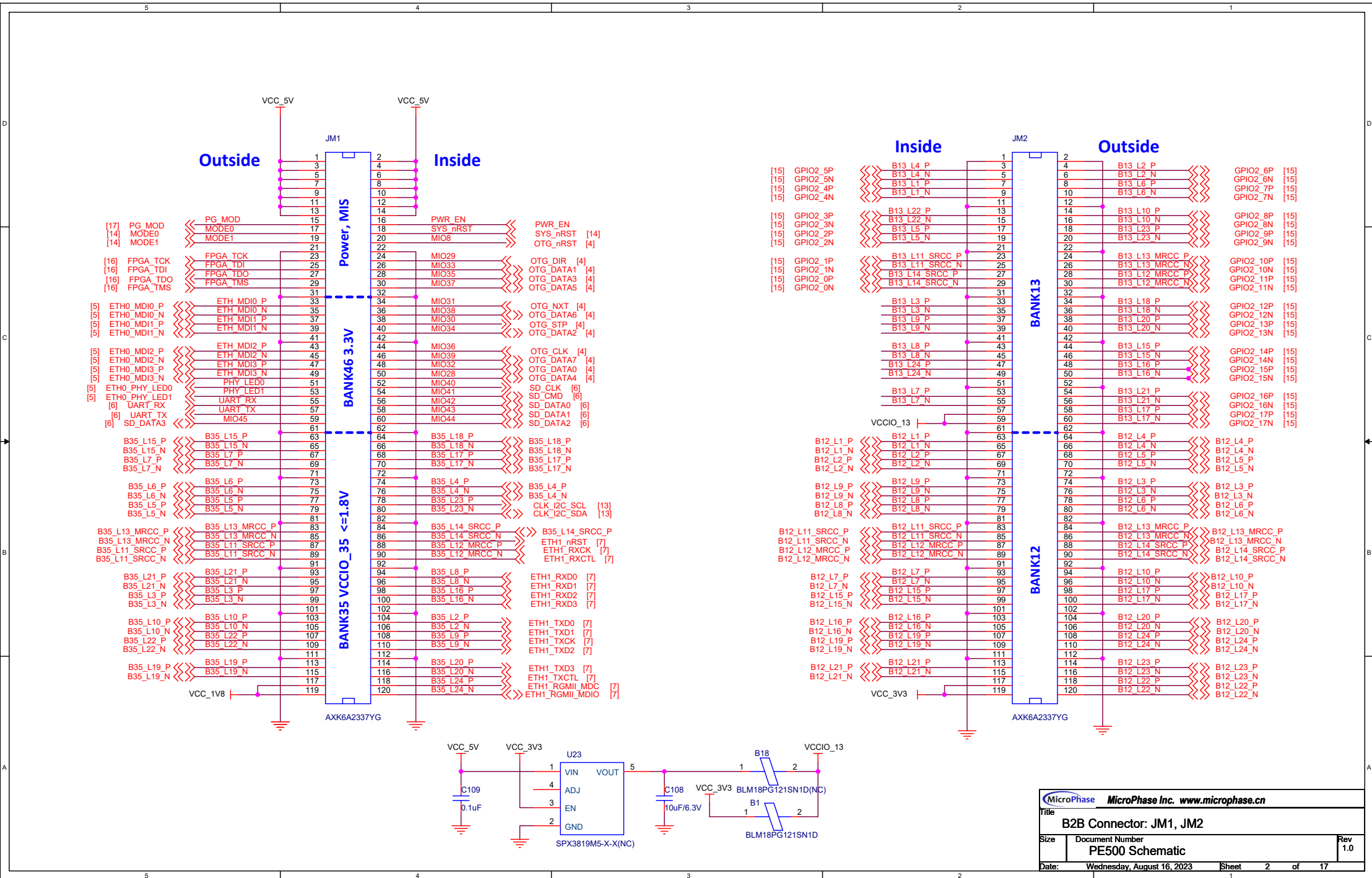
REV	DATE	PAGES	DESCRIPTION
1.0	8/06/2021	All	Rev 1.0 Release

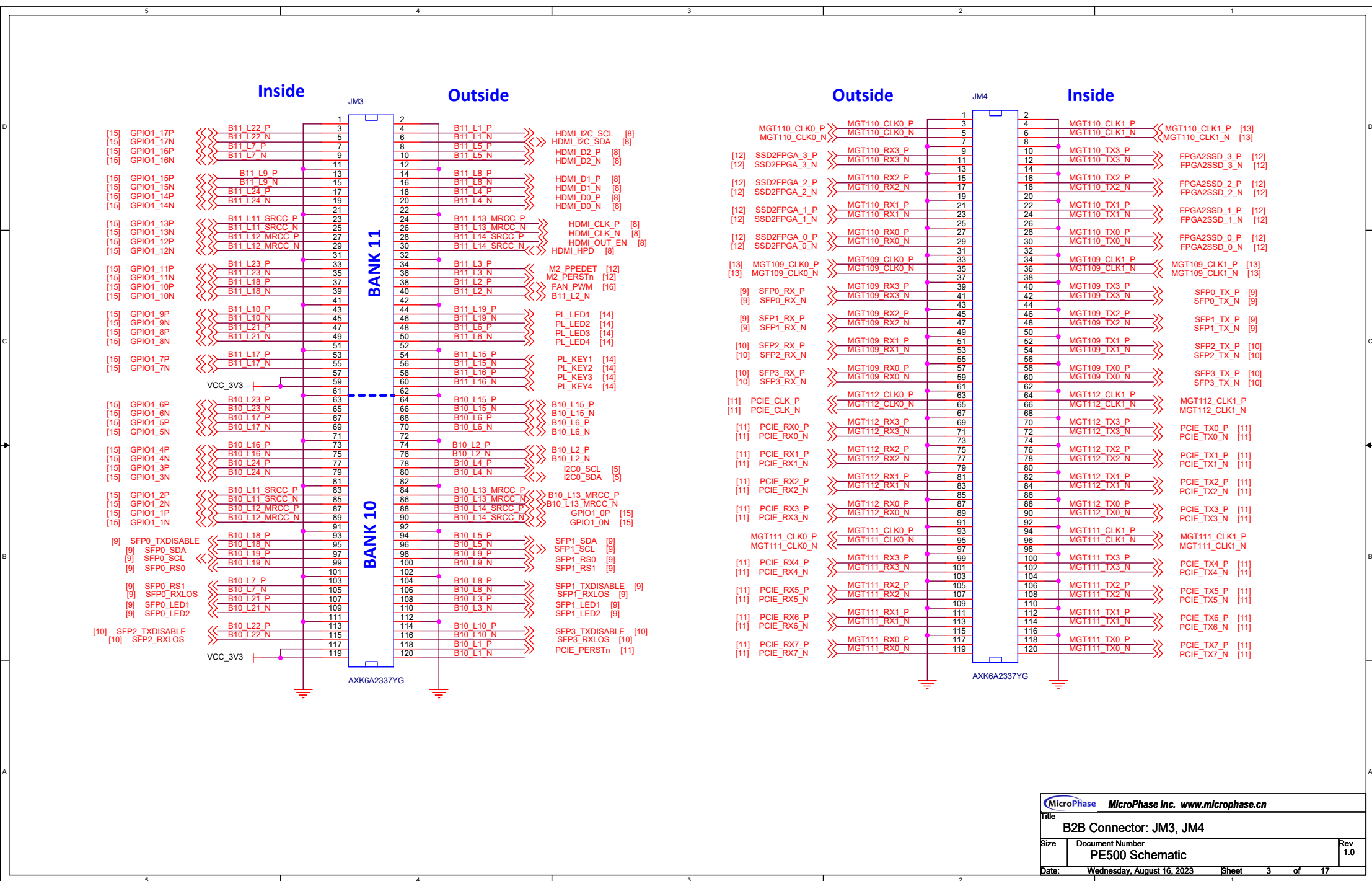
PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	B2B Connector: JM1, JM2
3	B2B Connector: JM3, JM4
4	USB
5	PS ETH&RTC&EEPROM
6	UART&SD
7	PL ETH
8	HDMI
9	SFP+0&1
10	SFP+2&3
11	PCIe
12	M.2
13	Clock
14	KEY&LED
15	GPIO Connetor
16	JTAG&FAN
17	Power
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	

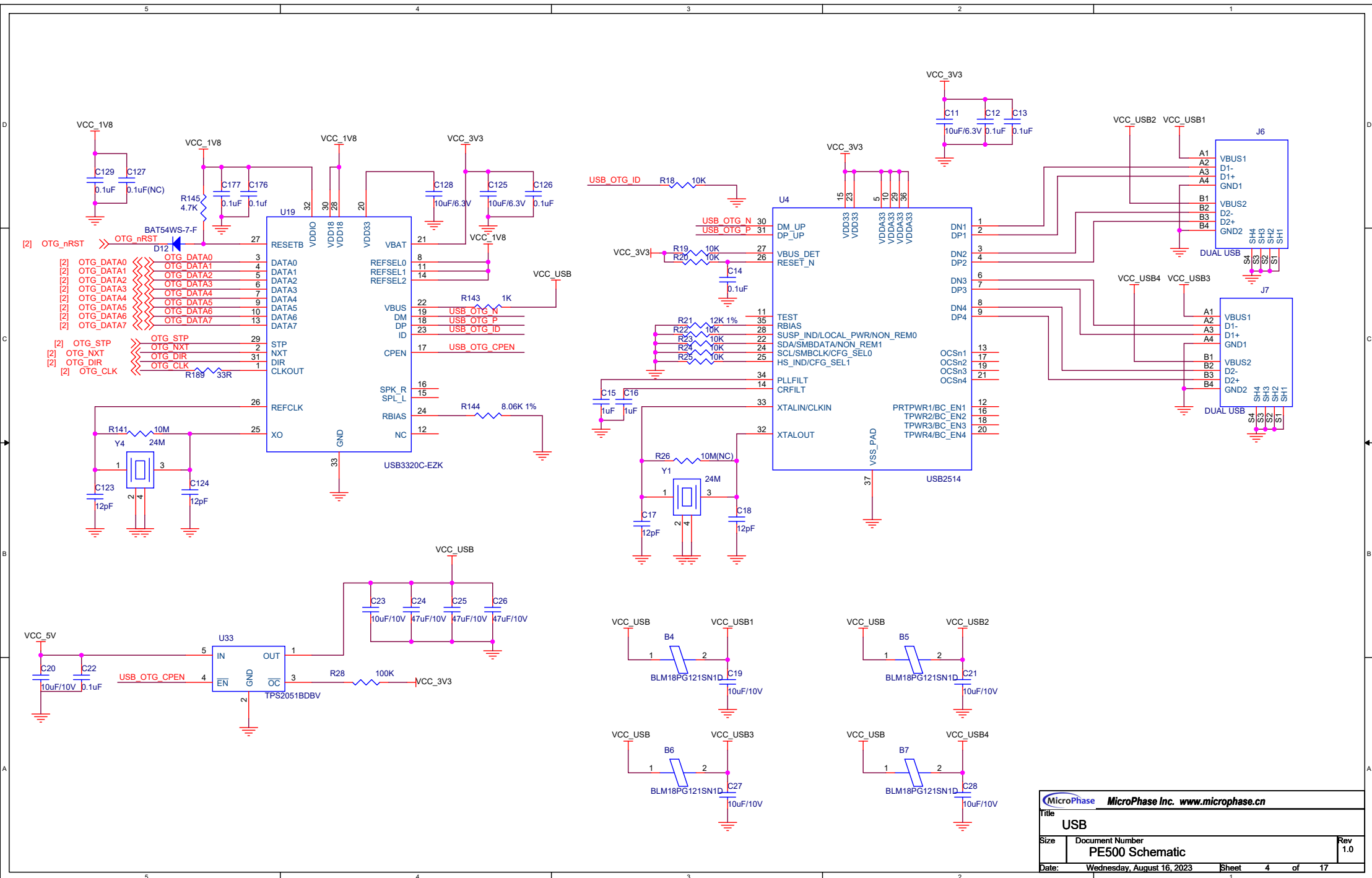
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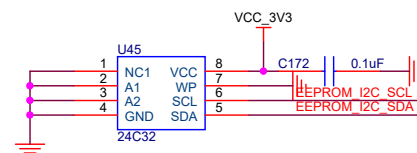
 MicroPhase Inc. www.microphase.cn	
Title Block Diagram	
Size	Document Number PE500 Schematic
Date:	Wednesday, August 16, 2023
Sheet	1 of 17
Rev	1.0



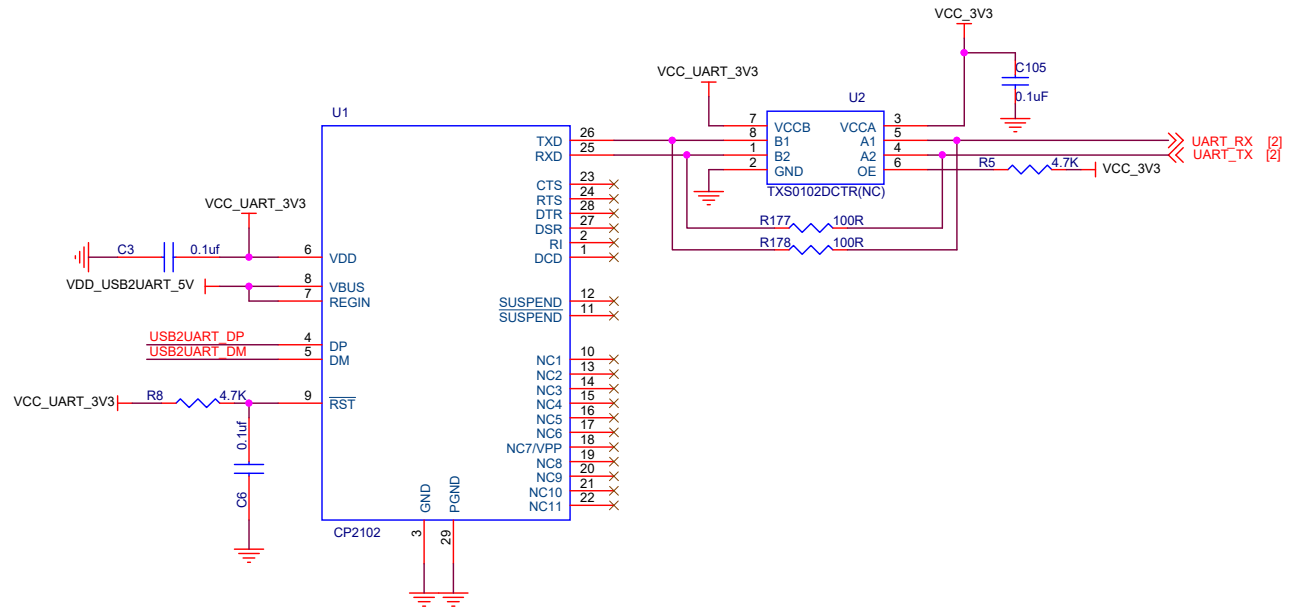
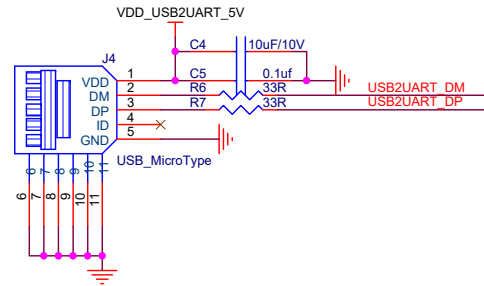




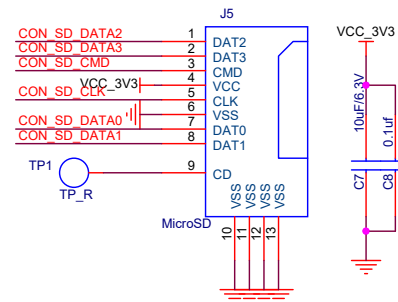
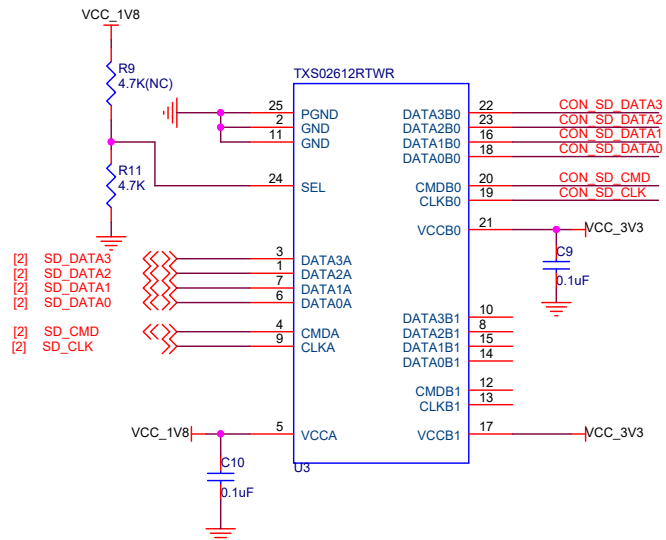
[2]	ETH0 MDIO P	ETH0 MDIO P
[2]	ETH0 MDIO N	ETH0 MDIO N
[2]	ETH0 MDI1 P	ETH0 MDI1 P
[2]	ETH0 MDI1 N	ETH0 MDI1 N
[2]	ETH0 MDI2 P	ETH0 MDI2 P
[2]	ETH0 MDI2 N	ETH0 MDI2 N
[2]	ETH0 MDI3 P	ETH0 MDI3 P
[2]	ETH0 MDI3 N	ETH0 MDI3 N
[2]	ETH0 PHY_LED0	ETH0 PHY_LED0
[2]	ETH0 PHY_LED1	ETH0 PHY_LED1

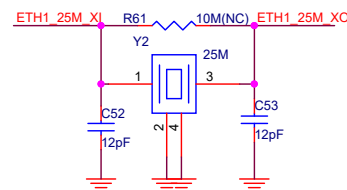
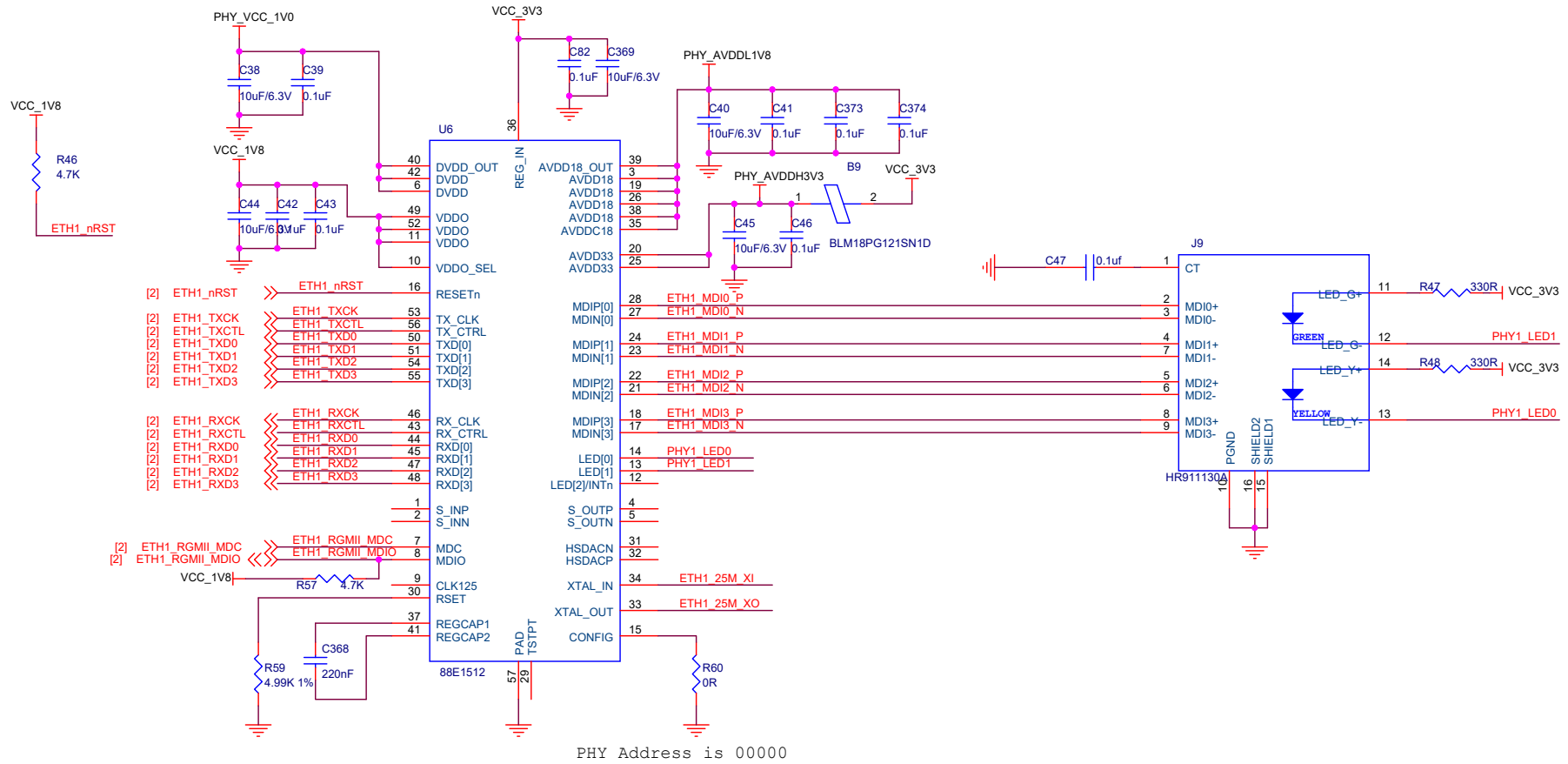


USB2UART

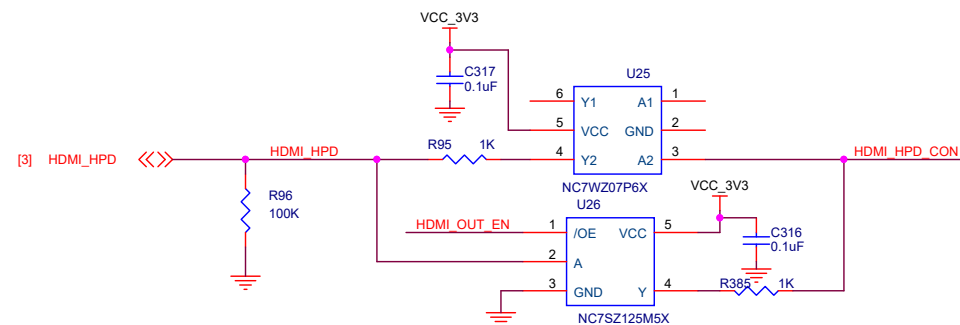
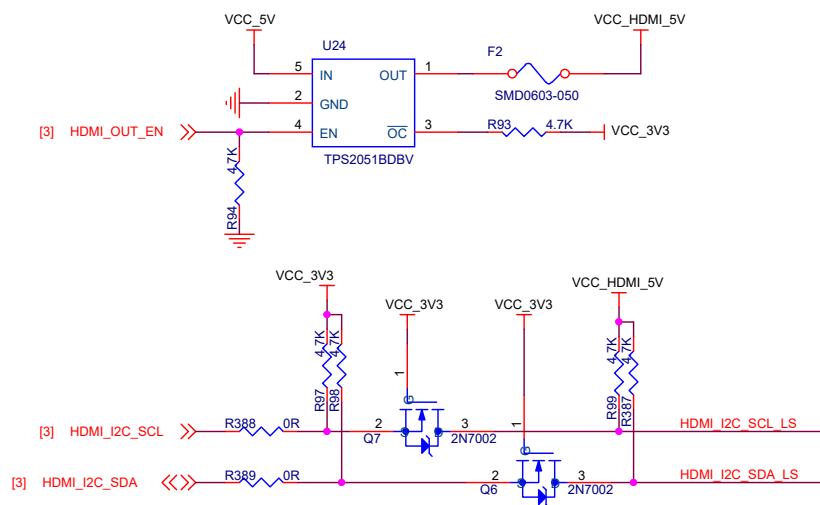
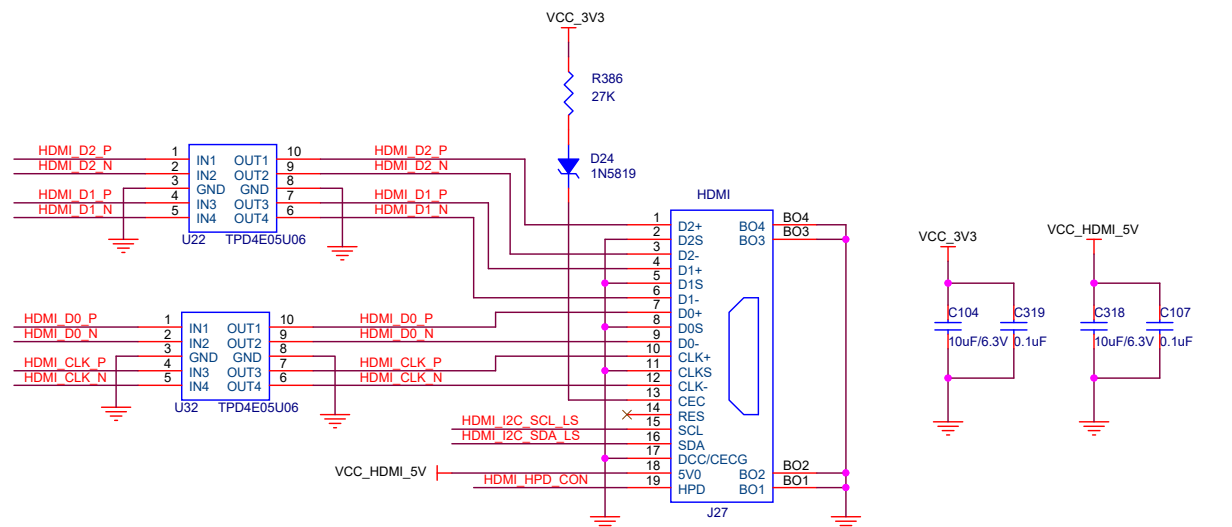
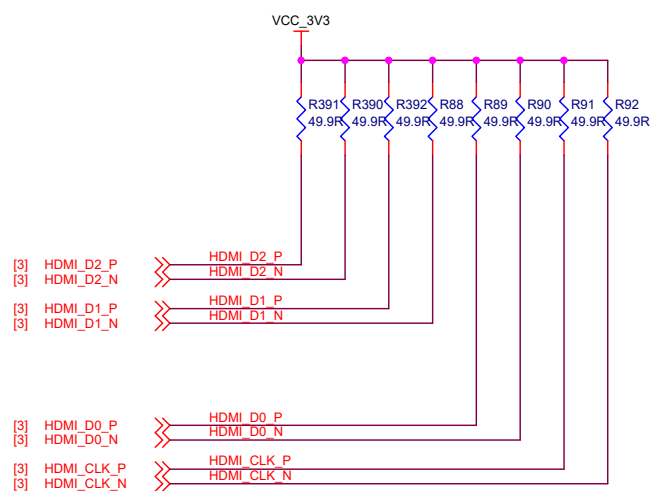


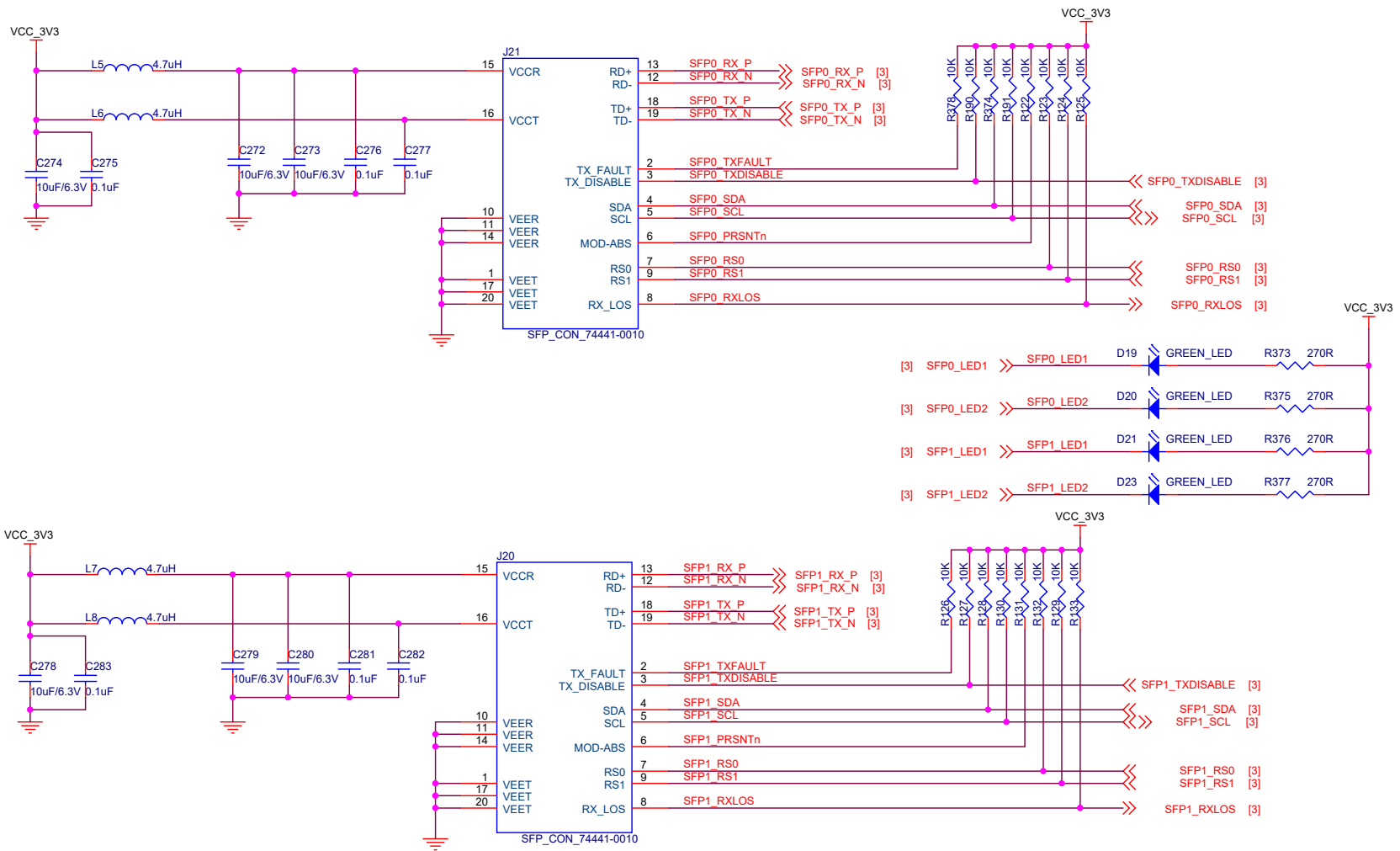
SD CARD

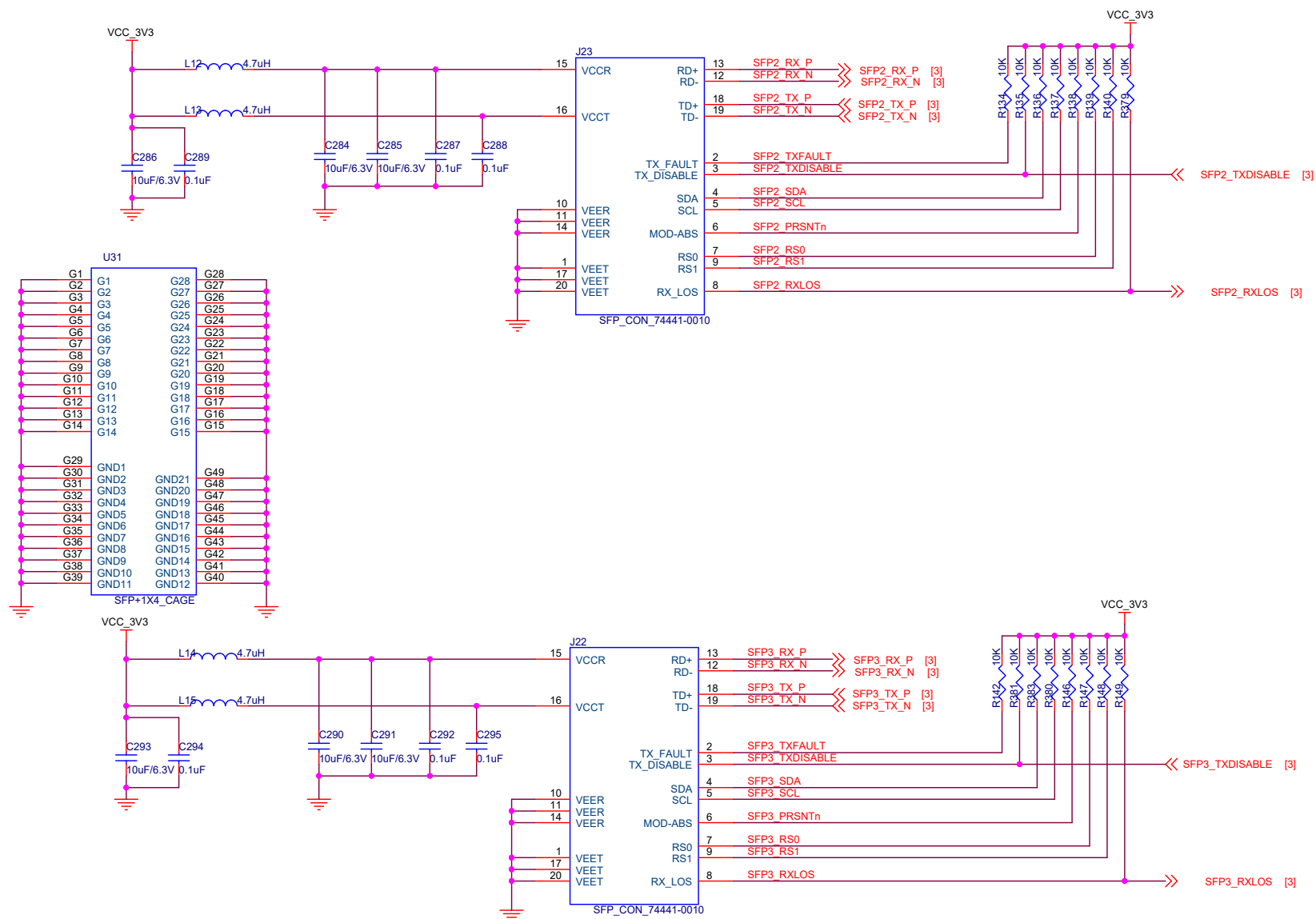


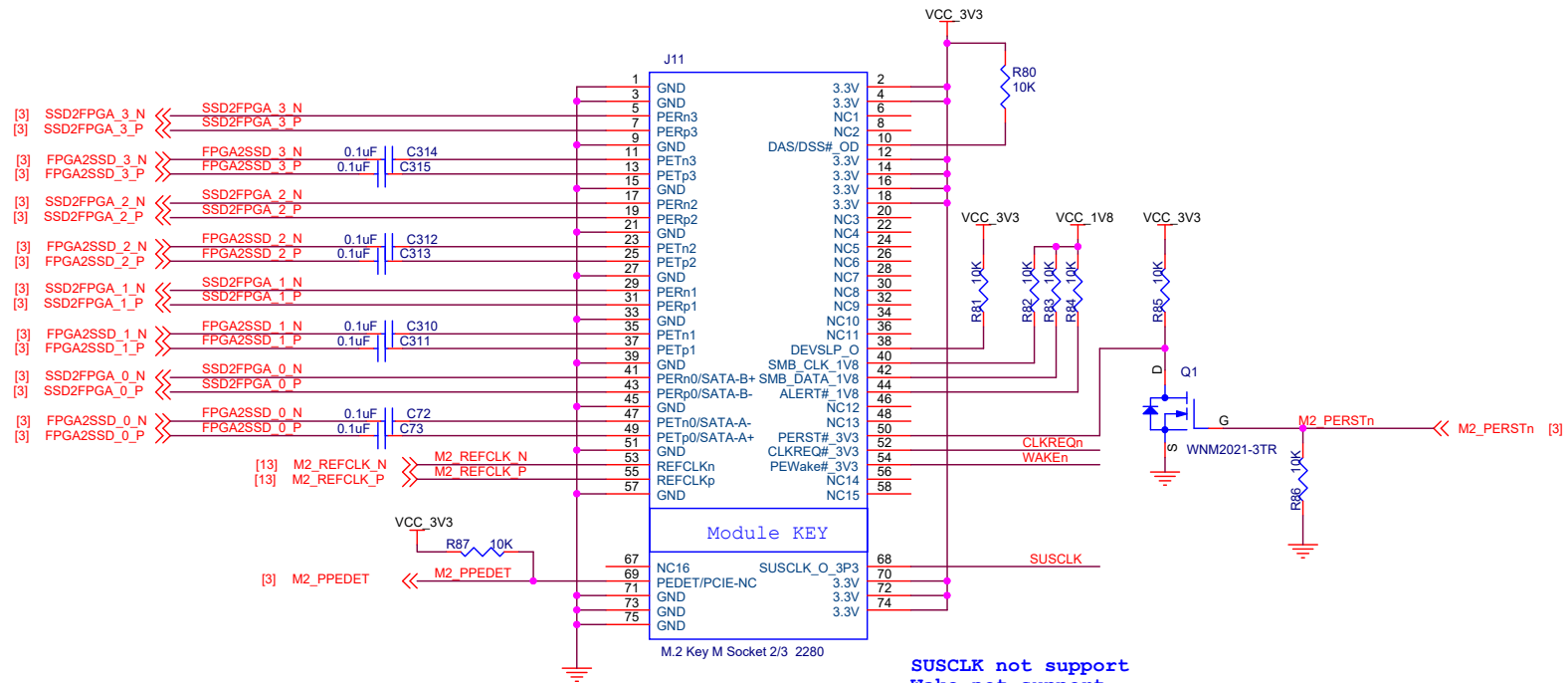


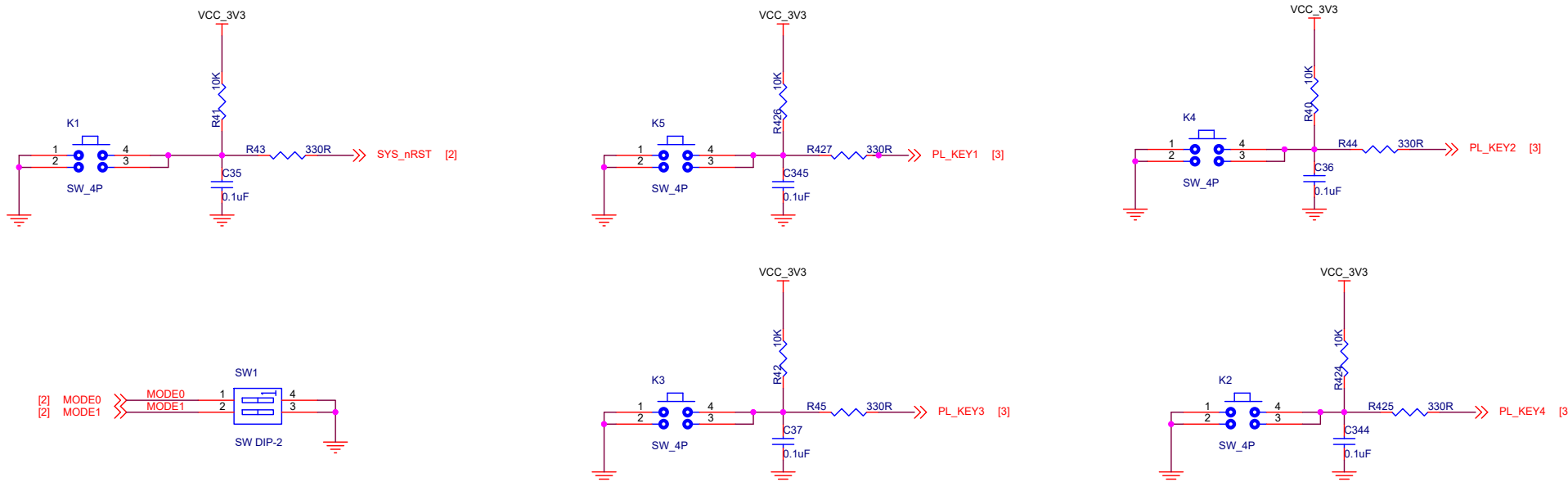
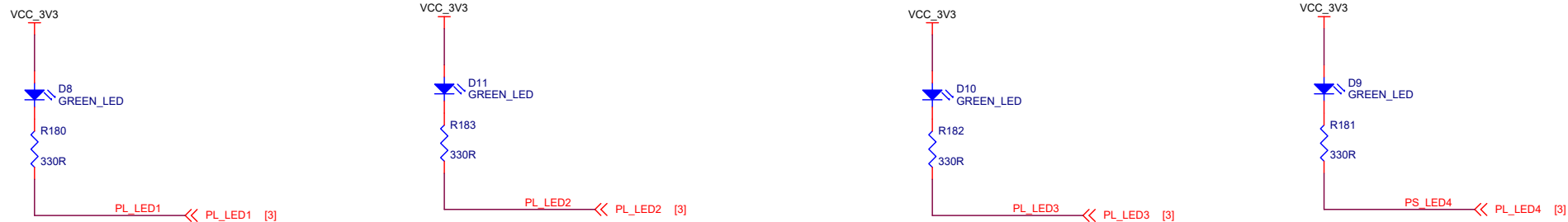
PL HDMI-TX



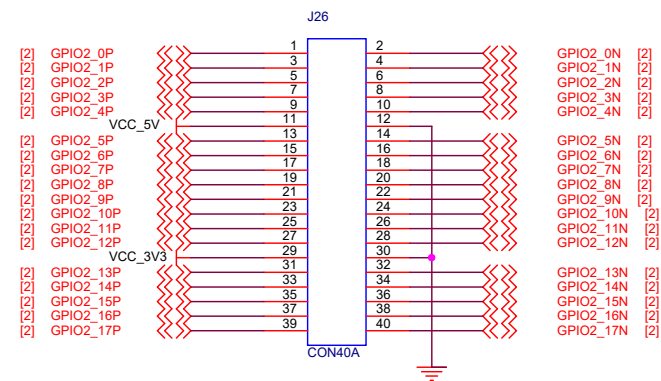
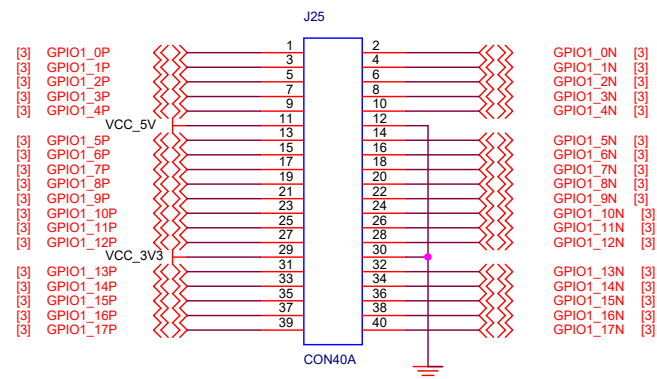




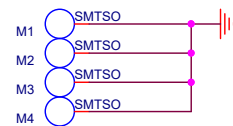
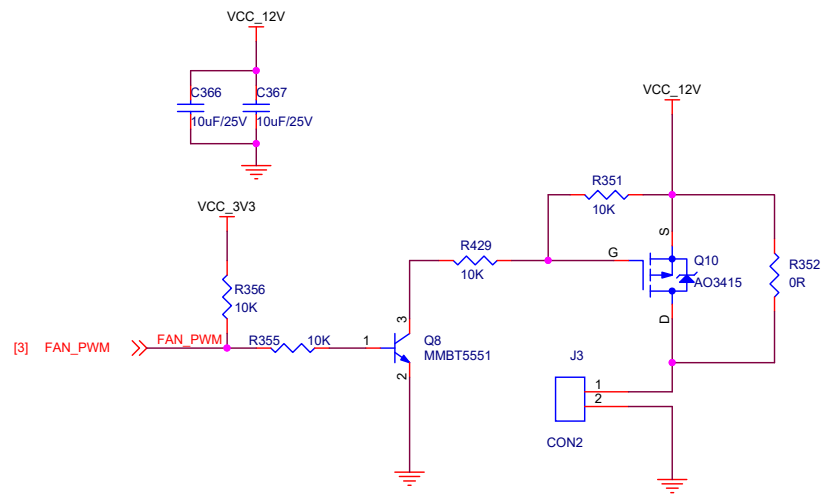




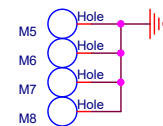
MODE	MODE0 SW1.1	MODE1 SW1.2
JTAG	0	0
QSPI	0	1
SD	1	1



FAN

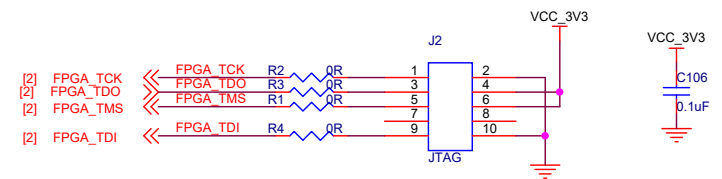


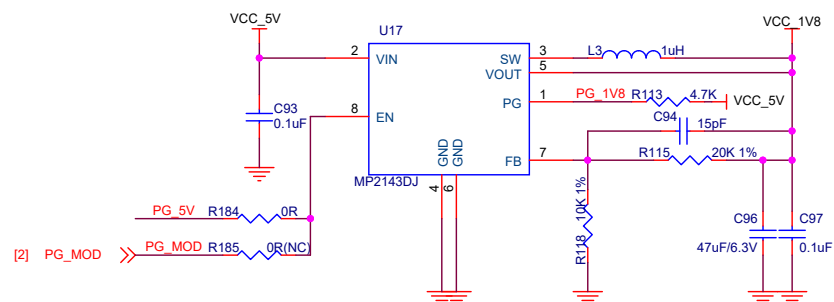
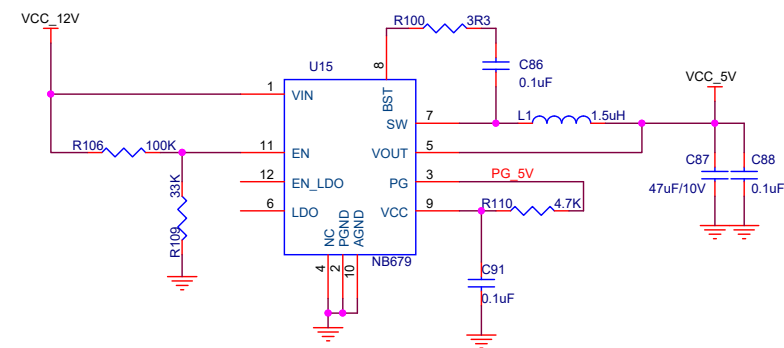
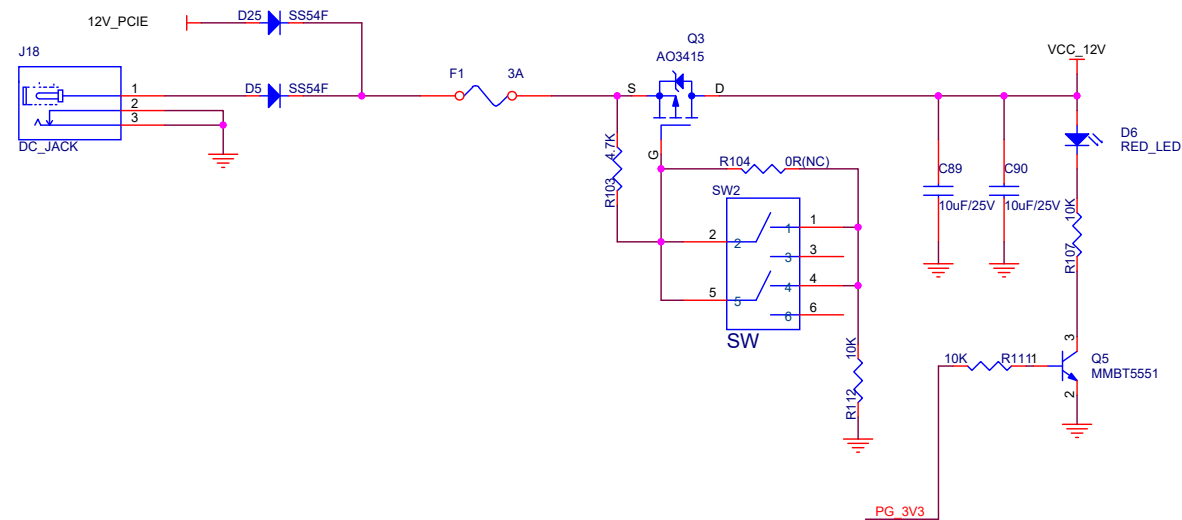
Core Board Fixed



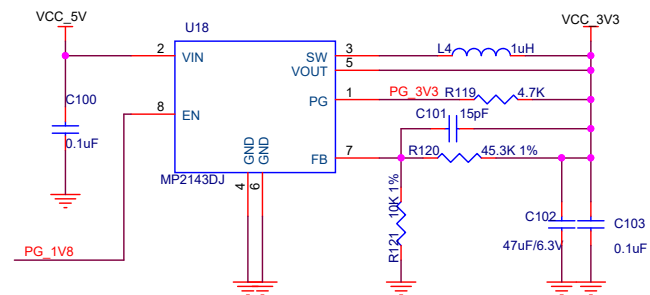
Mount.Hole

JTAG





Vref = 0.6V VOUT = 1.8V



Vref = 0.6V VOUT = 3.3V