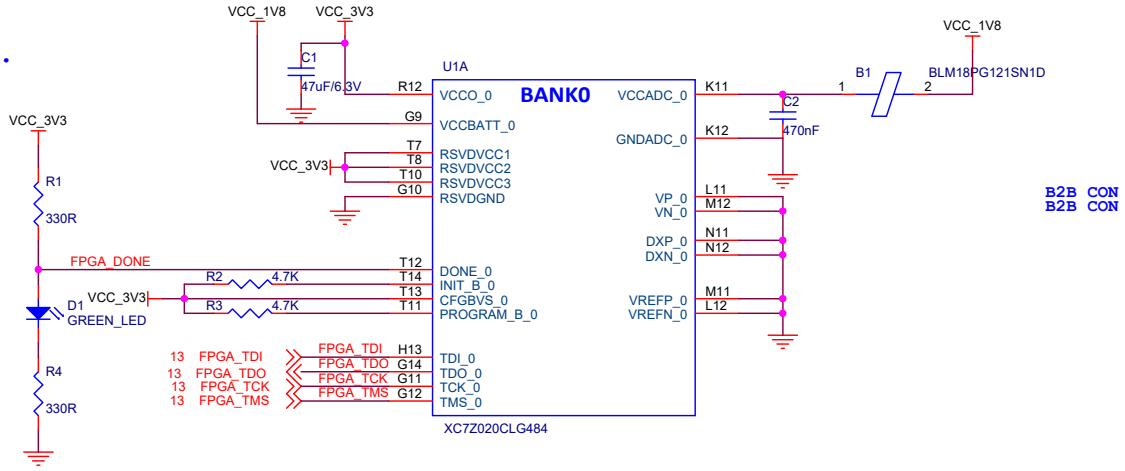
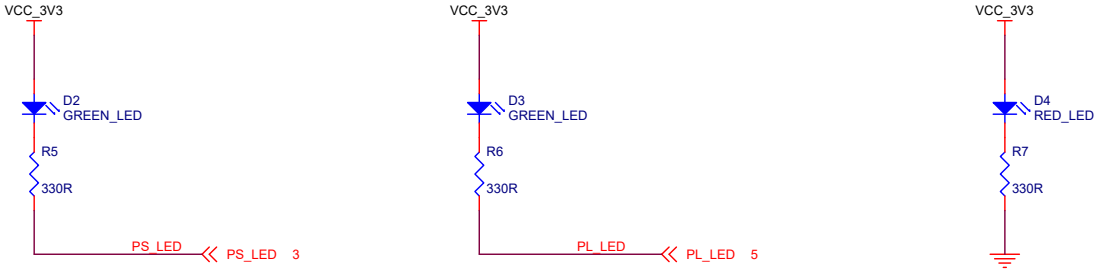
Title	<Title>
Size: B	Document Number: XME0720 Schematic
Rev: 1	
Date: Thursday, March 07, 2019	Sheet 1 of 14

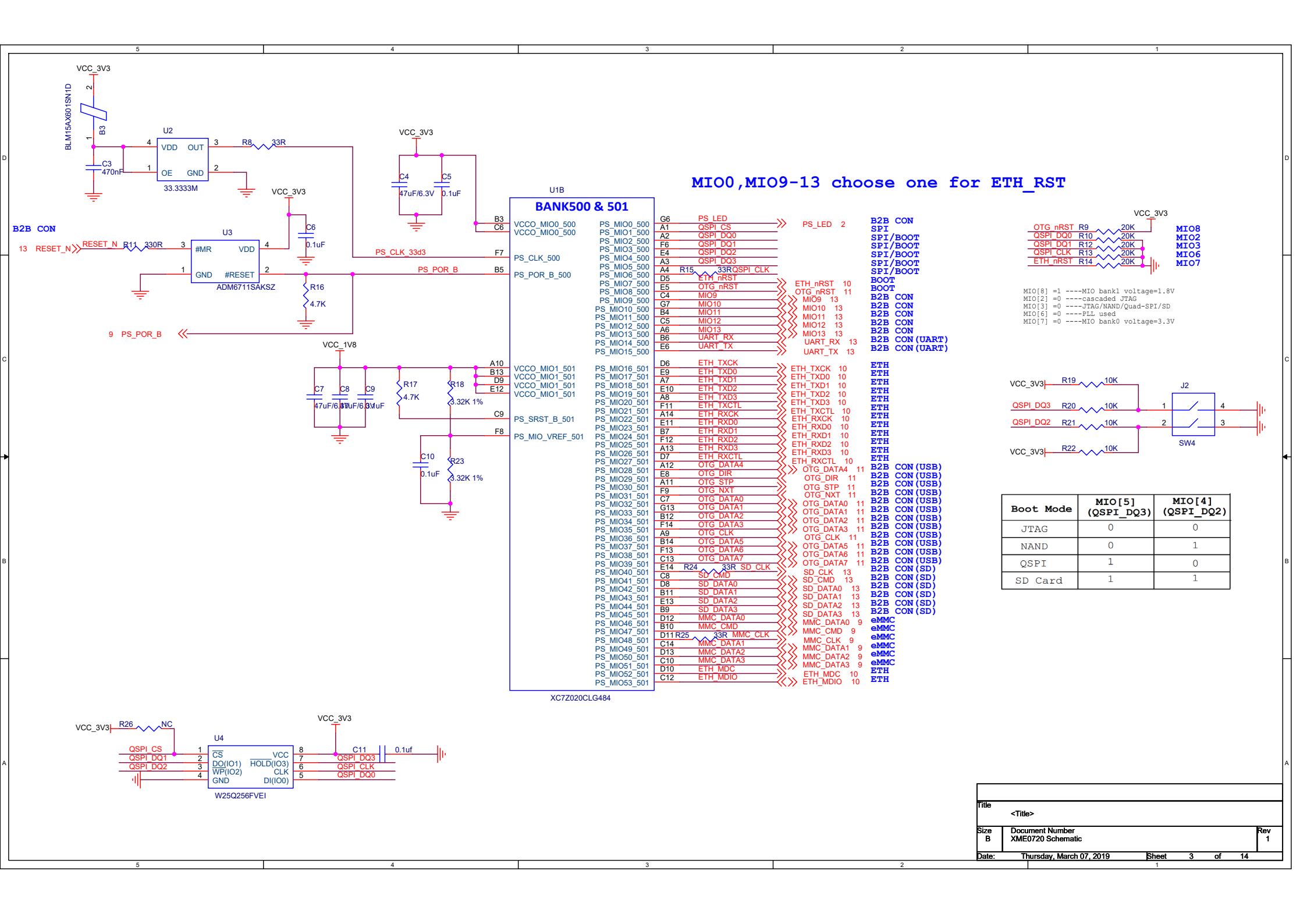
LEDs Layout Place together.



add user led and Power LED



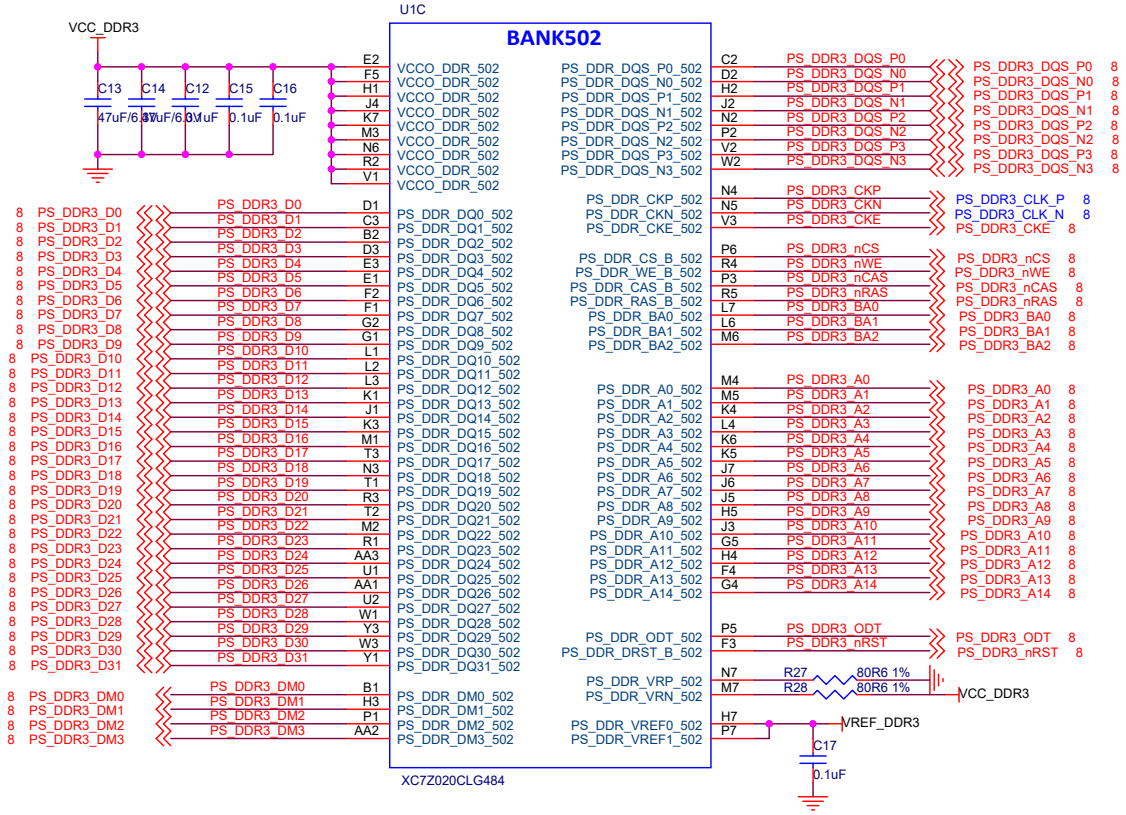
Title	<Title>	
Size B	Document Number XME0720 Schematic	Rev 1
Date: Thursday, March 07, 2019	Sheet 2 of 14	

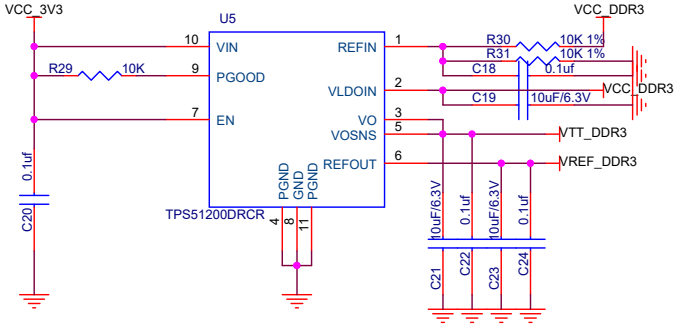


Boot Mode	MIO[5] (QSPI_DQ3)	MIO[4] (QSPI_DQ2)
JTAG	0	0
NAND	0	1
QSPI	1	0
SD Card	1	1

Title	<Title>		
Size B	Document Number XME0720 Schematic		Rev 1
Date: Thursday, March 07, 2019	Sheet 3	of 14	

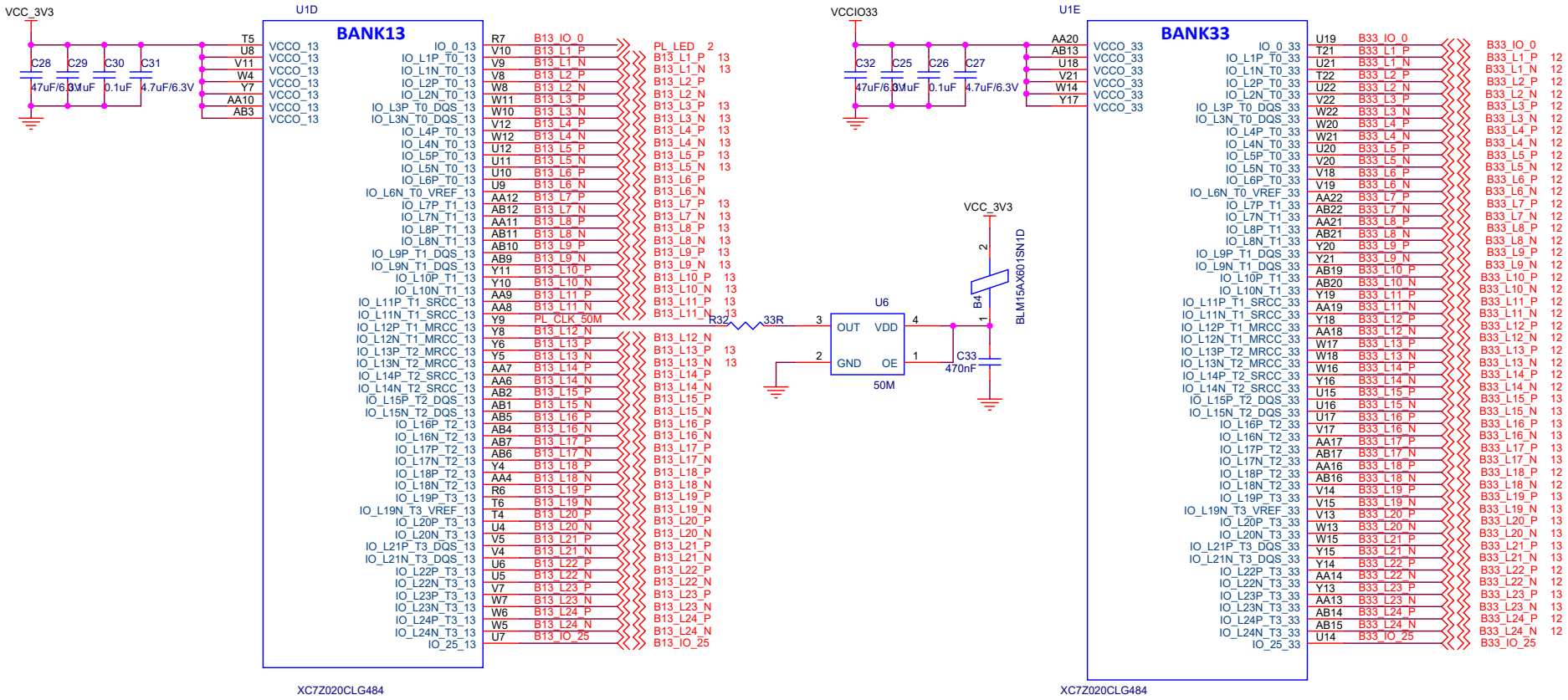
Double Check DDR3 signal Impendence
Check UG933 Chapter6



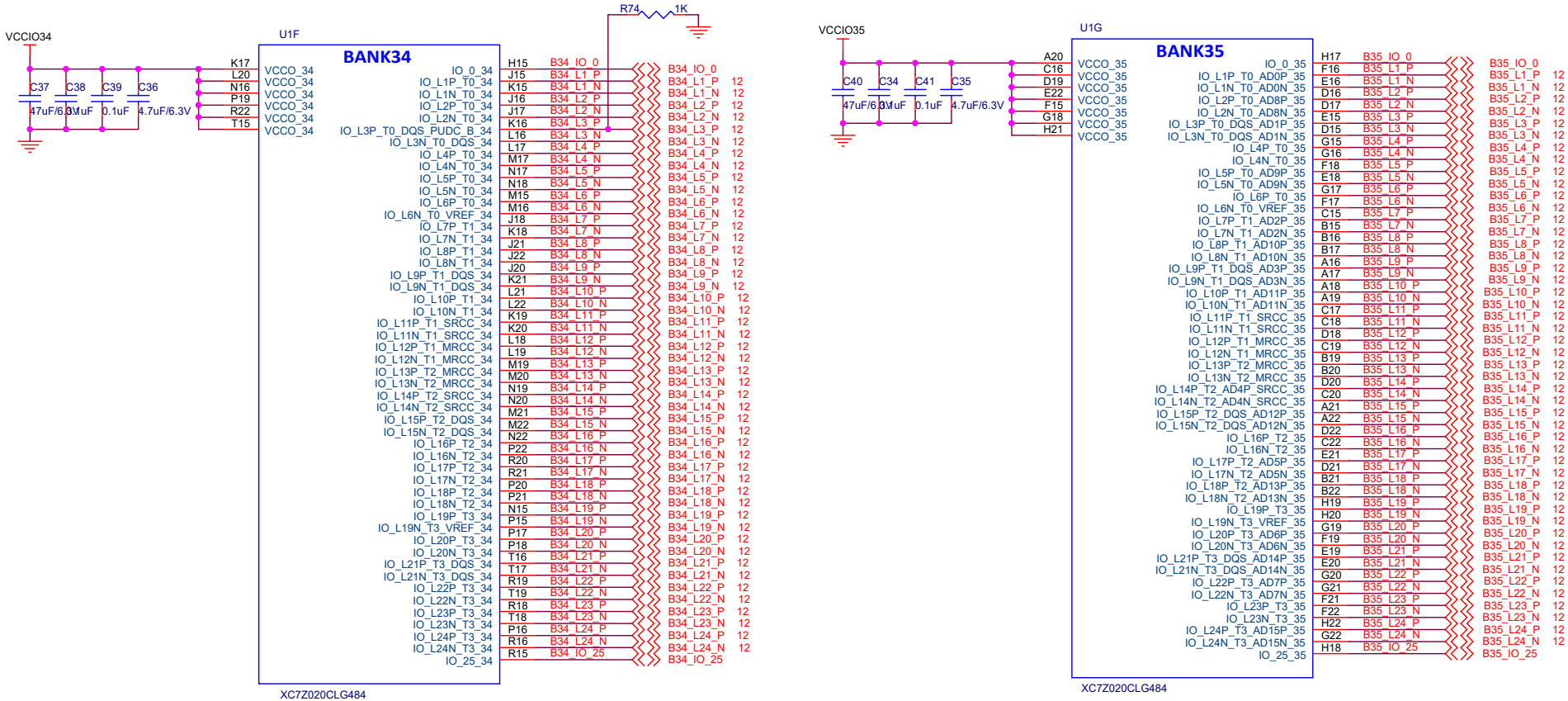


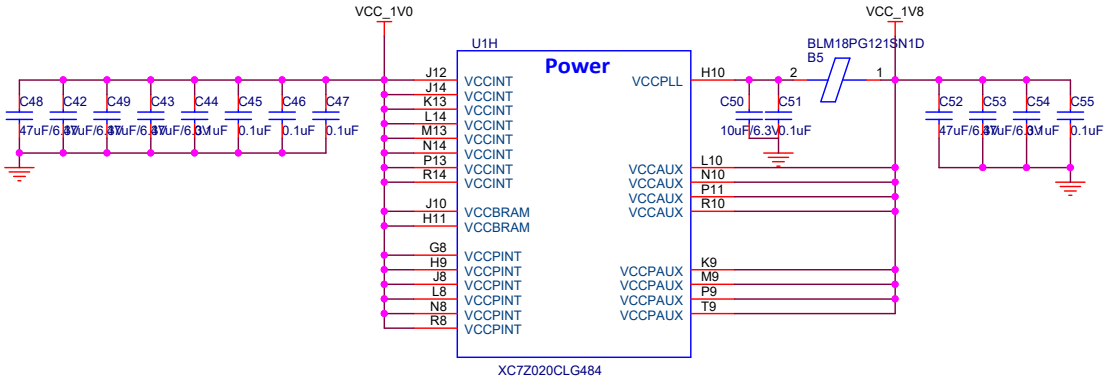
Title	<Title>	
Size B	Document Number XME0720 Schematic	Rev 1
Date: Thursday, March 07, 2019	Sheet 4 of 14	

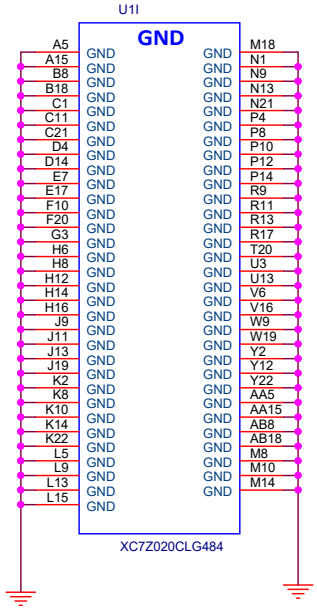
VCCIO13 VOLTAGE TBD



Title	<Title>		
Size B	Document Number XME0720 Schematic		Rev 1
Date: Thursday, March 07, 2019	Sheet 5 of 14		

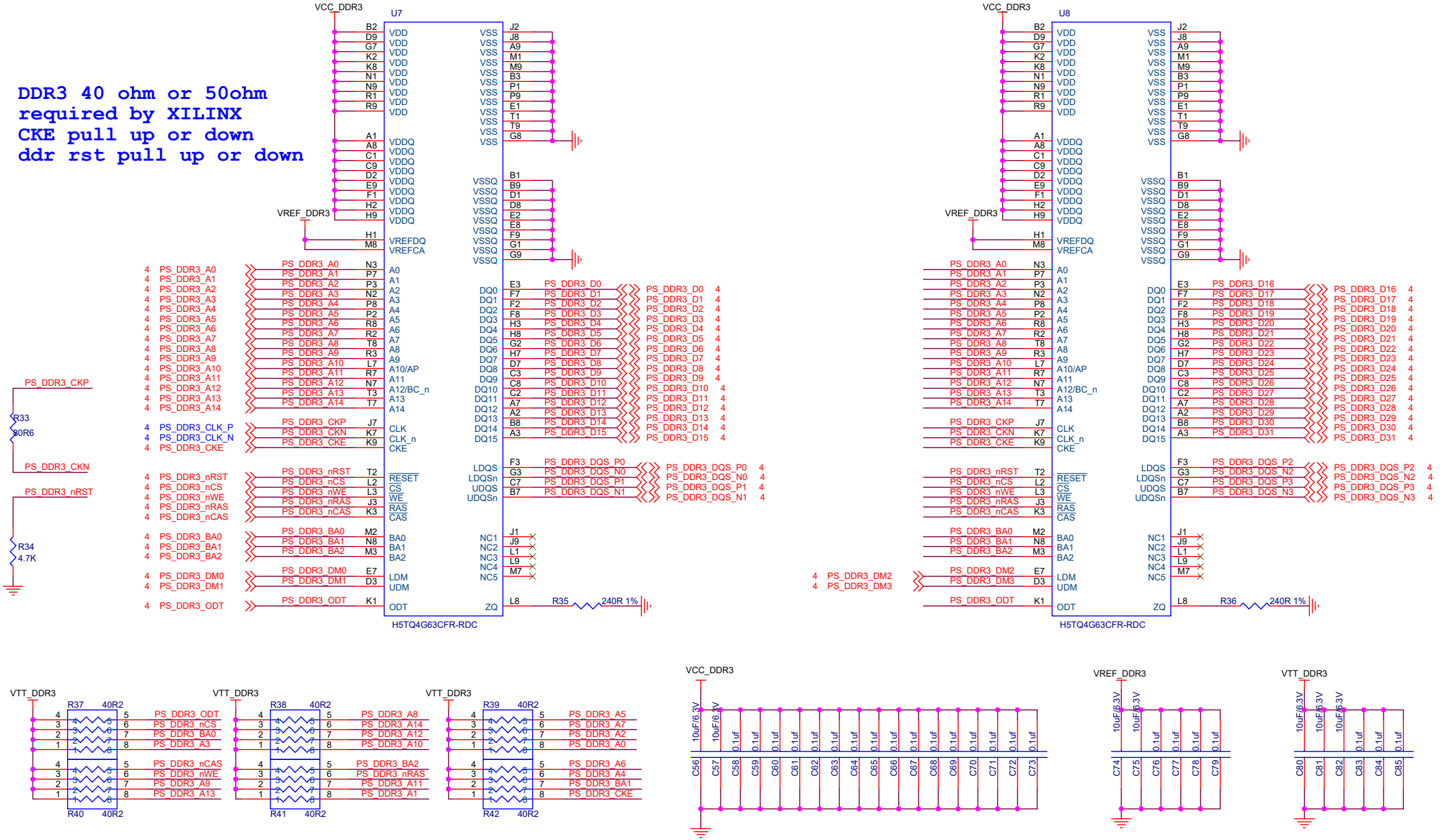

VCCIO34
C37
47uF/6.3V
C38
0.1uF
C39
0.1uF
C36
4.7uF/6.3V
K17
L20
N16
P19
R22
T15
VCCO_34
U1F
BANK34
R74
1K
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_PUDC_B_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
H15 B34_IO_0
J15 B34_L1_P
K15 B34_L1_N
J16 B34_L2_P
J17 B34_L2_N
K16 B34_L3_P
L16 B34_L3_N
L17 B34_L4_P
M17 B34_L4_N
N17 B34_L5_P
N18 B34_L5_N
M15 B34_L6_P
M16 B34_L6_N
J18 B34_L7_P
K18 B34_L7_N
J21 B34_L8_P
J22 B34_L8_N
J20 B34_L9_P
K21 B34_L9_N
L21 B34_L10_P
L22 B34_L10_N
K19 B34_L11_P
K20 B34_L11_N
L18 B34_L12_P
L19 B34_L12_N
M19 B34_L13_P
M20 B34_L13_N
N19 B34_L14_P
N20 B34_L14_N
M21 B34_L15_P
M22 B34_L15_N
N22 B34_L16_P
P22 B34_L16_N
R20 B34_L17_P
R21 B34_L17_N
P20 B34_L18_P
P21 B34_L18_N
N15 B34_L19_P
P15 B34_L19_N
P17 B34_L20_P
P18 B34_L20_N
T16 B34_L21_P
T17 B34_L21_N
R19 B34_L22_P
T19 B34_L22_N
R18 B34_L23_P
T18 B34_L23_N
P16 B34_L24_P
R16 B34_L24_N
R15 B34_IO_25
B34_IO_0
B34_L1_P 12
B34_L1_N 12
B34_L2_P 12
B34_L2_N 12
B34_L3_P 12
B34_L3_N 12
B34_L4_P 12
B34_L4_N 12
B34_L5_P 12
B34_L5_N 12
B34_L6_P 12
B34_L6_N 12
B34_L7_P 12
B34_L7_N 12
B34_L8_P 12
B34_L8_N 12
B34_L9_P 12
B34_L9_N 12
B34_L10_P 12
B34_L10_N 12
B34_L11_P 12
B34_L11_N 12
B34_L12_P 12
B34_L12_N 12
B34_L13_P 12
B34_L13_N 12
B34_L14_P 12
B34_L14_N 12
B34_L15_P 12
B34_L15_N 12
B34_L16_P 12
B34_L16_N 12
B34_L17_P 12
B34_L17_N 12
B34_L18_P 12
B34_L18_N 12
B34_L19_P 12
B34_L19_N 12
B34_L20_P 12
B34_L20_N 12
B34_L21_P 12
B34_L21_N 12
B34_L22_P 12
B34_L22_N 12
B34_L23_P 12
B34_L23_N 12
B34_L24_P 12
B34_L24_N 12
B34_IO_25
XC7Z020CLG484
VCCIO35
C40
47uF/6.3V
C34
0.1uF
C41
0.1uF
C35
4.7uF/6.3V
A20
C16
D19
E22
F15
G18
H21
VCCO_35
U1G
BANK35
IO_0_35
IO_L1P_T0_AD0P_35
IO_L1N_T0_AD0N_35
IO_L2P_T0_AD8P_35
IO_L2N_T0_AD8N_35
IO_L3P_T0_DQS_AD1P_35
IO_L3N_T0_DQS_AD1N_35
IO_L4P_T0_35
IO_L4N_T0_35
IO_L5P_T0_AD9P_35
IO_L5N_T0_AD9N_35
IO_L6P_T0_35
IO_L6N_T0_VREF_35
IO_L7P_T1_AD2P_35
IO_L7N_T1_AD2N_35
IO_L8P_T1_AD10P_35
IO_L8N_T1_AD10N_35
IO_L9P_T1_DQS_AD3P_35
IO_L9N_T1_DQS_AD3N_35
IO_L10P_T1_AD11P_35
IO_L10N_T1_AD11N_35
IO_L11P_T1_SRCC_35
IO_L11N_T1_SRCC_35
IO_L12P_T1_MRCC_35
IO_L12N_T1_MRCC_35
IO_L13P_T2_MRCC_35
IO_L13N_T2_MRCC_35
IO_L14P_T2_AD4P_SRCC_35
IO_L14N_T2_AD4N_SRCC_35
IO_L15P_T2_DQS_AD12P_35
IO_L15N_T2_DQS_AD12N_35
IO_L16P_T2_35
IO_L16N_T2_35
IO_L17P_T2_AD5P_35
IO_L17N_T2_AD5N_35
IO_L18P_T2_AD13P_35
IO_L18N_T2_AD13N_35
IO_L19P_T3_35
IO_L19N_T3_VREF_35
IO_L20P_T3_AD6P_35
IO_L20N_T3_AD6N_35
IO_L21P_T3_DQS_AD14P_35
IO_L21N_T3_DQS_AD14N_35
IO_L22P_T3_AD7P_35
IO_L22N_T3_AD7N_35
IO_L23P_T3_35
IO_L23N_T3_35
IO_L24P_T3_AD15P_35
IO_L24N_T3_AD15N_35
IO_25_35
H17 B35_IO_0
F16 B35_L1_P
E16 B35_L1_N
D16 B35_L2_P
D17 B35_L2_N
E15 B35_L3_P
D15 B35_L3_N
G15 B35_L4_P
G16 B35_L4_N
F18 B35_L5_P
E18 B35_L5_N
G17 B35_L6_P
F17 B35_L6_N
C15 B35_L7_P
B15 B35_L7_N
B16 B35_L8_P
B17 B35_L8_N
A16 B35_L9_P
A17 B35_L9_N
A18 B35_L10_P
A19 B35_L10_N
C17 B35_L11_P
C18 B35_L11_N
D18 B35_L12_P
C19 B35_L12_N
B19 B35_L13_P
B20 B35_L13_N
D20 B35_L14_P
C20 B35_L14_N
A21 B35_L15_P
A22 B35_L15_N
D22 B35_L16_P
C22 B35_L16_N
E21 B35_L17_P
D21 B35_L17_N
B21 B35_L18_P
B22 B35_L18_N
H19 B35_L19_P
H20 B35_L19_N
G19 B35_L20_P
F19 B35_L20_N
E19 B35_L21_P
E20 B35_L21_N
G20 B35_L22_P
G21 B35_L22_N
F21 B35_L23_P
F22 B35_L23_N
H22 B35_L24_P
G22 B35_L24_N
H18 B35_IO_25
B35_IO_0
B35_L1_P 12
B35_L1_N 12
B35_L2_P 12
B35_L2_N 12
B35_L3_P 12
B35_L3_N 12
B35_L4_P 12
B35_L4_N 12
B35_L5_P 12
B35_L5_N 12
B35_L6_P 12
B35_L6_N 12
B35_L7_P 12
B35_L7_N 12
B35_L8_P 12
B35_L8_N 12
B35_L9_P 12
B35_L9_N 12
B35_L10_P 12
B35_L10_N 12
B35_L11_P 12
B35_L11_N 12
B35_L12_P 12
B35_L12_N 12
B35_L13_P 12
B35_L13_N 12
B35_L14_P 12
B35_L14_N 12
B35_L15_P 12
B35_L15_N 12
B35_L16_P 12
B35_L16_N 12
B35_L17_P 12
B35_L17_N 12
B35_L18_P 12
B35_L18_N 12
B35_L19_P 12
B35_L19_N 12
B35_L20_P 12
B35_L20_N 12
B35_L21_P 12
B35_L21_N 12
B35_L22_P 12
B35_L22_N 12
B35_L23_P 12
B35_L23_N 12
B35_L24_P 12
B35_L24_N 12
B35_IO_25
XC7Z020CLG484
Title
<Title>
Size
B
Document Number
XME0720 Schematic
Rev
1
Date:
Thursday, March 07, 2019
Sheet
6
of
14



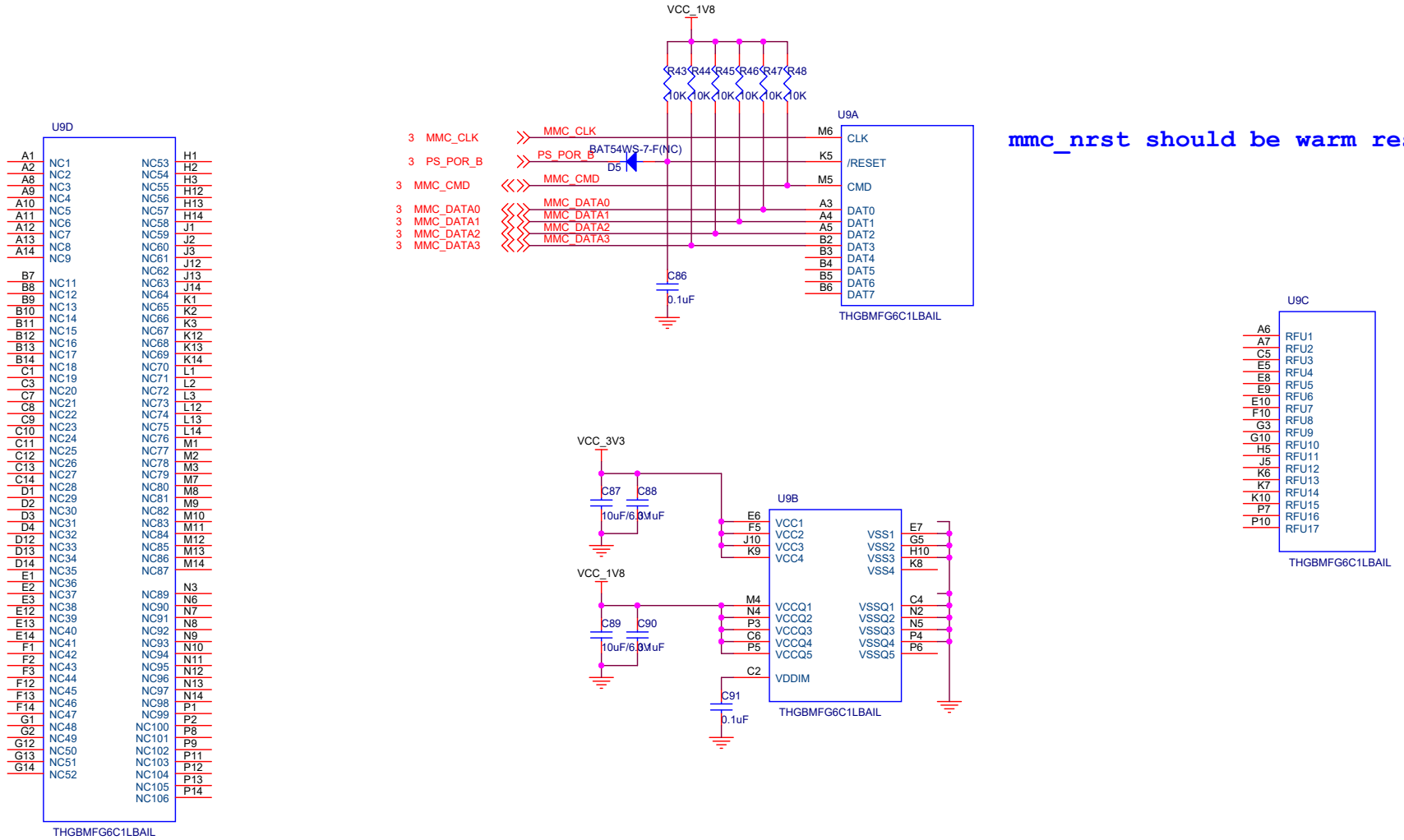


Title	<Title>	
Size B	Document Number XME0720 Schematic	Rev 1
Date: Thursday, March 07, 2019	Sheet 7 of 14	

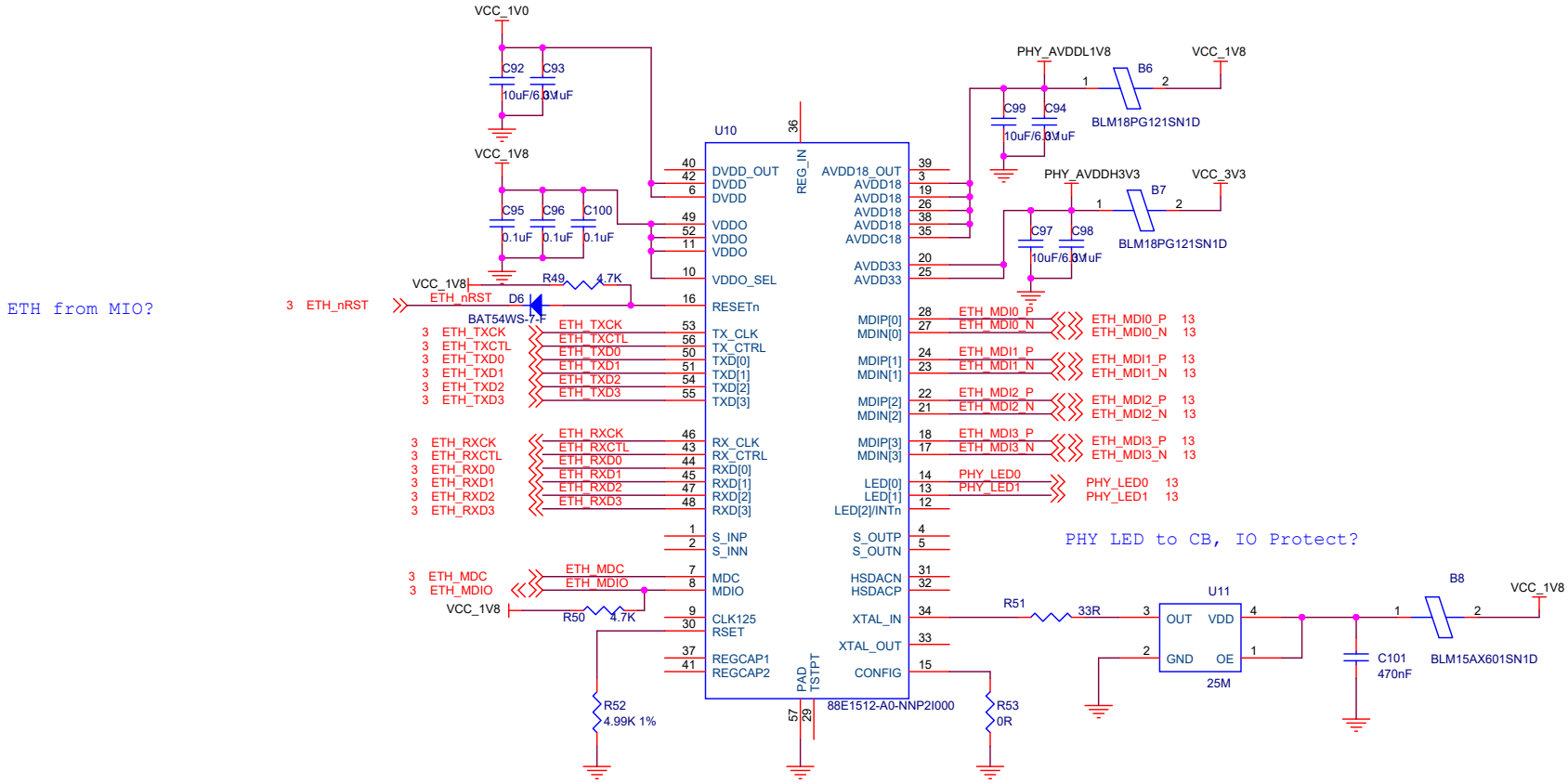
DDR3 40 ohm or 50ohm
required by XILINX
CKE pull up or down
ddr rst pull up or down



Title	<Title>		
Size B	Document Number XME0720 Schematic		Rev 1
Date: Thursday, March 07, 2019	Sheet 8	of 14	

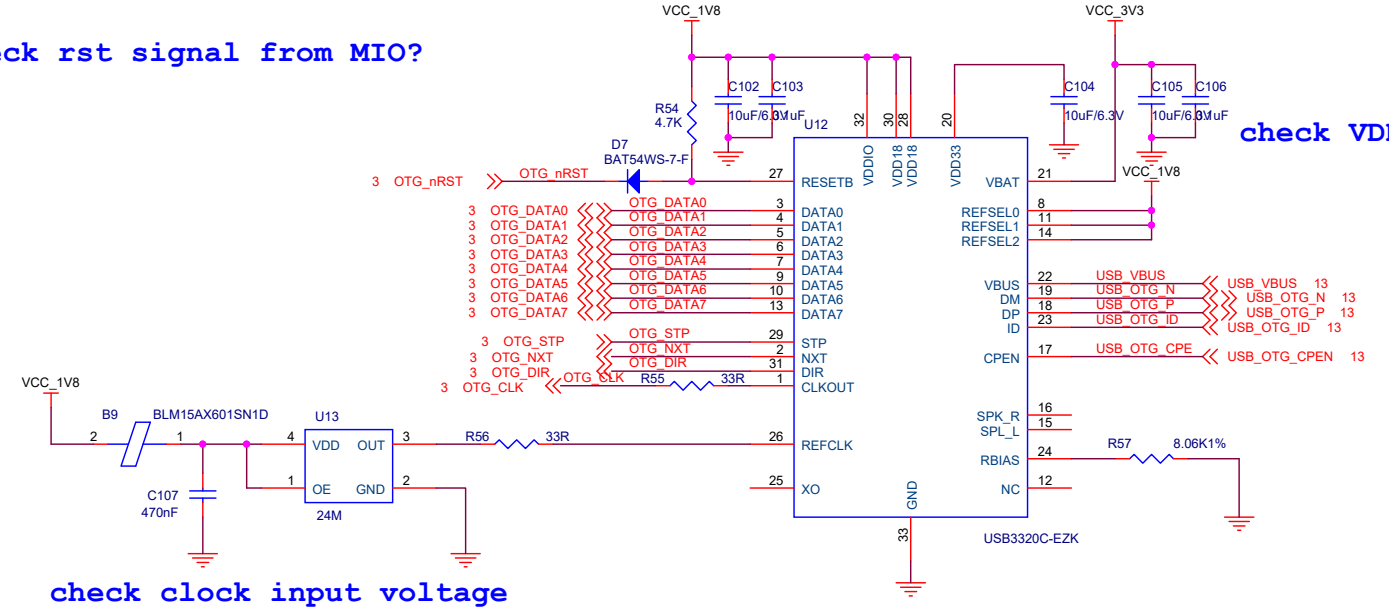


Title	<Title>	
Size B	Document Number XME0720 Schematic	Rev 1
Date: Thursday, March 07, 2019	Sheet 9 of 14	



Title	<Title>	
Size B	Document Number XME0720 Schematic	Rev 1
Date: Thursday, March 07, 2019	Sheet 10 of 14	

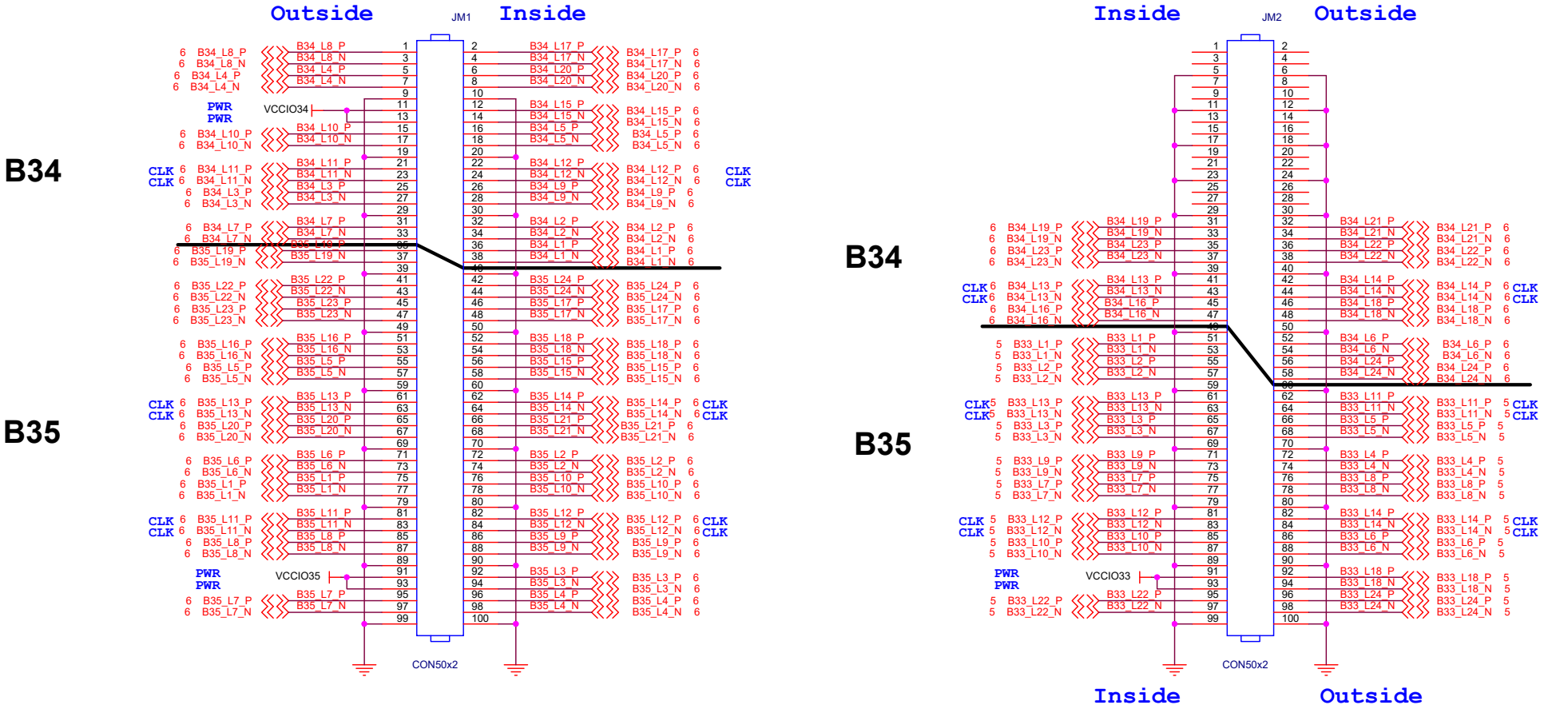
check rst signal from MIO?



check VDD33 output or input

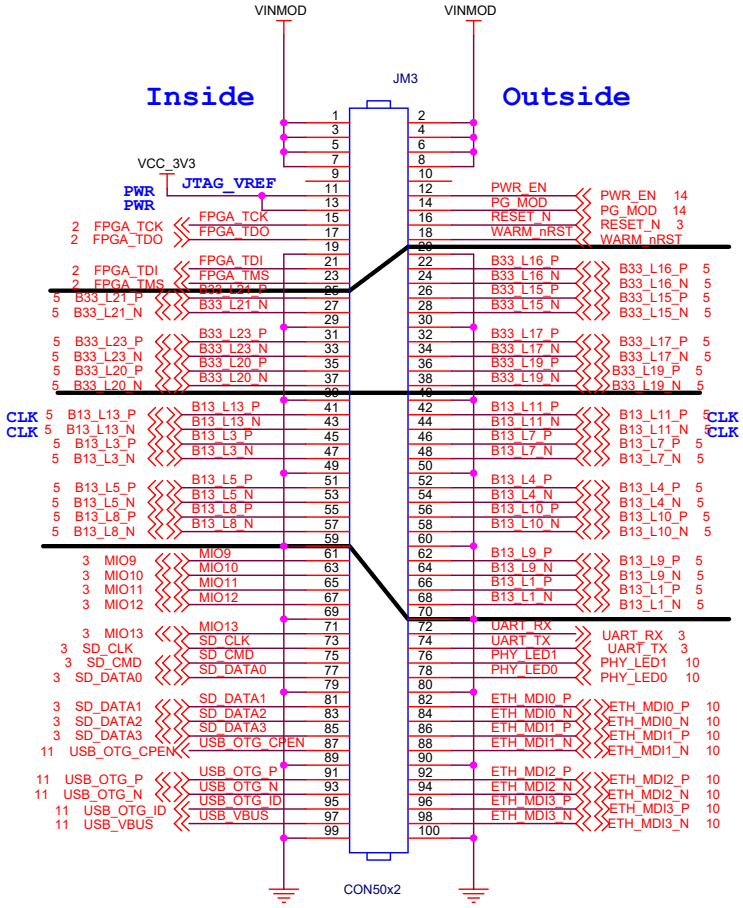
check clock input voltage

Title	<Title>		
Size B	Document Number XME0720 Schematic		Rev 1
Date: Thursday, March 07, 2019		Sheet 11 of 14	



Title	<Title>	
Size B	Document Number XME0720 Schematic	Rev 1
Date: Thursday, March 07, 2019	Sheet 12 of 14	

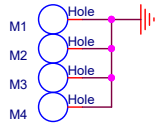
JTAG has not been assigned



B35

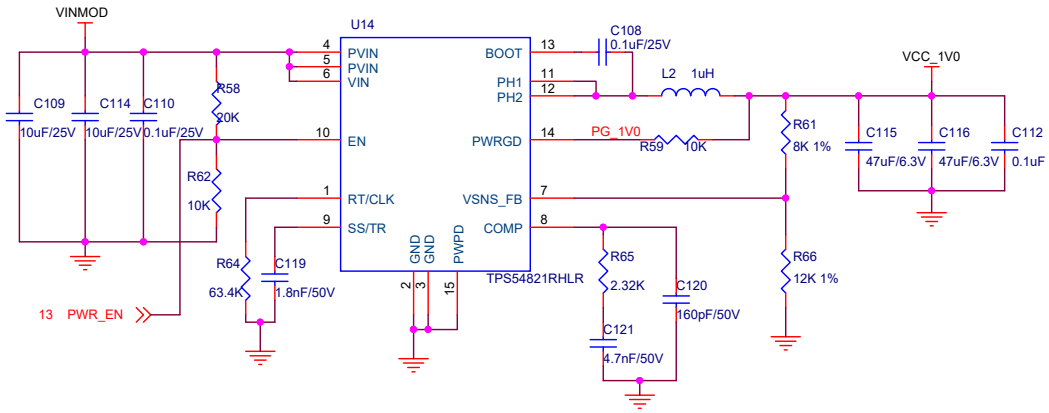
PS

Check PG_1V8, PWR_GOOD Voltage

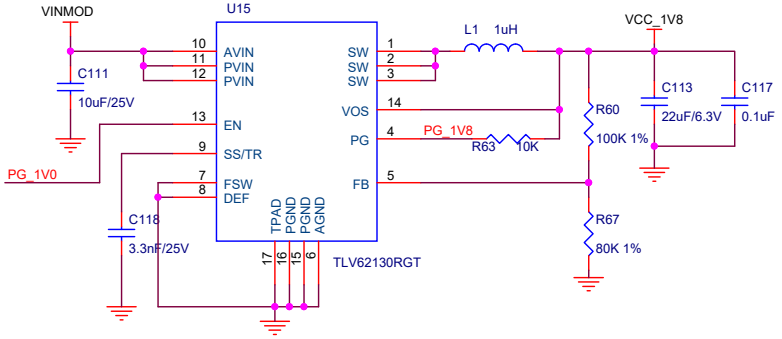


Mount.Hole 3.5mm

Title	<Title>	
Size B	Document Number XME0720 Schematic	Rev 1
Date: Thursday, March 07, 2019	Sheet 13 of 14	

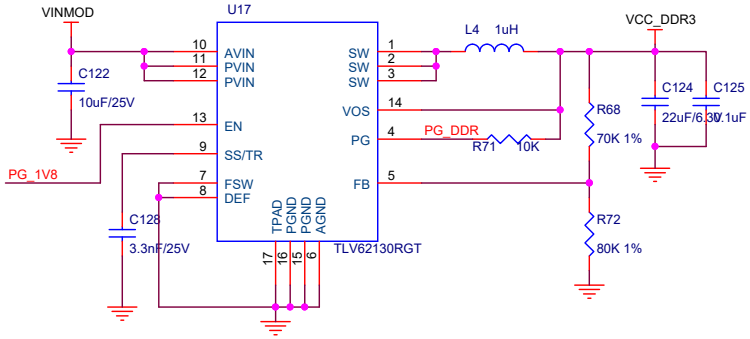


Vref = 0.6V, VOUT = 1.0V

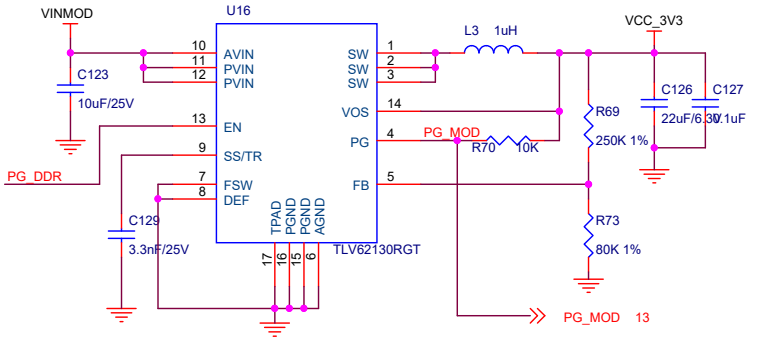


Vref = 0.8V, VOUT = 1.8V

DDRL Check DDR PN and Price



Vref = 0.8V, VOUT = 1.5V



Vref = 0.8V, VOUT = 3.3V

Title	<Title>	
Size B	Document Number XME0720 Schematic	Rev 1
Date: Thursday, March 07, 2019	Sheet 14 of 14	