XME7035 Module

33.33MHz

Power Monitor

QSPI Flash — QSPI0

Bank 500

ARM

Zynq-7000
XC7Z035
-FFG676

FPGA

PS LED — MIO0

UART0

200MHz

Bank 12,13,35 138 IOs(69 differential)
IO voltage adjustable

8x GTP 6.25Gbps

Bank 501

RTL8211F

MIOs

SDIO1 — eMMC

Bank 502 — DDR3 *2

PL LED

Bank 33&34 — DDR3*2

JTAG

MicroPhase   *MicroPhase Inc. www.microphase.cn*

Title
XME7035 FPGA Module

Size	Document Number	Rev
B	Block Diagram	1.2

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BANK0 LED

VCC_1V8 VCC_3V3

VCC_1V8

C1
47uF
6.3V

VCC_3V3

R1
330R

FPGA_DONE

VCC_3V3

R2 4.7K
R3 4.7K

D1
GREEN_LED

R4
330R

U1-1
BANK0

V12	VCCO_0	
V14	VCCO_0	
V15	VCCBATT_0	
W8	RSVDVCC1	
U8	RSVDVCC3	
V8	RSVDVCC2	
V13	RSVDGND	
W9	DONE_0	
R8	INIT_B_0	
T7	CFGBVS_0	
V9	PROGRAM_B_0	
V11	TDI_0	
W10	TDO_0	
W12	TCK_0	
W11	TMS_0	

VCCADC_0 M14
GNDADC_0 M13
VP_0 N14
VN_0 P13
DXP_0 R14
DXN_0 R13
VREFP_0 P14
VREFN_0 N13

XC7Z035-FFG676

B1
1 2
BLM18PG121SN1D

C2
470nF
AGND

AGND

B2 BLM18PG121SN1D
1 2
AGND

[14] FPGA_TDI FPGA_TDI
[14] FPGA_TDO FPGA_TDO
[14] FPGA_TCK FPGA_TCK
[14] FPGA_TMS FPGA_TMS

VCC_3V3

D2
GREEN_LED

R5
330R

PS_LED PS_LED [3]

VCC_3V3

D3
GREEN_LED

R6
330R

PL_LED PL_LED [7]

VCC_3V3

D4
RED_LED

R7
330R

PS BANK500&501

VCC_3V3

BLM15AX601SN1D B3
C3 470nF

U2
VDD OUT
OE   GND
33.3333M
R8 33R

VCC_3V3
C4 47uF C5 0.1uF

U3
#MR VDD
GND #RESET
STM811TW16F

B2B CON
[14] SYS_nRST SYS_nRST R15 330R
PS_POR_B

[12] PS_POR_B

VCC_3V3
C6 0.1uF
R16 4.7K

VCC_1V8
C7 100uF C8 0.1uF
R19 4.7K R20 3.32K 1%
R23 3.32K 1% C9 0.1uF

PS_CLK_33d3

BANK500

U1-2 XC7Z035-FFG676

Pin	Signal
A26	VCCO_MIO0_500
B23	VCCO_MIO0_500
E24	VCCO_MIO0_500
B24	PS_CLK_500
C23	PS_POR_B_500

PS_MIO0_500 ... PS_MIO15_500

Pin	Signal	Net
E26	PS_LED	PS_LED [2] B2B CON
D26	QSPI_CS	SPI
E25	QSPI_DQ0	SPI/BOOT
D25	QSPI_DQ1	SPI/BOOT
F24	QSPI_DQ2	SPI/BOOT
C26	QSPI_DQ3	SPI/BOOT
F23	QSPI_CLK	R14 33R SPI/BOOT
E23	ETH_nRST	BOOT
A24	MIO8	MIO8 [14] BOOT
D24	MIO9	MIO9 B2B CON
A25	MIO10	MIO10 B2B CON
B26	MIO11	MIO11 B2B CON
A23	MIO12	MIO12 B2B CON
B25	MIO13	MIO13 B2B CON
D23	UART_RX	UART_RX [14] B2B CON(UART)
C24	UART_TX	UART_TX [14] B2B CON(UART)

ETH_nRST [13]

BANK501

VCC_1V8

Pin	Signal
C20	VCCO_MIO1_501
D17	VCCO_MIO1_501
F21	VCCO_MIO1_501
G18	VCCO_MIO1_501
K18	VCCO_MIO1_501
H18	PS_MIO_VREF_501
A22	PS_SRST_B_501

PS_MIO16_501 ... PS_MIO53_501

Pin	Signal	Net
G21	ETH_TXCK	ETH_TXCK [13] ETH
G17	ETH_TXD0	ETH_TXD0 [13] ETH
G20	ETH_TXD1	ETH_TXD1 [13] ETH
G19	ETH_TXD2	ETH_TXD2 [13] ETH
H19	ETH_TXD3	ETH_TXD3 [13] ETH
F22	ETH_TXCTL	ETH_TXCTL [13] ETH
G22	ETH_RXCK	ETH_RXCK [13] ETH
F20	ETH_RXD0	ETH_RXD0 [13] ETH
J19	ETH_RXD1	ETH_RXD1 [13] ETH
F19	ETH_RXD2	ETH_RXD2 [13] ETH
H17	ETH_RXD3	ETH_RXD3 [13] ETH
F18	ETH_RXCTL	ETH_RXCTL [13] ETH
J18	MIO28	MIO28 [14] B2B
E20	MIO29	MIO29 [14] B2B
K19	MIO30	MIO30 [14] B2B
E21	MIO31	MIO31 [14] B2B
K17	MIO32	MIO32 [14] B2B
E22	MIO33	MIO33 [14] B2B
J16	MIO34	MIO34 [14] B2B
D19	MIO35	MIO35 [14] B2B
K16	MIO36	MIO36 [14] B2B
D20	MIO37	MIO37 [14] B2B
D21	MIO38	MIO38 [14] B2B
C21	MIO39	MIO39 [14] B2B
C22	MIO40	MIO40 [14] B2B
C19	MIO41	MIO41 [14] B2B
F17	MIO42	MIO42 [14] B2B
D18	MIO43	MIO43 [14] B2B
E18	MIO44	MIO44 [14] B2B
C18	MIO45	MIO45 [14] B2B
E17	MMC_DATA0	MMC_DATA0 [12] eMMC
B19	MMC_CMD	MMC_CMD [12] eMMC
B21	MMC_CLK	R24 33R MMC_CLK eMMC
A18	MMC_DATA1	MMC_DATA1 [12] eMMC
B22	MMC_DATA2	MMC_DATA2 [12] eMMC
B20	MMC_DATA3	MMC_DATA3 [12] eMMC
A20	ETH_MDC	ETH_MDC [13] B2B
A19	ETH_MDIO	ETH_MDIO [13] B2B

VCC_3V3
Net	R	Value	MIO
MIO8	R9	20K	MIO8
QSPI_DQ0	R10	20K	MIO2
QSPI_DQ1	R11	20K	MIO3
QSPI_CLK	R12	20K	MIO6
ETH_nRST	R13	20K	MIO7

MIO[8] =1 ----MIO bank1 voltage=1.8V
MIO[2] =0 ----cascaded JTAG
MIO[3] =0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] =0 ----PLL used
MIO[7] =0 ----MIO bank0 voltage=3.3V

Place DIP Switch ON Carrie board

VCC_3V3 R17 10K
QSPI_DQ3 R18 10K MODE1 MODE1 [14]
QSPI_DQ2 R21 10K MODE0 MODE0 [14]
VCC_3V3 R22 10K

Boot Mode	MIO[5] (QSPI_DQ3)	MIO[4] (QSPI_DQ2)
JTAG	0	0
NAND	0	1
QSPI	1	0
SD Card	1	1

Two QSPI Flash
VCC_3V3 R25 4.7k
U4
Pin		Pin	
1	CS	8	VCC
2	DO(IO1)	7	HOLD(IO3)
3	WP(IO2)	6	CLK
4	GND	5	DI(IO0)
W25Q256FVEI

QSPI_CS, QSPI_DQ1, QSPI_DQ2
QSPI_DQ3, QSPI_CLK, QSPI_DQ0
VCC_3V3 C10 0.1uf

PS BANK502

U1-3

BANK502

XC7Z035-FFG676

Pin	Signal		Pin	Signal	Net	[ref]
H25	VCCO_DDR_502	PS_DDR_DQS_P0_502	H24	PS_DDR3_DQS_P0	PS_DDR3_DQS_P0	[10]
J22	VCCO_DDR_502	PS_DDR_DQS_N0_502	G25	PS_DDR3_DQS_N0	PS_DDR3_DQS_N0	[10]
L26	VCCO_DDR_502	PS_DDR_DQS_P1_502	L24	PS_DDR3_DQS_P1	PS_DDR3_DQS_P1	[10]
M23	VCCO_DDR_502	PS_DDR_DQS_N1_502	L25	PS_DDR3_DQS_N1	PS_DDR3_DQS_N1	[10]
N20	VCCO_DDR_502	PS_DDR_DQS_P2_502	P25	PS_DDR3_DQS_P2	PS_DDR3_DQS_P2	[10]
R24	VCCO_DDR_502	PS_DDR_DQS_N2_502	R25	PS_DDR3_DQS_N2	PS_DDR3_DQS_N2	[10]
T21	VCCO_DDR_502	PS_DDR_DQS_P3_502	W24	PS_DDR3_DQS_P3	PS_DDR3_DQS_P3	[10]
V25	VCCO_DDR_502	PS_DDR_DQS_N3_502	W25	PS_DDR3_DQS_N3	PS_DDR3_DQS_N3	[10]
W22	VCCO_DDR_502					

VCC_DDR3

C12 47uF   C13 47uF   C11 0.1uF   C14 0.1uF   C15 0.1uF

[10]	Net	Pin	Signal
[10]	PS_DDR3_D0	J26	PS_DDR_DQ0_502
[10]	PS_DDR3_D1	F25	PS_DDR_DQ1_502
[10]	PS_DDR3_D2	J25	PS_DDR_DQ2_502
[10]	PS_DDR3_D3	G26	PS_DDR_DQ3_502
[10]	PS_DDR3_D4	H26	PS_DDR_DQ4_502
[10]	PS_DDR3_D5	H23	PS_DDR_DQ5_502
[10]	PS_DDR3_D6	J24	PS_DDR_DQ6_502
[10]	PS_DDR3_D7	J23	PS_DDR_DQ7_502
[10]	PS_DDR3_D8	K26	PS_DDR_DQ8_502
[10]	PS_DDR3_D9	L23	PS_DDR_DQ9_502
[10]	PS_DDR3_D10	M26	PS_DDR_DQ10_502
[10]	PS_DDR3_D11	K23	PS_DDR_DQ11_502
[10]	PS_DDR3_D12	M25	PS_DDR_DQ12_502
[10]	PS_DDR3_D13	N24	PS_DDR_DQ13_502
[10]	PS_DDR3_D14	M24	PS_DDR_DQ14_502
[10]	PS_DDR3_D15	N23	PS_DDR_DQ15_502
[10]	PS_DDR3_D16	R26	PS_DDR_DQ16_502
[10]	PS_DDR3_D17	P24	PS_DDR_DQ17_502
[10]	PS_DDR3_D18	N26	PS_DDR_DQ18_502
[10]	PS_DDR3_D19	P23	PS_DDR_DQ19_502
[10]	PS_DDR3_D20	T24	PS_DDR_DQ20_502
[10]	PS_DDR3_D21	T25	PS_DDR_DQ21_502
[10]	PS_DDR3_D22	T23	PS_DDR_DQ22_502
[10]	PS_DDR3_D23	R23	PS_DDR_DQ23_502
[10]	PS_DDR3_D24	V24	PS_DDR_DQ24_502
[10]	PS_DDR3_D25	U26	PS_DDR_DQ25_502
[10]	PS_DDR3_D26	U24	PS_DDR_DQ26_502
[10]	PS_DDR3_D27	U25	PS_DDR_DQ27_502
[10]	PS_DDR3_D28	W26	PS_DDR_DQ28_502
[10]	PS_DDR3_D29	Y25	PS_DDR_DQ29_502
[10]	PS_DDR3_D30	Y26	PS_DDR_DQ30_502
[10]	PS_DDR3_D31	W23	PS_DDR_DQ31_502

[10]	Net	Pin	Signal
[10]	PS_DDR3_DM0	G24	PS_DDR_DM0_502
[10]	PS_DDR3_DM1	K25	PS_DDR_DM1_502
[10]	PS_DDR3_DM2	P26	PS_DDR_DM2_502
[10]	PS_DDR3_DM3	V26	PS_DDR_DM3_502

Signal	Pin	Net	[ref]
PS_DDR_CKP_502	R21	PS_DDR3_CKP	PS_DDR3_CLK_P [10]
PS_DDR_CKN_502	P21	PS_DDR3_CKN	PS_DDR3_CLK_N [10]
PS_DDR_CKE_502	U21	PS_DDR3_CKE	PS_DDR3_CKE [10]
PS_DDR_CS_B_502	Y21	PS_DDR3_nCS	PS_DDR3_nCS [10]
PS_DDR_RAS_B_502	V23	PS_DDR3_nRAS	PS_DDR3_nRAS [10]
PS_DDR_CAS_B_502	Y23	PS_DDR3_nCAS	PS_DDR3_nCAS [10]
PS_DDR_WE_B_502	V22	PS_DDR3_nWE	PS_DDR3_nWE [10]
PS_DDR_BA0_502	U22	PS_DDR3_BA0	PS_DDR3_BA0 [10]
PS_DDR_BA1_502	T22	PS_DDR3_BA1	PS_DDR3_BA1 [10]
PS_DDR_BA2_502	R22	PS_DDR3_BA2	PS_DDR3_BA2 [10]
PS_DDR_ODT_502	Y22	PS_DDR3_ODT	PS_DDR3_ODT [10]
PS_DDR_DRST_B_502	H22	PS_DDR3_nRST	PS_DDR3_nRST [10]
PS_DDR_A0_502	K22	PS_DDR3_A0	PS_DDR3_A0 [10]
PS_DDR_A1_502	K20	PS_DDR3_A1	PS_DDR3_A1 [10]
PS_DDR_A2_502	N21	PS_DDR3_A2	PS_DDR3_A2 [10]
PS_DDR_A3_502	L22	PS_DDR3_A3	PS_DDR3_A3 [10]
PS_DDR_A4_502	M20	PS_DDR3_A4	PS_DDR3_A4 [10]
PS_DDR_A5_502	N22	PS_DDR3_A5	PS_DDR3_A5 [10]
PS_DDR_A6_502	L20	PS_DDR3_A6	PS_DDR3_A6 [10]
PS_DDR_A7_502	J21	PS_DDR3_A7	PS_DDR3_A7 [10]
PS_DDR_A8_502	T20	PS_DDR3_A8	PS_DDR3_A8 [10]
PS_DDR_A9_502	U20	PS_DDR3_A9	PS_DDR3_A9 [10]
PS_DDR_A10_502	M22	PS_DDR3_A10	PS_DDR3_A10 [10]
PS_DDR_A11_502	H21	PS_DDR3_A11	PS_DDR3_A11 [10]
PS_DDR_A12_502	P20	PS_DDR3_A12	PS_DDR3_A12 [10]
PS_DDR_A13_502	J20	PS_DDR3_A13	PS_DDR3_A13 [10]
PS_DDR_A14_502	R20	PS_DDR3_A14	PS_DDR3_A14 [10]

PS_DDR_VRN_502   V21   R26 80R6 1%
PS_DDR_VRP_502   W21   R27 80R6 1%   VCC_DDR3

PS_DDR_VREF0_502   K21
PS_DDR_VREF1_502   M21   PS_VREF_DDR3

C16 0.1uF

TPS51200DRCR power regulator

U5 TPS51200DRCR

VCC_3V3 — 10 VIN
R28 10K — 9 PGOOD
7 EN
C19 0.1uf

PGND 4 / GND 8 / PGND 11

REFIN 1 — R29 10K 1% / R30 10K 1% — VCC_DDR3
C17 0.1uf
VLDOIN 2 — C18 10uF — VCC_DDR3
VO 3
VOSNS 5 — PS_VTT_DDR3
REFOUT 6 — PS_VREF_DDR3

C20 10uF   C21 0.1uf   C22 10uF   C23 0.1uf

Title: **XME7035 FPGA Module**

Size	Document Number	Rev
B	PS BANK502	1.2

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PL BANK12&13

BANK12 HR — U1-4 (XC7Z035-FFG676)

VCCIO_12

C24 47uF

Pin	Signal		Net	
AA16	VCCO_12			
AB13	VCCO_12			
AC10	VCCO_12			
AD17	VCCO_12			
AE14	VCCO_12			
AF11	VCCO_12			
W14	IO_0_12	B12_IO_0		
Y12	IO_L1P_T0_12	B12_L22_P	B12_L22_P	[15]
Y11	IO_L1N_T0_12	B12_L22_N	B12_L22_N	[15]
AB12	IO_L2P_T0_12	B12_L9_P	B12_L9_P	[15]
AC11	IO_L2N_T0_12	B12_L9_N	B12_L9_N	[15]
Y10	IO_L3P_T0_DQS_12	B12_L24_P	B12_L24_P	[15]
AA10	IO_L3N_T0_DQS_12	B12_L24_N	B12_L24_N	[15]
AB11	IO_L4P_T0_12	B12_L23_P	B12_L23_P	[15]
AB10	IO_L4N_T0_12	B12_L23_N	B12_L23_N	[15]
W13	IO_L5P_T0_12	B12_L5_P	B12_L5_P	[15]
Y13	IO_L5N_T0_12	B12_L5_N	B12_L5_N	[15]
AA13	IO_L6P_T0_12	B12_L10_P	B12_L10_P	[15]
AA12	IO_L6N_T0_VREF_12	B12_L10_N	B12_L10_N	[15]
AE10	IO_L7P_T1_12	B12_L8_P	B12_L8_P	[15]
AD10	IO_L7N_T1_12	B12_L8_N	B12_L8_N	[15]
AE12	IO_L8P_T1_12	B12_L19_P	B12_L19_P	[15]
AF12	IO_L8N_T1_12	B12_L19_N	B12_L19_N	[15]
AE11	IO_L9P_T1_DQS_12	B12_L7_P	B12_L7_P	[15]
AF10	IO_L9N_T1_DQS_12	B12_L7_N	B12_L7_N	[15]
AE13	IO_L10P_T1_12	B12_L20_P	B12_L20_P	[15]
AF13	IO_L10N_T1_12	B12_L20_N	B12_L20_N	[15]
AC12	IO_L11P_T1_SRCC_12	B12_L11_SRCC_P	B12_L11_SRCC_P	[15]
AD11	IO_L11N_T1_SRCC_12	B12_L11_SRCC_N	B12_L11_SRCC_N	[15]
AC13	IO_L12P_T1_MRCC_12	B12_L12_MRCC_P	B12_L12_MRCC_P	[15]
AD13	IO_L12N_T1_MRCC_12	B12_L12_MRCC_N	B12_L12_MRCC_N	[15]
AC14	IO_L13P_T2_MRCC_12	B12_L13_MRCC_P	B12_L13_MRCC_P	[15]
AD14	IO_L13N_T2_MRCC_12	B12_L13_MRCC_N	B12_L13_MRCC_N	[15]
AB15	IO_L14P_T2_SRCC_12	B12_L14_SRCC_P	B12_L14_SRCC_P	[15]
AB14	IO_L14N_T2_SRCC_12	B12_L14_SRCC_N	B12_L14_SRCC_N	[15]
AD16	IO_L15P_T2_DQS_12	B12_L15_P	B12_L15_P	[15]
AD15	IO_L15N_T2_DQS_12	B12_L15_N	B12_L15_N	[15]
AF15	IO_L16P_T2_12	B12_L2_P	B12_L2_P	[15]
AF14	IO_L16N_T2_12	B12_L2_N	B12_L2_N	[15]
AE16	IO_L17P_T2_12	B12_L1_P	B12_L1_P	[15]
AE15	IO_L17N_T2_12	B12_L1_N	B12_L1_N	[15]
AE17	IO_L18P_T2_12	B12_L18_P	B12_L18_P	[15]
AF17	IO_L18N_T2_12	B12_L18_N		
Y17	IO_L19P_T3_12	B12_L17_P	B12_L17_P	[15]
AA17	IO_L19N_T3_VREF_12	B12_L17_N	B12_L17_N	[15]
AB17	IO_L20P_T3_12	B12_L3_P	B12_L3_P	[15]
AB16	IO_L20N_T3_12	B12_L3_N	B12_L3_N	[15]
AC17	IO_L21P_T3_DQS_12	B12_L6_P	B12_L6_P	[15]
AC16	IO_L21N_T3_DQS_12	B12_L6_N	B12_L6_N	[15]
AA15	IO_L22P_T3_12	B12_L21_P	B12_L21_P	[15]
AA14	IO_L22N_T3_12	B12_L21_N	B12_L21_N	[15]
Y16	IO_L23P_T3_12	B12_L16_P	B12_L16_P	[15]
Y15	IO_L23N_T3_12	B12_L16_N	B12_L16_N	[15]
W16	IO_L24P_T3_12	B12_L4_P	B12_L4_P	[15]
W15	IO_L24N_T3_12	B12_L4_N	B12_L4_N	[15]
W17	IO_25_12	B12_IO_25		

BANK13 HR — U1-5 (XC7Z035-FFG676)

VCCIO_13

C25 47uF

Pin	Signal		Net	
AA26	VCCO_13			
AB23	VCCO_13			
AC20	VCCO_13			
AE24	VCCO_13			
AF21	VCCO_13			
Y19	VCCO_13			
V19	IO_0_13	B13_IO_0		
AA25	IO_L1P_T0_13	B13_L17_P	B13_L17_P	[15]
AB25	IO_L1N_T0_13	B13_L17_N	B13_L17_N	[15]
AB26	IO_L2P_T0_13	B13_L6_P	B13_L6_P	[15]
AC26	IO_L2N_T0_13	B13_L6_N	B13_L6_N	[15]
AE25	IO_L3P_T0_DQS_13	B13_L16_P	B13_L16_P	[15]
AE26	IO_L3N_T0_DQS_13	B13_L16_N	B13_L16_N	[15]
AD25	IO_L4P_T0_13	B13_L15_P	B13_L15_P	[15]
AD26	IO_L4N_T0_13	B13_L15_N	B13_L15_N	[15]
AF24	IO_L5P_T0_13	B13_L3_P	B13_L3_P	[15]
AF25	IO_L5N_T0_13	B13_L3_N	B13_L3_N	[15]
AA24	IO_L6P_T0_13	B13_L1_P	B13_L1_P	[15]
AB24	IO_L6N_T0_VREF_13	B13_L1_N	B13_L1_N	[15]
AE22	IO_L7P_T1_13	B13_L18_P	B13_L18_P	[15]
AF22	IO_L7N_T1_13	B13_L18_N	B13_L18_N	[15]
AE23	IO_L8P_T1_13	B13_L4_P	B13_L4_P	[15]
AF23	IO_L8N_T1_13	B13_L4_N	B13_L4_N	[15]
AB21	IO_L9P_T1_DQS_13	B13_L2_P	B13_L2_P	[15]
AB22	IO_L9N_T1_DQS_13	B13_L2_N	B13_L2_N	[15]
AA22	IO_L10P_T1_13	B13_L20_P	B13_L20_P	[15]
AA23	IO_L10N_T1_13	B13_L20_N	B13_L20_N	[15]
AD23	IO_L11P_T1_SRCC_13	B13_L14_SRCC_P	B13_L14_SRCC_P	[15]
AD24	IO_L11N_T1_SRCC_13	B13_L14_SRCC_N	B13_L14_SRCC_N	[15]
AC23	IO_L12P_T1_MRCC_13	B13_L13_MRCC_P	B13_L13_MRCC_P	[15]
AC24	IO_L12N_T1_MRCC_13	B13_L13_MRCC_N	B13_L13_MRCC_N	[15]
AD20	IO_L13P_T2_MRCC_13	B13_L12_MRCC_P	B13_L12_MRCC_P	[15]
AD21	IO_L13N_T2_MRCC_13	B13_L12_MRCC_N	B13_L12_MRCC_N	[15]
AC21	IO_L14P_T2_SRCC_13	B13_L11_SRCC_P	B13_L11_SRCC_P	[15]
AC22	IO_L14N_T2_SRCC_13	B13_L11_SRCC_N	B13_L11_SRCC_N	[15]
AF19	IO_L15P_T2_DQS_13	B13_L23_P	B13_L23_P	[15]
AF20	IO_L15N_T2_DQS_13	B13_L23_N	B13_L23_N	[15]
AE20	IO_L16P_T2_13	B13_L7_P	B13_L7_P	[15]
AE21	IO_L16N_T2_13	B13_L7_N	B13_L7_N	[15]
AD18	IO_L17P_T2_13	B13_L24_P	B13_L24_P	[15]
AD19	IO_L17N_T2_13	B13_L24_N	B13_L24_N	[15]
AE18	IO_L18P_T2_13	B13_L10_P	B13_L10_P	[15]
AF18	IO_L18N_T2_13	B13_L10_N	B13_L10_N	[15]
W20	IO_L19P_T3_13	B13_L19_P	B13_L19_P	[15]
Y20	IO_L19N_T3_VREF_13	B13_L19_N	B13_L19_N	[15]
AA20	IO_L20P_T3_13	B13_L21_P	B13_L21_P	[15]
AB20	IO_L20N_T3_13	B13_L21_N	B13_L21_N	[15]
AC18	IO_L21P_T3_DQS_13	B13_L22_P	B13_L22_P	[15]
AC19	IO_L21N_T3_DQS_13	B13_L22_N	B13_L22_N	[15]
AA19	IO_L22P_T3_13	B13_L8_P	B13_L8_P	[15]
AB19	IO_L22N_T3_13	B13_L8_N	B13_L8_N	[15]
W18	IO_L23P_T3_13	B13_L9_P	B13_L9_P	[15]
W19	IO_L23N_T3_13	B13_L9_N	B13_L9_N	[15]
Y18	IO_L24P_T3_13	B13_L5_P	B13_L5_P	[15]
AA18	IO_L24N_T3_13	B13_L5_N	B13_L5_N	[15]
V18	IO_25_13	B13_IO_25		

PL BANK33&34

BANK33 HP (U1-6)

XC7Z035-FFG676

VCC_DDR3

Pin	Signal
M3	VCCO_33
L6	VCCO_33
J2	VCCO_33
H5	VCCO_33
F1	VCCO_33
E4	VCCO_33

C27 47uF

Pin	IO Signal	Net	External
L9	IO_0_VRN_33		R31 80R6 1% → VCC_DDR3
G4	IO_L1P_T0_33	PL_DDR3_D1	PL_DDR3_D1 [11]
F4	IO_L1N_T0_33	PL_DDR3_D2	PL_DDR3_D2 [11]
D4	IO_L2P_T0_33	PL_DDR3_D4	PL_DDR3_D4 [11]
D3	IO_L2N_T0_33	PL_DDR3_D7	PL_DDR3_D7 [11]
G2	IO_L3P_T0_DQS_33	PL_DDR3_DQS_P0	PL_DDR3_DQS_P0 [11]
F2	IO_L3N_T0_DQS_33	PL_DDR3_DQS_N0	PL_DDR3_DQS_N0 [11]
D1	IO_L4P_T0_33	PL_DDR3_D6	PL_DDR3_D6 [11]
C1	IO_L4N_T0_33	PL_DDR3_D5	PL_DDR3_D5 [11]
E2	IO_L5P_T0_33	PL_DDR3_DM0	PL_DDR3_DM0 [11]
E1	IO_L5N_T0_33	PL_DDR3_D0	PL_DDR3_D0 [11]
F3	IO_L6P_T0_33	PL_DDR3_D3	PL_DDR3_D3 [11]
E3	IO_L6N_T0_VREF_33		PL_VREF_DDR3
J1	IO_L7P_T1_33	PL_DDR3_D9	PL_DDR3_D9 [11]
H1	IO_L7N_T1_33	PL_DDR3_D10	PL_DDR3_D10 [11]
H4	IO_L8P_T1_33	PL_DDR3_D12	PL_DDR3_D12 [11]
H3	IO_L8N_T1_33	PL_DDR3_D11	PL_DDR3_D11 [11]
K2	IO_L9P_T1_DQS_33	PL_DDR3_DQS_P1	PL_DDR3_DQS_P1 [11]
K1	IO_L9N_T1_DQS_33	PL_DDR3_DQS_N1	PL_DDR3_DQS_N1 [11]
H2	IO_L10P_T1_33	PL_DDR3_D15	PL_DDR3_D15 [11]
G1	IO_L10N_T1_33	PL_DDR3_D13	PL_DDR3_D13 [11]
L3	IO_L11P_T1_SRCC_33	PL_DDR3_D14	PL_DDR3_D14 [11]
K3	IO_L11N_T1_SRCC_33	PL_DDR3_D8	PL_DDR3_D8 [11]
J4	IO_L12P_T1_MRCC_33	PL_DDR3_DM1	PL_DDR3_DM1 [11]
J3	IO_L12N_T1_MRCC_33		
M6	IO_L13P_T2_MRCC_33	PL_DDR3_D22	PL_DDR3_D22 [11]
M5	IO_L13N_T2_MRCC_33	PL_DDR3_D23	PL_DDR3_D23 [11]
L5	IO_L14P_T2_SRCC_33	PL_DDR3_D19	PL_DDR3_D19 [11]
L4	IO_L14N_T2_SRCC_33	PL_DDR3_D17	PL_DDR3_D17 [11]
N3	IO_L15P_T2_DQS_33	PL_DDR3_DQS_P2	PL_DDR3_DQS_P2 [11]
N2	IO_L15N_T2_DQS_33	PL_DDR3_DQS_N2	PL_DDR3_DQS_N2 [11]
M2	IO_L16P_T2_33	PL_DDR3_D20	PL_DDR3_D20 [11]
L2	IO_L16N_T2_33	PL_DDR3_D21	PL_DDR3_D21 [11]
N4	IO_L17P_T2_33	PL_DDR3_D18	PL_DDR3_D18 [11]
M4	IO_L17N_T2_33	PL_DDR3_D16	PL_DDR3_D16 [11]
N1	IO_L18P_T2_33	PL_DDR3_DM2	PL_DDR3_DM2 [11]
M1	IO_L18N_T2_33		
M7	IO_L19P_T3_33	PL_DDR3_D27	PL_DDR3_D27 [11]
L7	IO_L19N_T3_VREF_33		PL_VREF_DDR3
K5	IO_L20P_T3_33	PL_DDR3_D31	PL_DDR3_D31 [11]
J5	IO_L20N_T3_33	PL_DDR3_D24	PL_DDR3_D24 [11]
M8	IO_L21P_T3_DQS_33	PL_DDR3_DQS_P3	PL_DDR3_DQS_P3 [11]
L8	IO_L21N_T3_DQS_33	PL_DDR3_DQS_N3	PL_DDR3_DQS_N3 [11]
K6	IO_L22P_T3_33	PL_DDR3_D28	PL_DDR3_D28 [11]
J6	IO_L22N_T3_33	PL_DDR3_D25	PL_DDR3_D25 [11]
N7	IO_L23P_T3_33	PL_DDR3_D29	PL_DDR3_D29 [11]
N6	IO_L23N_T3_33	PL_DDR3_D26	PL_DDR3_D26 [11]
K8	IO_L24P_T3_33	PL_DDR3_D30	PL_DDR3_D30 [11]
K7	IO_L24N_T3_33	PL_DDR3_DM3	PL_DDR3_DM3 [11]
N8	IO_25_VRP_33		R35 80R6 1%

C28 0.1uF
C30 0.1uF

BANK34 HP (U1-7)

XC7Z035-FFG676

VCC_DDR3

Pin	Signal
A6	VCCO_34
B3	VCCO_34
C10	VCCO_34
D7	VCCO_34
G8	VCCO_34
K9	VCCO_34

C26 47uF

Pin	IO Signal	Net	External
K11	IO_0_VRN_34		R32 80R6 1% → VCC_DDR3
J11	IO_L1P_T0_34		
H11	IO_L1N_T0_34		
G6	IO_L2P_T0_34		
G5	IO_L2N_T0_34		R33 1k
H9	IO_L3P_T0_DQS_PUDC_B_34		
G9	IO_L3N_T0_DQS_34		
H7	IO_L4P_T0_34		
H6	IO_L4N_T0_34		
J10	IO_L5P_T0_34		
J9	IO_L5N_T0_34		
J8	IO_L6P_T0_34		
H8	IO_L6N_T0_VREF_34		
F5	IO_L7P_T1_34	PL_DDR3_BA2	PL_DDR3_BA2 [11]
E5	IO_L7N_T1_34	PL_DDR3_A0	PL_DDR3_A0 [11]
D9	IO_L8P_T1_34	PL_DDR3_A10	PL_DDR3_A10 [11]
D8	IO_L8N_T1_34	PL_DDR3_A14	PL_DDR3_A14 [11]
F9	IO_L9P_T1_DQS_34	PL_DDR3_CKE	PL_DDR3_CKE [11]
E8	IO_L9N_T1_DQS_34	PL_DDR3_A9	PL_DDR3_A9 [11]
E6	IO_L10P_T1_34	PL_DDR3_A2	PL_DDR3_A2 [11]
D5	IO_L10N_T1_34		
F8	IO_L11P_T1_SRCC_34		
E7	IO_L11N_T1_SRCC_34		
G7	IO_L12P_T1_MRCC_34	PL_DDR3_CLK_P	PL_DDR3_CLK_P [11]
F7	IO_L12N_T1_MRCC_34	PL_DDR3_CLK_N	PL_DDR3_CLK_N [11]
C8	IO_L13P_T2_MRCC_34	SYS_CLK_P	
C7	IO_L13N_T2_MRCC_34	SYS_CLK_N	
D6	IO_L14P_T2_SRCC_34	PL_DDR3_BA1	PL_DDR3_BA1 [11]
C6	IO_L14N_T2_SRCC_34	PL_DDR3_nCAS	PL_DDR3_nCAS [11]
C9	IO_L15P_T2_DQS_34	PL_DDR3_nRAS	PL_DDR3_nRAS [11]
B10	IO_L15N_T2_DQS_34	PL_DDR3_A13	PL_DDR3_A13 [11]
A10	IO_L16P_T2_34	PL_DDR3_A11	PL_DDR3_A11 [11]
A9	IO_L16N_T2_34	PL_DDR3_A8	PL_DDR3_A8 [11]
A8	IO_L17P_T2_34	PL_DDR3_A1	PL_DDR3_A1 [11]
B7	IO_L17N_T2_34	PL_DDR3_A6	PL_DDR3_A6 [11]
A7	IO_L18P_T2_34	PL_DDR3_A4	PL_DDR3_A4 [11]
C4	IO_L18N_T2_34		
C3	IO_L19P_T3_34		
B5	IO_L19N_T3_VREF_34	PL_DDR3_nRST	PL_DDR3_nRST [11]
B4	IO_L20P_T3_34	PL_DDR3_A7	PL_DDR3_A7 [11]
B6	IO_L20N_T3_34	PL_DDR3_A3	PL_DDR3_A3 [11]
A5	IO_L21P_T3_DQS_34	PL_DDR3_ODT	PL_DDR3_ODT [11]
A4	IO_L21N_T3_DQS_34	PL_DDR3_nCS	PL_DDR3_nCS [11]
A3	IO_L22P_T3_34	PL_DDR3_A5	PL_DDR3_A5 [11]
C2	IO_L22N_T3_34	PL_DDR3_A12	PL_DDR3_A12 [11]
B1	IO_L23P_T3_34	PL_DDR3_BA0	PL_DDR3_BA0 [11]
B2	IO_L23N_T3_34	PL_DDR3_nWE	PL_DDR3_nWE [11]
A2	IO_L24P_T3_34		
K10	IO_L24N_T3_34		
	IO_25_VRP_34		R36 80R6 1%

SYS_CLK_P [6]
SYS_CLK_N [6]
R34 100R 1%

PL_VREF_DDR3
C29 0.1uF
C31 0.1uF

U20 (TPS51200DRCR)

VCC_3V3

Pin	Signal
10	VIN
9	PGOOD
7	EN
1	REFIN
2	VLDOIN
3	VO
5	VOSNS
6	REFOUT
4	PGND
8	GND
11	PGND

R105 10K
R106 10K 1%
R107 10K 1%
C171 0.1uf
C174 10uF
C170 0.1uf
C176 10uF
C173 0.1uf
C175 10uF
C172 0.1uf

VCC_DDR3
PL_VTT_DDR3
PL_VREF_DDR3

U6 (200M)

VCC_3V3
B4 BLM15AX601SN1D

Pin	Signal
1	OE
2	NC
3	GND
6	VDD
5	CLKn
4	CLKp

PLL

C32 0.1uF

SYS_CLK_N [6]
SYS_CLK_P [6]

PL BANK35

VCCIO_35

U1-8

BANK35 HP

C33
47uF

Pin	Signal
A16	VCCO_35
B13	VCCO_35
E14	VCCO_35
F11	VCCO_35
H15	VCCO_35
J12	VCCO_35

IO_0_VRN_35
IO_L1P_T0_AD0P_35
IO_L1N_T0_AD0N_35
IO_L2P_T0_AD8P_35
IO_L2N_T0_AD8N_35
IO_L3P_T0_DQS_AD1P_35
IO_L3N_T0_DQS_AD1N_35
IO_L4P_T0_35
IO_L4N_T0_35
IO_L5P_T0_AD9P_35
IO_L5N_T0_AD9N_35
IO_L6P_T0_35
IO_L6N_T0_VREF_35
IO_L7P_T1_AD2P_35
IO_L7N_T1_AD2N_35
IO_L8P_T1_AD10P_35
IO_L8N_T1_AD10N_35
IO_L9P_T1_DQS_AD3P_35
IO_L9N_T1_DQS_AD3N_35
IO_L10P_T1_AD11P_35
IO_L10N_T1_AD11N_35
IO_L11P_T1_SRCC_35
IO_L11N_T1_SRCC_35
IO_L12P_T1_MRCC_35
IO_L12N_T1_MRCC_35
IO_L13P_T2_MRCC_35
IO_L13N_T2_MRCC_35
IO_L14P_T2_AD4P_SRCC_35
IO_L14N_T2_AD4N_SRCC_35
IO_L15P_T2_DQS_AD12P_35
IO_L15N_T2_DQS_AD12N_35
IO_L16P_T2_35
IO_L16N_T2_35
IO_L17P_T2_AD5P_35
IO_L17N_T2_AD5N_35
IO_L18P_T2_AD13P_35
IO_L18N_T2_AD13N_35
IO_L19P_T3_35
IO_L19N_T3_VREF_35
IO_L20P_T3_AD6P_35
IO_L20N_T3_AD6N_35
IO_L21P_T3_DQS_AD14P_35
IO_L21N_T3_DQS_AD14N_35
IO_L22P_T3_AD7P_35
IO_L22N_T3_AD7N_35
IO_L23P_T3_35
IO_L23N_T3_35
IO_L24P_T3_AD15P_35
IO_L24N_T3_AD15N_35
IO_25_VRP_35

XC7Z035-FFG676

PL_LED

PL_LED [2]

Pin	Net	[ref]
H16		
F12	B35_L1_P	B35_L1_P
E12	B35_L1_N	B35_L1_N
E10	B35_L22_P	B35_L22_P [14]
D10	B35_L22_N	B35_L22_N [14]
G10	B35_L19_P	B35_L19_P [14]
F10	B35_L19_N	B35_L19_N [14]
E11	B35_L20_P	B35_L20_P [14]
D11	B35_L20_N	B35_L20_N [14]
G12	B35_L9_P	B35_L9_P [14]
G11	B35_L9_N	B35_L9_N [14]
F13	B35_L10_P	B35_L10_P [14]
E13	B35_L10_N	B35_L10_N [14]
H13	B35_L24_P	B35_L24_P [14]
H12	B35_L24_N	B35_L24_N [14]
K13	B35_L8_P	B35_L8_P [14]
J13	B35_L8_N	B35_L8_N [14]
K15	B35_L18_P	B35_L18_P [14]
J15	B35_L18_N	B35_L18_N [14]
G16	B35_L6_P	B35_L6_P [14]
G15	B35_L6_N	B35_L6_N [14]
G14	B35_L11_SRCC_P	B35_L11_SRCC_P [14]
F14	B35_L11_SRCC_N	B35_L11_SRCC_N [14]
J14	B35_L12_MRCC_P	B35_L12_MRCC_P [14]
H14	B35_L12_MRCC_N	B35_L12_MRCC_N [14]
D15	B35_L13_MRCC_P	B35_L13_MRCC_P [14]
D14	B35_L13_MRCC_N	B35_L13_MRCC_N [14]
F15	B35_L14_SRCC_P	B35_L14_SRCC_P [14]
E15	B35_L14_SRCC_N	B35_L14_SRCC_N [14]
C17	B35_L7_P	B35_L7_P [14]
C16	B35_L7_N	B35_L7_N [14]
E16	B35_L17_P	B35_L17_P [14]
D16	B35_L17_N	B35_L17_N [14]
B16	B35_L4_P	B35_L4_P [14]
B15	B35_L4_N	B35_L4_N [14]
B17	B35_L15_P	B35_L15_P [14]
A17	B35_L15_N	B35_L15_N [14]
D13	B35_L21_P	B35_L21_P [14]
C13	B35_L21_N	B35_L21_N [14]
C14	B35_L23_P	B35_L23_P [14]
B14	B35_L23_N	B35_L23_N [14]
A15	B35_L5_P	B35_L5_P [14]
A14	B35_L5_N	B35_L5_N [14]
C12	B35_L3_P	B35_L3_P [14]
B12	B35_L3_N	B35_L3_N [14]
C11	B35_L2_P	B35_L2_P [14]
B11	B35_L2_N	B35_L2_N [14]
A13	B35_L16_P	B35_L16_P [14]
A12	B35_L16_N	B35_L16_N [14]
K12	B35_IO_25	

PS BANK111&112

U1-9

MGT PWR

1V_MGTAVCC

C34 C35
4.7uF 0.1uF

1V8_MGTAUX

C38
4.7uF

Pin	Signal		Signal	Pin
AA4	MGTAVCC		MGTAVTT	AB2
AA8	MGTAVCC		MGTAVTT	AC4
AB6	MGTAVCC		MGTAVTT	AD2
AC8	MGTAVCC		MGTAVTT	AE4
AD6	MGTAVCC		MGTAVTT	AF2
AE8	MGTAVCC		MGTAVTT	AF6
R4	MGTAVCC		MGTAVTT	T2
T6	MGTAVCC		MGTAVTT	V2
U4	MGTAVCC		MGTAVTT	W4
Y6	MGTAVCC		MGTAVTT	Y2
V6	MGTVCCAUX		MGTAVTTRCAL_112	AB7
			MGTRREF_112	AB8

1V2_MGTAVTT

C36 C37
4.7uF 0.1uF

R37 100R 1%

The Legnth between Resistor to Pin AB7 and Pin AB8 is the same

BANK111

[15] MGT111_CLK0_P	MGT111_CLK0_P	W6	MGTREFCLK0P_111
[15] MGT111_CLK0_N	MGT111_CLK0_N	W5	MGTREFCLK0N_111
[15] MGT111_CLK1_P	MGT111_CLK1_P	AA6	MGTREFCLK1P_111
[15] MGT111_CLK1_N	MGT111_CLK1_N	AA5	MGTREFCLK1N_111

[15] MGT111_RX0_P	MGT111_RX0_P	AD8	MGTXRXP0_111	MGTXTXP0_111	AF8	MGT111_TX0_P	MGT111_TX0_P [15]
[15] MGT111_RX0_N	MGT111_RX0_N	AD7	MGTXRXN0_111	MGTXTXN0_111	AF7	MGT111_TX0_N	MGT111_TX0_N [15]
[15] MGT111_RX1_P	MGT111_RX1_P	AE6	MGTXRXP1_111	MGTXTXP1_111	AF4	MGT111_TX1_P	MGT111_TX1_P [15]
[15] MGT111_RX1_N	MGT111_RX1_N	AE5	MGTXRXN1_111	MGTXTXN1_111	AF3	MGT111_TX1_N	MGT111_TX1_N [15]
[15] MGT111_RX2_P	MGT111_RX2_P	AC6	MGTXRXP2_111	MGTXTXP2_111	AE2	MGT111_TX2_P	MGT111_TX2_P [15]
[15] MGT111_RX2_N	MGT111_RX2_N	AC5	MGTXRXN2_111	MGTXTXN2_111	AE1	MGT111_TX2_N	MGT111_TX2_N [15]
[15] MGT111_RX3_P	MGT111_RX3_P	AD4	MGTXRXP3_111	MGTXTXP3_111	AC2	MGT111_TX3_P	MGT111_TX3_P [15]
[15] MGT111_RX3_N	MGT111_RX3_N	AD3	MGTXRXN3_111	MGTXTXN3_111	AC1	MGT111_TX3_N	MGT111_TX3_N [15]

BANK112

[15] MGT112_CLK0_P	MGT112_CLK0_P	R6	MGTREFCLK0P_112
[15] MGT112_CLK0_N	MGT112_CLK0_N	R5	MGTREFCLK0N_112
[15] MGT112_CLK1_P	MGT112_CLK1_P	U6	MGTREFCLK1P_112
[15] MGT112_CLK1_N	MGT112_CLK1_N	U5	MGTREFCLK1N_112

[15] MGT112_RX0_P	MGT112_RX0_P	AB4	MGTXRXP0_112	MGTXTXP0_112	AA2	MGT112_TX0_P	MGT112_TX0_P [15]
[15] MGT112_RX0_N	MGT112_RX0_N	AB3	MGTXRXN0_112	MGTXTXN0_112	AA1	MGT112_TX0_N	MGT112_TX0_N [15]
[15] MGT112_RX1_P	MGT112_RX1_P	Y4	MGTXRXP1_112	MGTXTXP1_112	W2	MGT112_TX1_P	MGT112_TX1_P [15]
[15] MGT112_RX1_N	MGT112_RX1_N	Y3	MGTXRXN1_112	MGTXTXN1_112	W1	MGT112_TX1_N	MGT112_TX1_N [15]
[15] MGT112_RX2_P	MGT112_RX2_P	V4	MGTXRXP2_112	MGTXTXP2_112	U2	MGT112_TX2_P	MGT112_TX2_P [15]
[15] MGT112_RX2_N	MGT112_RX2_N	V3	MGTXRXN2_112	MGTXTXN2_112	U1	MGT112_TX2_N	MGT112_TX2_N [15]
[15] MGT112_RX3_P	MGT112_RX3_P	T4	MGTXRXP3_112	MGTXTXP3_112	R2	MGT112_TX3_P	MGT112_TX3_P [15]
[15] MGT112_RX3_N	MGT112_RX3_N	T3	MGTXRXN3_112	MGTXTXN3_112	R1	MGT112_TX3_N	MGT112_TX3_N [15]

XC7Z035-FFG676

ZYNQ POWER

U1-11

GND

Pin	Net	Net	Pin
A1	GND	GND	M11
A11	GND	GND	M15
A21	GND	GND	M17
AA11	GND	GND	M19
AA21	GND	GND	M9
AA3	GND	GND	N10
AA7	GND	GND	N12
AA9	GND	GND	N16
AB1	GND	GND	N18
AB18	GND	GND	N25
AB5	GND	GND	N5
AB9	GND	GND	P1
AC15	GND	GND	P11
AC25	GND	GND	P15
AC3	GND	GND	P17
AC7	GND	GND	P19
AC9	GND	GND	P2
AD1	GND	GND	P22
AD12	GND	GND	P3
AD22	GND	GND	P4
AD5	GND	GND	P5
AD9	GND	GND	P6
AE19	GND	GND	P7
AE3	GND	GND	P9
AE7	GND	GND	R10
AE9	GND	GND	R16
AF1	GND	GND	R18
AF16	GND	GND	R3
AF26	GND	GND	R7
AF5	GND	GND	T1
AF9	GND	GND	T11
B18	GND	GND	T13
B8	GND	GND	T15
C15	GND	GND	T17
C25	GND	GND	T19
C5	GND	GND	T26
D12	GND	GND	T5
D2	GND	GND	T9
D22	GND	GND	U10
E19	GND	GND	U12
E9	GND	GND	U14
F16	GND	GND	U16
F26	GND	GND	U18
F6	GND	GND	U23
G13	GND	GND	U3
G23	GND	GND	U7
G3	GND	GND	V1
H10	GND	GND	V17
H20	GND	GND	V20
J17	GND	GND	V5
J7	GND	GND	V7
K14	GND	GND	W3
K24	GND	GND	W7
K4	GND	GND	Y1
L1	GND	GND	Y14
L10	GND	GND	Y24
L21	GND	GND	Y5
L18	GND	GND	Y7
L16	GND	GND	Y8
L14	GND	GND	Y9
L12	GND	GND	

XC7Z035-FFG676

U1-10

POWER

VCC_1V0

Pin	Net	Net	Pin
L11	VCCINT	VCCPLL	M18
L13	VCCINT		
L15	VCCINT	VCCAUX	N9
M12	VCCINT	VCCAUX	P8
N11	VCCINT	VCCAUX	R9
N15	VCCINT	VCCAUX	T8
P12	VCCINT	VCCAUX	U9
R11	VCCINT	VCCAUX	V10
R15	VCCINT		
T12	VCCINT	VCCAUX_IO_G0	M10
T14	VCCINT	VCCAUX_IO_G0	P10
U11	VCCINT	VCCAUX_IO_G0	T10
U13	VCCINT		
U15	VCCINT	VCCPAUX	L19
		VCCPAUX	N19
L17	VCCPINT	VCCPAUX	R19
N17	VCCPINT	VCCPAUX	U19
P18	VCCPINT		
R17	VCCPINT	VCCBRAM	M16
T18	VCCPINT	VCCBRAM	P16
U17	VCCPINT	VCCBRAM	T16
		VCCBRAM	V16

XC7Z035-FFG676

C43 330uF   C41 330uF   C42 330uF

C48 4.7uF   C49 4.7uF

C54 0.1uF   C55 0.1uF   C56 0.1uF

B5 2 1 VCC_1V8
BLM18PG121SN1D

C39 10uF   C40 0.1uF

VCC_1V8

C44 47uF   C45 47uF   C46 0.1uF   C47 0.1uF

VCC_1V8

C50 100uF   C51 4.7uF   C52 0.1uF   C53 0.1uF

VCC_1V0

C57 0.1uF   C58 4.7uF

PS DDR3 RAM

Schematic — PS DDR3 RAM. Two MT41K256M16 DDR3 devices (U7, U8) with associated address/data nets, VTT parallel termination resistor networks (R42–R47, 51R), and decoupling capacitor banks (C59–C88).

connect to Parrel resistor NET ADJUSTABLE

PL DDR3 RAM

U9 — MT41K256M16

VDD: B2, D9, G7, K2, K8, N1, N9, R1, R9
VSS: J2, J8, A9, M1, M9, B3, P1, P9, E1, T1, T9, G8
VDDQ: A1, A8, C1, C9, D2, E9, F1, H2, H9
VSSQ: B1, B9, D1, D8, E2, E8, F9, G1, G9
VREFDQ: H1
VREFCA: M8

Pin	Addr		Signal	Pin
N3	A0	DQ0	PL_DDR3_D0	E3
P7	A1	DQ1	PL_DDR3_D5	F7
P3	A2	DQ2	PL_DDR3_D3	F2
N2	A3	DQ3	PL_DDR3_D6	F8
P8	A4	DQ4	PL_DDR3_D1	H3
P2	A5	DQ5	PL_DDR3_D7	H8
R8	A6	DQ6	PL_DDR3_D2	G2
R2	A7	DQ7	PL_DDR3_D14	H7
T8	A8	DQ8	PL_DDR3_D8	D7
R3	A9	DQ9	PL_DDR3_D11	C3
L7	A10/AP	DQ10	PL_DDR3_D15	C8
R7	A11	DQ11	PL_DDR3_D12	C2
N7	A12/BC_n	DQ12	PL_DDR3_D9	A7
T3	A13	DQ13	PL_DDR3_D13	A2
T7	A14	DQ14		B8
		DQ15		A3

CLK: J7, CLK_n: K7, CKE: K9
LDQS: F3, LDQSn: G3, UDQS: C7, UDQSn: B7
RESET: T2, CS: L2, WE: L3, RAS: J3, CAS: K3
BA0: M2, BA1: N8, BA2: M3
NC1: J1, NC2: J9, NC3: L1, NC4: L9, NC5: M7
LDM: E7, UDM: D3
ODT: K1, ZQ: L8

R48 80R6
R49 4.7K
R51 240R 1%

PL_DDR3_CKP, PL_DDR3_CKN, PL_DDR3_nRST

PL_DDR3 address signals A0–A14, CLK_P, CLK_N, CKE, nRST, nCS, nWE, nRAS, nCAS, BA0–BA2, DM0, DM1, ODT

U10 — MT41K256M16

VDD: B2, D9, G7, K2, K8, N1, N9, R1, R9
VSS: J2, J8, A9, M1, M9, B3, P1, P9, E1, T1, T9, G8
VDDQ: A1, A8, C1, C9, D2, E9, F1, H2, H9
VSSQ: B1, B9, D1, D8, E2, E8, F9, G1, G9
VREFDQ: H1
VREFCA: M8

Pin	Addr		Signal	Pin
N3	A0	DQ0	PL_DDR3_D16	E3
P7	A1	DQ1	PL_DDR3_D21	F7
P3	A2	DQ2	PL_DDR3_D18	F2
N2	A3	DQ3	PL_DDR3_D19	F8
P8	A4	DQ4	PL_DDR3_D22	H3
P2	A5	DQ5	PL_DDR3_D17	H8
R8	A6	DQ6	PL_DDR3_D23	G2
R2	A7	DQ7	PL_DDR3_D26	H7
T8	A8	DQ8	PL_DDR3_D25	D7
R3	A9	DQ9	PL_DDR3_D30	C3
L7	A10/AP	DQ10	PL_DDR3_D24	C8
R7	A11	DQ11	PL_DDR3_D27	C2
N7	A12/BC_n	DQ12	PL_DDR3_D28	A7
T3	A13	DQ13	PL_DDR3_D29	A2
T7	A14	DQ14	PL_DDR3_D31	B8
		DQ15		A3

CLK: J7, CLK_n: K7, CKE: K9
LDQS: F3, LDQSn: G3, UDQS: C7, UDQSn: B7
RESET: T2, CS: L2, WE: L3, RAS: J3, CAS: K3
BA0: M2, BA1: N8, BA2: M3
NC1: J1, NC2: J9, NC3: L1, NC4: L9, NC5: M7
LDM: E7, UDM: D3
ODT: K1, ZQ: L8

R50 240R 1%

PL_DDR3_D20, PL_DDR3_D16–D31 [6]
PL_DDR3_DQS_P2, PL_DDR3_DQS_N2, PL_DDR3_DQS_P3, PL_DDR3_DQS_N3 [6]
PL_DDR3_DM2, PL_DDR3_DM3 [6]

---

connect to Parrel resistor NET ADJUSTABLE

R52 51R / R55 51R (PL_VTT_DDR3):
PL_DDR3_A13, PL_DDR3_A9, PL_DDR3_A2, PL_DDR3_A0
PL_DDR3_A3, PL_DDR3_A5, PL_DDR3_A7, PL_DDR3_nRAS

R53 51R / R56 51R (PL_VTT_DDR3):
PL_DDR3_BA2, PL_DDR3_nWE, PL_DDR3_A8, PL_DDR3_A14
PL_DDR3_BA1, PL_DDR3_A12, PL_DDR3_A10, PL_DDR3_CKE

R54 51R / R57 51R (PL_VTT_DDR3):
PL_DDR3_A11, PL_DDR3_A6, PL_DDR3_A4, PL_DDR3_A1
PL_DDR3_ODT, PL_DDR3_nCAS, PL_DDR3_nCS, PL_DDR3_BA0

VCC_DDR3 decoupling: C89 10uF, C90 10uF, C91–C106 0.1uF
PL_VREF_DDR3: C107 10uF, C108 10uF, C109–C112 0.1uF
PL_VTT_DDR3: C113 10uF, C114 10uF, C115–C118 0.1uF

eMMC

VCC_1V8

R58 R59 R60 R61 R62 R63
10K 10K 10K 10K 10K 10K

U11A

Pin	Signal
M6	CLK
K5	/RESET
M5	CMD
A3	DAT0
A4	DAT1
A5	DAT2
B2	DAT3
B3	DAT4
B4	DAT5
B5	DAT6
B6	DAT7

THGBMFG6C1LBAIL

[3] MMC_CLK — MMC_CLK
[3] PS_POR_B — PS_POR_B
BAT54WS-7-F(NC)
D5
[3] MMC_CMD — MMC_CMD
MMC_DATA0
[3] MMC_DATA0 — MMC_DATA1
[3] MMC_DATA1 — MMC_DATA2
[3] MMC_DATA2 — MMC_DATA3
[3] MMC_DATA3

C119
0.1uF

U11D

Pin	Signal		Pin	Signal
A1	NC1		H1	NC53
A2	NC2		H2	NC54
A8	NC3		H3	NC55
A9	NC4		H12	NC56
A10	NC5		H13	NC57
A11	NC6		H14	NC58
A12	NC7		J1	NC59
A13	NC8		J2	NC60
A14	NC9		J3	NC61
B7			J12	NC62
B8	NC11		J13	NC63
B9	NC12		J14	NC64
B10	NC13		K1	NC65
B11	NC14		K2	NC66
B12	NC15		K3	NC67
B13	NC16		K12	NC68
B14	NC17		K13	NC69
C1	NC18		K14	NC70
C3	NC19		L1	NC71
C7	NC20		L2	NC72
C8	NC21		L3	NC73
C9	NC22		L12	NC74
C10	NC23		L13	NC75
C11	NC24		L14	NC76
C12	NC25		M1	NC77
C13	NC26		M2	NC78
C14	NC27		M3	NC79
D1	NC28		M7	NC80
D2	NC29		M8	NC81
D3	NC30		M9	NC82
D4	NC31		M11	NC83
D12	NC32		M12	NC84
D13	NC33		M13	NC85
D14	NC34		M14	NC86
E1	NC35			NC87
E2	NC36			
E3	NC37		N3	
E12	NC38		N6	NC89
E13	NC39		N7	NC90
E14	NC40		N8	NC91
F1	NC41		N9	NC92
F2	NC42		N10	NC93
F3	NC43		N11	NC94
F12	NC44		N12	NC95
F13	NC45		N13	NC96
F14	NC46		N14	NC97
G1	NC47		P1	NC98
G2	NC48		P2	NC99
G12	NC49		P8	NC100
G13	NC50		P9	NC101
G14	NC51		P11	NC102
	NC52		P12	NC103
			P13	NC104
			P14	NC105
				NC106

THGBMFG6C1LBAIL

U11C

Pin	Signal
A6	RFU1
A7	RFU2
C5	RFU3
E5	RFU4
E8	RFU5
E9	RFU6
E10	RFU7
F10	RFU8
G3	RFU9
G10	RFU10
H5	RFU11
J5	RFU12
K6	RFU13
K7	RFU14
K10	RFU15
P7	RFU16
P10	RFU17

THGBMFG6C1LBAIL

VCC_3V3

C120 C121
10uF 0.1uF

VCC_1V8

C122 C123
10uF 0.1uF

C124
0.1uF

U11B

Pin	Signal		Signal	Pin
E6	VCC1		VSS1	E7
F5	VCC2		VSS2	G5
J10	VCC3		VSS3	H10
K9	VCC4		VSS4	K8
M4	VCCQ1		VSSQ1	C4
N4	VCCQ2		VSSQ2	N2
P3	VCCQ3		VSSQ3	N5
C6	VCCQ4		VSSQ4	P4
P5	VCCQ5		VSSQ5	P6
C2	VDDIM			

THGBMFG6C1LBAIL

PS ETH

VCC_1V0

C125 C126
10uF 0.1uF

VCC_1V8

VCC_3V3

C127
0.1uF

C131 C128
0.1uF 0.1uF

PHY_AVDDL1V0

C129 C130
10uF 0.1uF

B6   VCC_1V0
1   2
BLM15AX601SN1D

PHY_AVDDH3V3

C132 C133
10uF 0.1uF

B7   VCC_3V3
1   2
BLM15AX601SN1D

U12

Pin	Signal		Signal	Pin
28	DVDD_RG		AVDD10	38
21	DVDD10		AVDD10	8
29	DVDD33		AVDD10	3
20	TXC		AVDD33	40
19	TXCTL		AVDD33	11
18	TXD[0]			
17	TXD[1]		MDIP[0]	1
16	TXD[2]		MDIN[0]	2
15	TXD[3]		MDIP[1]	4
			MDIN[1]	5
27	RXC/PHYAD1		MDIP[2]	6
26	RXCTL/PHYAD2		MDIN[2]	7
25	RXD[0]/RXDLY		MDIP[3]	9
24	RXD[1]/TXDLY		MDIN[3]	10
23	RXD[2]/PLLOFF			
22	RXD[3]/PHYAD0			
13	MDC		LED0/CFG_EXT	32
14	MDIO		LED1/CFG_LDO0	33
31	INTB/PMEB		LED2/CFG_LDO1	34
39	RSET		XTAL_IN	36
30	REG_OUT		XTAL_OUT/EXT_CLK	37
12	PHYRSTB		CLKOUT	35

PAD 41

RTL8211FI

ETH_TXCK [3]
ETH_TXCTL [3]
ETH_TXD0 [3]
ETH_TXD1 [3]
ETH_TXD2 [3]
ETH_TXD3 [3]

ETH_RXCK [3]
ETH_RXCTL [3]
ETH_RXD0 [3]
ETH_RXD1 [3]
ETH_RXD2 [3]
ETH_RXD3 [3]

ETH_MDC [3]
ETH_MDIO [3]

VCC_1V8
R64 4.7K

R65 2.49K 1%

R66 4.7K
VCC_1V8

ETH_nRST D6 BAT54WS-7-F
[3] ETH_nRST

ETH_MDI0_P [14]
ETH_MDI0_N [14]
ETH_MDI1_P [14]
ETH_MDI1_N [14]
ETH_MDI2_P [14]
ETH_MDI2_N [14]
ETH_MDI3_P [14]
ETH_MDI3_N [14]

PHY_LED0
PHY_LED1
PHY_LED2

PHY_LED1 [14]
PHY_LED2 [14]

Y1
3 OUT VDD 4
2 GND OE 1
25M_OSC_1.8V 20PPM

R67 33R

C134
0.1uF

B8   VCC_1V8
1   2
BLM15AX601SN1D

VCC_1V8 R68 4.7K(NC) ETH_nRST

ETH_RXCTL R69 4.7K
ETH_RXCK R70 4.7K
PHY Address:001

VCC_1V8 R71 4.7K ETH_RXD3

ETH_RXD2 R72 4.7K
PLL continue

VCC_1V8 R73 4.7K ETH_RXD1 R74 NC
R75 4.7K ETH_RXD0 R76 NC
TX RX Delay

VCC_3V3 R78 4.7K PHY_LED2
PHY_LED1 R79 4.7K
LDO Output:1.8V

VCC_3V3 R77 4.7K PHY_LED0
Use the external Power

MicroPhase MicroPhase Inc. www.microphase.cn

Title
XME7035 FPGA Module

Size
B

Document Number
eMMC

Rev
1.2

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B2B JM1

B2B JM3&4

Inside   JM3   **Outside**

BANK13 / BANK12 (JM3, AXK5A2137YG)

Inside (left) signals:
- [5] B13_L1_P / B13_L1_N
- [5] B13_L2_P / B13_L2_N
- [5] B13_L3_P / B13_L3_N
- [5] B13_L4_P / B13_L4_N
- [5] B13_L11_SRCC_P / B13_L11_SRCC_N (CLK)
- [5] B13_L12_MRCC_P / B13_L12_MRCC_N (CLK)
- [5] B13_L7_P / B13_L7_N
- [5] B13_L8_P / B13_L8_N
- [5] B13_L9_P / B13_L9_N
- [5] B13_L10_P / B13_L10_N
- [5] B13_L5_P / B13_L5_N
- VCCIO_13

Outside (right) signals:
- [5] B13_L17_P / B13_L17_N
- [5] B13_L6_P / B13_L6_N
- [5] B13_L15_P / B13_L15_N
- [5] B13_L16_P / B13_L16_N
- [5] B13_L13_MRCC_P / B13_L13_MRCC_N (CLK)
- [5] B13_L14_SRCC_P / B13_L14_SRCC_N (CLK)
- [5] B13_L18_P / B13_L18_N
- [5] B13_L20_P / B13_L20_N
- [5] B13_L21_P / B13_L21_N
- [5] B13_L22_P / B13_L22_N
- [5] B13_L23_P / B13_L23_N
- [5] B13_L24_P / B13_L24_N

BANK12:
- [5] B12_L1_P / B12_L1_N
- [5] B12_L2_P / B12_L2_N
- [5] B12_L3_P / B12_L3_N
- [5] B12_L4_P / B12_L4_N
- [5] B12_L11_SRCC_P / B12_L11_SRCC_N (CLK)
- [5] B12_L12_MRCC_P / B12_L12_MRCC_N (CLK)
- [5] B12_L7_P / B12_L7_N
- [5] B12_L8_P / B12_L8_N
- [5] B12_L9_P / B12_L9_N
- [5] B12_L10_P / B12_L10_N
- [5] B12_L5_P / B12_L5_N
- VCCIO_12
- [5] B12_L17_P / B12_L17_N
- [5] B12_L6_P / B12_L6_N
- [5] B12_L15_P / B12_L15_N
- [5] B12_L16_P / B12_L16_N
- [5] B12_L13_MRCC_P / B12_L13_MRCC_N (CLK)
- [5] B12_L14_SRCC_P / B12_L14_SRCC_N (CLK)
- [5] B12_L19_P / B12_L19_N
- [5] B12_L20_P / B12_L20_N
- [5] B12_L21_P / B12_L21_N
- [5] B12_L22_P / B12_L22_N
- [5] B12_L23_P / B12_L23_N
- [5] B12_L24_P / B12_L24_N

AXK5A2137YG

Outside   JM4   **Inside**

JM4 (AXK5A2137YG) MGT signals:
- [8] MGT112_CLK0_P / MGT112_CLK0_N — MGT112_CLK1_P / MGT112_CLK1_N [8]
- [8] MGT112_RX3_P / MGT112_RX3_N — MGT112_TX3_P / MGT112_TX3_N [8]
- [8] MGT112_RX2_P / MGT112_RX2_N — MGT112_TX2_P / MGT112_TX2_N [8]
- [8] MGT112_RX1_P / MGT112_RX1_N — MGT112_TX1_P / MGT112_TX1_N [8]
- [8] MGT112_RX0_P / MGT112_RX0_N — MGT112_TX0_P / MGT112_TX0_N [8]
- [8] MGT111_CLK0_P / MGT111_CLK0_N — MGT111_CLK1_P / MGT111_CLK1_N [8]
- [8] MGT111_RX3_P / MGT111_RX3_N — MGT111_TX3_P / MGT111_TX3_N [8]
- [8] MGT111_RX2_P / MGT111_RX2_N — MGT111_TX2_P / MGT111_TX2_N [8]
- [8] MGT111_RX1_P / MGT111_RX1_N — MGT111_TX1_P / MGT111_TX1_N [8]
- [8] MGT111_RX0_P / MGT111_RX0_N — MGT111_TX0_P / MGT111_TX0_N [8]

AXK5A2137YG

M1 Hole / M2 Hole / M3 Hole / M4 Hole

Mount.Hole 3.2mm

Title: **XME7035 FPGA Module**
Size: B
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POWER

R181 NC for A,B version
Mount for C D version

1V@24A

C136 0.1uF/25V

R80
0R

U13

VCCIN_5V

C138 C137
22uF/25V 22uF/25V

R82
150K

R108 R81
0R(NC) 0R(NC)

Pin	Signal
23	BOOT
24	PHASE
1	VIN1
2	VIN2
22	VIN3
26	VIN4
19	EN
12	VDRV
15	VDD
21	MODE1
20	MODE2
14	PGOOD

SW1 9
SW2 8
SW3 7
SW4 6
SW5 5
SW6 29
VOUT 18
FB 17
GL1 10
GL2 11
GL3 28

L1 220nH

VCC_1V0

TP1

C139 C140
0.1uF 330uF

R84
6.65K 1%

R88
10K 1%

[14] PWR_EN

PWR_EN

R83
100K

C141 4.7uF/10V
C142 0.1uF

VCC_LDO

R85
100K

R86 100K
R87 200K

[17] PG_1V

PG_1V

PGND PGND PGND AGND AGND PGND
3 4 13 25 16 27

SiC431AED-T1-GE3

POWER

U14 MP2143DJ

VCCIN_5V

- VIN (2)
- EN (8)
- SW (3)
- VOUT (5)
- PG (1)
- FB (7)
- GND GND (4)(6)

C145 10uF/10V C146 0.1uF

[16] PG_1V ➤ PG_1V

PG_1V8 [18]

TP3

VCC_1V8

L3 1.5uH

PG_1V8 R90 4.7K

C148 15pF

R93 200K 1%

R94 100K 1%

C151 47uF/6.3V C152 0.1uF

1.8V@3A

Vref = 0.6V   VOUT = 1.8V

U15 MP2143DJ

VCCIN_5V

- VIN (2)
- EN (8)
- SW (3)
- VOUT (5)
- PG (1)
- FB (7)
- GND GND (4)(6)

C143 10uF/10V C144 0.1uF

PG_1V8

VCC_DDR3

TP2

L2 1.5uH

PG_DDR R89 4.7K

C147 15pF

R91 126K 1%

R95 100K 1%

C149 47uF/6.3V C150 0.1uF

1.35V@3A

Vref = 0.6V   VOUT = 1.35V

U16 MP2143DJ

VCCIN_5V

- VIN (2)
- EN (8)
- SW (3)
- VOUT (5)
- PG (1)
- FB (7)
- GND GND (4)(6)

C153 10uF/10V C154 0.1uF

PG_1V8

PG_MOD [14]

TP4

VCC_3V3

L4 1.5uH

PG_MOD R96 4.7K

C155 15pF

R97 200K 1%

R98 44.2K 1%

C156 47uF/6.3V C157 0.1uF

3.3V@3A

Vref = 0.6V   VOUT = 3.3V

POWER

VCCIN_5V

PG_MGTAVCC

1V_MGTAVCC

TP5

U17
MP2143DJ

2 VIN
8 EN
SW / VOUT 3 / 5
PG 1
FB 7
GND GND 4 / 6

C158 10uF/10V
C159 0.1uF

L5 1.5uH

1.0V@3A

R99 10K VCCIN_5V

C162 15pF
R100 100K 1%

R101 150K 1%

C163 47uF/6.3V
C164 0.1uF

[17] PG_1V8 PG_1V8

Vref = 0.6V   VOUT = 1.0V

Place it on toplay

VCC_3V3

1V8_MGTAUX

TP6

U18
SPX3819M5-L-1-8

1 VIN VOUT 5
4 ADJ
3 EN
2 GND

C160 0.1uF

C161 0.1uF

VCCIN_5V

1V2_MGTAVTT

TP7

U19
MP2143DJ

2 VIN
8 EN
SW / VOUT 3 / 5
PG 1
FB 7
GND GND 4 / 6

C165 10uF/10V
C166 0.1uF

L6 1.5uH

1.2V@3A

R102 4.7K
C167 15pF
R103 100K 1%

R104 100K 1%

C168 47uF/6.3V
C169 0.1uF

PG_MGTAVCC

Vref = 0.6V   VOUT = 1.2V

MicroPhase Inc. www.microphase.cn

Title
XME7035 FPGA Module

Size B
Document Number
Power
Rev 1.2

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