Experiment 1 – Clock and Periodic Signal Generation

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Abstract— **This experiment aims to teach the basics of how digital logic gates work, how long they take to switch and how to make a clock signal using various analog ICs.**

1.1. Ring Oscillator

A ring oscillator is an electronic circuit that produces a repeating signal without external input. It consists of odd number of inverters connected in a loop, and the frequency of the output signal is determined by the delay of each inverter. The output can be used as a clock signal in digital circuits or for frequency generation.

In this section we attempt to construct a ring oscillator using 74HCT04 circuit by connecting five inverters in a chain. The circuit is shown in figure 1 and the waveform is shown in figure 2.

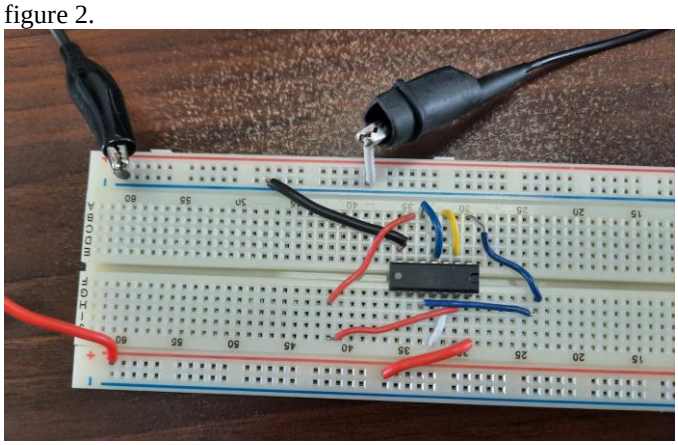

Fig. 1 ring oscillator circuit

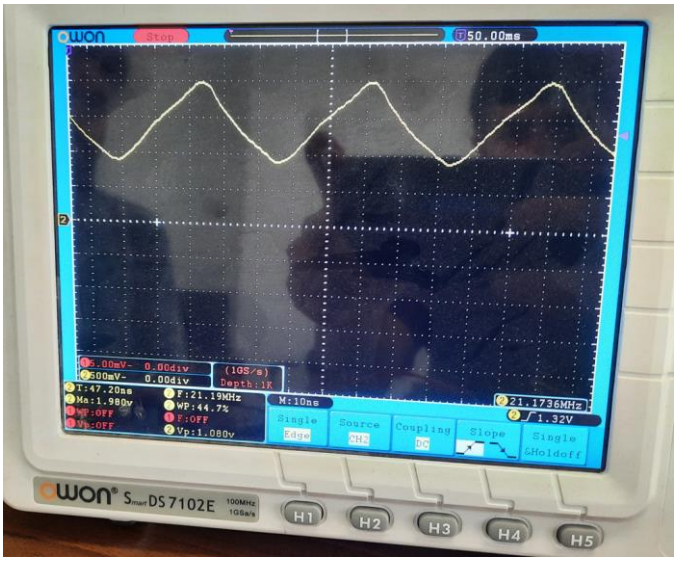

Fig. 2 ring oscillator waveform

The measured frequency is 21.19 MHz, here we calculate the time period of the original output from the frequency:

$$T = \frac{1}{f} = 47.19ns$$

Calculation of the propagation delay is shown below:

$$T_{chain} = \frac{T}{2} = 23.60ns$$

The delay of each inverter is computed here:

$$T_{inverter} = \frac{T_{chain}}{5} = 4.719ns$$

1.2. LM555 Timer

The LM555 timer is an integrated circuit used in electronic circuits as a timing device. It can be used in three different modes: Monostable, Astable and Bistable, to produce pulses, oscillations, or flip-flop operations. The LM555 is widely used in various electronic applications.

We only use the astable mode in this experiment. We fix R1 at 1kΩ and vary R2. Then we compare the measured and calculated duty cycles for each R2 value.

The implemented circuit is shown in figure 3.

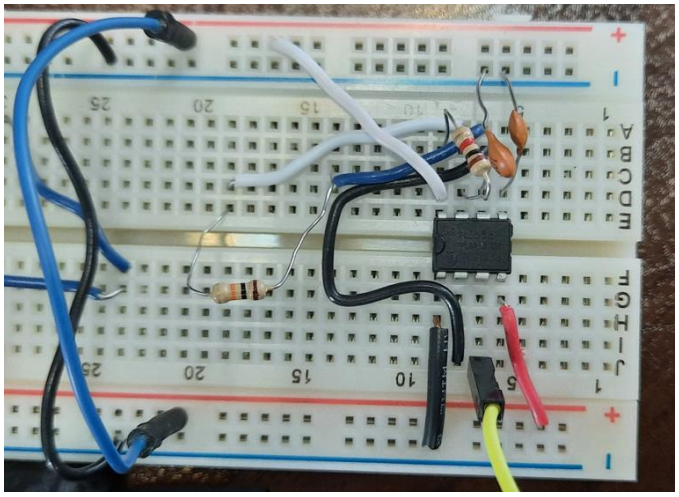

Fig. 3 LM555 timer circuit

1) R2 = 1kΩ

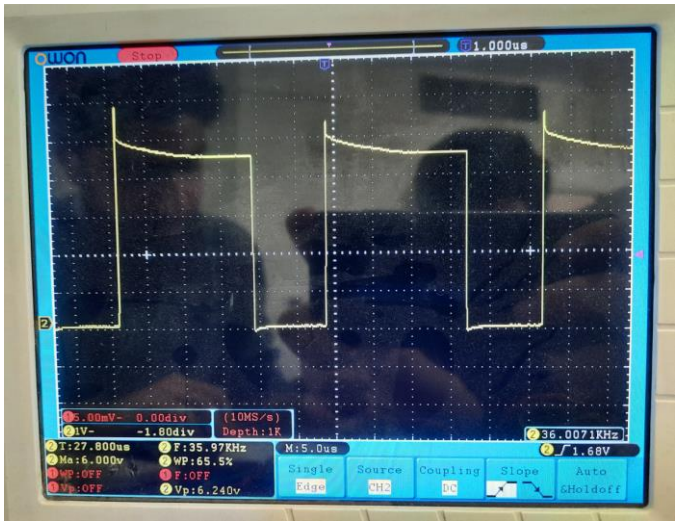

Fig. 4 R2 = 1kΩ

observed clock frequency and time period:

$$f = 36.01kHz$$

$$T = \frac{1}{f} = 27.8\mu s$$

observed duty cycle: 65.5%

calculating theoretical clock frequency period, and duty cycle:

$$T = 0.693 \times (\mathrm{R_1} + 2\mathrm{R_2}) \times \mathrm{C} = 20.79\mu s$$

$$f = \frac{1}{T} = 48.1kHz$$

$$Duty\ Cycle = \frac{R_1 + R_2}{\mathrm{R_1} + 2\mathrm{R_2}} = 66.7\%$$

2) R2 = 10kΩ

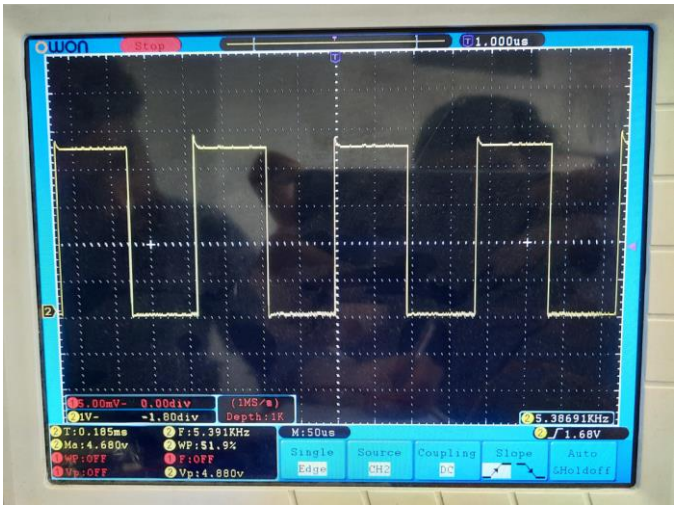

Fig. 5 R2 = 10kΩ

observed clock frequency and time period:

$$f = 5.387kHz$$

$$T = \frac{1}{f} = 0.186ms$$

observed duty cycle: 51.9%

calculating theoretical clock frequency period, and duty cycle:

$$T = 0.693 \times (\mathrm{R_1} + 2\mathrm{R_2}) \times \mathrm{C} = 0.14553\mathrm{ms}$$

$$f = \frac{1}{T} = 6.87kHz$$

$$Duty\ Cycle = \frac{R_1 + R_2}{\mathrm{R_1} + 2\mathrm{R_2}} = 52.4\%$$

3) R2 = 47kΩ

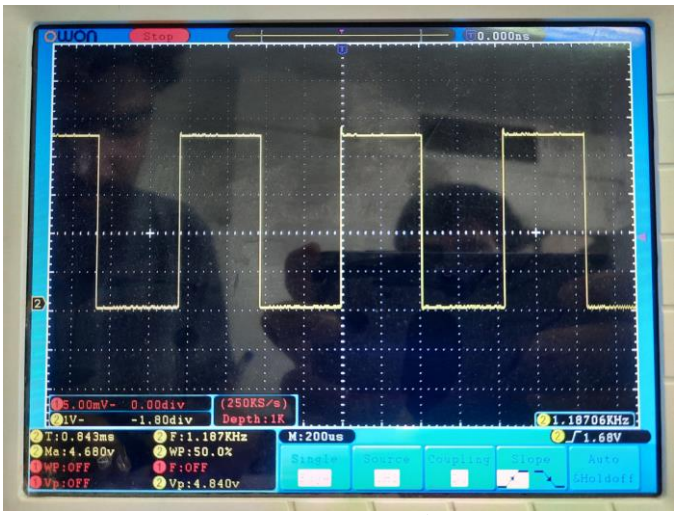

Fig. 6 R2 = 47kΩ waveform

observed clock frequency and time period:

$$f = 1.187kHz$$

$$T = \frac{1}{f} = 0.843ms$$

observed duty cycle: 50.0%

calculating theoretical clock frequency, period and duty cycle:

$$T = 0.693 \times (R_1 + 2R_2) \times C = 0.6584\text{ms}$$
$$f = \frac{1}{T} = 1.5189kHz$$
$$Duty\ Cycle = \frac{R_1 + R_2}{R_1 + 2R_2} = 50.53\%$$

4) R2 = 100kΩ

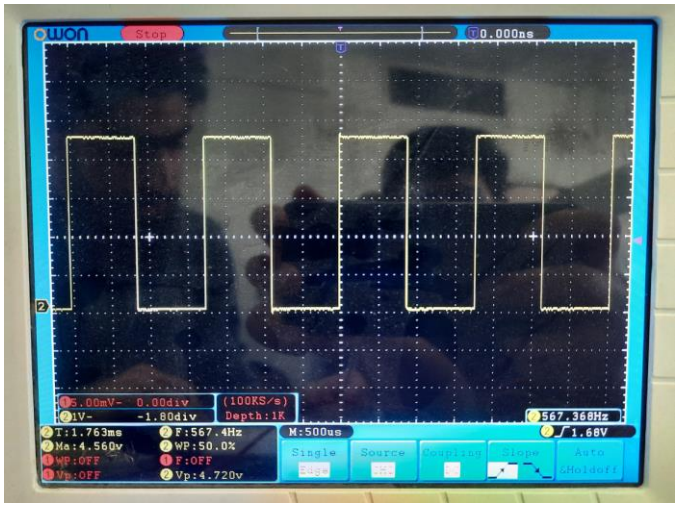

Fig. 4 R2 = 100kΩ

observed clock frequency and time period:

$$f = 567.4Hz$$
$$T = \frac{1}{f} = 1.762ms$$

observed duty cycle: 65.5%

calculating theoretical clock frequency, period and duty cycle:

$$T = 0.693 \times (R_1 + 2R_2) \times C = 1.393\text{ms}$$
$$f = \frac{1}{T} = 717.91Hz$$
$$Duty\ Cycle = \frac{R_1 + R_2}{R_1 + 2R_2} = 50.25\%$$

1.3. Schmitt Trigger Oscillator

Schmitt Trigger oscillator is a circuit that generates a square wave output signal by using a Schmitt Trigger as the active element. The Schmitt Trigger provides hysteresis, which makes the circuit more stable and less susceptible to noise. The oscillation frequency is determined by the values of the resistors and capacitors in the circuit.

We use 74HCT14 for the Schmitt inverter oscillator circuit.

The implemented circuit is shown in figure 8.

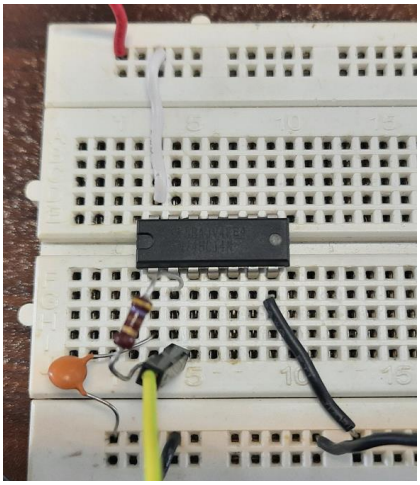

Fig. 8 Schmitt Trigger oscillator circuit

For C = 10nF and different values of R, the result will be as follows:

1) R = 470Ω

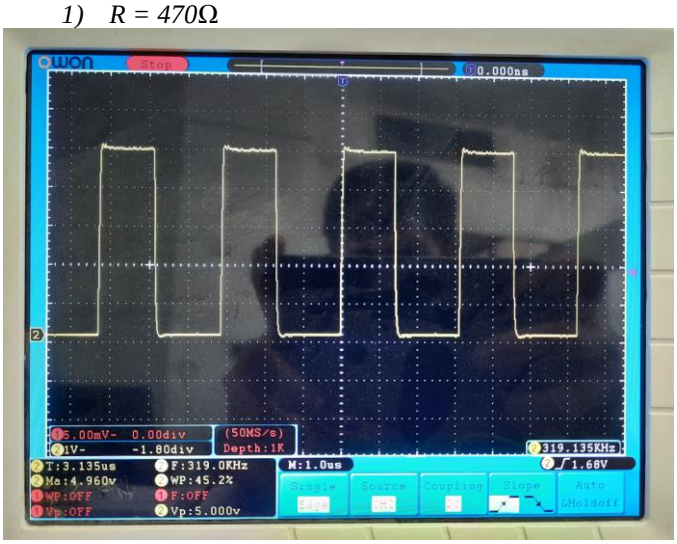

Fig. 9 R = 470Ω

$$f = 319.0kHz$$
$$T = \frac{1}{f} = 3.135\mu s$$
$$Duty\ Cycle = 45.2\%$$
$$\alpha = fRc = 1.4993$$

2) R = 1kΩ

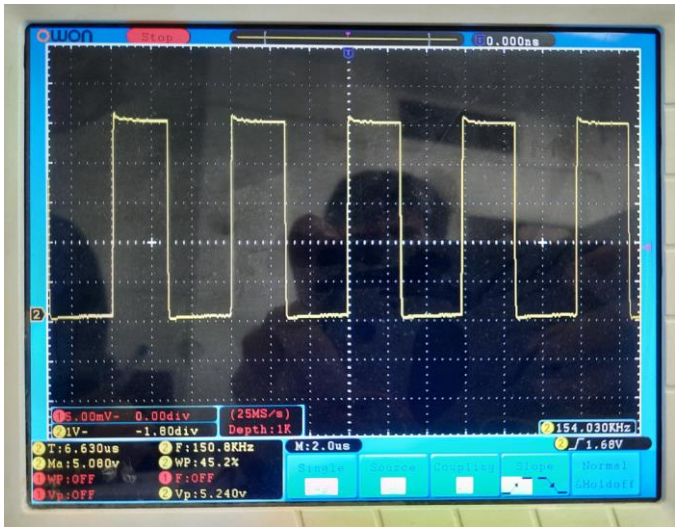

Fig. 10 R = 1kΩ

$$f = 150.8kHz$$

$$T = \frac{1}{f} = 6.63\mu s$$

$$Duty\ Cycle = 45.2\%$$

$$\alpha = fRc = 1.508$$

3) R = 2.2kΩ

$$f = 69.74kHz$$

$$T = \frac{1}{f} = 14.34\mu s$$

$$Duty\ Cycle = 45.3\%$$

$$\alpha = fRc = 1.53428$$

1.4. Synchronous Counter as a Frequency Divider

A synchronous counter is a type of digital counter that uses flip-flops to count pulses or events. It operates synchronously with an external clock signal and can divide the frequency of an input signal by a factor of $2^n - I$ where n is the number of flip-flops in the counter and I is the initial number loaded into the counter each time.

$$256 - 200 = 56$$

$$(56)_{dec} = (0011\ 1000)_{bin}$$

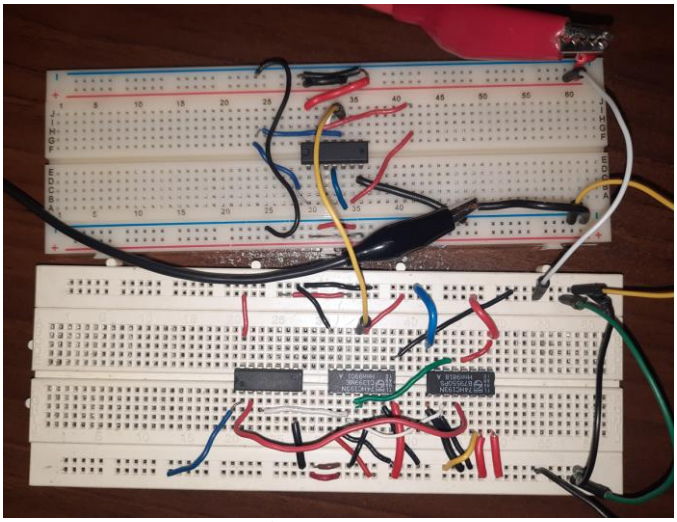

Fig. 12 frequency divider circuit

Ring Oscillator Output Frequency:

$$f_1 = 22.79MHz$$

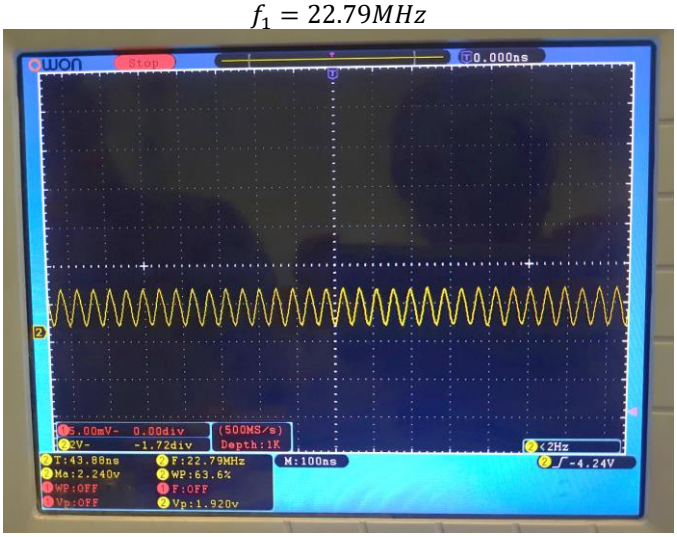

Fig. 13 Ring Oscillator Output waveform

Counter Output Frequency:

$$f_2 = 105.7kHz$$

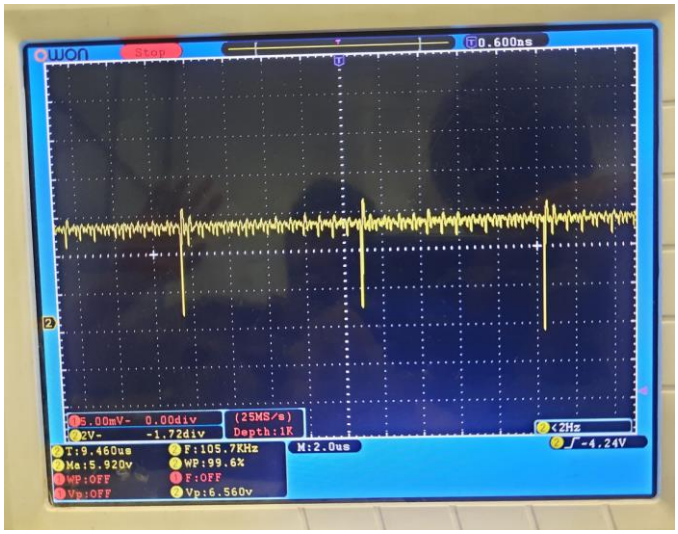

Fig. 14 counter output waveform

$$\frac{f_1}{f_2} = 216$$

1.5. T Flip-Flop

We use a T flip-Flop after counter to produce a 50 percent duty cycle signal.

A T flip-flop is a circuit that can toggle its output between 0 and 1 with a single input T and a clock signal Clk. It is a modified version of a JK flip-flop with J and K connected together.

By feeding the output of our previous counter to the T input of the T flip-flop we can generate a clock signal with a 50% duty cycle.

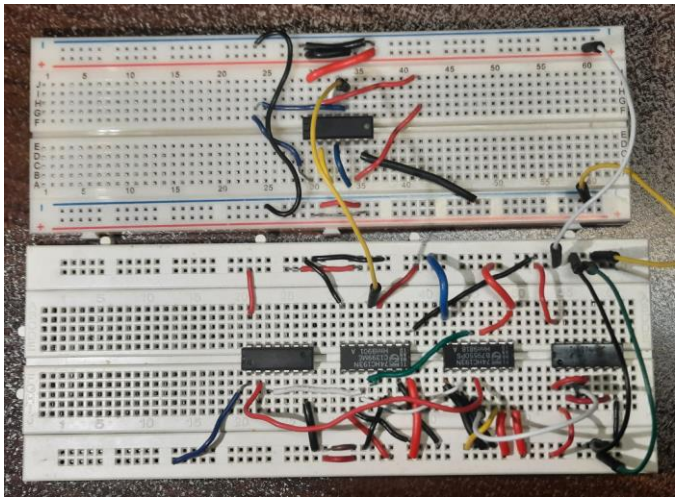

Fig. 15 clock generation circuit with a synchronous counter and a T flip-flop

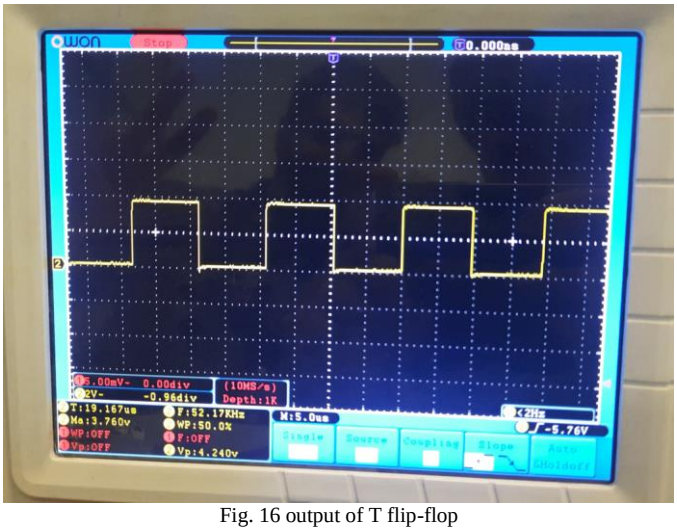

Fig. 16 output of T flip-flop

D Flip-Flop Output Frequency:

$$f_3 = 52.17kHz$$

$$Duty\ Cycle = 50\%$$