UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, 894, Spring 1399-00
Computer Assignment 1
Basic Switch and Gate Structures in SystemVerilog
Week 3

Name:

Date:

1. Generate a CMOS NAND gate and verify its timing and functionality. Write the SystemVerilog description of this structure using NMOS and PMOS transistors. Use #(3, 4, 5) delay for the NMOS transistors and #(5, 6, 7) for the PMOS transistors. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making To1 and To0 transitions. Make sure the time distance between your input changes is much larger than the gate delay values.

2. Generate a CMOS Tri-State Buffer (functionality like BUFIF1 of SystemVerilog) using four transistors for the buffer and two for its inverter. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making To1, To0, and ToZ transitions. Make sure the time distance between your input changes is much larger than the gate delay values.

3. Using the NAND gate of Problem 1, generate a 4-to-1 MUX with two select inputs, *s1* and *s0*, and four data inputs *a*, *b*, *c*, and *d*. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making To1 and To0. Make sure the time distance between your input changes is much larger than the gate delay values.

4. Using the Tri-State Buffer of Problem 2, generate a 4-to-1 MUX with two select inputs, *s1* and *s0*, and four data inputs *a*, *b*, *c*, and *d*. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making To1 and To0 transitions. Make sure the time distance between your input changes is much larger than the gate delay values.

5. In a testbench, instantiate the MUX circuits of Part 3 and Part 4 and compare the timing of these circuits. Explain the differences between these two circuits as far as the number of transistors and other physical parameters such as power consumption.