به نام خدا
دانشگاه تهران
پردیس دانشکده‌های فنی
دانشکده مهندسی برق و کامپیوتر

سیستم های دیجیتال 1

--- ECE 894 ---

استاد: پروفسور نوابی

Computer Assignment 1

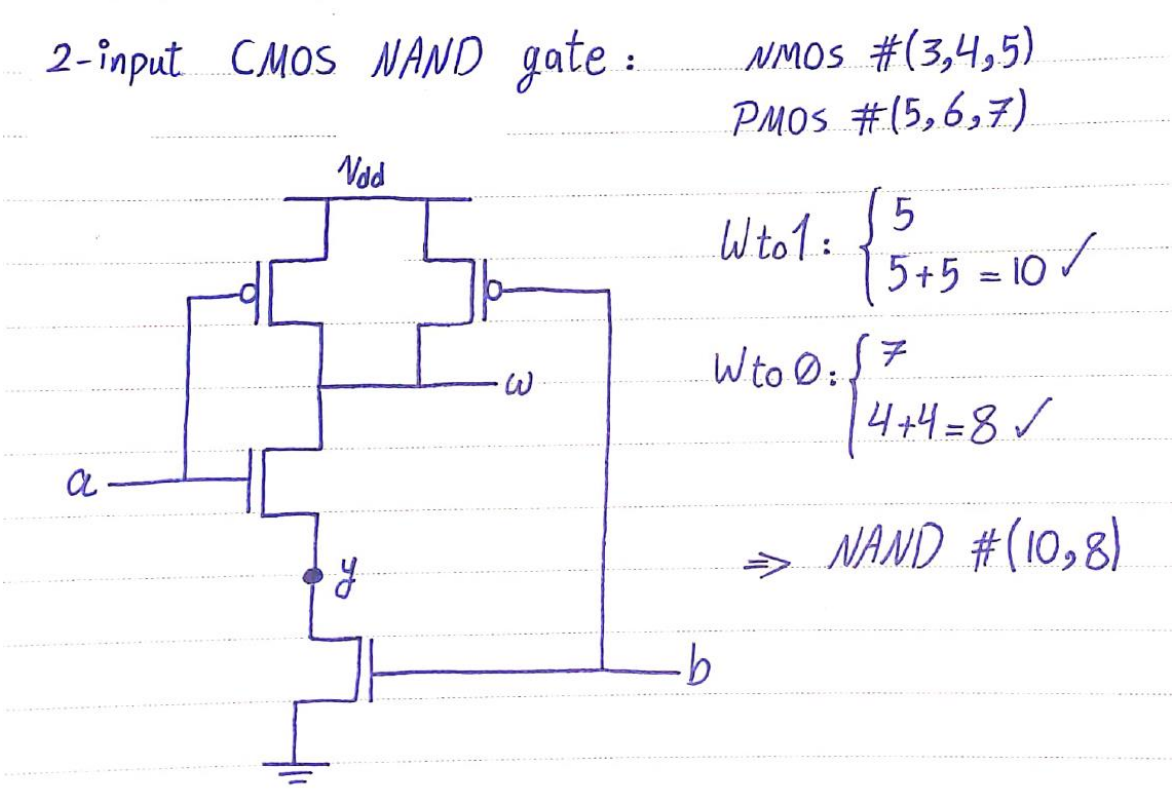
محمدمهدی عبدالحسینی

810 198 434

نیمسال دوم 1399 – 1400

سوال 1 :

Circuit diagram and worst-case delays :

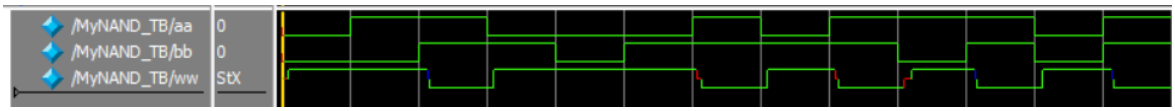


2-input CMOS NAND gate :

```
1   module MyNAND (input a,b , output w);
2           wire y;
3           supply1 Vdd;
4           supply0 Gnd;
5           pmos #(5,6,7) T1(w,Vdd,a);
6           pmos #(5,6,7) T2(w,Vdd,b);
7           nmos #(3,4,5) T3(y,Gnd,b);
8           nmos #(3,4,5) T4(w,y,a);
9   endmodule
10
11  module MyNAND2 (input a,b , output w);
12          nand #(10,8) (w,a,b);
13  endmodule
```

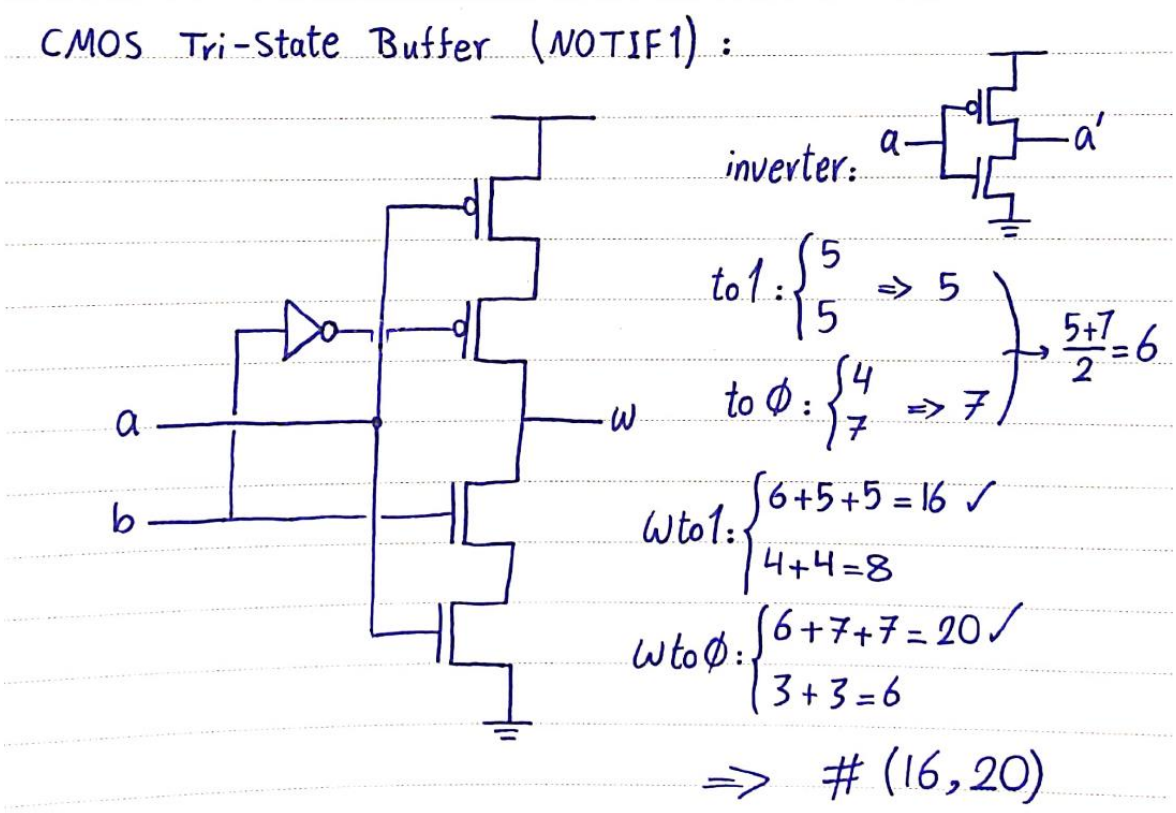
2-input CMOS NAND gate TestBench :

```
module MyNAND_TB ();
        reg aa=0,bb=0;
        wire ww;
        MyNAND CUT1(aa,bb,ww);
        initial begin
        #50 aa=1;
        #50 bb=1;
        #50 aa=0;
        #50 bb=0;
        #50 bb=1;
        #50 aa=1;
        #50 aa=0;
        #50 aa=1;
        #50 bb=0;
        #50 bb=1;
        #50 aa=0; bb=0;
        #50 aa=1; bb=1;
        #50 $stop;
        end
endmodule
```



سوال 2 :

CMOS Tri-State Buffer (functionality like NOTIF1 of SystemVerilog) using four transistors for the buffer and two for its inverter :

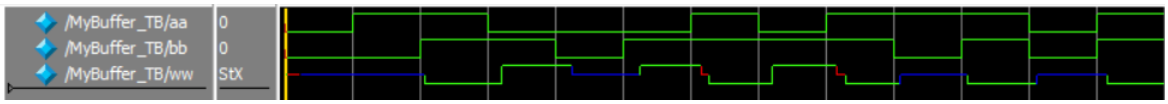


Verilog :

```
module MyBuffer (input a,b , output w);
        wire y1,y2,y3;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(5,6,7) T1(y1,Vdd,a);
        pmos #(5,6,7) T2(w,y1,y2);

        //inverter:
        pmos #(5,6,7) T3(y2,Vdd,b);
        nmos #(3,4,5) T4(y2,Gnd,b);

        nmos #(3,4,5) T5(w,y3,b);
        nmos #(3,4,5) T6(y3,Gnd,a);

endmodule
```

TestBench :

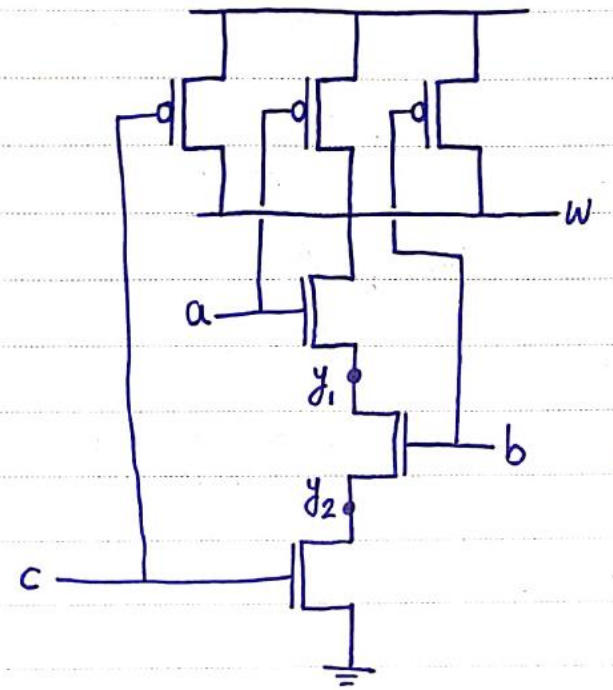
```
module MyBuffer_TB ();
        reg aa=0,bb=0;
        wire ww;
        MyBuffer CUT1(aa,bb,ww);
        initial begin
        #50 aa=1;
        #50 bb=1;
        #50 aa=0;
        #50 bb=0;
        #50 bb=1;
        #50 aa=1;
        #50 aa=0;
        #50 aa=1;
        #50 bb=0;
        #50 bb=1;
        #50 aa=0; bb=0;
        #50 aa=1; bb=1;
        #50 $stop;
        end
endmodule
```



سوال 3 :

Circuit diagram and worst-case delays :

3-input NAND:

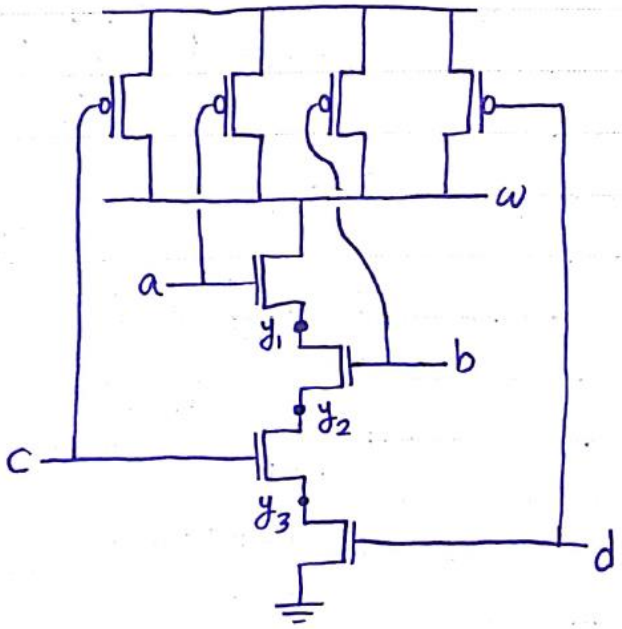


$$Wto1:\begin{cases}5\\5+5+5=15\ \checkmark\end{cases}$$

$$Wto0:\begin{cases}4+4+4=12\ \checkmark\\ \not\exists\end{cases}$$

MyNAND_3 #(15,12)

4-input NAND:

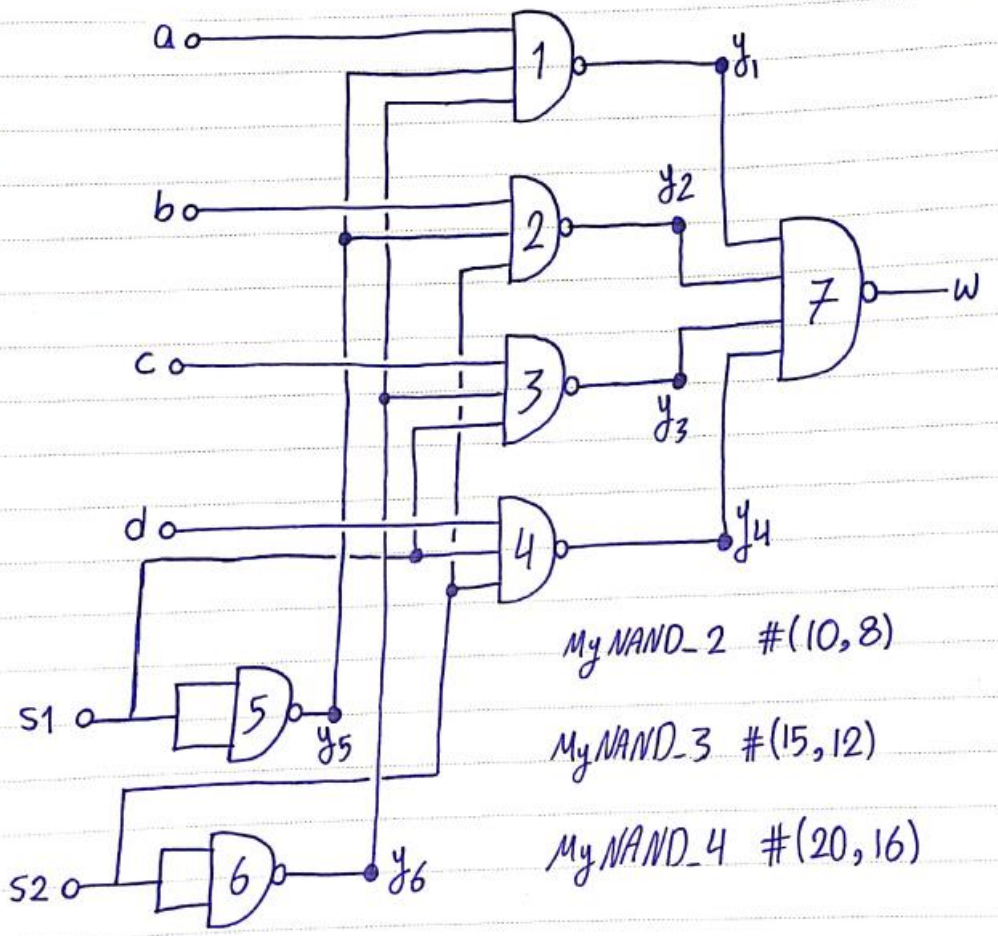


$$Wto1:\begin{cases}5\\5+5+5+5=20\ \checkmark\end{cases}$$

$$Wto0:\begin{cases}4+4+4+4=16\ \checkmark\\ \not\exists\end{cases}$$

MyNAND_4 #(20,16)

4-to-1 MUX with 2 Select input with NAND gates :



MyNAND_2 #(10,8)

MyNAND_3 #(15,12)

MyNAND_4 #(20,16)

Wto1 : 20 + 12 + 10 = 42

Wto0 : 16 + 15 + 8 = 39

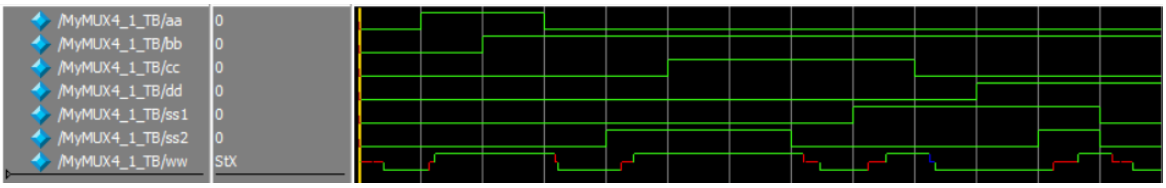
⇒ MyMUX4_1 #(42,39)

Verilog :

```
module MyNAND_2 (input a,b , output w);
        wire y;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(5,6,7) T1(w,Vdd,a);
        pmos #(5,6,7) T2(w,Vdd,b);
        nmos #(3,4,5) T3(y,Gnd,b);
        nmos #(3,4,5) T4(w,y,a);
endmodule

module MyNAND_3 (input a,b,c , output w);
        wire y1,y2;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(5,6,7) T1(w,Vdd,a);
        pmos #(5,6,7) T2(w,Vdd,b);
        pmos #(5,6,7) T3(w,Vdd,c);
        nmos #(3,4,5) T4(w,y1,a);
        nmos #(3,4,5) T5(y1,y2,b);
        nmos #(3,4,5) T6(y2,Gnd,c);
endmodule

module MyNAND_4 (input a,b,c,d , output w);
        wire y1,y2,y3;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(5,6,7) T1(w,Vdd,a);
        pmos #(5,6,7) T2(w,Vdd,b);
        pmos #(5,6,7) T3(w,Vdd,c);
        pmos #(5,6,7) T4(w,Vdd,d);
        nmos #(3,4,5) T5(w,y1,a);
        nmos #(3,4,5) T6(y1,y2,b);
        nmos #(3,4,5) T7(y2,y3,c);
        nmos #(3,4,5) T8(y3,Gnd,d);
endmodule

module MyMUX4_1 (input a,b,c,d,s1,s2 , output w);
        wire y1,y2,y3,y4,y5,y6;
        supply1 Vdd;
        supply0 Gnd;
        MyNAND_3 G1(a,y5,y6,y1);
        MyNAND_3 G2(b,y5,s2,y2);
        MyNAND_3 G3(c,y6,s1,y3);
        MyNAND_3 G4(d,s1,s2,y4);
        MyNAND_2 G5(s1,s1,y5); //inverter
        MyNAND_2 G6(s2,s2,y6); //inverter
        MyNAND_4 G7(y1,y2,y3,y4,w);
endmodule
```

TestBench :

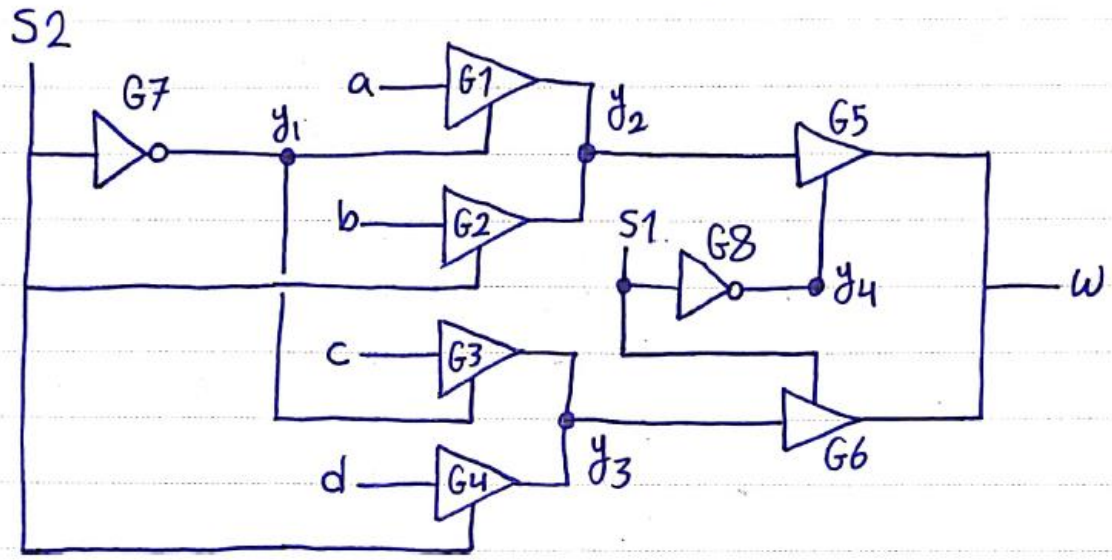
```
module MyMUX4_1_TB ();
        reg aa=0,bb=0,cc=0,dd=0,ss1=0,ss2=0;
        wire ww;
        MyMUX4_1 CUT1(aa,bb,cc,dd,ss1,ss2,ww);
        initial begin
        #50 aa=1;
        #50 bb=1;
        #50 aa=0;
        #50 ss2=1;
        #50 cc=1;
        #50 bb=1;
        #50 ss2=0;
        #50 ss1=1;
        #50 cc=0;
        #50 dd=1;
        #50 ss2=1;
        #50 ss1=0; ss2=0;
        #50 $stop;
        end
endmodule
```



سوال 4 :

Circuit diagram and worst-case delays :

4-to-1 MUX 2 select inputs using Tri-State Buffer :



MyBuffer #(16,20) ; MyInverter #6

Wto1: 16+6 + 16+6 = 44

Wto0: 20+6 + 20+6 = 52

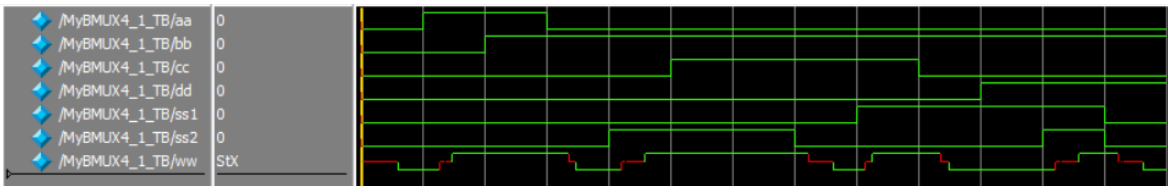
⟹ MyBMUX4_1 #(44,52)

Verilog :

```
module MyInverter (input a, output w);
        supply1 Vdd;
        supply0 Gnd;
        pmos #(5,6,7) T1(w,Vdd,a);
        nmos #(3,4,5) T2(w,Gnd,a);
endmodule

module MyBuffer (input a,b , output w);
        wire y1,y2,y3;
        supply1 Vdd;
        supply0 Gnd;
        pmos #(5,6,7) T1(y1,Vdd,a);
        pmos #(5,6,7) T2(w,y1,y2);

        //inverter:
        pmos #(5,6,7) T3(y2,Vdd,b);
        nmos #(3,4,5) T4(y2,Gnd,b);

        nmos #(3,4,5) T5(w,y3,b);
        nmos #(3,4,5) T6(y3,Gnd,a);

endmodule

module MyBMUX4_1 (input a,b,c,d,s1,s2 , output w);
        wire y1,y2,y3,y4;
        supply1 Vdd;
        supply0 Gnd;
        MyBuffer G1(a,y1,y2);
        MyBuffer G2(b,s2,y2);
        MyBuffer G3(c,y1,y3);
        MyBuffer G4(d,s2,y3);
        MyBuffer G5(y2,y4,w);
        MyBuffer G6(y3,s1,w);
        MyInverter G7(s2,y1);
        MyInverter G8(s1,y4);
endmodule
```

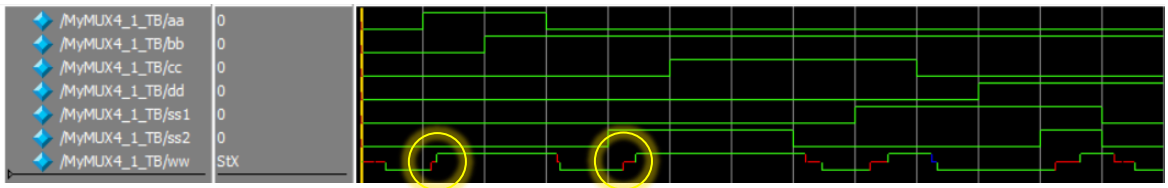
TestBench :

```
module MyBMUX4_1_TB ();
        reg aa=0,bb=0,cc=0,dd=0,ss1=0,ss2=0;
        wire ww;
        MyBMUX4_1 CUT1(aa,bb,cc,dd,ss1,ss2,ww);
        initial begin
        #50 aa=1;
        #50 bb=1;
        #50 aa=0;
        #50 ss2=1;
        #50 cc=1;
        #50 bb=1;
        #50 ss2=0;
        #50 ss1=1;
        #50 cc=0;
        #50 dd=1;
        #50 ss2=1;
        #50 ss1=0; ss2=0;
        #50 $stop;
        end
endmodule
```

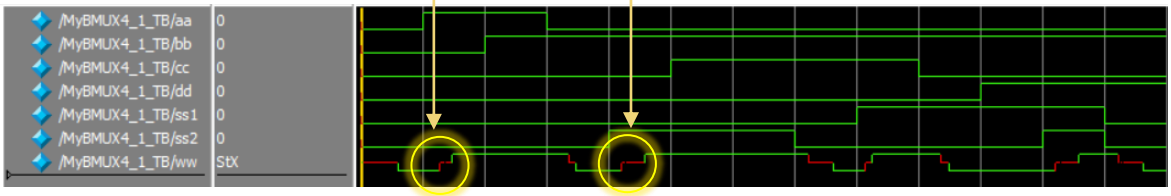


سوال 5 :

4-to-1 MUX 2-select inputs using NAND gates :



4-to-1 MUX 2-select inputs using Tri-State Buffer :



باتوجه به نتایج بدست آمده از شبیه سازی و همینطور بر اساس محاسبات تئوری میتوان گفت:

بطور کلی استفاده از گیت های Tri-State Buffer برای ساخت 4-1MUX ، delay بیشتری ایجاد میکند.

حال به بررسی تعداد ترانزیستورها در هر یک از مدارها میپردازیم:

4-to-1 MUX 2-select inputs using NAND gates :

Four 3-input NAND; every 3-input NAND includes 3 NMOS and 3 PMOS transistor.

Two 2-input NAND for inverter; every 2-input NAND includes 2 NMOS and 2 PMOS transistor.

One 4-input NAND; every 4-input NAND includes 4 NMOS and 4 PMOS transistor.

= > All NMOS: 4*3 + 2*2 + 4*4 = 32

= > All PMOS: 4*3 + 2*2 + 4*4 = 32

= > All Transistors: 64

4-to-1 MUX 2-select inputs using Tri-State Buffer :

seven Tri-State Buffer; every Tri-State Buffer includes 3 NMOS and 3 PMOS transistor.

Two Inverter; every Inverter includes 1 NMOS and 1 PMOS transistor.

= > All NMOS: 7*3 + 2*1 = 23

= > All PMOS: 7*3 + 2*1 = 23

= > All Transistors: 46

تعداد ترانزیستورهای کمتر در MUX ساخته شده از Tri-State Buffer یک مزیت (از آنجا که مصرف توان کمتری هم خواهد داشت) در برابر MUX ساخته شده از NAND gates میباشد. اما متاسفانه delay بیشتری بهمراه دارد!