UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1399-00
Computer Assignment 1
Basic Switch and Gate Structures in SystemVerilog
Week 3

Name:
Date:

Deliverables:

Generate a report that includes item discussed below for each of the five parts of this CA.

A. Show the circuit diagram that you are analyzing. Show gates and/or transistors according to the specified delays.
B. Hand-simulate the circuit you have shown in Part A and write your expected values. For example, indicate what values you expect for the worst-case delays and express your reason for that.
C. Show your SystemVerilog description of the design you are simulating and the testbench for it. Best is to use the Snip tools to get the image from Notepad++. This way you see all keywords and indentations. Make sure your SV codes are properly indented and all line-up rules are followed.
D. Show an image of the project that you have created in ModelSim for the simulation of your circuit.
E. When simulation is complete, or even if you have a partial simulation, include an image of the output waveform showing signal names being displayed.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.