6.7 Driver Strength and Bus Timing for 1.8V Signaling

6.7.1 Output Driver Strength

6.7.1.1 4-Level Driver Strength

To keep flexible design of the host system, output driver can see a wide range of host loads. 4-selectable drive strength enables host system to adjust drive strength that is optimized for the specific host load. That gives the SD card the flexibility to be supported by different system loads and system targets, while giving a very good signal integrity performance.
4-selectable drive strength types are defined for UHS-I card 1.8V signaling level. It is also serves as a reference for host output driver design. The host should select the most appropriate drive strength of the card to drive its specific PCB as explained in Section 6.7.1.5.

6.7.1.2 I/O Drive Strength Types

The load of the card output driver depends on the host PCB design. The equivalent capacitance load seen from the driver is determined by transmission line impedance, signal propagation delay on transmission line and rise / fall time of the signal. When a rise / fall time is longer than several number of wave reflection time on the transmission line, the load is considered as "lumped", otherwise, "distributed". The total capacitance load of card input, transmission line and host input are estimated for the lumped system. In contrast, the sum of the lumped elements on the path, up to a certain distance from the source is estimated for the distributed system. The rest of the path capacitance is unseen by the driver. Therefore, usually the Host controller input capacitance is not seen by the driver in this case.

For testing purposes, the transmission line load is converted to an equivalent lumped load, which gives same rise / fall time as in the transmission line case. Two estimated capacitance loads are defined for each driver type to define driver characteristics of UHS50 and UHS104 cards.

(1) Driver Type B
Type B driver is the default drive strength, targeted for a fixed impedance distributed system with 50 ohm transmission line, at all available frequencies. Therefore, it is defined as 50 ohm nominal driver. This driver can support total C_L of about 15pF for UHS104 card and about 30pF for UHS50 card. Drive strength B is the reference driver for definitions of all the rest of the drive strengths.

(2) Driver Type A
Type A driver is the x1.5 driver, defined as 33 ohm nominal driver, and supporting up to 208MHz operation.

(3) Driver Type C
Type C driver is the x0.75 driver, it is the weakest driver that supports 208MHz operation, and is defined as 66 ohm nominal driver.

(4) Driver Type D
Type D driver is a x0.5 driver, it is best for a system which the speed is not critical, but the more important is low noise / low EMI. Type D generates the slowest rise / fall time. Using a very slow rise time, the system usually will be considered as a lumped load system. Type D is defined as 100 ohm nominal driver, and the maximum operating frequency is depends on the host design.

Support of selectable driver strength depends on the card type as shown in Table 6-7.

Driver Type	Nominal Impedance	Driving capability	UHS50 Card	UHS104 Card
A	33 Ω	x1.5	Optional	Mandatory
B	50 Ω	x1	Mandatory	Mandatory
C	66 Ω	x0.75	Optional	Mandatory
D	100 Ω	x0.5	Optional	Mandatory

Note: Nominal impedance is defined by I-V characteristics of output driver at 0.9V.

Table 6-7 : I/O Driver Strength Types

6.7.1.3 I/O Driver Target AC Characteristics

This section describes design target for I/O designer. The characteristics of output driver are measured by Figure 6-12 under all maximum to minimum delay conditions.

6.7.1.3.1 Requirement for Rise / Fall Time

Table 6-8 is the requirement from the default drive strength (Type B), for UHS104 and UHS50 card. The I-V curve (current-voltage characteristics) of drivers types A, C and D are approximately x1.5, x0.75 and x0.5 from the default driver type B.

Driver Type	Symbol	Driver Rise / Fall Time Requirements				Condition
		Min.	Typ.	Max.	Units	C_L
Type B for UHS104	T_RB, T_FB	0.40	0.88	1.32	ns	15pF
Type B for UHS50	T_RB, T_FB	0.70	1.83	2.75	ns	30pF

Table 6-8 : I/O Driver Design Target

Notes:

1. Typical rise / fall time values are a design target. Any actual rise / fall time that is between the minimum and the maximum is conforming to this specification.
2. Output rise time is measured between V_{OL} (0.45V) to V_{OH}(1.4V),output fall time is measured between V_{OH}(1.4V) to V_{OL}(0.45V).

Application Note:
Table 6-8 is also useful to determine drive strength of host output driver. One of driver capabilities should be measured depending on the capacitance load of host system.
When selecting type D driver, the maximum frequency is determined by the host system.

6.7.1.3.2 Design Target for Ratio of Rise / Fall Time

All the measurements performed in Section 6.7.1.3.1 satisfy the admissible difference between rise time and fall time as described in Table 6-9. Usually the worst case R_{RF} is experienced at unbalanced process condition fast N-channel and slow P-channel or slow N-channel and fast P-channel.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
The Ratio of Rise / Fall Time	R_{RF}	0.7	1.0	1.4	-	$R_{RF} = T_R / T_F$

Table 6-9 : Design Target for Ratio of Rise / Fall Time

6.7.1.3.3 Output Driver Test Circuit

The test circuit as shown in Figure 6-12 is used to verify driver characteristics.

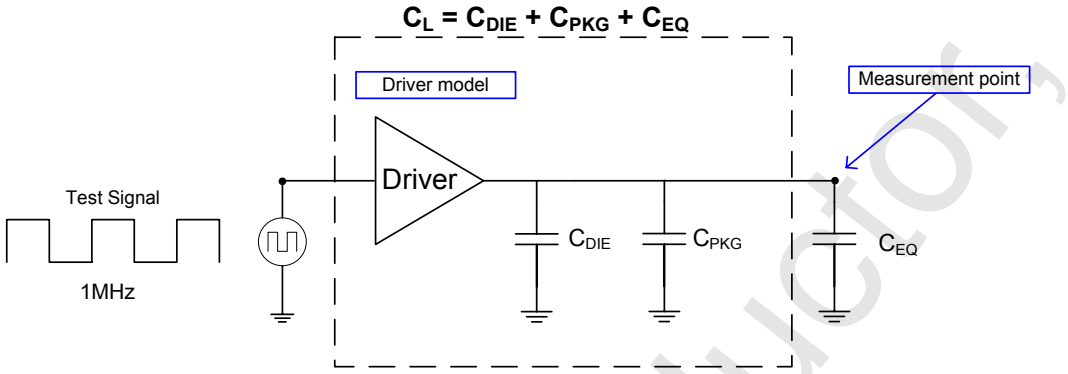

Figure 6-12 : Outputs Test Circuit for Rise/Fall Time Measurement

Notes:

1. The ratio of rise time to fall time is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given temperature and voltage combination, it represents the maximum difference between rise and fall time due to process variation.
2. Terminology is defined as follows:

$C_{L:}$	Total system effective capacitance for each line. (In distributed loads, not all trace elements are counted as effective capacitance)
$C_{CARD:}$	Card capacitance
$C_{EQ:}$	Equivalent lumped load, external to card. (Transmission lines are converted to an equivalent lumped load)
$C_{DIE:}$	Card die capacitance
$C_{PKG:}$	Card package capacitance
C_{CARD}	$= C_{DIE} + C_{PKG}$
C_L	$= C_{CARD} + C_{EQ}$

3. Card capacitance range is defined as follows:

Capacitance	Min	Max	Units	Notes
C_{CARD} ($C_{DIE} + C_{PKG}$)	5	10	pF	---

Table 6-10 : Card Capacitance Range

6.7.1.4 Driver Strength Selection

CMD6 Function Group 3 is used to select driver strength. 4 levels are defined from Function 0 to 3. Function 0 is default drive strength. Selecting method follows CMD6 definition. If the change of driver strength is failed, the current driver strength is still selected.

Table 6-11 shows drive strength support in CMD6 Status. Host can change to supported driver strength of the card.

CMD6 Status Bit	Meaning
432	Support bit of Type B Driver (Always 1 as default)
433	Support bit of Type A Driver
434	Support bit of Type C Driver
435	Support bit of Type D Driver

Table 6-11 : Output Driver Type Support Bits

6.7.1.5 How to Select Optimal Drive Strength

The host should simulate its specific system, to verify the optimal drive strength at the desired operating frequency. The host should select the weakest drive strength that meets rise / fall time requirement at system operating frequency.
Or simply, whenever a stronger driver than type B is needed, driver type A can be selected and whenever a weaker driver than type B is needed, driver type C can be selected. However, as driver strength of UHS50 card is optional except type B, the host needs to use type B when the other driver types are not supported. Host which type A is optimal should reduce clock frequency in case of using type B.

Type D should be used where the system design target is a low noise system. As of that, the maximum operating frequency is reduced, and shall be determined by the specific host system.

Table 6-12 gives approximation of the total capacitance that each of the drive strength can support:

Driver Type	Type A	Type B	Type C	Type D
C_L at 208MHz	21pF	15pF	11pF	Note 1
C_L at 100MHz SDR **C_L at 50 MHz DDR**	43pF	30pF	23pF	Note 1

Table 6-12 : Approximation of Total Capacitance for Each of Drive Strength

Note 1:
Type D support total C_L of about 22pF or more, for slower rise / fall time than at 100MHz SDR operation. When selecting type D driver, the maximum frequency is determined by the host system.

6.7.2 Bus Operating Conditions for 1.8V Signaling

6.7.2.1 Threshold Level for 1.8V Signaling

Table 6-13 shows DC specification of 1.8V signaling. As signaling level is generated by regulator in host and card, some of the values are defined by fixed value rather than based on VDD.

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	V_{DD}	2.70	3.60	V	
Regulator Voltage	V_{DDIO}	1.70	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.40	-	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{SS}-0.30	0.58V	V	

Table 6-13 : Threshold Level for 1.8V Signaling

Application Note:
Manufacturers should take care in design presuming occurrence of voltage mismatch between card and host.

6.7.2.2 Leakage Current

Parameter	Symbol	Min.	Max.	Unit	Remark
Input Leakage Current		-2	2	µA	DAT3 pull-up is disconnected.

Table 6-14 : Input Leakage Current

6.7.3 Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

6.7.3.1 Clock Timing

Figure 6-13 shows clock signal timing and Table 6-15 shows required values of this timing. Clock timing is requirement for the host. t_{CLK} is used to define rise / fall timing. Rise and fall time shall be less than 0.2* t_{CLK}. SDCLK input shall satisfy the clock timing over all variable conditions, and is measured as close as possible to SD socket pins to the card while CMD and DAT[3:0] are in quiet state (not toggling). V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.) in Figure 6-13.

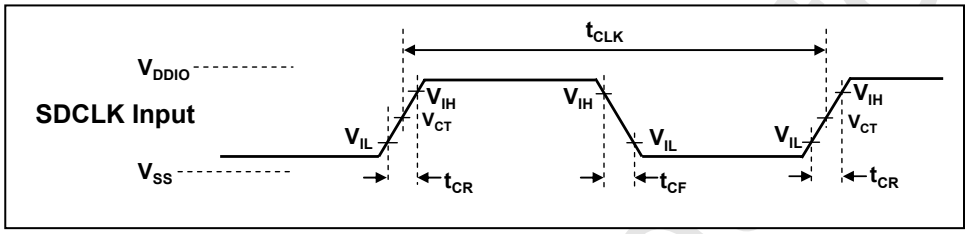

Figure 6-13 : Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Table 6-15 : Clock Signal Timing

6.7.3.2 Card Input Timing

Figure 6-14 shows card input timing and Table 6-16 shows required values of card input timing. The new parameter Clock Threshold (V_{CT}) is introduced to indicate clock reference point. V_{CT} is defined as 0.975V. Data setup time and hold time are measured at Data Threshold (V_{IL}(max.) and V_{IH}(min.)). V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.) in Figure 6-14.

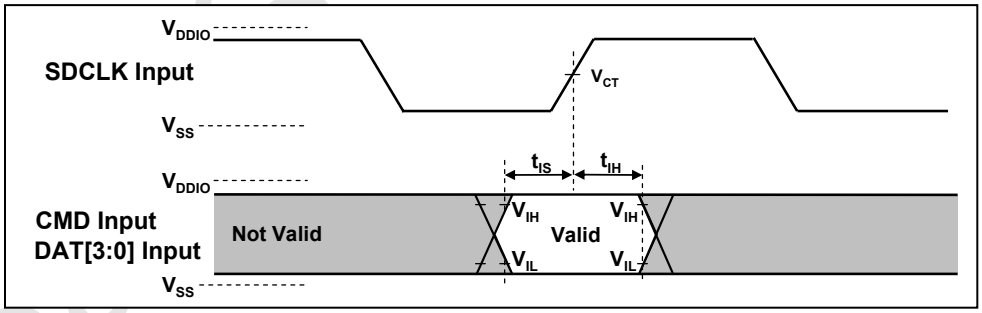

Figure 6-14 : Card Input Timing

Symbol	Min.	Max.	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, **V_{CT}= 0.975V**
t_{IH}	0.80		ns	C_{CARD} =5pF, **V_{CT}= 0.975V**
Symbol	**Min.**	**Max.**	**Unit**	**SDR50 mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, **V_{CT}= 0.975V**
t_{IH}	0.80	-	ns	C_{CARD} =5pF, **V_{CT}= 0.975V**

Table 6-16 : SDR50 and SDR104 Input Timing

6.7.3.3 Card Output Timing

6.7.3.3.1 Frequency Range Consideration

The maximum frequency of UHS-I is 208MHz. Hosts can use any frequency less than the UHS-I card supported. Considering the relation between clock period and output delay time, there is a border frequency around 100MHz. Therefore, two output timing diagrams are defined in this document.

(1) Fixed Output Data Window Case (SDR12, SDR25, SDR50 and DDR50)

If output delay is less than clock period (t_{ODLY}(max.) < t_{CLK}), DAT[3:0] can be sampled by SDCLK because fixed data window synchronized to SDCLK is always available. Considering t_{ODLY} (delay from SDCLK input to CMD and DAT[3:0] output), overlapped area of valid window is available under all maximum and minimum delay conditions (Variation of Temperature and voltage). Refer to Figure 6-15. Fixed Output Data Window Timing (Figure 6-16) defines overlapped area of valid data window.

Host can create sampling clock by loopback SDCLK method (refer to Appendix C.1). This timing mode enables the host to configure a simple data receiver circuit. The Fixed Output Data Window case is supported in SDR12, SDR25, SDR50 and DDR50. The frequency range is up to 100MHz.

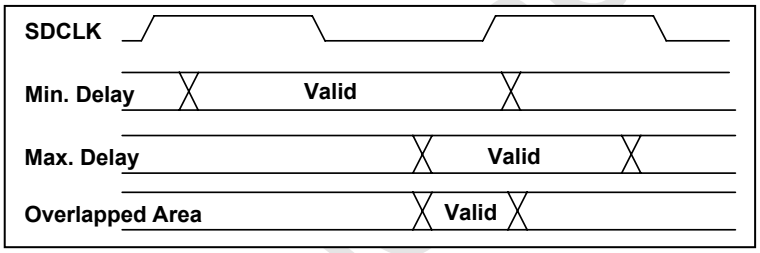

Figure 6-15 : Fixed Output Data Window

(2) Variable Output Data Window Case (SDR104)

Output delay may be bigger than one clock period. In this case, another timing parameter t_{OP} is adopted. t_{OP} is the momentary output phase from SDCLK input to CMD and DAT[3:0] output. After initialization, the t_{OP} can start at any phase in relation to the clock. At the initialization step the host should take care to find the optimal sampling point for the card outputs. The Variable Output Data Window is supported in SDR104. The frequency range is up to 208MHz.

Application Notes: The fixed timing supported host can use SDR12, SRD25 and SDR50 modes and cannot use SDR104 mode.

6.7.3.3.2 Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

Figure 6-16 shows card output timing of fixed data window and Table 6-17 shows required values of this timing for SDR12, SDR25 and SDR50. A valid window is specified by the minimum and maximum of output delay (t_{ODLY}). The valid data window synchronized to SDCLK is available regardless of all temperature and voltage variation. Output valid window is calculated by t_{CLK} - t_{ODLY} + t_{OH}. Host can create sampling clock by delayed SDCLK. V_{OH} denote V_{OH}(min.) and V_{OL} denotes V_{OL}(max.) in Figure 6-16.

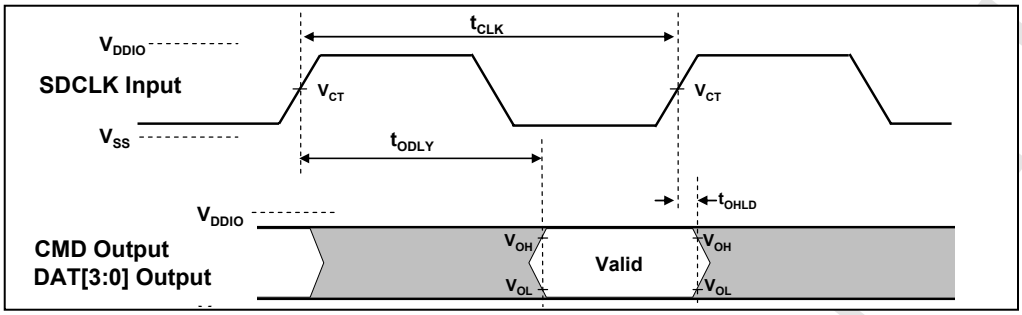

Figure 6-16 : Output Timing of Fixed Data Window

Symbol	Min.	Max.	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50,
t_{ODLY}		14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

Table 6-17 : Output Timing of Fixed Data Window

6.7.3.3.3 Output Timing of Variable Window (SDR104)

Figure 6-17 shows card output timing of variable data window and Table 6-18 shows required values of this timing. t_{OP} is introduced to express output delay. t_{OP} does not include a long term temperature drift in contrast t_{ODLY} which includes all delay variation. The temperature drift is expressed by ΔT_{OP}. t_{OP} after initialization, can be in range from 0 to 2UI. On determining sampling point of data, a long term drift, which is mainly depends on temperature drift, should be considered. Output valid data window (t_{ODW}) is available regardless of the drift (ΔT_{OP}) but position of data window varies by the drift. V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.) in Figure 6-17.

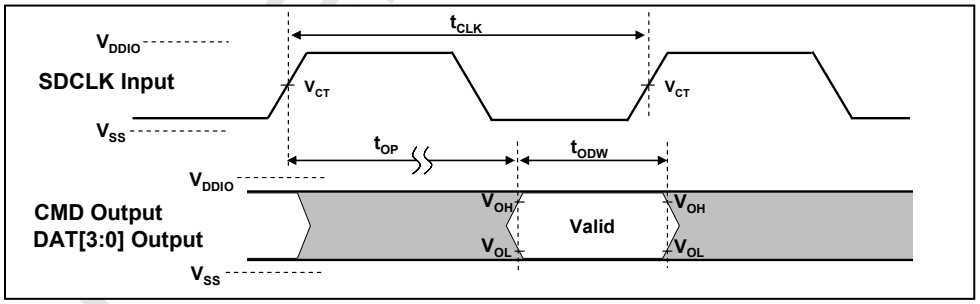

Figure 6-17 : Output Timing of Variable Data Window

Symbol	Min.	Max.	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW}=2.88ns at 208MHz

Table 6-18 : Output Timing of Variable Data Window

Card Δ_{TOP} is the total allowable shift of output valid window (T_{ODW}) from last system Tuning procedure.

Card Δ_{TOP} =1550pS for junction temperature of ΔT= 90 deg.C during operation.
Card Δ_{TOP} =-350pS for junction temperature of ΔT= -20 deg.C during operation.

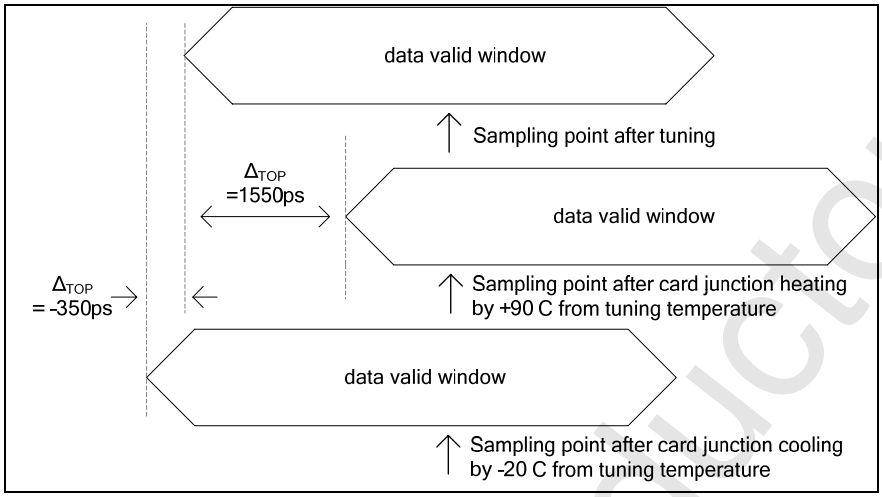

Figure 6-18 : Δt_{OP} Consideration for Variable Data Window Mode

The range of Δt_{OP} is 2600ps when card junction temperature changes from -25 deg.C to 125 deg.C during operation.

It is important note that Figure 6-16 and Figure 6-17 are output timings of the same output circuit expressed under different conditions. Two output timing figures are required because two types of read data sampling methods are presumed depends on host implementation. These output timings are defined at the test circuit measurement point. T_{ODW} for card is defined in this table, using an external noise free test circuit in Section 6.7.1. The valid window defined by output timings include skew among CMD and DAT[3:0] created by the card.
The host designer should consider the host transmission path which will add some Signal Integrity induced noise, skew between bus members, and timing errors. Expected T_{ODW} at host input is lager than 0.50UI.

Application Notes:
The host needs to consider drift of data window. A temperature drift after tuning procedure completes translates into a limited output valid window drift (ΔT_{OP}). The Host designer should take into consideration this drift, and design correctly to avoid being affected by this drift.
It is good practice to activate tuning procedure after sleep.
Host can use different techniques to overcome temperature effect (include reducing operating frequency).

6.7.4 Bus Timing Specification in DDR50 Mode

6.7.4.1 Clock Timing

Figure 6-19 shows clock signal timing and Table 6-19 shows required values of this timing. Clock timing is requirement for the host. t_{CLK} is used to define rise / fall timing. Rise and fall time shall be less than 0.2* t_{CLK}. SDCLK input shall satisfy the clock timing over all variable conditions, and is measured as close as possible to SD socket pins to the card while CMD and DAT[3:0] are in quiet state (not toggling). V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.) in Figure 6-19.

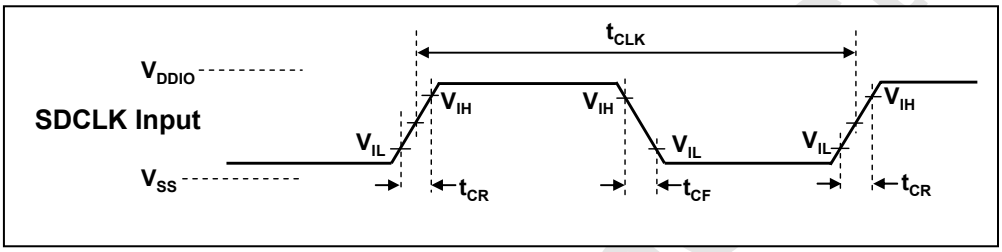

Figure 6-19 : Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

Table 6-19 : Clock Signal Timing

CMD signal timings are not shown in Figure 6-20. For CMD signal timing refers to Figure 6-14 and Figure 6-16 (Timing Diagram of SDR mode).

6.7.4.2 Bus Timing for DDR50

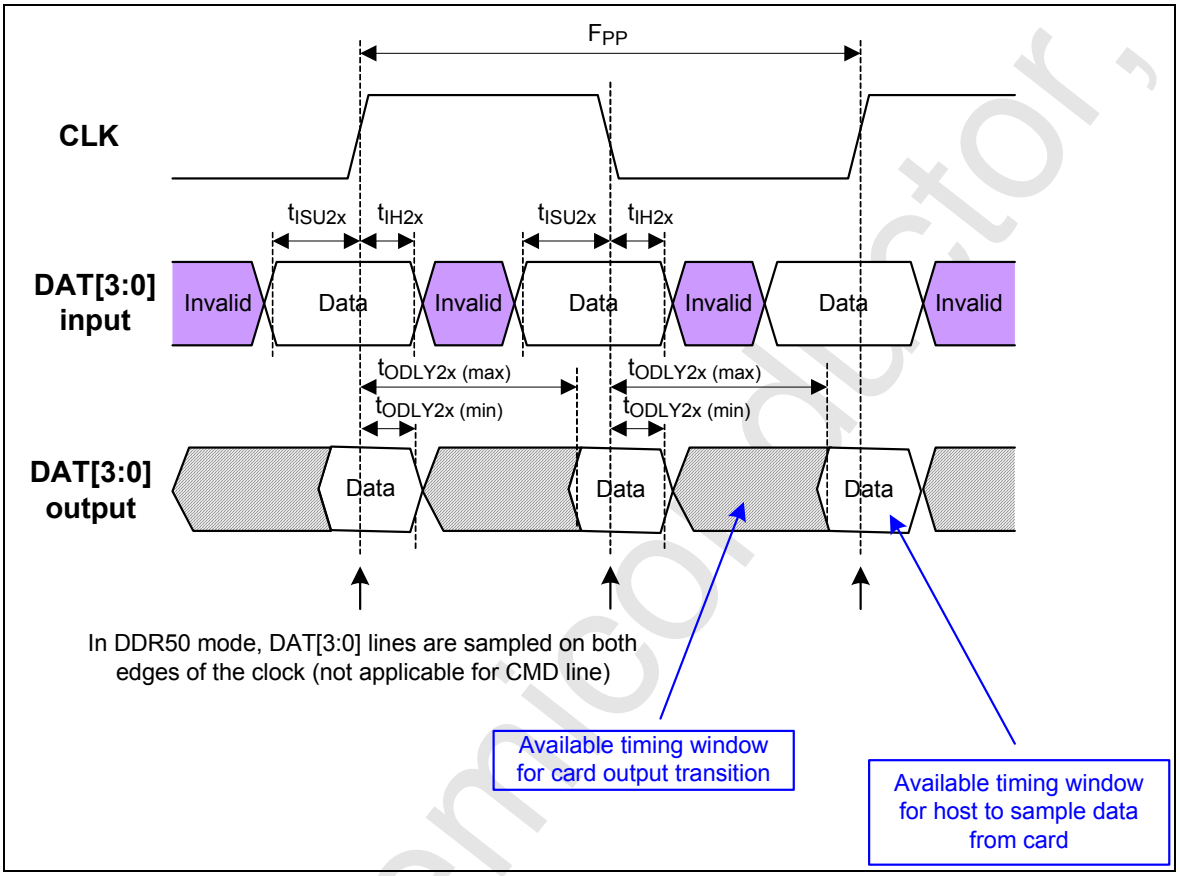

Figure 6-20 : Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{CARD} ≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} ≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	C_L ≤ 30 pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L ≥ 15pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{CARD} ≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{CARD} ≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L ≤ 25 pF (1 card)
Output hold time	t_{ODLY2x}	1.5	-	ns	C_L ≥ 15pF (1 card)

Table 6-20 : Bus Timings – Parameters Values (DDR50 mode)