Cheatsheet - Chapter 5
PDK Examination

KLayout:

.lyp	Layer properties file
.lyt	Technologies file for Layout ↔ Technology mapping

XScheme:

.sym	Schematics file

Hardware Description Languages (HDL):

Verilog
VHDL

Abbreviations:

LVS	Layout versus Schematic
CDL	Circuit design language
GDS II	Graphic data system (II)
LEF	Library exchange format
techLEF	Additional info about the technology
.lib	Liberty timing file: ASCII descriptions of timing / power of cells.