# Chapter 3 - Verilog - TRAINING - Common

Course authors (Git file)

1. ORFS examples

# ORFS examples

The Trainings for chapter 3 (Verilog) start with two of the given examples inside ORFS:

- The gdc (greatest common denominator) example
- The ibex (RISC-V) example

For this Training no Verilog code must be written. The Tasks are only about reading and understanding the existing Verilog code.

# GDC example

## Task: Find the gdc example

- Find the Verilog file of the gdc example in ORSF
- Open the Verilog file with an editor

## Task: Questions about the code

- What are the port definitions
- How many inputs and outputs will the chip have?
- Can you identify other parts of the code?
- What would be the list of pins of a microchip with this design?

# IBEX example

## Task: Find the ibex example

- Find the top level Verilog file of the ibex example in ORSF
- Open the top level Verilog file with an editor

## Task: Questions about the code

- What are the port definitions?
- How many inputs and outputs has the top level module?
- Can you identify other parts of the code?
- What would be the list of pins of a microchip with this design?