Chapter 3 - Verilog - TRAINING - Common

Course authors (Git file)

1. ORFS examples

GDC example

- Find the Verilog file of the gdc example in ORSF
- Open the Verilog file with an editor

Questions about the code: - What are the port definitions - How many inputs and outputs will the chip have? - Can you identify other parts of the code?

IBEX example

- Find the top level Verilog file of the ibex example in ORSF
- Open the top level Verilog file with an editor

Questions about the code: - What are the port definitions? - How many inputs and outputs has the top level module? - Can you identify other parts of the code?