Chapter 3 - Verilog crash course - QUESTIONS

Course authors (Git file)

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Recap questions for Chapter 3

Questions

- What are HDL?
- What is Verilog?
- Are there other HDL?
- What is the main difference between HDL and programming languages?
- List and describe the structure of a simple Verilog file.
- Yosys is … ?
- How to define ports in Verilog?
- Describe the concept of module instanciation in Verilog.
- What is the difference between combinational and sequential circuits?