

Chapter 1 - Introduction and overview

Course authors (Git file)



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Section 1

Welcome



Trainer profile

Me:

Name, Company / Uni

Why i'm here. My motivation.

What i've done before.

What interests me most.



Participants backgrounds and motivations

You:

Name, Company / Uni

Why i'm here. My motivation.

What i've done before.

What interests me most.



Section 2

Course overview








Chapter names

- 1 Introduction
- 2 OpenROAD tools
- 3 Verilog
- 4 OpenROAD first run
- 5 PDK
- 6 OpenROAD GUI
- 7 OpenROAD flow scripts
- 8 Tapeout



Schedule for the course

Mon	Tue	Wed	Thu	Fri
L1: Introduction	Q1, Q2: Recap Feedback	Q3, Q4: Recap Feedback	Q5, Q6: Recap Feedback	Q7: Recap
T1: Training	L3: Verilog T3: Training	L5: PDK T5: Training	L7: OpenROAD Flow scripts T7: Training	L8: Tapeout Feedback
				
L2: OpenROAD tools	L4: OpenROAD first run	L6: OpenROAD GUI	L7: OpenROAD Flow scripts 2	Spare time and Wrap-Up
T2: Training	T4: Training	T6: Training	T7: Training	

L : Lectures

T : Training and
Hands-On

Q : Questions



Section 3

Course components



Get the course materials here:

Course materials (Release):

<https://github.com/OS-EDA/Course/releases>

- Download the latest release
- Unpack into a directory on your computer



Additional links:

OS-EDA Github organization:

<https://github.com/OS-EDA>

Course Github repository:

<https://github.com/OS-EDA/Course>



Lectures



Lectures:

- All the chapters start with a lecture slide deck.
- The trainer will walk you through the content of the lectures.
- Whenever you have a question in between: ask directly.
- The lectures contain the base knowledge of the course.



Trainings



Common training tasks:

Every training sessions starts with the common part. The tasks of the common part are sufficient to follow along the content of the course. If you're a beginner, these trainings should be your goal to reach.



Advanced training tasks:

The advanced training sessions are for those With pre knowledge. If the common training was finished fast or was just to easy, the advanced sessions get you convered.



Bonus training tasks:

Still time left to do some tasks? Want something to take with you as homework? Please enjoy the bonus rounds of the training sessions.

Questions



Questions:

- The questions are for re-visiting and remembering a previous chapter.
- They guide an interactive session between the trainer and the room:
 - Trainer: Asks the questions.
 - Room: Answers the questions.
 - Skipping a question is fine.
 - Not knowing the answer is fine.
 - This is not a test nor a challenge.
 - Think of this as a helpfull recap of yesterdays content.
 - If no answer is found, the trainer helps with the answer.



Section 4

Feedback and Cheat Sheets



Feedback and Cheat Sheets

- We please you to give us feedback for the course.
- There is a short timeframe each day reserved for feedback.

We have two ideas about this:

- 1 Developing Cheatsheets together
- 2 Collecting general feedback



Cheatsheets




Some things are really hard to remember:

- Abbreviations
- Complex relations and graphics
- EDA tools workflow
- Schedule of the week
- Mathematics (joking, we're not doing math here)
- ...

- That is why we would like to develop Cheat Sheets.
- They're made for cheating the hard parts.
- Cheatsheets work best when printed as handouts.
- One can have them nearby the computer while learning.



Cheatsheet example








Mon	Tue	Wed	Thu	Fri
L1: Introduction	Q1, Q2: Recap Feedback	Q3, Q4: Recap Feedback	Q5, Q6: Recap Feedback	Q7: Recap
T1: Training	L3: Verilog T3: Training	L5: PDK T5: Training	L7: OpenROAD Flow scripts T7: Training	L8: Tapeout Feedback
				
L2: OpenROAD tools T2: Training	L4: OpenROAD first run T4: Training	L6: OpenROAD GUI T6: Training	L7: OpenROAD Flow scripts 2 T7: Training	Spare time and Wrap-Up

Figure 1: Cheatsheet Chapter 1



Cheatsheet example



Cheatsheet - Chapter 5 PDK Examination

KLayout:

.lyp	Layer properties file
.lyt	Technologies file for Layout ↔ Technology mapping

XScheme:

.sym	Schematics file

Hardware Description Languages (HDL):

Verilog	
VHDL	

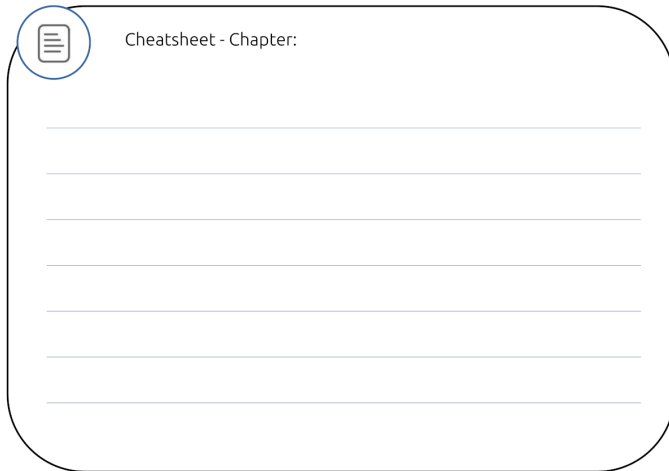
Abbreviations:

LVS	Layout versus Schematic
CDL	Circuit design language
GDS II	Graphic data system (II)
LEF	Library exchange format
techLEF	Additional info about the technology
.lib	Liberty timing file: ASCII descriptions of timing / power of cells.

Figure 2: Cheatsheet Chapter 5



Empty Cheatsheet printversion



A template for a cheatsheet, consisting of a rounded rectangle with a black border. In the top-left corner, there is a blue circular icon containing a document symbol. To the right of this icon, the text "Cheatsheet - Chapter:" is written. Below this text, there are seven horizontal blue lines for writing.

Cheatsheet - Chapter:

Figure 3: Cheatsheet Chapter 5



General feedback

General feedback:

- The general feedback will be collected verbally in the room.
- Everyone has the opportunity to give feedback
- We will write down the feedback, without your name.



What will happen with your feedback?

- We will put the feedback into Github issues.
- Right now, think of Github issues as some sort of tracker- or ticketsystem.
- Your feedback will not be connected to you (Anonymous).
- You can join a public discussion in the Github issues, if you want to.

Weblink to the issues of the course:

<https://github.com/OS-EDA/Course/issues?q=is%3Aissue>



Section 5

The Training sessions



Login at IHP

Now:

- Onboarding to the computers for everyone



Levels

- The Trainings should create success points inbetween lectures
- This is going too slow for me:
 - Try the advanced and bonus trainings (even from past chapters)
- This keeps me busy every minnute:
 - Stick to the common trainings. You will be able to follow all chapters then.



Section 6

Certificate



Certificate

We will explain live about the certificate of the course.

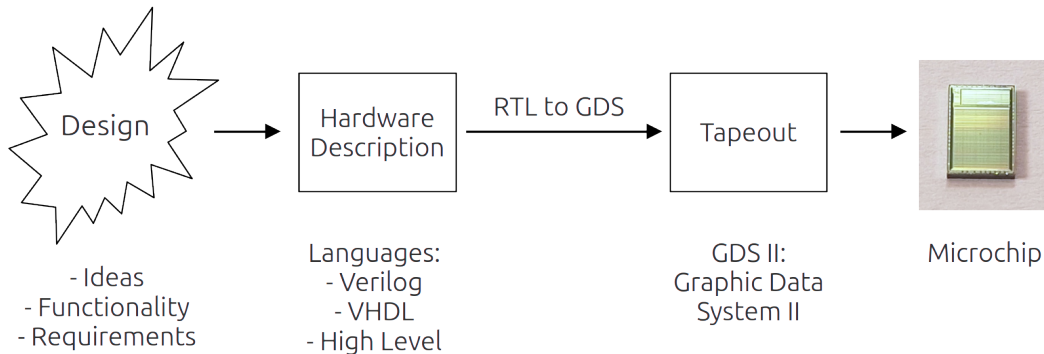


Section 7

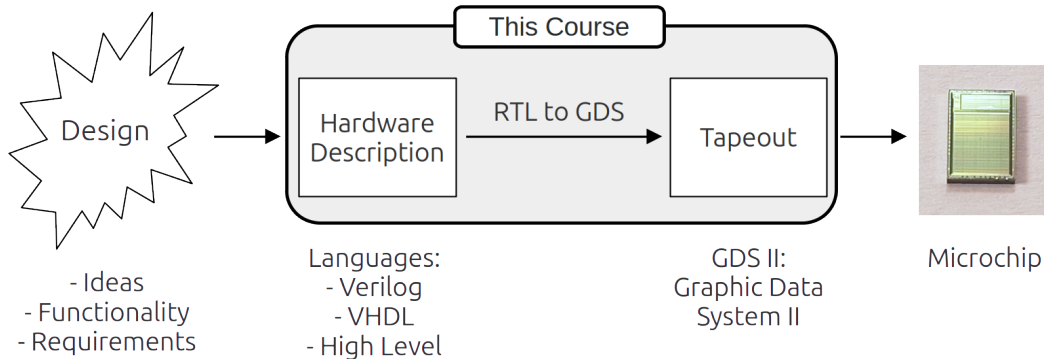
Open-source EDA for digital designs



From Design to Microchip



RTL to GDS - Workflow



Naming of RTL-to_GDS tools:

The naming of the tools is confusing:

- RTL-to-GDS
- = RTL-2-GDS
- = End-to-End-ASIC tools
- = EDA toolchain

They all mean the same.



Different open-Source EDA toolchains

Most known RTL-to-GDS toolchains:

- OpenLANE
- OpenLANE 2
- Silicon Compiler
- Coriolis

Used with IHP PDK and in this course:

- OpenROAD flow scripts

which is based on

- OpenROAD



A toolchain based on scripts and configuration files

OpenROAD flow scripts are

- based on scripts (obvious in the name)
- based on configuration files

Want most developers know from the commercial tools is:

- Graphical GUIs, used with a mouse and keyboard (shortcuts).
- Configuration through graphical masks, windows, forms.

This might feel uncomfortable at the beginning. But it still has some advantages.



Section 8

Further introductory topics



Advantages of open-source in EDA

- A word by Andrew Kahng (head of OpenROAD) about the relevance of open-source EDA

Andrews slides from the keynote speech at the Chipdesign Network June 2024. As pptx:

<https://vlsicad.ucsd.edu/NEWS24/InnovationKeynote-v6-ACTUAL-DISTRIBUTED.pptx>

Andrews news page with the link (scroll to june 2024) <https://vlsicad.ucsd.edu/>

- The actual state of open-source EDA
- Goals of this course.
- How to participate and interact with this course.
- Producing chips at IHP with the open PDK

