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FEATURES

MST6M48RVS, a single chip Multimedia TV SoC that supports TV channel decoding, and media-centre functionality enabled by a high performance AV CODEC and CPU

Key features includes,

1. *Analog TV Front-End Demodulator*
2. *A Multi-Standard A/V Format Decoder*
3. *The MStarACE-5^{UC} Video Processor*
4. *Home Theater Sound Processor*
5. *Peripheral and Power Management*

- High Performance Micro-processor
  - High speed/performance 32-bit RISC CPU
  - Memory Mangement Unit for Linux support
  - Three full duplex UARTs
  - Supports USB and ISP programming
  - DMA Engine
- MPEG-2 Video Decoder
  - ISO/IEC 13818-2 MPEG-2 video MP@HL
  - Automatic frame rate conversion
  - Supports resolution up to HDTV (1080i, 720p) and SDTV
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding
  - Supports resolutions up to HDTV (1080p@30fps)
  - Supports DivX[1] Home Theater & HD profiles[Optional]
  - Supports VC-1, FLV video format decoding
- H.264 Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.1) video decoding
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports resolution up to 1080p@30fps
  - Supports CABAC and CAVLC stream types
  - Processing of ES and PES streams, extraction and provision of time stamps
  - Up to 40 Mbits bitrate (Blu-ray spec.)
- RealMedia Decoder
  - Supports maximum resolution up to 1080p@30fps
  - Supports RV8, RV9, RV10, RA8-LBR and HE-AAC decoders
  - Supports file formats with RM and RMVB
  - Supports Picture Re-sampling
  - Supports in-loop de-block for B-frame
- Hardware JPEG
  - Supports sequential mode, single scan
  - Supports both color and grayscale pictures
  - Following the file header scan the hardware decoder fully handles the decode process
  - Supports programmable Region of Interest (ROI)
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2, 1/4, 1/8
  - Supports picture rotation
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Five configurable CVBS & Y/C S-video inputs
  - Supports Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE
- Multi-Standard TV Sound Processor
  - SIF audio decoding
  - Supports BTSC/A2/EIA-J demodulation
  - Supports FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC/ EIA-J mode
  - Supports Mono/Stereo/Dual in A2 mode
  - Built-in audio sampling rate conversion (SRC)

[1] **Trademark of DivX, Inc.**

Optional **Please contact MStar sales for the correct suffix.**

- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
- Advanced sound processing options available, for example: Dolby[1], SRS[2], BBE[3], QSound[4]
- Supports digital audio format decoding:
  - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3), AAC-LC, WMA
  - Dolby Digital Plus (E-AC-3) decoding[Optional]
  - HE-AAC 5.1 level 4 multi-channel decoding
- Simultaneously supports format decoding and transcoding to AC-3 (for AC-3 output support)
- Supports karaoke in MIDI media

Audio Interface

- One SIF audio input interface with minimal external saw filters
- Five L/R audio line-inputs
- Two L/R outputs for main speakers and additional line-outputs and one headphone output
- Supports stereo headphone driver
- I2S digital audio input & output
- S/PDIF digital audio output
- HDMI audio channel processing
- Programmable delay for audio/video synchronization

Analog RGB Compliant Input Ports

- Two analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG Sync-on-Green
- Automatic color calibration
- AV-link support

Analogue RGB Auto-Configuration & Detection

- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Ports

- Two HDMI/DVI Input ports
- HDMI 1.3 Compliant
- HDCP 1.1 Compliant
- 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
- CEC support
- Single link DVI 1.0 compliant
- Robust receiver with excellent long-cable support

MStar Advanced Color Engine (MStarACE-5[UC])

- 10/12-bit internal data processing
- Fully programmable multi-function scaling engine
  - Nonlinear video scaling supports various modes including Panorama
  - Supports dynamic scaling for RM, VC-1
- UltraClear DTV video processing engine
  - UltraClear-base 3D video deinterlacer with edge and artifact smoother
  - Edge-oriented deinterlacer with edge and artifact smoother
  - Automatic 3:2/2:2/M:N pull-down detection and recovery
  - UltraClear-base 3D noise reduction for DTV or lousy air/cable input
  - MPEG artifact removal including de-blocking and mosquito noise reduction
  - Arbitrary frame rate conversion
- MStar Professional Picture Enhancement:
  - Dynamic brilliant and fresh color
  - Dynamic *Blue Stretch*
  - Intensified contrast and details
  - Dynamic *Vivid Skin*
  - Dynamic sharpened Luma/Chroma edges
  - Global and local dynamic depth of field perception
  - Accurate and independent color control
  - Supports sRGB and xvYCC color processing
  - Supports HDMI 1.3 deep color format
- Programmable 12-bit RGB gamma CLUT

Output Interface

- Single/dual link 8/10-bit LVDS output
- Supports panel resolution up to Full-HD (1920x1080) @ 60Hz

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[1] **Trademark of Dolby Laboratories**
[2] **Trademark of SRS Labs, Inc.**
[3] **Registered trademark of BBE Sound, Inc.**
[4] **Registered trademark of QSound Labs, Inc.**
[Optional] **Please contact MStar sales for the correct suffix.**

- Supports TH/TI format
- Supports dithering options to 6/8-bit output
- Spread spectrum output for EMI suppression

■ CVBS Video Outputs
- Allows CVBS output of digital content
- Supports CVBS bypass output

■ 2D Graphics Engine
- Hardware Graphics Engine for responsive interactive applications
- Supports point draw, line draw, rectangle draw/fill, text draw and trapezoid draw
- BitBlt, stretch BitBlt, trapezoid BitBlt, mirror BitBlt and rotate BitBlt
- Supports alpha and destination alpha compare
- Raster Operation (ROP)
- Support Porter-Duff

■ VIF Demodulator
- Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
- Digital low IF architecture
- Audio/Video dual-path processor
- Stepped-gain PGA with 25 dB tuning range and 1 dB tuning resolution
- Maximum IF gain of 37 dB
- Programmable TOP to accommodate different tuner gain and SAW filter insertion loss to optimize noise and linearity performance
- Multi-standard processing with single SAW
- Supports silicon tuner low IF output architecture

■ Connectivity
- Two USB 2.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting

■ Miscellaneous
- DRAM interface supporting single 16-bit DDR2 @ 1066MHz
- Bootable SPI interface with serial flash support
- Power control module with ultra low power MCU available in standby mode
- 216-pin LQFP package
- Operating Voltages: 1.26V (core), 1.8V (DDR2), 2.5V and 3.3V (I/O and analog)

GENERAL DESCRIPTION

The MST6M48RVS is MStar's most up-to-date system-on-chip solution for flat panel integrated digital television products. Building on the success of MStar's preceding SOC series, the MST6M48RVS provides most cost-effective solution for multimedia TV application with creative and attractive features exclusively presented by MStar.

The MST6M48RVS integrates TV/multi-media all-purpose AV decoder, VIF demodulator, and advanced Sound/Video processor into a single device. This allows the overall BOM to be reduced significantly making the MST6M48RVS a very competitive multi-media TV solution.

The powerful multimedia A/V decoder inside MST6M48RVS is hosted with a dedicated hardware video codec engine to secure fast and stable video stream playback, an audio application specific DSP for digital audio format decoding and advanced sound effects, and a high performance RISC CPU to manipulate all possible user playback and control activities. With extendable USB 2.0 connectivity, an MST6M48RVS based system can be switched to a high quality media-center in a simple manner.

For standard users, the MST6M48RVS provides multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. The build-in audio decoder is capable of decoding FM, AM, -A2, BTSC and EIA-J sound standards. The MST6M48RVS supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selection multiplexed for video and audio are integrated, including full SCART support with CVBS output. The equipped MStar MStarACE-5^{UC} color engine is the latest masterpiece of MStar famous color engine series providing excellent video and picture quality in Full-HD and large-scale displaying system.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MST6M48RVS has an ultra low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		TBD		LSB
Integral Nonlinearity		TBD		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum		0.5		V p-p
Maximum		TBD		V p-p
Input Bias Current			1	uA
SWITCHING PERFORMANCE				
Maximum Conversion Rate	170			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		170	MHz
PLL Jitter		TBD		ps p-p
Sampling Phase Tempco		TBD		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		0.2		V
Output High		1.2		V
AUDIO				
ADC Input		2.8		V p-p
DAC Output		2.8		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p

Parameter	Min	Typ	Max	Unit
SAR ADC Input	0		3.3	V
FB ADC Input*	0		1.2	V

Specifications subject to change without notice.
Note: Input full scale is 1.2V, but input range is 0 ~ 3.3V.

Recommended Operating Power Conditions

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
2.5V Supply Voltages	V_{VDD_25}	2.38		2.62	V
1.8V Supply Voltages	V_{VDD_18}	1.70		1.90	V
1.26V Supply Voltages	V_{VDD_126}	1.20		1.32	V

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
3.3V Supply Voltages	V_{VDD_33}		3.6	V
2.5V Supply Voltages	V_{VDD_25}		2.75	V
1.8V Supply Voltages	V_{VDD_18}		1.98	V
1.26V Supply Voltages	V_{VDD_126}		1.32	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Ambient Operating Temperature	T_A	0	70	℃
Storage Temperature	T_{STG}	-40	150	℃
Junction Temperature	T_J		150	℃

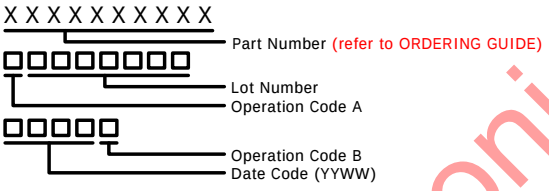
Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MST6M48RVS-LF	0°C to +70°C	LQFP	216
MST6M48RVS-LF-XX	0°C to +70°C	LQFP	216

Note:
XX suffix represents advanced features. Please contact MStar sales for details.

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST6M48RVS comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST6M48RVS_ds_v01	• Initial release	Dec 2009
MST6M48RVS_ds_v02	• Removed Teletext and NICAM related information	Dec 2009

REGISTER DESCRIPTION

Scaler1 Register (Bank = 102F)

GOP_INT Register (Bank = 102F, Sub-bank = 00)

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102F00h)	**REG102F00**	**7:0**	**Default: 0xFF**	**Access: R/W**
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler.	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]: SWRST1[4]: IP, including F1 and F2. SWRST1[3]: OP, including OP1, VIP and VOP. SWRST1[2]: IP_F2. SWRST1[1]: IP_F1. SWRST1[0]: All engines.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	PDMD[1:0]	1:0	Power Down mode: 01: IDCLK. Others: IDCLK and ODCLK.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 VS INT Edge. 1: Tailing. 0: Leading.	
	IPVSINT_EDGE	0	IP VS INT Edge. 1: Tailing. 0: Leading.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CHG_HMD	0	CHG_HMD: H Change Mode for INT. 0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x08**	**Access: R/W**
	IP_SYNC_TO_GOP_SEL	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.	
	GOP2IP_EN	5	GOP blending to IP enable.	
	-	4:0	Reserved.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:6	Reserved.	
	GOP2IP_DATA_SEL	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	COP_EN	7	Enable COP for VOP2.	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: -**	**Access: RO**
	IRQ_FINAL_STATUS_7_0[7:0]	7:0	Final status of interrupt in SC_TOP. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: -**	**Access: RO**
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	Final status of interrupt in SC_TOP. D[7]: IPHCS_DET_INT_F1.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: -**	**Access: RO**
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	Final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: -**	**Access: RO**
	IRQ_FINAL_STATUS_31_24[7:0]	7:0	Final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for: D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F25h)	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for: D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for: D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for: D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0xFF**	**Access: R/W**
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0xFF**	**Access: R/W**
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0xFF**	**Access: R/W**
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[0]: N/A.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: -**	**Access: RO**
	IRQ_RAW_STATUS_7_0[7:0]	7:0	Raw status of interrupt source. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[2]: N/A. D[1]: N/A. D[0]: N/A.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: -**	**Access: RO**
	IRQ_RAW_STATUS_15_8[7:0]	7:0	Raw status of interrupt source. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: -**	**Access: RO**
	IRQ_RAW_STATUS_23_16[7:0]	7:0	Raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: -**	**Access: RO**
	IRQ_RAW_STATUS_31_24[7:0]	7:0	Raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: -**	**Access: RO**
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: -**	**Access: RO**
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	See description of '102F40h'.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default: -**	**Access: RO**
	-	7	Reserved.	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: -**	**Access: RO**
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: -**	**Access: RO**
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: -**	**Access: RO**
	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: -**	**Access: RO**
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	See description of '102F48h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0xE1**	**Access: R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	WDT_EN	0	H/V sync lose watch dog timer count enable.	

IP1_M Register (Bank = 102F, Sub-bank = 01)

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default: -**	**Access: RO**
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.	

IP1_M Register (Bank = 102F, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. 00: Auto detect. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.
	CSC_EN	3	Input CSC function. 0: Disable (RGB -> RGB, default). 1: Enable (RGB -> YCbCr).
	SOURCE_SELECT[2:0]	2:0	Input Source Select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: Reserved. 111: HDMI.
02h (102F05h)	**REG102F05**	**7:0**	**Default: -** **Access: RO**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. 0: Disable (Auto selected by h/W, used when input is video, default). 1: Enable (using 0Dh[3:0] as divider).
	-	6:4	Reserved.
	VDEXT_SYNMD	3	External VD Using Sync. 0: Sync is generated from data internally. 1: Sync from external source.
	YCBCR_EN	2	Input Source is YPbPr Format.
	VIDEO_SELECT[1:0]	1:0	Video Port Select. 00: External 8/10 bit video port. 01: Internal video decoder mode A. 10: External 16/20 bit video port. 11: Internal video decoder mode B.
03h (102F06h)	**REG102F06**	**7:0**	**Default: -** **Access: RO**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted.

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Use SPRHST and SPRHDC as sample range, both H and V positions can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. 0: Delay 1/4 input HSYNC. 1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. 0: Disable. 1: Enable.	
	HARDWARERAP	0	Input image Horizontal wrap. 0: Disable. 1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: -**	**Access: RO**
	FRCV	7	Source Sync Enable. 1: Display will adaptively follow the Source if Display selects this source. 0: Display Free Run if Display selects this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When mode is changed, the Sync Process for this window will be stopped until Source Sync Enable is set to 1 again. This is the backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bit input mode.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: -**	**Access: RO**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: -**	**Access: RO**
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: -**	**Access: RO**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: -**	**Access: RO**
	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: -**	**Access: RO**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: -**	**Access: RO**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: -**	**Access: RO**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. 0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, counted from Hsync to first pixel UV order. 00: Normal. 01: 1. 10: 2.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. 0: Mask. 1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010 (ADC): 0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. 1: Use Hsync only. When ISEL = 011 (DVI): 0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL = 100 (VD): 0: Normal. 1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. 0: Normal. 1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: -**	**Access: RO**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. 0: Use Separate Hs for Coast Period. 1: Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: -**	**Access: RO**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. 0: Leading edge. 1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method (03h[5]=0 is preferred).	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INTLAC_AUTO	4	Interlace/Progressive Manual Switch mode. 0: Auto Switch VST(04), VDC (06). 1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. 0000: 8 Line Ahead from SPRANGE_VST. 0001: 1 Line Ahead from SPRANGE_VST. 0010: 2 Line Ahead from SPRANGE_VST. 0011: 3 Line Ahead from SPRANGE_VST. ... 1111: 15 Line Ahead from SPRANGE_VST.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: -**	**Access: RO**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: -**	**Access: RO**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: -**	**Access: RO**
	DUMMY0B_0_14[7:0]	7:0		
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: -**	**Access: RO**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: -**	**Access: RO**
	HDMI_444_REP	7	HDMI 444 format repetition.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: -**	**Access: RO**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. 0: HARDWARE Auto Decide. 1: SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: -**	**Access: RO**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR. 0: No down, 5-tap supported. 1: Down Enable, ratio / tap depending on 0D[3:0].	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR. 0: No down, 5-tap. 1: 2 to 1 down, 11-tap. Others: Reserved. For ExtVD = BT.656, setting this register to 0 and OVERSAP_EN to 1 will do 2X oversampling.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: -**	**Access: RO**
	DUMMY0D_8_15[7:0]	7:0		
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). 0: Normal. 1: Max value (255) when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). 0: Normal. 1: Max value (255) when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). 0: Normal. 1: Max value (255) when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. 0: Disable. 1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared until ATG_EN = 0).	
	ATG_READY	1	Auto Gain Result Ready. 0: Result not ready.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. 0: Disable. 1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7	Reserved.	
	AV_DET	6	AV Detect for Cb Cr. 0: CbCr Range is defined by 03[2] YCBCR_EN. 1: Cb Cr Min is defined in 89 ATP_GTH, Cb Cr Max is defined in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: -**	**Access: RO**
	AUTO_COAST	7	Auto Coast enable when mode is changed. 0: Disable. 1: Enable.	
	OP2_COAST	6	Coast Status (Read only). 0: Coast is inactive. 1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F).	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. 1. VD. 2. Ext VD 656 Format. 3. Ext 444 Format. The purpose is to provide 2X Pixel Rate for FIR Down Sample, and to give 11-tap filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. 000: Minimum R value. 001: Minimum G value. 010: Minimum G value. 011: Maximum R value. 100: Maximum G value. 101: Maximum B value. 11x: Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: -**	**Access: RO**
	DUMMY0F_8_15[7:0]	7:0		
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: Right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. 0: Not clear. 1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. 0: Update every frame. 1: Keep the history value.	
	JITTER	3	Jitter function Result. 0: No jitter. 1: Jitter present.	
	ATS_HISMD	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.	
	ATS_READY	1	Auto position result Ready.	

IP1_M Register (Bank = 102F, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Result ready. 1: Result not ready.	
	ATS_EN	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs to have an interim of at least 2 frames apart for the ready bit to settle.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: -**	**Access: RO**
	THOLD[3:0]	7:4	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. ... 1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Position Force Pixel Mode. 0: DE or Pixel decided by the Source. 1: Force Pixel Mode.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: -**	**Access: RO**
	ATGSEL_VALUE[7:0]	7:0	Auto Gain Value (selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default: -**	**Access: RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: -**	**Access: RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	ATS_VSTDBUF[12:8]	4:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: -**	**Access: RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	ATS_HSTDBUF[12:8]	4:0	See description of '102F26h'.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (102F28h)	**REG102F28**	**7:0**	**Default: -**	**Access: RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	ATS_VEDDBUF[12:8]	4:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: -**	**Access: RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	ATS_HEDDBUF[12:8]	4:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: -**	**Access: RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right Most point state (previous frame) depending on REG_10H[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	REG_JLST[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: -**	**Access: RO**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. 111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: -**	**Access: RO**
	DUMMY17_8_15[7:0]	7:0		
18h (102F30h)	**REG102F30**	**7:0**	**Default: -**	**Access: RO**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: -**	**Access: RO**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Noise Mask. 000: Mask 0 bit, default value.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			001: Mask 1 bit. 010: Mask 2 bits. 011: Mask 3 bits. 100: Mask 4 bits. 101: Mask 5 bits. 110: Mask 6 bits. 111: Mask 7 bits.	
	ATP_READY	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. 0: Disable. 1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: -**	**Access: RO**
	DUMMY19_8_15[7:0]	7:0		
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: -**	**Access: RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: -**	**Access: RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: -**	**Access: RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: -**	**Access: RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x20**	**Access: RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. 0: In display. 1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: -**	**Access: RO**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x05**	**Access: RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Position Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. 5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: -**	**Access: RO**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Separator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. 0: Disable. 1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This will auto set Current Bank 02[7] = 1 if mode is changed.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. 1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly (Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: -**	**Access: RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. 0: Not active. 1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. 0: Not active. 1: Active.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CS_DET	5	Composite Sync Detect status. 0: Input is not composite sync. 1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detect status. 0: Input is not SOG. 1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: -**	**Access: RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulse Width for measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: -**	**Access: RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. 0: 1 line. 1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Separator Htt.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Htt Report by Mode Detector. 1: Htt Report by Sync Separator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: -**	**Access: RO**
	FIELD_SWMD	7	Shift Line Method when field is switched. 0: Old method. 1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. 0: Active low. 1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_VSPOL).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. 0: Active low. 1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_HSPOL).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_INTLAC).	
21h (102F43h)	**REG102F43**	**7:0**	**Default: -**	**Access: RO**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. 00: Sample V End. 01: Sample V Start. 10: Sample V Start Ahead by Current Bank 09[3:0]. 11: Sample V Start Ahead by Current Bank 09[3:0] x 2.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. 0: Mode Change provided in Data Clock domain. 1: Mode Change provided in Data Clock and Fix Clock domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. 0: From Input DE. 1: From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion when ADC_VIDEO = 1 for Data Align. 0: Normal. 1: Invert.	
	EXT_FIELDMD	2	Video External Field. 0: Use result of internal circuit detection. 1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. 0: Normal. 1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: -**	**Access: RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: -**	**Access: RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, the video interlace freerun mode will be activated.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: -**	**Access: RO**
	VS_SEP_SEL	7	SYNC Separator VSYNC for Mode Detect. 0: Raw VSYNC (H / V Relationship is Kept for Interlace Detect). 1: HSYNC Align VSYNC (H / V Relationship is lost for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			(VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Lines for Another Field. 10: Delay 3 Lines for Another Field. 11: Delay 4 Lines for Another Field.	
	ADC_VIDEO	5	ADC Input Select. 0: PC Source. 1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Lines for Another Field. 10: Delay 3 Lines for Another Field. 11: Delay 4 Lines for Another Field.	
	-	3	Reserved.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when COAST_SRCS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. 0: Internal Separated VSYNC (Default). 1: External VSYNC (Test Purpose).	
	COAST_POL	0	Coast Polarity to pad.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: -**	**Access: RO**
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast starts from 1 HSYNC leading edge. 01: Coast starts from 2 HSYNC leading edge, default value. ... 254: Coast starts from 255 HSYNC leading edge. 255: Coast starts from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: -**	**Access: RO**
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast ends at 1 HSYNC leading edge. 01: Coast ends at 2 HSYNC leading edge, default value. ... 254: Coast ends at 255 HSYNC leading edge.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			255: Coast ends at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: -**	**Access: RO**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. 0: Disable. 1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI: 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPVS_ACT, IPHS_ACT (E1[7:6]) (recommended).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. 0: Normal. 1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: -**	**Access: RO**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: -**	**Access: RO**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames).	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). 0: Disable. 1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). 0: Disable. 1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable. 1: Enable.	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: -**	**Access: RO**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: -**	**Access: RO**
	DUMMY28_0_15[7:0]	7:0		
28h (102F51h)	**REG102F51**	**7:0**	**Default: -**	**Access: RO**
	DUMMY28_0_15[15:8]	7:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. 00: Off. 01: Only for line total number = even. 10: All cases. 11: Off.	
	EUP_AU_HDTV_DET	3	UR/AUS 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUR 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. 0: Defined automatically. 1: Defined by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: -**	**Access: RO**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: -**	**Access: RO**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: -**	**Access: RO**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: -**	**Access: RO**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: -**	**Access: RO**
	-	7:2	Reserved.	

IP1_M Register (Bank = 102F, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description
	GOP_CLK_FREE	1	GOP clock gating enable. 0: Gate the GOP clock. 1: Not gate the GOP clock.
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. 0: Not gate the IDCLK. 1: Gate the IDCLK.
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default: -** **Access: RO**
	-	7:3	Reserved.
	ATS_B_SKIP	2	Auto search ignores B data.
	ATS_G_SKIP	1	Auto search ignores G data.
	ATS_R_SKIP	0	Auto search ignores R data.
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default: -** **Access: RO**
	DE_BYPASS_MODE	7	Use input DE to replace SPRANGE_H as output DE.
	-	6:0	Reserved.
30h (102F60h)	**REG102F60**	**7:0**	**Default: -** **Access: RO**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMBER_OFFSET.
30h (102F61h)	**REG102F61**	**7:0**	**Default: -** **Access: RO**
	INSERT_SEL	7	Vsync INSERT_NUMBER_OFFSET enable.
	-	6:3	Reserved.
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.
31h (102F62h)	**REG102F62**	**7:0**	**Default: -** **Access: RO**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMBER_OFFSET.
31h (102F63h)	**REG102F63**	**7:0**	**Default: -** **Access: RO**
	LOCK_SEL	7	Vsync LOCK_NUMBER_OFFSET enable.
	-	6:3	Reserved.
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.
32h (102F64h)	**REG102F64**	**7:0**	**Default: -** **Access: RO**
	VLOCK_MD	7	Vlock mode.
	-	6	Reserved.
	VLOCK_VAL[5:0]	5:0	Vlock value.
32h (102F65h)	**REG102F65**	**7:0**	**Default: -** **Access: RO**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. 0x: Reference 21[15:14]. 10: Sample V end delay 1 line.

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: -**	**Access: RO**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same time.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: -**	**Access: RO**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: -**	**Access: RO**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: -**	**Access: RO**
	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enabled and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovision or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. 0: Not valid.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Valid.	
	CNT_NUMBER_SEL	6	Select the number of lines of valid input composite/SOG signals to make sure the input signal is stable. 0: 60 lines. 1: 120 lines.	
	MACROVISION_FILTER_SEL [1:0]	5:4	When MACROVISION_FILTER_EN is enabled and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovision or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_ RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: -**	**Access: RO**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: -**	**Access: RO**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: -**	**Access: RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	

IP1_M Register (Bank = 102F, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: -**	**Access: RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: -**	**Access: RO**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: -**	**Access: RO**
	ATGSEL_VALUE_Q[7:0]	7:0	Auto Gain value latch by Vsync pulse.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default: -**	**Access: RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE_Q[9:8]	1:0	See description of '102F7Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: -**	**Access: RO**
	-	7	Reserved.	
	FDET_CHECK_EN	6	H/V sync status check enable.	
	FDET_H_INV	5	H sync invert.	
	FDET_V_INV	4	V sync invert.	
	FDET_VTOTAL_PIX_CNT_EN	3	V total count by pixel clock enable.	
	FDET_SYNC_SRC_SEL[1:0]	2:1	H/V sync source select for mode detection.	
	FDET_EN	0	New mode interlaced detect enable.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: -**	**Access: RO**
	FDET_VWIDTH_TOR[7:0]	7:0	V sync pulse width tolerance.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: -**	**Access: RO**
	FDET_VTOTAL_TOR[7:0]	7:0	V total tolerance.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: -**	**Access: RO**
	-	7:3	Reserved.	
	FDET_STATUS_INTLAC_DET2	2	Mode detect result 2.	
	FDET_STATUS_INTLAC_DET1	1	Mode detect result 1.	
	FDET_STATUS_INTLAC_DET0	0	Mode detect result 0.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VWIDTH0[7:0]	7:0	V sync pulse width 0.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH0[13:8]	5:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VWIDTH1[7:0]	7:0	V sync pulse width 1.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH1[13:8]	5:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL0[7:0]	7:0	V total report 0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL0[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL0[23:16]	7:0	See description of '102F9Ah'.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default: -**	**Access: RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL0[24]	0	See description of '102F9Ah'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL1[7:0]	7:0	V total report 1.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL1[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL1[23:16]	7:0	See description of '102F9Eh'.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: -**	**Access: RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL1[24]	0	See description of '102F9Eh'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL2[7:0]	7:0	V total report 2.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL2[15:8]	7:0	See description of '102FA2h'.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL2[23:16]	7:0	See description of '102FA2h'.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: -**	**Access: RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL2[24]	0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL3[7:0]	7:0	V total report 3.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL3[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: -**	**Access: RO**
	FDET_STATUS_VTOTAL3[23:16]	7:0	See description of '102FA6h'.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: -**	**Access: RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL3[24]	0	See description of '102FA6h'.	
60h ~ 60h (102FC0h ~ 102FC1h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

IP2_M Register (Bank = 102F, Sub-bank = 02)

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bit to 8-bit.	
	DITH_10TO8_EN	2	Dither enable for 10-bit to 8-bit.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '102F08h'.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode. 0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**

IP2_M Register (Bank = 102F, Sub-bank = 02)

Index (Absolute)	Mnemonic	Bit	Description	
(102F0Eh)	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	-	4:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP	6	Cb/Cr swap for 444 to 422.	
	-	5	Reserved.	
	YDELAY_EN	4	Y delay enable.	
	YCDELAY_STEP[3:0]	3:0	Y/C delay pipe step.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0xF2**	**Access: R/W**
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x1F**	**Access: R/W**
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x5E**	**Access: R/W**
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0xF4**	**Access: R/W**
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Format: S7 of 2's complement (-31 <= Y0 <= 31).	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x0C**	**Access: R/W**
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x5A**	**Access: R/W**
	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x37**	**Access: R/W**
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0xF5**	**Access: R/W**
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0xFA**	**Access: R/W**
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0xF7**	**Access: R/W**
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y0. Format: S7 of 2's complement (-15 <= Y0 <= 15).	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0xFE**	**Access: R/W**
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x4B**	**Access: R/W**
	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 127).	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:4	Reserved.	
	PRE_ALIGN_WIDTH[3:0]	3:0	Insert pixel number for mirror mode.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x81**	**Access: R/W**
	IP2_STATUS_CLR	7	IP2 status clear.	
	-	6:1	Reserved.	
	DLAST_ALIGN_EN	0	Data last signal align with IPM fetch number.	
34h	**REG102F69**	**7:0**	**Default: 0x00**	**Access: R/W**

IP2_M Register (Bank = 102F, Sub-bank = 02)

Index (Absolute)	Mnemonic	Bit	Description	
(102F69h)	-	7:5	Reserved.	
	IP2_FLOW_CTRL_EN	4	IP2 flow control enable.	
	FLOW_CTRL_VALUE[3:0]	3:0	IP2 flow control count.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	VIN_CTRL_EN	4	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	3	IP2 VSD input line count number setting enable.	
	VSD_IN_NUM_USR[10:8]	2:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	VOUT_CTRL_EN	4	IP2 VSD output line count control enable.	
	-	3	Reserved.	
	VSD_OUT_NUMBER[10:8]	2:0	See description of '102F6Eh'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: -**	**Access: RO**
	MAX_LBUF_CNT[7:0]	7:0	IP2 line buffer max pixel count.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default: -**	**Access: RO**
	-	7:1	Reserved.	
	BW_NOT_ENOUGH	0	IP2 line buffer full.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: -**	**Access: RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	READ_HSD_OUT_CNT[11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: -**	**Access: RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default: -**	**Access: RO**
	-	7:3	Reserved.	
	READ_VSD_OUT_CNT[10:8	2:0	See description of '102F7Eh'.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	]			
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	
70h ~ 75h (102FE0h ~ 102FEBh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

PNR Register (Bank = 102F, Sub-bank = 05)

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h ~ 10h (102F0Ch ~ 102F21h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_FB2[1:0]	1:0	Main Window Motion Ratio.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for NOC_SEL.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x58**	**Access: R/W**
	PCCS_YMR_SEL_F2	7	Main Window PCCS for YMR selection.	
	PCCS_RC_SATU_EN_F2	6	Main Window PCCS for RC saturation en.	

PNR Register (Bank = 102F, Sub-bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
	PCCS_PAL_MODE_F2	5	Main Window PCCS for PAL enable.	
	DITH_MODE_F2[1:0]	4:3	Main Window PNR dither mode. 00: No process. 01: Truncate. 10: Rounding. 11: Dither.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_INOUT_SWAP_F2	7	Main Window PNR input/output swap.	
	PCCS_EXTPIX_SEL_F2	6	Main Window PCCS pre pixel selection. 0: Select pre pixel (NTSC/n-2). 1: Select ext pixel (PAL/n-4).	
	-	5:0	Reserved.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for c.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window c motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window y motion divide mode.	
16h ~ 1Ch (102F2Ch ~ 102F39h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV	5	DHD Interleaved History MR invert.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DHD_HMR_INT_EN	4	DHD Interleaved History MR enable.	
	DHD_CEDGE_UV_INV	3	DHD C Edge UV invert.	
	DHD_CVAL_UV_INV	2	DHD C Value UV invert.	
	DHD_YMR02_EN	1	DHD YMR02 enable.	
	DHD_EN	0	DHD enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x1C**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_YMR02_TH[5:0]	5:0	DHD YMR02 threshold.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:4	Reserved.	
	DHD_YMR02_GAIN[3:0]	3:0	DHD YMR02 gain.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x18**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_YMR04_TH[5:0]	5:0	DHD YMR04 threshold.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:4	Reserved.	
	DHD_YMR04_GAIN[3:0]	3:0	DHD YMR04 gain.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x10**	**Access: R/W**
	DHD_CVAL_GAIN[7:0]	7:0	DHD C value gain.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:4	Reserved.	
	DHD_DIFFPIX_GAIN[3:0]	3:0	DHD pixel diff gain.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x18**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_CMR02_TH[5:0]	5:0	DHD C motion02 threshold.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:4	Reserved.	
	DHD_CMR02_GAIN[3:0]	3:0	DHD C motion02 gain.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_CMR04_TH[5:0]	5:0	DHD C motion04 threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:4	Reserved.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DHD_CMR04_GAIN[3:0]	3:0	DHD C motion04 gain.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x30**	**Access: R/W**
	DHD_CEDGE_GAIN[7:0]	7:0	DHD C edge gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x10**	**Access: R/W**
	DHD_YEDGE_GAIN[7:0]	7:0	DHD Y edge gain.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DHD_DEBUG0_EN	7	DHD debug0 enable.	
	DHD_DEBUG1_EN	6	DHD debug1 enable.	
	-	5:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x22**	**Access: R/W**
	PNR_TABLEY_15_0[7:0]	7:0	PNR Table Y.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x22**	**Access: R/W**
	PNR_TABLEY_15_0[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x12**	**Access: R/W**
	PNR_TABLEY_31_16[7:0]	7:0	PNR Table Y.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEY_31_16[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEY_47_32[7:0]	7:0	PNR Table Y.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEY_47_32[15:8]	7:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEY_63_48[7:0]	7:0	PNR Table Y.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEY_63_48[15:8]	7:0	See description of '102F66h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x22**	**Access: R/W**
	PNR_TABLEC_15_0[7:0]	7:0	PNR Table C.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x22**	**Access: R/W**
	PNR_TABLEC_15_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x12**	**Access: R/W**
	PNR_TABLEC_31_16[7:0]	7:0	PNR Table C.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEC_31_16[15:8]	7:0	See description of '102F82h'.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEC_47_32[7:0]	7:0	PNR Table C.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEC_47_32[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEC_63_48[7:0]	7:0	PNR Table C.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLEC_63_48[15:8]	7:0	See description of '102F86h'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PCCS_PAL_YEV_W[7:0]	7:0	PCCS Y edge weighting for PAL.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PCCS_PAL_YEV_POW[3:0]	3:0	PCCS Y edge POWNUM for PAL.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PCCS_PAL_CEV_W[7:0]	7:0	PCCS C edge weighting for PAL.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PCCS_PAL_CEV_POW[3:0]	3:0	PCCS C edge POWNUM for PAL.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_PAL_YEV_OFFSET[7:0]	7:0	PCCS Y edge offset for PAL.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_PAL_CEV_OFFSET[7:0]	7:0	PCCS C edge offset for PAL.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_RC_OFFSET[7:0]	7:0	PCCS RC offset.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PCCS_RC_POW[3:0]	3:0	PCCS RC POWNUM.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x05**	**Access: R/W**
	-	7:6	Reserved.	
	PCCS_RC_SATU_W[5:0]	5:0	PCCS RC Saturation weighting.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PCCS_RC_SATU_POW[3:0]	3:0	PCCS RC Saturation POWNUM.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: 0x60**	**Access: R/W**
	PCCS_RC_SATU_OFFSET[7:0]	7:0	PCCS RC Saturation offset.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PCCS_TDELTAC_W[3:0]	3:0	PCCS Saturation compensation weighting.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PCCS_TDELTAC_POW[3:0]	3:0	PCCS Saturation compensation POWNUM.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default: 0x10**	**Access: R/W**
	PCCS_TDELTAC_OFFSET[7:0]	7:0	PCCS Saturation compensation offset.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLECCS_15_0[7:0]	7:0	PNR CCS Table, SMOOTH_EN, SMOOTH_STEP, MV_GAIN, MV_POWNUM.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x38**	**Access: R/W**
	PNR_TABLECCS_15_0[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLECCS_31_16[7:0]	7:0	PNR CCS Table, MV_OFFSET, EV_GAIN_CC, EV_WEIGHT_CC.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x06**	**Access: R/W**
	PNR_TABLECCS_31_16[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x04**	**Access: R/W**
	PNR_TABLECCS_47_32[7:0]	7:0	PNR CCS Table, PRE_WEIGHT_C, PRE_WEIGHT_Y.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x02**	**Access: R/W**
	PNR_TABLECCS_47_32[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PNR_TABLECCS_63_48[7:0]	7:0	PNR CCS Table, POST_WEIGHT_C, POST_WEIGHT_Y.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x01**	**Access: R/W**
	PNR_TABLECCS_63_48[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PNR_TABLECCS_79_64[7:0]	7:0	PNR CCS Table, Y_EV_WEIGHT_Y, Y_EV_OFFSET_Y.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x08**	**Access: R/W**
	PNR_TABLECCS_79_64[15:8]	7:0	See description of '102FA8h'.	
55h	**REG102FAA**	**7:0**	**Default: 0x0F**	**Access: R/W**

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FAAh)	PNR_TABLECCS_95_80[7:0]	7:0	PNR CCS Table, Y_EV_WEIGHT_C, Y_EV_OFFSET_C.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	PNR_TABLECCS_95_80[15:8]	7:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:5	Reserved.	
	PNR_TABLECCS_99_96[4:0]	4:0	PNR CCS Table, EV_WEIGHT_RC.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_CORING_Y[7:0]	7:0	PCCS coring Y.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x0C**	**Access: R/W**
	PCCS_CORING_C[7:0]	7:0	PCCS coring C.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE_15_0[7:0]	7:0	PCCS Table.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE_15_0[15:8]	7:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE_31_16[7:0]	7:0	PCCS Table.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE_31_16[15:8]	7:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x31**	**Access: R/W**
	PCCS_TABLE_47_32[7:0]	7:0	PCCS Table.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x75**	**Access: R/W**
	PCCS_TABLE_47_32[15:8]	7:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE_63_48[7:0]	7:0	PCCS Table.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE_63_48[15:8]	7:0	See description of '102FC6h'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_TABLE_15_0[7:0]	7:0	Reserved Table.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_TABLE_15_0[15:8]	7:0	See description of '102FE0h'.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_TABLE_31_16[7:0]	7:0	Reserved Table.	
71h	**REG102FE3**	**7:0**	**Default: 0x00**	**Access: R/W**

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FE3h)	RESERVED_TABLE_31_16[15:8]	7:0	See description of '102FE2h'.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_TABLE_47_32[7:0]	7:0	Reserved Table.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_TABLE_47_32[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_TABLE_63_48[7:0]	7:0	Reserved Table.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_TABLE_63_48[15:8]	7:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:3	Reserved.	
	PCCS_YEV_SEL	2	New PCCS YEV method enable.	
	BLEND_LPF_TURN_OFF	1	Turn off PCCS blend LPF.	
	MEDIAN_TURN_OFF	0	Turn off PCCS 5tap median filter.	

DNR Register (Bank = 102F, Sub-bank = 06)

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	F2_MR_SOURCE_NRY	4	F2 Motion Source Cur Select. 0: Cur after NR. 1: Cur non-NR.	
	-	3:2	Reserved.	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION enable.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION enable.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	F2_LUT_SOURCE_C[1:0]	7:6	F2 DNR Table C source select. x1: From Y-diff. 10: From MED. 00: From C-diff.	
	F2_LUT_SOURCE_Y[1:0]	5:4	F2 DNR Table Y source select.	

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			x1: From C-diff. 10: From MED. 00: From Y-diff.	
	F2_DNR_TABLEC_LSB_EN	3	F2 DNR Table C LSB Mapping enable.	
	F2_DNR_TABLEY_LSB_EN	2	F2 DNR Table Y LSB Mapping enable.	
	F2_NR_TABLE_SEL_C	1	F2 DNR Table C Mapping Select. 0: non-linear. 1: linear.	
	F2_NR_TABLE_SEL_Y	0	F2 DNR Table Y Mapping Select. 0: non-linear. 1: linear.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	F2_SNR_PATCH_DITH_EN	3	F2_SNR_PATCH_DITH_ENABLE.	
	F2_SNR_PATCH_EN	2	F2_SNR_PATCH_ENABLE.	
	F2_SNR_MD_MODE_EN	1	F2 SNR Motion Mode enable.	
	F2_SNR_EN	0	F2 SNR FUNCTION enable.	
22h (102F45h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DNR_PIX_DITH_EN	4	DNR_PIX_DITH_EN.	
	DNR_LUM_EN	3	DNR_LUM_EN.	
	DNR_MR_EXTRA_EN	2	DNR_MR_EXTRA_EN.	
	DNR_POST_TUNE_EN[1:0]	1:0	DNR_POST_TUNE_EN [0]:Y_EN [1]:C_EN.	
23h ~ 24h (102F47h ~ 102F49h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	F2_NR_ROUND_BIT_C	5	Set C_ROUND described as above.	
	F2_NR_ROUND_BIT_Y	4	Set Y_ROUND described as above.	
	F2_ROUND_MODE_C[1:0]	3:2	F2 DNR C blend rounding select. 00: Add {C_ROUND,0}. 01: Add {dither,0}.	

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: Add frame-base dither. 11: Add {dither[1:0]}.	
	F2_ROUND_MODE_Y[1:0]	1:0	F2 DNR Y blend rounding select. 00: Add {Y_ROUND,0}. 01: Add {dither,0}. 10: Add frame-base dither. 11: Add {dither[1:0]}.	
25h (102F4Bh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	F2_MAX_MOT_ENABLE_C	3	F2_MAX_MOT_ENABLE_C.	
	F2_MAX_MOT_ENABLE_Y	2	F2_MAX_MOT_ENABLE_Y.	
	F2_DNR_FILTER_EN_C	1	F2_DNR_FILTER_EN_C.	
	F2_DNR_FILTER_EN_Y	0	F2_DNR_FILTER_EN_Y.	
26h (102F4Dh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	F2_DNR_FILTER_DIV0_C[2:0]	7:5	F2_DNR_FILTER_DIV0_C.	
	F2_DNR_FILTER_DIV0_Y[2:0]	4:2	F2_DNR_FILTER_DIV0_Y.	
	F2_DNR_FILTER_SIGN_C	1	F2_DNR_FILTER_SIGN_C.	
	F2_DNR_FILTER_SIGN_Y	0	F2_DNR_FILTER_SIGN_Y.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	F2_DNR_FILTER_MODE_C[1:0]	7:6	F2_DNR_FILTER_MODE_C.	
	F2_DNR_FILTER_MODE_Y[1:0]	5:4	F2_DNR_FILTER_MODE_Y.	
	F2_DNR_FILTER_DIV1_C[1:0]	3:2	F2_DNR_FILTER_DIV1_C.	
	F2_DNR_FILTER_DIV1_Y[1:0]	1:0	F2_DNR_FILTER_DIV1_Y.	
28h ~ 2Ah (102F50h ~ 102F55h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x08**	**Access: R/W**
	F2_SHARP_LEVEL[7:0]	7:0	F2 SNR sharpness level.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x07**	**Access: R/W**
	-	7:4	Reserved.	

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F2_POW_NUM[3:0]	3:0	F2 SNR power number.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	F2_SNR_MDIFF_WT[2:0]	2:0	F2 MED motion different shift.	
2Ch (102F59h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: 0x80**	**Access: R/W**
	DNR_Y_MR_MUL[3:0]	7:4	MR MUL.	
	-	3	Reserved.	
	DNR_Y_MR_OFFSET[2:0]	2:0	2's complement MR OFFSET.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DNR_Y_MR_RSH[3:0]	3:0	MR Right Shift.	
2Eh ~ 3Fh (102F5Ch ~ 102F7Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0xBD**	**Access: R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x79**	**Access: R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x56**	**Access: R/W**
	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x34**	**Access: R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x12**	**Access: R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '102F86h'.	
44h	**REG102F88**	**7:0**	**Default: 0xBD**	**Access: R/W**

DNR Register (Bank = 102F, Sub-bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(102F88h)	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x79**	**Access: R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x56**	**Access: R/W**
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x34**	**Access: R/W**
	DNR_TABLEC_1[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x12**	**Access: R/W**
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x70**	**Access: R/W**
	DNR_TABLEY_LSB[7:0]	7:0	DNR TABLEY_LSB.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x07**	**Access: R/W**
	-	7:4	Reserved.	
	DNR_TABLEY_LSB[11:8]	3:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x70**	**Access: R/W**
	DNR_TABLEC_LSB[7:0]	7:0	DNR TABLEC_LSB.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x07**	**Access: R/W**
	-	7:4	Reserved.	
	DNR_TABLEC_LSB[11:8]	3:0	See description of '102F92h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x70**	**Access: R/W**
	DNR_TABLE_LUMFAC_0[7:0]	7:0	DNR TABLE_LUM_0.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: 0x07**	**Access: R/W**
	DNR_TABLE_LUMFAC_0[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: 0x70**	**Access: R/W**
	DNR_TABLE_LUMFAC_1[7:0]	7:0	DNR TABLE_LUM_0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: 0x07**	**Access: R/W**
	DNR_TABLE_LUMFAC_1[15:8]	7:0	See description of '102F9Ah'.	

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default: 0x70**	**Access: R/W**
	DNR_TABLE_LUMFAC_2[7:0]	7:0	DNR TABLE_LUM_0.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default: 0x07**	**Access: R/W**
	DNR_TABLE_LUMFAC_2[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default: 0x70**	**Access: R/W**
	DNR_TABLE_LUMFAC_3[7:0]	7:0	DNR TABLE_LUM_0.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default: 0x07**	**Access: R/W**
	DNR_TABLE_LUMFAC_3[15:8]	7:0	See description of '102F9Eh'.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default: 0x80**	**Access: R/W**
	DNR_COMPLEX_TH[3:0]	7:4	DNR_COMPLEX_TH.	
	DNR_STEADY_TH[3:0]	3:0	Steady Threshold.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DNR_WEIGHT_OFFSET[3:0]	3:0	DNR_WEIGHT_OFFSET.	
69h (102FD2h ~ 102FD3h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default: 0x20**	**Access: R/W**
	DNR_STEADY_TABLE[7:0]	7:0	Steady Threshold LUT.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default: 0xFE**	**Access: R/W**
	DNR_STEADY_TABLE[15:8]	7:0	See description of '102FD4h'.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_STEADY_CNT[7:0]	7:0	Total Steady Count.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_STEADY_CNT[15:8]	7:0	See description of '102FD6h'.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_MEAN_CUR[7:0]	7:0	Total current pix mean.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_MEAN_CUR[15:8]	7:0	See description of '102FD8h'.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_MEAN_MOT[7:0]	7:0	Total motion mean.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_MEAN_MOT[15:8]	7:0	See description of '102FDAh'.	

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_STD_CUR[7:0]	7:0	Total current pix Deviation.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_STD_CUR[15:8]	7:0	See description of '102FDCh'.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_STD_MOT[7:0]	7:0	Total motion Deviation.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default: -**	**Access: RO**
	STATUS_TOTAL_STD_MOT[15:8]	7:0	See description of '102FDEh'.	
70h ~ 7Bh (102FE0h ~ 102FF7h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	

DNR2 Register (Bank = 102F, Sub-Bank = 07)

DNR2 Register (Bank = 102F, Sub-Bank = 07)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_DNR_GAIN_0[4:0]	4:0	COLOR_DNR_GAIN_0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_DNR_GAIN_1[4:0]	4:0	COLOR_DNR_GAIN_1.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_DNR_GAIN_2[4:0]	4:0	COLOR_DNR_GAIN_2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_DNR_GAIN_3[4:0]	4:0	COLOR_DNR_GAIN_3.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_DNR_GAIN_4[4:0]	4:0	COLOR_DNR_GAIN_4.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	

DNR2 Register (Bank = 102F, Sub-Bank = 07)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	COLOR_DNR_GAIN_5[4:0]	4:0	COLOR_DNR_GAIN_5.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_DNR_GAIN_6[4:0]	4:0	COLOR_DNR_GAIN_6.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_DNR_GAIN_7[4:0]	4:0	COLOR_DNR_GAIN_7.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_SNR_GAIN_0[4:0]	4:0	COLOR_SNR_GAIN_0.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_SNR_GAIN_1[4:0]	4:0	COLOR_SNR_GAIN_1.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_SNR_GAIN_2[4:0]	4:0	COLOR_SNR_GAIN_2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_SNR_GAIN_3[4:0]	4:0	COLOR_SNR_GAIN_3.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_SNR_GAIN_4[4:0]	4:0	COLOR_SNR_GAIN_4.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_SNR_GAIN_5[4:0]	4:0	COLOR_SNR_GAIN_5.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_SNR_GAIN_6[4:0]	4:0	COLOR_SNR_GAIN_6.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COLOR_SNR_GAIN_7[4:0]	4:0	COLOR_SNR_GAIN_7.	

FILM Register (Bank = 102F, Sub-bank = 0A)

FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x0C**	**Access: R/W**
	FILM32_EN_F2	7	F2 32 film mode enable.	
	FILM22_EN_F2	6	F2 22 film mode enable.	
	-	5:4	Reserved.	
	PRE32_F2	3	F2 pre32.	
	PRE32_F1	2	F1 pre32.	
	-	1:0	Reserved.	
11h ~ 7Fh (102F22h ~ 102FFFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	

SNR Register (Bank = 102F, Sub-bank = 0C)

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x06**	**Access: R/W**
	DBK_TEST_EN	7	De-blocking test mode.	
	-	6:3	Reserved.	
	DBK_EN_V_F2	2	Vertical de-blocking enable F2.	
	DBK_EN_H_F2	1	Horizontal de-blocking enable F2.	
	DBK_EN_F2	0	De-blocking enable F2.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x30**	**Access: R/W**
	DBK_STD_LOW_THRD[7:0]	7:0	De-blocking active threshold.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x0F**	**Access: R/W**
	DBK_ALPHA_STEP[2:0]	7:5	De-blocking alpha step.	
	-	4	Reserved.	
	DBK_STRENGTH_GAIN_F2[3:0]	3:0	De-blocking strength F2 (.xxxx).	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_MOTION_RATIO_EN_F2	4	De-blocking motion ratio enable F2.	
	-	3:0	Reserved.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0xEF**	**Access: R/W**
	DBK_TABLE_01[7:0]	7:0	De-blocking LUT_01.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0xCD**	**Access: R/W**
	DBK_TABLE_23[7:0]	7:0	De-blocking LUT_23.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0xAB**	**Access: R/W**
	DBK_TABLE_45[7:0]	7:0	De-blocking LUT_45.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x89**	**Access: R/W**
	DBK_TABLE_67[7:0]	7:0	De-blocking LUT_67.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x67**	**Access: R/W**
	DBK_TABLE_89[7:0]	7:0	De-blocking LUT_89.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x45**	**Access: R/W**
	DBK_TABLE_AB[7:0]	7:0	De-blocking LUT_AB.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x23**	**Access: R/W**
	DBK_TABLE_CD[7:0]	7:0	De-blocking LUT_CD.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x01**	**Access: R/W**
	DBK_TABLE_EF[7:0]	7:0	De-blocking LUT_EF.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBK_H_INIT_1_F2[7:0]	7:0	De-blocking H counter initial value[7:0] F2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBK_H_INIT_2_F2[7:0]	7:0	De-blocking H counter initial value[15:8] F2.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DBK_H_INIT_3_F2[3:0]	3:0	De-blocking H counter initial value[19:16] F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_H_INIT_4_F2[4:0]	4:0	De-blocking H counter initial value[24:20] F2.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBK_V_INIT_1_F2[7:0]	7:0	De-blocking V counter initial value[7:0] F2.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBK_V_INIT_2_F2[7:0]	7:0	De-blocking V counter initial value[15:8] F2.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DBK_V_INIT_3_F2[3:0]	3:0	De-blocking V counter initial value[19:16] F2.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_V_INIT_4_F2[4:0]	4:0	De-blocking V counter initial value[24:20] F2.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBK_H_RATIO_1_F2[7:0]	7:0	De-blocking H counter ratio[7:0] F2.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBK_H_RATIO_2_F2[7:0]	7:0	De-blocking H counter ratio[15:8] F2.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DBK_H_RATIO_3_F2[3:0]	3:0	De-blocking H counter ratio[19:16] F2.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_H_RATIO_4_F2[4:0]	4:0	De-blocking H counter ratio[24:20] F2.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBK_V_RATIO_1_F2[7:0]	7:0	De-blocking V counter ratio[7:0] F2.	
1Eh	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Dh)	DBK_V_RATIO_2_F2[7:0]	7:0	De-blocking V counter ratio[15:8] F2.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DBK_V_RATIO_3_F2[3:0]	3:0	De-blocking V counter ratio[19:16] F2.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_V_RATIO_4_F2[4:0]	4:0	De-blocking V counter ratio[24:20] F2.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_H_BLOCK_WIDTH_F2[4:0]	4:0	H block width F2.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_V_BLOCK_WIDTH_F2[4:0]	4:0	V block width F2.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x06**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_H_BOUNDARY_LEFT_F2[4:0]	4:0	H block left boundary F2.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_H_BOUNDARY_RIGHT_F2[4:0]	4:0	H block right boundary F2.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x06**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_V_BOUNDARY_UP_F2[4:0]	4:0	V block up boundary F2.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_V_BOUNDARY_DOWN_F2[4:0]	4:0	V block down boundary F2.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SNR_STD_MOTION_RATIO_EN_F2	2	De-blocking and SNR active threshold motion ratio enable F2.	
	SNR_MOTION_RATIO_EN_F2	1	SNR motion ratio enable F2.	
	SNR_EN_F2	0	SNR enable F2.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x0A**	**Access: R/W**
	SNR_STD_LOW_THRD[7:0]	7:0	SNR active threshold.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x48**	**Access: R/W**
	SNR_ALPHA_STEP[2:0]	7:5	SNR alpha step.	
	-	4	Reserved.	
	SNR_STRENGTH_GAIN_F2[3:0]	3:0	SNR strength F2.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0xCF**	**Access: R/W**
	SNR_TABLE_01[7:0]	7:0	SNR LUT_01.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x69**	**Access: R/W**
	SNR_TABLE_23[7:0]	7:0	SNR LUT_23.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x24**	**Access: R/W**
	SNR_TABLE_45[7:0]	7:0	SNR LUT_45.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x01**	**Access: R/W**
	SNR_TABLE_67[7:0]	7:0	SNR LUT_67.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_TABLE_89[7:0]	7:0	SNR LUT_89.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_TABLE_AB[7:0]	7:0	SNR LUT_AB.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_TABLE_CD[7:0]	7:0	SNR LUT_CD.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_TABLE_EF[7:0]	7:0	SNR LUT_EF.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: 0x62**	**Access: R/W**
	DBK_CORING_STEP_F2[1:0]	7:6	De-blocking blockiness coring step F2.	
	DBK_DEC_STEP_F2[1:0]	5:4	De-blocking decrease step in new mode F2.	
	-	3:2	Reserved.	
	DBK_CORING_EN_F2	1	De-blocking blockiness coring enable F2.	
	DBK_DEC_MODE_EN_F2	0	De-blocking new mode enable F2.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x09**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_BKN_INTERVAL_LEFT_ F2[4:0]	4:0	De-blocking blockiness left interval F2. Location from 2 to 20.	
39h	**REG102F73**	**7:0**	**Default: 0x07**	**Access: R/W**

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F73h)	-	7:5	Reserved.	
	DBK_BKN_INTERVAL_RIGHT_F2[4:0]	4:0	De-blocking blockiness right interval F2. Location from 2 to 20.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: 0x57**	**Access: R/W**
	-	7	Reserved.	
	DBK_BKN_INTERVAL_IIR_ALPHA_INI_F2[2:0]	6:4	De-blocking blockiness interval IIR alpha initial boundary strength F2.	
	-	3	Reserved.	
	DBK_BKN_INTERVAL_IIR_ALPHA_F2[2:0]	2:0	De-blocking blockiness interval IIR alpha strength F2.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0x0A**	**Access: R/W**
	DBK_CORING_THRD_F2[7:0]	7:0	De-blocking blockiness coring low threshold F2.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x47**	**Access: R/W**
	-	7	Reserved.	
	DBK_BLOCKINESS_INTERVAL_IIR_EN_F2	6	De-blocking blockiness interval IIR enable F2.	
	DBK_BLOCKINESS_PIXEL_EN_F2	5	De-blocking blockiness pixel active enable F2.	
	-	4	Reserved.	
	DBK_COARSE_STEP_F2[1:0]	3:2	De-blocking coarse detect step F2.	
	DBK_BK_PULSE_FILTER_EN_F2	1	De-blocking blockiness pulse filter enable F2.	
	DBK_BLOCKINESS_EN_F2	0	De-blocking blockiness detect enable F2.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x03**	**Access: R/W**
	DBK_COARSE_LOW_THRD_F2[7:0]	7:0	De-blocking coarse active threshold F2.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x42**	**Access: R/W**
	-	7	Reserved.	
	DBK_BLOCKINESS_IIR_GAIN_F2[2:0]	6:4	De-blocking blockiness IIR gain F2.	
	-	3	Reserved.	
	DBK_SIDE_STEP_F2[1:0]	2:1	De-blocking side detect step F2.	
	-	0	Reserved.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBK_SIDE_LOW_THRD_F2[7:0]	7:0	De-blocking side active threshold F2.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:6	Reserved.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DBK_BLOCKINESS_STEP_F2[1:0]	5:4	De-blocking blockiness strength step F2.	
	-	3	Reserved.	
	DBK_BK_PULSE_FILTER_F2[2:0]	2:0	De-blocking blockiness pulse filter F2. 0: [-1 -1 4 -1 -1]/2. 1: [-2 -2 4 -2 -2]/2. 2: [-2 0 4 0 -2]/2. 3: [-1 0 4 0 -1]/2. 4: [-2 0 0 4 0 0 -2]/2. 5: [-2 0 0 4 0 0 -2].	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:4	Reserved.	
	DBK_BK_REF_STEP_RIGHT_F2[1:0]	3:2	De-blocking blockiness right reference step F2. 0: No reference. 1: One more right pixel reference. 2: Two more right pixel references.	
	DBK_BK_REF_STEP_LEFT_F2[1:0]	1:0	De-blocking blockiness left reference step F2. 0: No reference. 1: One more left pixel reference. 2: Two more left pixel references.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x18**	**Access: R/W**
	-	7:5	Reserved.	
	DBK_ALPHA_MAX[4:0]	4:0	De-blocking alpha maximum value.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SNR_MR_LPF_EN_F2	0	De-blocking and SNR motion ratio low pass filter enable F2 (LPF is 3x3 mask).	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x10**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_01[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_01.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x32**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_23[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_23.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x54**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_45[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_45.	
59h	**REG102FB3**	**7:0**	**Default: 0x76**	**Access: R/W**

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB3h)	SNR_STD_LOW_MOTION_TABLE_67[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_67.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x98**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_89[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_89.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0xBA**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_AB[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_AB.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0xDC**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_CD[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_CD.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0xFE**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_EF[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_EF.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x10**	**Access: R/W**
	SNR_MOTION_TABLE_01[7:0]	7:0	SNR motion ratio LUT_01.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x32**	**Access: R/W**
	SNR_MOTION_TABLE_23[7:0]	7:0	SNR motion ratio LUT_23.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x54**	**Access: R/W**
	SNR_MOTION_TABLE_45[7:0]	7:0	SNR motion ratio LUT_45.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x76**	**Access: R/W**
	SNR_MOTION_TABLE_67[7:0]	7:0	SNR motion ratio LUT_67.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x98**	**Access: R/W**
	SNR_MOTION_TABLE_89[7:0]	7:0	SNR motion ratio LUT_89.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0xBA**	**Access: R/W**
	SNR_MOTION_TABLE_AB[7:0]	7:0	SNR motion ratio LUT_AB.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0xDC**	**Access: R/W**
	SNR_MOTION_TABLE_CD[7:0]	7:0	SNR motion ratio LUT_CD.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: 0xFE**	**Access: R/W**
	SNR_MOTION_TABLE_EF[7:0]	7:0	SNR motion ratio LUT_EF.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SNR_FUN_BYPASS_EN	0	SNR function bypass enable.	
71h	**REG102FE2**	**7:0**	**Default: 0x13**	**Access: R/W**

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FE2h)	-	7:1	Reserved.	
	DBK_LINE_EN_F2	0	De-blocking method select F2.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default: 0x10**	**Access: R/W**
	DBK_MOTION_TABLE_01[7:0]	7:0	De-blocking motion ratio LUT_01.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default: 0x32**	**Access: R/W**
	DBK_MOTION_TABLE_23[7:0]	7:0	De-blocking motion ratio LUT_23.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default: 0x54**	**Access: R/W**
	DBK_MOTION_TABLE_45[7:0]	7:0	De-blocking motion ratio LUT_45.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default: 0x76**	**Access: R/W**
	DBK_MOTION_TABLE_67[7:0]	7:0	De-blocking motion ratio LUT_67.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default: 0x98**	**Access: R/W**
	DBK_MOTION_TABLE_89[7:0]	7:0	De-blocking motion ratio LUT_89.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default: 0xBA**	**Access: R/W**
	DBK_MOTION_TABLE_AB[7:0]	7:0	De-blocking motion ratio LUT_AB.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default: 0xDC**	**Access: R/W**
	DBK_MOTION_TABLE_CD[7:0]	7:0	De-blocking motion ratio LUT_CD.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default: 0xFE**	**Access: R/W**
	DBK_MOTION_TABLE_EF[7:0]	7:0	De-blocking motion ratio LUT_EF.	
7Ch ~ 7Fh (102FF8h ~ 102FFFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:1	Reserved.	
	MW_BD_REG_EN	0	Main Window Border Register Enable. 0: Sub window Border register enable. 1: Main window Border register Enable.	
02h	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**

S_VOP Register (Bank = 102F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(102F04h)	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDLO_BO[3:0]	7:4	Main window border outside height of Left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.	
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.	
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.	
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.	
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.	
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.	
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.	
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:2	Reserved.	
	181FWINSEL[1:0]	1:0	18h~1Fh Display Window Select. 00: 1st window. 01: 2nd window. 10: 3rd window. 11: 4th window.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEST[7:0]	7:0	Sub window Horizontal Start.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEST[7:0]	7:0	Sub window Vertical Star.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEEND[7:0]	7:0	Sub window Vertical End.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEEND[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.	
0Ch	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F19h)	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEST_3RD[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	See description of '102F24h'.	
13h	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F26h)	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEST_4TH[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEEND_4TH[11:8]	3:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEEND_4TH[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SWBCOL[7:0]	7:0	Sub Window Border Color.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	
18h	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F31h)	S_HBC_GAIN[3:0]	7:4	HBC gain for sub window.	
	S_HBC_EN	3	HBC function enable for sub window.	
	S_HBC_ROUNDING	2	HBC rounding enable for sub window.	
	-	1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	KSTPD[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F3Eh'.	
20h	**REG102F40**	**7:0**	**Default: 0x00**	**Access: R/W**

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F40h)	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control. 0: Disable.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SMEN	7	SVM Main window Enable.	
	SMTE	6	SVM Main window Tap Enable.	
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
	SSWEN	3	SVM Sub window Enable.	
	SSWETE	2	SVM Sub window Tap Enable.	
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.	
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.	
	SVMBYS[1:0]	5:4	SVM Bypass Y Select.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0x: SMV data. 10: Original Y data. 11: Y with tap filter.	
	SCORING[3:0]	3:0	SVM Coring.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SVMLMT[7:0]	7:0	SVM Limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM Main window Step.	
	SMGAIN[3:0]	3:0	SVM Main window Gain.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM Sub window Step.	
	SWGAIN[3:0]	3:0	SVM Sub window Gain.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM Pipe Adjust.	
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	SVM_SEP_DLY	7	SVM Separate Delay Enable.	
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x00**	**Access: R/W**
	C1080I	7	1080i mode. 0: Follow DE. 1: Follow HSYNC.	
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.	
	IPFI	5	To Pad Field Invert enable.	
	I1440	4	Interlace 1440 mode.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			This bit works at frame SBPCM= 0. 0: Disable, horizontal valid pixel = 720; SVM support. 1: Enable, horizontal valid pixel = 1440; does not support SVM.	
	IRDEN	3	Random 10 bit DAC Enable.	
	IHSRE	2	HSYNC Shift control. 0: Shift left. 1: Shift right.	
	IOFI	1	Interlace Output Field Invert.	
	IOEN	0	Interlace Output Enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.	
	-	3:0	Reserved.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	IP_FINV	7	IP Field Inverse.	
	IP_ITLC	6	IP Interlace.	
	SIM	5	Single Interlace Mode. 0: Disable. 1: Enable.	
	LPM	4	LVDS 10-bit Mode. 0: Disable. 1: Enable.	
	BES[1:0]	3:2	Border Extend for SVM.	
	OES[1:0]	1:0	OSD Extend for SVM.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSOFFS[7:0]	7:0	HSYNC Shift Offset.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.	
	RESERVED[1:0]	6:5	RESERVED.	
	-	4	Reserved.	
	HSOFFS[11:8]	3:0	See description of '102F58h'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	R_BRI_OFFSET[7:0]	7:0	Offset for R data.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x00**	**Access: R/W**
	BRI_EN	7	Brightness enable (after gamma).	
	CON_EN	6	Contrast enable (after gamma).	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	G_BRI_OFFSET[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	M_BRI_R[7:0]	7:0	Brightness offset (BRI_FUNCTION) for main window R.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	M_BRI_G[7:0]	7:0	Brightness offset (BRI_FUNCTION) for main window G.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	M_BRI_G[10:8]	2:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: 0x00**	**Access: R/W**
	M_BRI_B[7:0]	7:0	Brightness offset (BRI_FUNCTION) for main window B.	
38h (102F71h)	**REG102F71**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_BRI_R[7:0]	7:0	Brightness offset (BRI_FUNCTION) for sub window R.	
39h (102F73h)	**REG102F73**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_BRI_G[7:0]	7:0	Brightness offset (BRI_FUNCTION) for sub window G.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_BRI_B[7:0]	7:0	Brightness offset (BRI_FUNCTION) for sub window B.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_R_	7:0	Check value for auto mload base0 R channel.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BASE0[7:0]			
3Ch (102F79h)	**REG102F79**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE0 [11:8]	3:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_R_BASE1 [7:0]	7:0	Check value for auto mload base1 R channel.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE1 [11:8]	3:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_G_BASE0 [7:0]	7:0	Check value for auto mload base0 G channel.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE0 [11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_G_BASE1 [7:0]	7:0	Check value for auto mload base1 G channel.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_G_	7	Base1 G channel check error.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ERR_1			
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE1 [11:8]	3:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_B_BASE0 [7:0]	7:0	Check value for auto mload base0 B channel.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE0 [11:8]	3:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_B_BASE1 [7:0]	7:0	Check value for auto mload base1 B channel.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE1 [11:8]	3:0	See description of '102F82h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: R/W**
	CAP_STAGE[3:0]	7:4	Capture stage selection. 0: VOP2_DP input data. 1: BRI output. 2: HBC output. 3: CON_BRI output. 4: FWC output. 5: Gamma output. 6: Noise dither output.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:0	Reserved.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_R_CON_GAIN[11:8]	3:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_G_CON_GAIN[11:8]	3:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_B_CON_GAIN[11:8]	3:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.	
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			CON_BRI.	
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.	
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.	
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	FREEZ_VCNT_VALUE[10:8]	2:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when NEW_LOCK_POINT is set high.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	LOCK_VCNT_VALUE[10:8]	2:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.	
	OTUPUT_FIELD_INV	4	Invert field for output reference signal.	
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.	
	IVS_SEL	2	Select INSERT_END point as input reference for frame PLL.	
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.	
	INPUT_FREEZ	0	V-counter freeze enable.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VCNT_FREEZ_REGION	7	In V-counter freeze status.	
	-	6:2	Reserved.	
	IVS_CNT[9:8]	1:0	Frame number for input reference generate.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for BT.656 format.	
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for BT.656 format.	
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.	
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.	
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.	
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.	
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.	
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.	
	NOISE_DITH_EN	5	Noise dither enable.	
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.	
	CAP_EN	3	Capture image to IP enable.	
	-	2:0	Reserved.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. MAIN_R_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_R_MIN_LIMIT. MAIN_R_MIN_SIGN = 0: MAIN_R_MIN = MAIN_R_MIN_LIMIT.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. MAIN_G_MIN_SIGN = 1: MAIN_G_MIN = -MAIN_G_MIN_LIMIT.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			MAIN_G_MIN_SIGN = 0: MAIN_G_MIN = MAIN_G_MIN_LIMIT.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. MAIN_B_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_B_MIN_LIMIT. MAIN_B_MIN_SIGN = 0: MAIN_R_MIN = MAIN_B_MIN_LIMIT.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value. S.12 format sign bit is bit-12. SUB_R_MIN_SIGN = 1: MAIN_R_MIN = -SUB_R_MIN_LIMIT. SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '102FBCh'.	
5Fh	**REG102FBE**	**7:0**	**Default: 0x00**	**Access: R/W**

S_VOP Register (Bank = 102F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(102FBEh)	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. SUB_G_MIN_SIGN = 1: MAIN_G_MIN = -SUB_G_MIN_LIMIT. SUB_G_MIN_SIGN = 0: MAIN_G_MIN = SUB_G_MIN_LIMIT.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. SUB_B_MIN_SIGN = 1: MAIN_R_MIN = -SUB_B_MIN_LIMIT. SUB_B_MIN_SIGN = 0: MAIN_R_MIN = SUB_B_MIN_LIMIT.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '102FC6h'.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FWC_SAT_FROM_YUV	5	Saturation Calculation from YUV domain.	
	FWC_SUB_EN	4	Sub window fresh white correction function on/off.	
	-	3:2	Reserved.	
	FWC_DITHER_EN	1	Fresh white correction function dither enable.	
	FWC_MAIN_EN	0	Main window fresh white correction function on/off.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	FWC_STRENGTH[3:0]	3:0	Fresh white strength.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FWC_SLOPE[5:0]	5:0	Fresh white strength decreasing slope between gray color and non-gray color area.	
71h	**REG102FE3**	**7:0**	**Default: 0x00**	**Access: R/W**

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FE3h)	FWC_CTH[7:0]	7:0	Fresh white function saturation threshold.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[7:0]	7:0	R adjust offset.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[23:16]	7:0	See description of '102FE4h'.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[31:24]	7:0	See description of '102FE4h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[39:32]	7:0	See description of '102FE4h'.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[47:40]	7:0	See description of '102FE4h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[55:48]	7:0	See description of '102FE4h'.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[63:56]	7:0	See description of '102FE4h'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[71:64]	7:0	See description of '102FE4h'.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[79:72]	7:0	See description of '102FE4h'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[87:80]	7:0	See description of '102FE4h'.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[95:88]	7:0	See description of '102FE4h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[7:0]	7:0	B adjust offset.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[15:8]	7:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[23:16]	7:0	See description of '102FF4h'.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[31:24]	7:0	See description of '102FF4h'.	

S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[39:32]	7:0	See description of '102FF4h'.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[47:40]	7:0	See description of '102FF4h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[55:48]	7:0	See description of '102FF4h'.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[63:56]	7:0	See description of '102FF4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[71:64]	7:0	See description of '102FF4h'.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[79:72]	7:0	See description of '102FF4h'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[87:80]	7:0	See description of '102FF4h'.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[95:88]	7:0	See description of '102FF4h'.	

VOP Register (Bank = 102F, Sub-bank = 10)

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSEND0[7:0]	7:0	20h: Recommended value (power on default value is 0).	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	DB_MASK	0	Double buffer register mask signal. The double buffer register is updated with DB_MASK and DB_LOAD.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSST[7:0]	7:0	Output VSYNC start (only useful when AOVS= 1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h - 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No Signal VSYNC. Registers 22h and 23h are used to define minimum H total.	
	VSST[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSEND[7:0]	7:0	Output VSYNC end (only useful when AOVS= 1). 304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	VSEND[10:8]	2:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEHST[7:0]	7:0	External VD using Sync. 0: Sync is generated from data internally. 1: Sync from external source.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DEHST[11:8]	3:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEHEND[7:0]	7:0	Output DE Horizontal end. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DEHEND[11:8]	3:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEVST[7:0]	7:0	Output DE Vertical Start. 00: Default value.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSTSEL	7	Vertical Start Select. 0: DEVST[10:0] is Output DE vertical start. 1: DEVST[10:0] is Scaling Image Window vertical start.	
	-	6:4	Reserved.	
	DEVST[11:8]	3:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEVEND[7:0]	7:0	Output DE Vertical End. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DEVEND[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start. 48h: Recommended value (power on default is 0).	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SIHST[11:8]	3:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SIHEND[11:8]	3:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	SIVST[7:0]	7:0	Scaling Image window Vertical Start.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SIVST[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: R/W**
	SIVEND[7:0]	7:0	Scaling Image window Vertical End.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SIVEND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: R/W**
	HDTOT[7:0]	7:0	Output Horizontal Total. 53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	HDTOT[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	VDTOT[7:0]	7:0	Output Vertical Total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	VDTOT[11:8]	3:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSEND[7:0]	7:0	20h: Recommended value (power on default value is 0).	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x4C**	**Access: R/W**
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 - 0x23).	
	OUTM	6	Output Mode. 0: Mode 0. 1: Mode 1.	
	HRSM	5	HSYNC Remove Mode. 0: Normal. 1: Remove HSYNC when GPOA (Bank 2 register0x62 - 0x6A) is low.	
	VSGP	4	VSYNC uses GPO9.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable (using Bank 2 register 0x59 - 0x61 to define OVSYNC).	
	EHTT	3	Even H Total. 0: Enable, Output H Total is always even pixels. 1: Disable, Output H Total is always odd pixels.	
	MOD2	2	Mode 2. 0: Disable. 1: Enable.	
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	FPLLMD0	7	Frame PLL Mode 0.	
	SL_TUNE_EN	6	Short line tune enable.	
	AUTO_H_TOTAL_UPDATE_EN	5	Enable update AUTO_H_TOTAL value to H_TOTAL.	
	-	4:2	Reserved.	
	SSC_SHIFT	1	0: Enable. 1: Disable.	
	CLKDIV2_POINT_SELECT	0	0: Original. 1: New.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x20**	**Access: R/W**
	LCK_TH[7:0]	7:0	Frame PLL Lock Threshold.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x08**	**Access: R/W**
	LCK_TH[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x10**	**Access: R/W**
	FTNF[7:0]	7:0	Frame Tune Number of Frame.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x10**	**Access: R/W**
	FTNS[3:0]	7:4	Tune Frame Number of Short-line tune.	
	-	3	Reserved.	
	PIP_REG_EN	2	PIP Register Enable.	
	FPLL_REP_EN	1	Frame PLL Report Enable.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NOISY_GEN	0	Noise Generator.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	PFLL_LMT1[7:0]	7:0	Frame PLL Limit.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	PFLL_LMT0[7:0]	7:0	Frame PLL Limit.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	PFLL_LMT[7:0]	7:0	Frame PLL Limit.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	FPLL_LMT_OFST0[7:0]	7:0	Frame PLL Limit Offset low byte.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	FPLL_LMT_OFST1[7:0]	7:0	Frame PLL Limit Offset high byte.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0xF0**	**Access: R/W**
	M_HBC_GAIN[3:0]	7:4	Main window High brightness gain.	
	M_HBC_EN	3	Main window High brightness enable.	
	M_HBC_ROUNDING	2	Main window High brightness enable.	
	-	1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	ADEAD_EN	7	Ahead mode enable.	
	SWBLBK	6	Sub window Blue screen color. 0: Black color. 1: Blue color.	
	SWBLUE	5	Sub window Blue screen control. 0: Off. 1: On.	
	S_FMCLR_EN	4	Sub window frame color enable.	
	-	3	Reserved.	
	MBD_EN	2	Main window Border Enable.	
	MBLK	1	Main window Black screen control. 0: Off. 1: On.	
	NOSC_EN	0	No Signal Color Enable.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCL_R[7:0]	7:0	Frame Color - Red.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCL_G[7:0]	7:0	Frame Color - Green.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCL_B[7:0]	7:0	Frame Color - Blue.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x02**	**Access: R/W**
	DITHG[1:0]	7:6	Dither coefficient for G channel.	
	DITHB[1:0]	5:4	Dither coefficient for B channel.	
	SROT	3	Spatial coefficient Rotate. 0: Disable. 1: Enable.	
	TROT	2	Temporal coefficient Rotate. 0: Disable. 1: Enable.	
	OBN	1	Output Bits Number (used for 8/10-bit gamma). 0: 8-bit output. 1: 6-bit output (power on default value).	
	DITH	0	Dither function. 0: Off. 1: On.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x2D**	**Access: R/W**
	TL[1:0]	7:6	Top - Left dither coefficient.	
	TR[1:0]	5:4	Top - Right dither coefficient.	
	BL[1:0]	3:2	Bottom - Left dither coefficient.	
	BR[1:0]	1:0	Bottom - Right dither coefficient.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	RST_E_4_FRAME	7	Reset noise generator by frame enable.	
	NDMD	6	Noise Dithering Method.	
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.	
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DT3	3	Dither Type 2 control. 0: Disable dither type 2. 1: Enable dither type 2.	
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.	
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.	
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SHORT_1LINE_DISABLE	6	1: Disable. 0: Enable.	
	-	5	Reserved.	
	EGWT	4	Encode Gamma Write.	
	HTOTAL	3	H Total End 11.	
	HDE_END	2	HDE End 11.	
	HFDE_END	1	HFDE End 11.	
	OUTFRR_EN0	0	Output Free-run Enable.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x03**	**Access: R/W**
	IVS_DIFF_THR[7:0]	7:0	Input vs Different Thresholds.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x07**	**Access: R/W**
	TUNE_FIELD_IP	7	Select insert point of one field for VOP_DISP inset signal.	
	IVS_STB_THR[6:0]	6:0	Input vs Stable Thresholds.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	LMT_ADD_NMB[7:0]	7:0	Limit adjust Number in ACC_FPLL mode.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	FPLL_MD1	7	FPLL Mode 1.	
	FPLL_DIS	6	FPLL Stop.	
	ACC1_SEL[1:0]	5:4	Select modify numbers. 00: 3/4 diff numbers.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			01: 1/2 diff numbers. Others: 1/4 diff numbers.	
	-	3	Reserved.	
	ADD_LINE_SEL	2	Select Add Line into frame or pixel into line.	
	CH_CH_MD1	1	ACC FPLL Mode 1.	
	CH_CH_MD0	0	ACC FPLL Mode 0.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	IVS_PRD_NUM[7:0]	7:0	Count Number per Input v.s.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	IVS_PRD_NUM[11:8]	3:0	See description of '102F3Eh'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCPS	7	LVDS Channel Polarity Swap (P/N swap). 0: Disable. 1: Enable.	
	LCS	6	LVDS Channel Swap. 0: Disable. 1: Enable. When enabled in dual LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap, LVB0M/LVB3M swap, LVB0P/LVB3P swap, LVB1M/LVBCKM swap, LVB1P/LVBCKP swap. When enabled in single LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap.	
	MLXT0	5	MSB/LSB Exchange Type for 6/8/10-bit.	
	LTIM	4	LVDS TI Mode. 0: Normal. 1: TI Mode.	
	OMLX	3	Odd channel MSB/LSB Exchange. 0: Normal. 1: Exchange.	
	EMLX	2	Even channel MSB/LSB Exchange. 0: Normal.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Exchange.	
	ORBX	1	Odd channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.	
	ERBX	0	Even channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLXT1	7	MSB/LSB Exchange Type for 6/8/10-bit.	
	DOT	6	Differential Output Type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/Increased-swing RSDS.	
	WHTS	5	White Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	BLSK	4	Black Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	REVERSE	3	REVERSE luminosity. 0: Off. 1: On.	
	STO	2	Stagger Output (only used when DPO= 1). 0: Disable. 1: Enable.	
	DPX	1	A/B Port Swap (only used when DPO= 1). 0: Disable. 1: Enable.	
	DUAL_PIXEL_OUTPUT	0	Dual Pixel Output. 0: Single pixel. 1: Dual pixel.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	AB_SWAP	5	LVDS A/B Port Swap.	
	CKSEL[4:0]	4:0	Enable clock of internal control. 00h: TTL output. 11H: Single LVDS output. 13h: Dual LVDS output.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	FBLALL_SET	7	Frame buffer less all set.	
	PUT_REG_PTT1	6	Register overwrite 0 bit 1.	
	PDP10BIT	5	PDP 10-bit mode, supporting single 10-bit LVDS PDP.	
	TTL_LVDS	4	TTL LVDS mode, let single TTL and LVDS use same board.	
	BRGS	3	B port pixel R/G Swap. 0: Disable. 1: Enable.	
	ARGS	2	A port pixel R/G Swap. 0: Disable. 1: Enable.	
	BGBS	1	B port pixel G/B Swap. 0: Disable. 1: Enable.	
	AGBS	0	A port pixel G/B Swap. 0: Disable. 1: Enable.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSDCHBLEND	7	OSD Character Blending mode.	
	-	6	Reserved.	
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).	
	-	4	Reserved.	
	GATP	3	Gamma Automatically On/Off based on Auto Phase value. 0: Disable. 1: Enable.	
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			111: 100% transparency.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	MNS_COL[7:0]	7:0	Main Window No Signal Color.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	MBCOL[7:0]	7:0	Main Window Border Color.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	SLOW_RAW_LIM[3:0]	6:3	RAW_THRESHOLD in FPLL_TUNE_SLOW.	
	SLOW_CNT_LIM[2:0]	2:0	Count threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLOCK_DL_LN[2:0]	5:3	Delay line number in Flock mode.	
	FLOCK_AH_LN[2:0]	2:0	Ahead line in Flock mode.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F52h'.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: -128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: -128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: -128~127.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SSFD	7	Sub window Shift Field. 0: Shift even field. 0: Shift odd field.	
	SSLN[1:0]	6:5	Sub window Shift Line Numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.	
	ILIM	4	Insert Line when in Interlace Mode. 0: Do not insert. 1: Insert.	
	MSFD	3	Main window Shift Field. 0: Shift even field. 1: Shift odd field.	
	MSLN[2:0]	2:0	Main window Shift Line Numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 lines between odd and even field. 010: Shift 2 lines between odd and even field. 011: Shift 3 lines between odd and even field. 1xx: Shift 4 lines between odd and even field.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: -**	**Access: RO**
	IFVP[7:0]	7:0	Insert Fraction Vertical Position.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: -**	**Access: RO**
	IFVP[15:8]	7:0	See description of '102F60h'.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
31h (102F62h)	**REG102F62**	**7:0**	**Default: -**	**Access: RO**
	IFRACTW[7:0]	7:0	Insert Fraction Width. PD Down value.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: -**	**Access: RO**
	IFRACTW[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: -**	**Access: RO**
	OVSSTAT[7:0]	7:0	Output Vertical Total Status. Lock status. Equal to 1 when phase error is less than 29h/2Ah.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: -**	**Access: RO**
	-	7	Reserved.	
	OVERDESTAT	6	Output Vertical DE Status.	
	-	5:3	Reserved.	
	OVSSTAT[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	OHTSTAT0[7:0]	7:0	OHSTAT initial value.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: -**	**Access: RO**
	OHTSTAT1[7:0]	7:0	Output H Total Status.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	FRACST0[7:0]	7:0	Fraction initial value.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: -**	**Access: RO**
	FRACST1[7:0]	7:0	Fraction Status.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	FRACST2[2:0]	2:0	Fraction Status.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: -**	**Access: RO**
	-	7:3	Reserved.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FRACST3[2:0]	2:0	Fraction Status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x00**	**Access: R/W**
	HTTMGN[7:0]	7:0	H Total Margin.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x00**	**Access: R/W**
	SSCMGN[7:0]	7:0	SSC Margin.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0x00**	**Access: R/W**
	RSTVALUE0[7:0]	7:0	Read Start initial value.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: -**	**Access: RO**
	RSTVALUE1[7:0]	7:0	Read Start Value.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	RSTVALUE2[4:0]	4:0	Read Start initial value.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	RSTVALUE3[4:0]	4:0	Read Start Value.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FRONT_BACK	5	Set front back mode.	
	-	4:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	INP8	7	This bit along with INE_DRV3 enables G replace R and B for gamma mapping.	
	ONE_DRV3	6	Gamma uses G replace R and B for gamma mapping.	
	GABYP	5	Bypass gamma function.	
	-	4:3	Reserved.	
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	LFCOEF1[2:0]	7:5	Loop filter coefficient 1.	
	LFCOEF2[4:0]	4:0	Loop filter coefficient 2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: R/W**
	TUNE_SLOW[7:0]	7:0	Tune number for OVDE lock value fine tune.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	TFRACN[7:0]	7:0	Target Fraction Number /	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Frame PLL limit RK[7:0].	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7:5	Reserved.	
	FX_PROT	4	Frame Change Protect.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x40**	**Access: R/W**
	TSTMD_REG_EN	7	Test Mode Register Enable. 0: Disable. 1: Enable.	
	EOCK	6	Use External Clock (pin) as Output Dot Clock. 0: Disable (use internal dot clock). 1: Enable (use external dot clock).	
	-	5:3	Reserved.	
	BPM	2	Bypass clock Mode (IDCLK as ODCLK). 0: Disable. 1: Enable.	
	PTEN	1	PLL Test register protect bit. 0: Disable. 1: Enable.	
	LRTM	0	LVDS/RSDS Test Mode enable. 0: Disable. 1: Enable.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: R/W**
	CLKDLYSEL[3:0]	7:4	OCKDLY[3:0]: OCLK Delay adjustment (TCON feature only). 0: 16 steps to adjust. 1: Typical 0.8ns delay/step.	
	OCLK	3	Output CLK control. 0: Normal. 1: Invert.	
	ODE	2	Output DE control. 0: Active high. 1: Active low.	
	OVS	1	Output VSYNC control. 0: Active high. 1: Active low.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OHS	0	Output HSYNC control. 0: Active high. 1: Active low.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	OEDB	5	Output Even Data Bus pin control. 0: Normal. 1: Tri-state.	
	OODB	4	Output Odd Data Bus pin control. 0: Normal. 1: Tri-state.	
	OVS0	3	OVSYNC pin control. 0: Normal. 1: Tri-state.	
	OHS0	2	OHSYNC pin control. 0: Normal. 1: Tri-state.	
	ODE0	1	ODE pin control. 0: Normal. 1: Tri-state.	
	OCLK0	0	OCLK pin control. 0: Normal. 1: Tri-state.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEDRV[1:0]	7:6	Output DE Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
	CLKDRV[1:0]	5:4	Output Clock Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
	ODDDRV[1:0]	3:2	Output data Odd channel Driving current select. 00: 4mA. 01: 6mA. 10: 8mA.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: 12mA.	
	EVENDRV[1:0]	1:0	Output data Even channel Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SKEW[1:0]	5:4	Output data SKEW.	
	ECLKDLY[3:0]	3:0	ECLK Delay adjustment (TCON feature only). 0: 16 steps to adjust. 1: Typical 0.8ns delay/step.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	TEST_CLK_MODE	7	0: Disable. 1: Enable.	
	PLL_DIV2	6	0: Normal. 1: Test clock output divided by 2.	
	DDR_TEST	5	1: Select DDR 29est bus.	
	TEST_MD_D	4	1: Enable 24-bit test bus output.	
	-	3:0	Reserved.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x44**	**Access: R/W**
	LP_SET0[7:0]	7:0	Output PLL Set.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: 0x55**	**Access: R/W**
	LP_SET0[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x00**	**Access: R/W**
	LP_SET1[7:0]	7:0	Output PLL Set.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	OBN10	7	10-bit Bus enable.	
	DITHER_MINUS	6	1: Enable.	
	GPODDC	5	GPO, GPO[3] use for DDC DAT/CLK.	
	M_GRG	4	Main window Gamma Rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIM_HS	7	Limit Htotal by PWM counter enable.	
	NEW_FIELD_SEL	6	Select field create method. 0: Created by Vsync and Hsync. 1: Created by VFDE.	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end. 1: Vsync end.	
	-	4:0	Reserved.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: -**	**Access: RO**
	REM[7:0]	7:0	Htotal REMainder value.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	REM[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5DIV[7:0]	7:0	PWM5 CLK div factor.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	PWM5DIV[8]	0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5DUTY[7:0]	7:0	PWM5 period.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: R/W**
	TRACE_PHASE_HTOTAL[7:0]	7:0	New Htotal for fast phase offset reduction, only active when TRACE_PHASE_EN is set to 1.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	NEW_HBC_CLAMP	6	Clamp function for HBC gain.	
	NEW_HBC_GAIN	5	HBC gain mode. 0: 0.4. 1: 0.04.	
	TRACE_PHASE_EN	4	Enable modify Htotal for fast phase offset reduction.	
	TRACE_PHASE_HTOTAL[11:8]	3:0	See description of '102FB4h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x07**	**Access: R/W**
	BIUCLK_DIV[7:0]	7:0	Calculate VDE ratio BIUCLK divider.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	RPT_VRATIO_EN	0	Report VDE Vtotal ratio enable.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_0_REG[7:0]	7:0		
65h (102FCBh)	**REG102FCB**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_1_REG[7:0]	7:0		
66h (102FCCh)	**REG102FCC**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_2_REG[7:0]	7:0		
66h (102FCDh)	**REG102FCD**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_3_REG[7:0]	7:0		
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_4_REG[7:0]	7:0		
67h (102FCFh)	**REG102FCF**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_5_REG[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default: -**	**Access: RO**
	VDE_PRD_VALUE[7:0]	7:0	Input VDE PRD value.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default: -**	**Access: RO**
	VDE_PRD_VALUE[15:8]	7:0	See description of '102FD0h'.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default: -**	**Access: RO**
	VTT_PRD_VALUE[7:0]	7:0	Input Vtt PRD value.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default: -**	**Access: RO**
	VTT_PRD_VALUE[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default: 0x00**	**Access: R/W**
	HIFRC_SROT	7	Enable HIFRC spatial rotation.	
	RAN[1:0]	6:5	Enable HIFRC RANdom noise latch for rotation.	
	F2_EN	4	Enable noise repeats 2 frames.	
	NEW_DITH_M	3	New dither method select.	
	-	2	Reserved.	
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.	
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.	
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.	
	H_RAN_EN	3	H direction using random noise enable for HIFRC.	
	NEW_ACBD	2	Swap HIFRC probability sequence.	
	OLD_HIFRC	1	Select old HIFRC dither method.	
	RAN_DIR_EN	0	Enable noise as rotate direction.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default: 0x00**	**Access: R/W**
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table read/write address.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default: 0x00**	**Access: R/W**
	LUT_W_FLAG2	7	LUT table blue write command.	
	LUT_W_FLAG1	6	LUT table green write command.	
	LUT_W_FLAG0	5	LUT table red write command.	
	-	4	Reserved.	
	LUT_BW_CH_SEL[1:0]	3:2	Lut table burst write channel selection: 00: Select R channel. 01: Select G channel. 10: Select B channel. 11: Select all R/G/B channels.	
	-	1	Reserved.	
	LUT_BW_MAIN_EN	0	Lut table burst write enable.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default: 0x00**	**Access: R/W**
	LUT_R_FLAG2	7	LUT table blue read command.	
	LUT_R_FLAG1	6	LUT table green read command.	
	LUT_R_FLAG0	5	LUT table red read command.	
	-	4:1	Reserved.	
	LUT_BW_FLAG	0	Lut table burst write status when burst write is enabled.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default: 0x00**	**Access: R/W**
	WR_R[7:0]	7:0	Data write to R LUT SRAM and burst mode data write to selected channel.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	WR_R[11:8]	3:0	See description of '102FDCh'.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default: 0x00**	**Access: R/W**
	WR_G[7:0]	7:0	Data write to G LUT SRAM.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	WR_G[11:8]	3:0	See description of '102FDEh'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	WR_B[7:0]	7:0	Data write to B LUT SRAM.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	WR_B[11:8]	3:0	See description of '102FE0h'.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default: -**	**Access: RO**
	RD_R[7:0]	7:0	Data read from R LUT SRAM.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	RD_R[11:8]	3:0	See description of '102FE2h'.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default: -**	**Access: RO**
	RD_G[7:0]	7:0	Data read from G LUT SRAM.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	RD_G[11:8]	3:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default: -**	**Access: RO**
	RD_B[7:0]	7:0	Data read from B LUT SRAM.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	RD_B[11:8]	3:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7:4	Reserved.	
	CLR_MLOAD_TOO_SLOW	3	Clear auto mload gamma too slow flag.	
	MLOAD_TOO_SLOW	2	Auto mload gamma too slow flag.	
	AUTO_MLOAD_SWITCH	1	Enable auto mload gamma switch gamma table by frame.	
	AUTO_MLOAD_GAMMA	0	Enable auto mload gamma function.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE0[15:8]	7:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE0[23:16]	7:0	See description of '102FEAh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE1[15:8]	7:0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE1[23:16]	7:0	See description of '102FEEh'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default: 0x00**	**Access: R/W**
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	R_MAX_BASE0[11:8]	3:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default: 0x00**	**Access: R/W**
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	R_MAX_BASE1[11:8]	3:0	See description of '102FF6h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default: 0x00**	**Access: R/W**
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	G_MAX_BASE0[11:8]	3:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default: 0x00**	**Access: R/W**
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	G_MAX_BASE1[11:8]	3:0	See description of '102FFAh'.	
7Eh	**REG102FFC**	**7:0**	**Default: 0x00**	**Access: R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FFCh)	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	B_MAX_BASE0[11:8]	3:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	B_MAX_BASE1[11:8]	3:0	See description of '102FFEh'.	

SCMI Register (Bank = 102F, Sub-bank = 12)

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data configuration from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data configuration from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data configuration from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data configuration from mode 5 change to mode 4.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	
	STILL_MODE_F2	3	F2 image freeze enable.	
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.	
02h	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(102F04h)	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.	
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	CAPTURE_START_F2	7	F2 image capture start.	
	IPM_READ_OFF_F2	6	F2 force IP read request disable.	
	MADI_FORCE_OFF_F2	5	F2 force MADI off.	
	MADI_FORCE_ON_F2	4	F2 force MADI on.	
	FBL_25D	3	F2 frame buffer less de-interlace mode.	
	YC_SEPARATE_F2	2	F2 YC separate in FB.	
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.	
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.	
	DUMMY03_6_6	6		
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.	
	IPM_LINEAR_EN_F2	4	F2 IP linear address enable.	
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.	
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.	
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.	
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x08**	**Access: R/W**
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.	
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.	
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.	
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.	
	DOT_LN_PON_SEL_F2	1	F2 OP MADI dot line data select.	
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.	
	8FRAME_MODE_F2	6	F2 8 frames buffer for progressive mode.	
	-	5:4	Reserved.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	Y8_M4_ONLY_MODE_F2	3	F2 FB store Y8/M4 only mode.	
	Y8_ONLY_MODE_F2	2	F2 FB store Y-8bits only.	
	BOB_YMR_10_EN_F2	1	F2 10-bits Bob mode with Y motion.	
	BOB_YMR_8_EN_F2	0	F2 8-bits Bob mode with Y motion.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	DUMMY04_14_14	6	F2 FB store Y-8bits only.	
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.	
	IP_2FRAME_BYPASS_F2	4	F2 IP bypass two frames data to OPM.	
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.	
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.	
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.	
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY05_6_13[1:0]	7:6		
	FRC_FREEMD_F2	5	F2 Force output odd/even toggle when 2DDi for interlace input.	
	MIU_SELECT_F2	4	F2 access MIU0 or MIU1 select.	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	CCS4PAL_EN_F2	7	F2 post CCS for PAL enable.	
	READ_Y_F_FN4_F2	6	F2 read Y(n) and Y(n-4) for PAL CCS.	
	DUMMY05_6_13[7:2]	5:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY06_0_15[7:0]	7:0		
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY06_0_15[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x88**	**Access: R/W**
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.	
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.	
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.	
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.	
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	RW_BANK_MAP_F2[1:0]	7:6	F2 read/write bank mapping mode.	
	4FRAME_MODE_F2	5	F2 4 frames buffer for progressive mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F10h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR1_F2[7:0]	7:0	F2 IP frame buffer base address 1.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR1_F2[15:8]	7:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR1_F2[23:16]	7:0	See description of '102F14h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR2_F2[7:0]	7:0	F2 IP frame buffer base address 2.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR2_F2[15:8]	7:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR2_F2[23:16]	7:0	See description of '102F18h'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	IPM_OFFSET_F2[11:8]	3:0	See description of '102F1Ch'.	
0Fh	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F1Eh)	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	IPM_FETCH_NUM_F2[11:8]	3:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F20h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '102F24h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR2_F2[7:0]	7:0	F2 OP frame buffer base address 2.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR2_F2[15:8]	7:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR2_F2[23:16]	7:0	See description of '102F28h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OPM_OFFSET_F2[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '102F2Eh'.	
18h	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F30h)	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	IPM_VCNT_LIMIT_EN_F2	4	F2 IP line count limit enable.	
	IPM_VCNT_LIMIT_NUM_F2[11:8]	3:0	See description of '102F30h'.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	IPM_W_LIMIT_EN_F2	1	F2 IP write limit enable.	
	IPM_W_LIMIT_MIN_F2	0	F2 IP write limit flag 0: maximum 1: minimum.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SW_HMIR_OFFSET_EN_F2	4	F2 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F2[11:8]	3:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY1D_0_15[7:0]	7:0		
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY1D_0_15[15:8]	7:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY1E_0_15[7:0]	7:0		
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY1E_0_15[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY1F_0_15[7:0]	7:0		
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY1F_0_15[15:8]	7:0	See description of '102F3Eh'.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x10**	**Access: R/W**
	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x10**	**Access: R/W**
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x20**	**Access: R/W**
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.	
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x28**	**Access: R/W**
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x28**	**Access: R/W**
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY26_13_15[2:0]	7:5		
	-	4:0	Reserved.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x88**	**Access: R/W**
	OPW_VP_CNT_CLR_F2	7	OPW write mask field count clear.	
	OPW_MASK_MODE_F2[2:0]	6:4	OPW write mask number by field.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPW_STATUS_CLR_F2	3	OPW status clear enable.	
	-	2:1	Reserved.	
	OPW_WREQ_OFF_F2	0	OPW write request disable.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	OPW_LCNT_STATUS_SEL_F2[2:0]	2:0	OPW write line count status select.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPW_FORCE_ACK	7	OPW read request max number.	
	-	6:4	Reserved.	
	OPW_WBK_OFFSET_EN	3	OPW high priority threshold for read request.	
	OPW_WBK_OFFSET[2:0]	2:0	OPW bank offset.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x10**	**Access: R/W**
	OPW_WREQ_THRD[7:0]	7:0	OPW FIFO threshold for read request.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x10**	**Access: R/W**
	OPW_WREQ_HPRI[7:0]	7:0	OPW high priority threshold for read request.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x20**	**Access: R/W**
	OPW_WREQ_MAX[7:0]	7:0	OPW read request max number.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x20**	**Access: R/W**
	OPW_WFIFO_DEPTH[7:0]	7:0	OPW line buffer length for memory data write.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_2C_F2[7:0]	7:0	F2 status read out for debug.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_2C_F2[15:8]	7:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_2D_F2[7:0]	7:0	F2 status read out for debug.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_2D_F2[15:8]	7:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_2E_F2[7:0]	7:0	F2 status read out for debug.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_2E_F2[15:8]	7:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_2F_F2[7:0]	7:0	F2 status read out for debug.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_2F_F2[15:8]	7:0	See description of '102F5Eh'.	
30h ~ 33h (102F60h ~ 102F67h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY34_7_7	7		
	-	6:0	Reserved.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_35_F2[7:0]	7:0	F2 status read out for debug.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_35_F2[15:8]	7:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_36_F2[7:0]	7:0	F2 status read out for debug.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_36_F2[15:8]	7:0	See description of '102F6Ch'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_38_F2[7:0]	7:0	F2 status read out for debug.	
38h (102F71h)	**REG102F71**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_38_F2[15:8]	7:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_39_F2[7:0]	7:0	F2 status read out for debug.	
39h (102F73h)	**REG102F73**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_39_F2[15:8]	7:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3A_F2[7:0]	7:0	F2 status read out for debug.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3A_F2[15:8]	7:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3B_F2[7:0]	7:0	F2 status read out for debug.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3B_F2[15:8]	7:0	See description of '102F76h'.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3C_F2[7:0]	7:0	F2 status read out for debug.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3C_F2[15:8]	7:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3D_F2[7:0]	7:0	F2 status read out for debug.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3D_F2[15:8]	7:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3E_F2[7:0]	7:0	F2 status read out for debug.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default: -**	**Access: RO**
	STATUS_READ_3E_F2[15:8]	7:0	See description of '102F7Ch'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x08**	**Access: R/W**
	DUMMY40_4_15[3:0]	7:4		
	UPDATE_MEM_CONFIG_EN	3	Update memory format enable.	
	-	2	Reserved.	
	IPM_REG_DBF_EN_F2	1	F2 Register latch with input V sync enable.	
	OPM_REG_DBF_EN	0	Register latch with output V sync enable.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY40_4_15[11:4]	7:0	See description of '102F80h'.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x83**	**Access: R/W**
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.	
	-	3	Reserved.	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: Reserved. 111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. 0: Disable (Auto selected by h/W, used when input is video, default). 1: Enable (using 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. 0: Sync is generated from data internally. 1: Sync from external source.	
	-	2	Reserved.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. 00: External 8/10 bit video port. 01: Internal video decoder mode A. 10: External 16/20 bit video port. 11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x18**	**Access: R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V positions can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Delay 1/4 input HSYNC. 1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.	
	-	1:0	Reserved.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x08**	**Access: R/W**
	FRCV	7	Source Sync Enable. 1: Display will adaptively follow the Source if Display selects this source. 0: Display Free Run if Display selects this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode is changed, the Sync Process for this window will be stopped until Source Sync Enable is set to 1 again. This is the backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10-bit input mode.	
	DATA8_ROUND	2	Use rounding for 8-bit input mode.	
	-	1:0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x01**	**Access: R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x01**	**Access: R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**

OFFLINE Register (Bank = 102F, Sub-bank = 13)

Index (Absolute)	Mnemonic	Bit	Description	
(102F0Bh)	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x10**	**Access: R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x10**	**Access: R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x20**	**Access: R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. 0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, counted from Hsync to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. 0: Mask. 1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010 (ADC): 0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. 1: Use Hsync only. When ISEL = 011 (DVI): 0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL = 100 (VD): 0: Normal.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. 0: Normal. 1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. 0: Use Separate Hs for Coast Period. 1: Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. 0: Leading edge. 1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method (03h[5]=0 is preferred).	
	INTLAC_AUTO	4	Interlace/Progressive Manual Switch mode. 0: Auto Switch VST(04), VDC (06). 1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. 0000: 8 Lines Ahead from SPRANGE_VST. 0001: 1 Line Ahead from SPRANGE_VST. 0010: 2 Lines Ahead from SPRANGE_VST. 0011: 3 Lines Ahead from SPRANGE_VST. ... 1111: 15 Lines Ahead from SPRANGE_VST.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY09_8_15[7:0]	7:0		

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY0B_0_14[7:0]	7:0		
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: R/W**
	HDMI_444_REP	7	HDMI 444 format repetition.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. 0: HARDWARE Auto Decide. 1: SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR. 0: No down, 5 tap supported. 1: Down Enable, ratio / tap depending on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR. 0: No down, 5 tap. 1: 2 to 1 down, 11 tap. Others: Reserved. For ExtVD = BT.656, setting this register to 0 and OVERSAP_EN to 1 will do 2X oversampling.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY0D_8_15[7:0]	7:0		
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	AUTO_COAST	7	Auto Coast enable when mode is changed. 0: Disable.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Enable.	
	OP2_COAST	6	Coast Status (Read only). 0: Coast is inactive. 1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for: 1. VD. 2. Ext VD 656 Format. 3. Ext 444 Format. The purpose is to provide 2X Pixel Rate for FIR Down Sample, and to give 11-tap filter.	
	-	2:0	Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY0F_8_15[7:0]	7:0		
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. 111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY17_8_15[7:0]	7:0		
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x01**	**Access: R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x10**	**Access: R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24].	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray Scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Noise Mask. 000: Mask 0 bit, default value.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			001: Mask 1 bit. 010: Mask 2 bits. 011: Mask 3 bits. 100: Mask 4 bits. 101: Mask 5 bits. 110: Mask 6 bits. 111: Mask 7 bits.	
	ATP_READY	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. 0: Disable. 1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY19_8_15[7:0]	7:0		
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: -**	**Access: RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: -**	**Access: RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: -**	**Access: RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: -**	**Access: RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x20**	**Access: RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line after Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. 0: In display. 1: In blanking.	
	-	2:0	Reserved.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x05**	**Access: RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Position Mode.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. 5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x01**	**Access: R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Separator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. 0: Disable. 1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This will auto set Current Bank 02[7] = 1 if mode is changed.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. 1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly (Active Low).	
	-	1:0	Reserved.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: -**	**Access: RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. 0: Not active. 1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. 0: Not active. 1: Active.	
	CS_DET	5	Composite Sync Detect status. 0: Input is not composite sync. 1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detect status. 0: Input is not SOG. 1: Input is detected as SOG.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: -**	**Access: RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulse Width for measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: -**	**Access: RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. 0: 1 line. 1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Separator Htt. 0: Htt Report by Mode Detector. 1: Htt Report by Sync Separator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	FIELD_SWMD	7	Shift Line Method when field is switched. 0: Old method. 1: New method.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. 0: Active low. 1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_VSPOL).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. 0: Active low. 1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_HSPOL).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_INTLAC).	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	_	7:6	Reserved.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. 0: Mode Change provided in Data Clock domain. 1: Mode Change provided in Data Clock and Fix Clock domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. 0: From input DE. 1: From re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion when ADC_VIDEO = 1 for Data Alignment. 0: Normal. 1: Invert.	
	EXT_FIELDMD	2	Video External Field.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Use result of internal circuit detection. 1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. 0: Normal. 1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: -**	**Access: RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: -**	**Access: RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, video interlace freerun mode is activated.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	VS_SEP_SEL	7	SYNC Separator VSYNC for Mode Detect. 0: Raw VSYNC (H / V Relationship is Kept for Interlace Detect). 1: HSYNC Aligned with VSYNC (H / V Relationship is lost for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Lines for Another Field. 10: Delay 3 Lines for Another Field. 11: Delay 4 Lines for Another Field.	
	ADC_VIDEO	5	ADC Input Select. 0: PC Source. 1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Lines for Another Field. 10: Delay 3 Lines for Another Field.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: Delay 4 Lines for Another Field.	
	-	3	Reserved.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when COAST_SRCS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. 0: Internal Separated VSYNC (Default). 1: External VSYNC (Test Purpose).	
	COAST_POL	0	Coast Polarity to pad.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast starts from 1 HSYNC leading edge. 01: Coast starts from 2 HSYNC leading edge (default). ... 254: Coast starts from 255 HSYNC leading edge. 255: Coast starts from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast ends at 1 HSYNC leading edge. 01: Coast ends at 2 HSYNC leading edge, default value. ... 254: Coast ends at 255 HSYNC leading edge. 255: Coast ends at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x10**	**Access: R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. 0: Disable. 1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI: 000: 0x8 input clock. 001: 1x8 input clock.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			010: 2x8 input clock. 111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPVS_ACT, IPHS_ACT (E1[7:6]) (recommended).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. 0: Normal. 1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY26_8_15[7:0]	7:0		
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). 0: Disable. 1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). 0: Disable. 1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). 0: Disable. 1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Enable.	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY27_8_15[7:0]	7:0		
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY28_0_15[7:0]	7:0		
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY28_0_15[15:8]	7:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. 00: Off. 01: Only for line total number = even. 10: All cases. 11: Off.	
	EUP_AU_HDTV_DET	3	EUR/AUS 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUR 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. 0: Define automatically. 1: Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x01**	**Access: R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	_	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x01**	**Access: R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x10**	**Access: R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: 0x10**	**Access: R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same time.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/V sync lose watch dog enable.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	MACROVISION_FILTER_ RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enabled and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovision or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. 0: Not valid. 1: Valid.	
	CNT_NUMBER_SEL	6	Select the number of lines of valid input composite/SOG signals to make sure the input signal is stable. 0: 60 lines. 1: 120 lines.	
	MACROVISION_FILTER_ SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enabled and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovision or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_ RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	

OFFLINE Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: -**	**Access: RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	Field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: -**	**Access: RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: -**	**Access: RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: -**	**Access: RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	

ACE Register (Bank = 102F, Sub-bank = 18)

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_FCC_8T_EN	7	Main window FCC region 8 enable.	
	MAIN_FCC_7T_EN	6	Main window FCC region 7 enable.	
	MAIN_FCC_6T_EN	5	Main window FCC region 6 enable.	
	MAIN_FCC_5T_EN	4	Main window FCC region 5 enable.	
	MAIN_FCC_4T_EN	3	Main window FCC region 4 enable.	
	MAIN_FCC_3T_EN	2	Main window FCC region 3 enable.	
	MAIN_FCC_2T_EN	1	Main window FCC region 2 enable.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_FCC_1T_EN	0	Main window FCC region 1 enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_FCC_9T_FIRST_EN	1	Main window FCC window 9 priority one enable.	
	MAIN_FCC_9T_EN	0	Main window FCC window 9 enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_FCC_8T_EN	7	Sub window FCC region 8 enable.	
	SUB_FCC_7T_EN	6	Sub window FCC region 7 enable.	
	SUB_FCC_6T_EN	5	Sub window FCC region 6 enable.	
	SUB_FCC_5T_EN	4	Sub window FCC region 5 enable.	
	SUB_FCC_4T_EN	3	Sub window FCC region 4 enable.	
	SUB_FCC_3T_EN	2	Sub window FCC region 3 enable.	
	SUB_FCC_2T_EN	1	Sub window FCC region 2 enable.	
	SUB_FCC_1T_EN	0	Sub window FCC region 1 enable.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_FCC_9T_FIRST_EN	1	Sub window FCC window 9 priority one enable.	
	SUB_FCC_9T_EN	0	Sub window FCC region 9 enable.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T1[7:0]	7:0	FCC region 1 cb target.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T1[7:0]	7:0	FCC region 1 cr target.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T2[7:0]	7:0	FCC region 2 cb target.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T2[7:0]	7:0	FCC region 2 cr target.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T3[7:0]	7:0	FCC region 3 cb target.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T3[7:0]	7:0	FCC region 3 cr target.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T4[7:0]	7:0	FCC region 4 cb target.	
1Bh	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F37h)	FCC_CR_T4[7:0]	7:0	FCC region 4 cr target.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T5[7:0]	7:0	FCC region 5 cb target.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T5[7:0]	7:0	FCC region 5 cr target.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T6[7:0]	7:0	FCC region 6 cb target.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T6[7:0]	7:0	FCC region 6 cr target.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T7[7:0]	7:0	FCC region 7 cb target.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T7[7:0]	7:0	FCC region 7 cr target.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T8[7:0]	7:0	FCC region 8 cb target.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T8[7:0]	7:0	FCC region 8 cr target.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FCC_K_2T[3:0]	7:4	FCC region 2 strength.	
	FCC_K_1T[3:0]	3:0	FCC region 1 strength.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FCC_K_4T[3:0]	7:4	FCC region 4 strength.	
	FCC_K_3T[3:0]	3:0	FCC region 3 strength.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FCC_K_6T[3:0]	7:4	FCC region 6 strength.	
	FCC_K_5T[3:0]	3:0	FCC region 5 strength.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FCC_K_8T[3:0]	7:4	FCC region 8 strength.	
	FCC_K_7T[3:0]	3:0	FCC region 7 strength.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	FCC_K_9T[3:0]	3:0	FCC region 9 strength.	
24h	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F48h)	FCC_WIN1_CB_UP[1:0]	7:6	FCC region 1 target cb up distance.	
	FCC_WIN1_CB_DOWN[1:0]	5:4	FCC region 1 target cb down distance.	
	FCC_WIN1_CR_UP[1:0]	3:2	FCC region 1 target cr up distance.	
	FCC_WIN1_CR_DOWN[1:0]	1:0	FCC region 1 target cr down distance.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN2_CB_UP[1:0]	7:6	FCC region 2 target cb up distance.	
	FCC_WIN2_CB_DOWN[1:0]	5:4	FCC region 2 target cb down distance.	
	FCC_WIN2_CR_UP[1:0]	3:2	FCC region 2 target cr up distance.	
	FCC_WIN2_CR_DOWN[1:0]	1:0	FCC region 2 target cr down distance.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN3_CB_UP[1:0]	7:6	FCC region 3 target cb up distance.	
	FCC_WIN3_CB_DOWN[1:0]	5:4	FCC region 3 target cb down distance.	
	FCC_WIN3_CR_UP[1:0]	3:2	FCC region 3 target cr up distance.	
	FCC_WIN3_CR_DOWN[1:0]	1:0	FCC region 3 target cr down distance.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN4_CB_UP[1:0]	7:6	FCC region 4 target cb up distance.	
	FCC_WIN4_CB_DOWN[1:0]	5:4	FCC region 4 target cb down distance.	
	FCC_WIN4_CR_UP[1:0]	3:2	FCC region 4 target cr up distance.	
	FCC_WIN4_CR_DOWN[1:0]	1:0	FCC region 4 target cr down distance.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN5_CB_UP[1:0]	7:6	FCC region 5 target cb up distance.	
	FCC_WIN5_CB_DOWN[1:0]	5:4	FCC region 5 target cb down distance.	
	FCC_WIN5_CR_UP[1:0]	3:2	FCC region 5 target cr up distance.	
	FCC_WIN5_CR_DOWN[1:0]	1:0	FCC region 5 target cr down distance.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN6_CB_UP[1:0]	7:6	FCC region 6 target cb up distance.	
	FCC_WIN6_CB_DOWN[1:0]	5:4	FCC region 6 target cb down distance.	
	FCC_WIN6_CR_UP[1:0]	3:2	FCC region 6 target cr up distance.	
	FCC_WIN6_CR_DOWN[1:0]	1:0	FCC region 6 target cr down distance.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN7_CB_UP[1:0]	7:6	FCC region 7 target cb up distance.	
	FCC_WIN7_CB_DOWN[1:0]	5:4	FCC region 7 target cb down distance.	
	FCC_WIN7_CR_UP[1:0]	3:2	FCC region 7 target cr up distance.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FCC_WIN7_CR_DOWN[1:0]	1:0	FCC region 7 target cr down distance.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN8_CB_UP[1:0]	7:6	FCC region 8 target cb up distance.	
	FCC_WIN8_CB_DOWN[1:0]	5:4	FCC region 8 target cb down distance.	
	FCC_WIN8_CR_UP[1:0]	3:2	FCC region 8 target cr up distance.	
	FCC_WIN8_CR_DOWN[1:0]	1:0	FCC region 8 target cr down distance.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FCC_WIN9_CB[2:0]	5:3	FCC region 9 target cb distance.	
	FCC_WIN9_CR[2:0]	2:0	FCC region 9 target cr distance.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CBCR_TO_UV	7	Main window cbcr to uv enable.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:4	Reserved.	
	SUB_CBCR_TO_UV	3	Sub window cbcr to uv enable.	
	SUB_ICC_EN	2	Sub window ICC enable.	
	-	1:0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SA_USER_R[3:0]	7:4	Sub window ICC saturation adjustment of R.	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SA_USER_G[3:0]	7:4	Sub window ICC saturation adjustment of G.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SA_USER_B[3:0]	7:4	Sub window ICC saturation adjustment of B.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SA_USER_C[3:0]	7:4	Sub window ICC saturation adjustment of C.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SA_USER_M[3:0]	7:4	Sub window ICC saturation adjustment of M.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F67h)	SUB_SA_USER_Y[3:0]	7:4	Sub window ICC saturation adjustment of Y.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SA_USER_F[3:0]	7:4	Sub window ICC saturation adjustment of F.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SIGN_SA_USER[7:0]	7:0	Sub window ICC decrease saturation.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0xFF**	**Access: R/W**
	WPL_WHITE_PEAK_LIMIT_THRD[7:0]	7:0	White peak limit threshold.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_IBC_EN	7	Main window IBC enable.	
	SUB_IBC_EN	6	Sub window IBC enable.	
	-	5:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_YR_ADJ[5:0]	5:0	Sub window IBC Y adjustment of R.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_YG_ADJ[5:0]	5:0	Sub window IBC Y adjustment of G.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_YB_ADJ[5:0]	5:0	Sub window IBC Y adjustment of B.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_YC_ADJ[5:0]	5:0	Sub window IBC Y adjustment of C.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_YM_ADJ[5:0]	5:0	Sub window IBC Y adjustment of M.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_YY_ADJ[5:0]	5:0	Sub window IBC Y adjustment of Y.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_YF_ADJ[5:0]	5:0	Sub window IBC Y adjustment of F.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_HIGH_PASS_EN	7	Main window Y H_CORING as high pass filter.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_Y_TABLE_STEP[2:0]	6:4	Main window Y H_CORING LUT step.	
	MAIN_PC_MODE	3	Main window PC mode.	
	-	2	Reserved.	
	MAIN_Y_BAND2_H_CORING_EN	1	Main window Y band2 H_CORING enable.	
	MAIN_Y_BAND1_H_CORING_EN	0	Main window Y band1 H_CORING enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_HIGH_PASS_EN	7	Main window C H_CORING as high pass filter.	
	MAIN_C_TABLE_STEP[2:0]	6:4	Main window C H_CORING LUT step.	
	MAIN_WHITE_PEAK_LIMIT_EN	3	Main window white peak limit enable.	
	-	2	Reserved.	
	MAIN_C_BAND2_H_CORING_EN	1	Main window C band2 H_CORING enable.	
	MAIN_C_BAND1_H_CORING_EN	0	Main window C band1 H_CORING enable.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_GAIN_TABLE1[7:0]	7:0	Main window Y gain table 1.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_GAIN_TABLE2[7:0]	7:0	Main window Y gain table 2.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_GAIN_TABLE3[7:0]	7:0	Main window Y gain table 3.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_GAIN_TABLE4[7:0]	7:0	Main window Y gain table 4.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_GAIN_TABLE1[7:0]	7:0	Main window C gain table 1.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_GAIN_TABLE2[7:0]	7:0	Main window C gain table 2.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_GAIN_TABLE3[7:0]	7:0	Main window C gain table 3.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_GAIN_TABLE4[7:0]	7:0	Main window C gain table 4.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_NOISE_MASKING_EN	7	Main window horizontal Y noise-masking enable.	
	MAIN_Y_COLOR_NOISE_MASKING_EN	6	Main window horizontal Y noise-masking color adaptive enable.	
	MAIN_Y_NOISE_MASK_GAIN[5:0]	5:0	Main window horizontal Y noise-masking gain	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			(xxxx.xx).	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_NOISE_MASKING_EN	7	Main window horizontal C noise-masking enable.	
	MAIN_C_COLOR_NOISE_MASKING_EN	6	Main window horizontal C noise-masking color adaptive enable.	
	MAIN_C_NOISE_MASK_GAIN[5:0]	5:0	Main window horizontal C noise-masking gain (xxxx.xx).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	MAIN_Y_NM_MIN_THRD[3:0]	7:4	Main window Y noise-masking min value threshold.	
	MAIN_Y_NM_MAX_THRD[3:0]	3:0	Main window Y noise-masking max value threshold.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0xFF**	**Access: R/W**
	MAIN_C_NM_MIN_THRD[3:0]	7:4	Main window C noise-masking min value threshold.	
	MAIN_C_NM_MAX_THRD[3:0]	3:0	Main window C noise-masking max value threshold.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x81**	**Access: R/W**
	COLOR_PK_WIN1_NM_ENTRY_VALUE[3:0]	7:4	Flesh color adaptive noise-masking strength (x.xxx).	
	-	3:2	Reserved.	
	MAIN_COLOR_NM_STEP[1:0]	1:0	Main window color noise-masking step.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x81**	**Access: R/W**
	COLOR_PK_WIN2_NM_ENTRY_VALUE[3:0]	7:4	Blue color adaptive noise-masking strength (x.xxx).	
	-	3:2	Reserved.	
	SUB_COLOR_NM_STEP[1:0]	1:0	Sub window color noise-masking step.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_HIGH_PASS_EN	7	Sub window Y H_CORING as high pass filter.	
	SUB_Y_TABLE_STEP[2:0]	6:4	Sub window Y H_CORING LUT step.	
	SUB_PC_MODE	3	Sub window PC mode.	
	-	2	Reserved.	
	SUB_Y_BAND2_H_CORING_EN	1	Sub window Y band2 H_CORING enable.	
	SUB_Y_BAND1_H_CORING_EN	0	Sub window Y band1 H_CORING enable.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_C_HIGH_PASS_EN	7	Sub window C H_CORING as high pass filter.	
	SUB_C_TABLE_STEP[2:0]	6:4	Sub window C H_CORING LUT step.	
	SUB_WHITE_PEAK_LIMIT_EN	3	Sub window white peak limit enable.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	2	Reserved.	
	SUB_C_BAND2_H_CORING_EN	1	Sub window C band2 H_CORING enable.	
	SUB_C_BAND1_H_CORING_EN	0	Sub window C band1 H_CORING enable.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_GAIN_TABLE1[7:0]	7:0	Sub window Y gain table 1.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_GAIN_TABLE2[7:0]	7:0	Sub window Y gain table 2.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_GAIN_TABLE3[7:0]	7:0	Sub window Y gain table 3.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_GAIN_TABLE4[7:0]	7:0	Sub window Y gain table 4.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_C_CORE_TABLE1[7:0]	7:0	Sub window C gain table 1.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_C_CORE_TABLE2[7:0]	7:0	Sub window C gain table 2.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_C_CORE_TABLE3[7:0]	7:0	Sub window C gain table 3.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_C_CORE_TABLE4[7:0]	7:0	Sub window C gain table 4.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_NOISE_MASKING_EN	7	Sub window horizontal Y noise-masking enable.	
	SUB_Y_COLOR_NOISE_MASKING_EN	6	Sub window horizontal Y noise-masking color adaptive enable.	
	SUB_Y_NOISE_MASK_GAIN[5:0]	5:0	Sub window horizontal Y noise-masking gain (xxxx.xx).	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_C_NOISE_MASKING_EN	7	Sub window horizontal C noise-masking enable.	
	SUB_C_COLOR_NOISE_MASKING_EN	6	Sub window horizontal C noise-masking color adaptive enable.	
	SUB_C_NOISE_MASK_GAIN[5:0]	5:0	Sub window horizontal C noise-masking gain (xxxx.xx).	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	SUB_Y_NM_MIN_THRD[3:0]	7:4	Sub window Y noise-masking min value threshold.	
	SUB_Y_NM_MAX_THRD[3:0]	3:0	Sub window Y noise-masking max value threshold.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0xFF**	**Access: R/W**
	SUB_C_NM_MIN_THRD[3:0]	7:4	Sub window C noise-masking min value threshold.	
	SUB_C_NM_MAX_THRD[3:0]	3:0	Sub window C noise-masking max value threshold.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_IHC_EN	7	Main window IHC enable.	
	SUB_IHC_EN	6	Sub window IHC enable.	
	-	5:3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Pseudo return to initial value frame numbers. 00: 1 frame initial. 01: 2 frame initial. 10: 4 frame initial. 11: 8 frame initial.	
	PSEUDO_VCLR_EN	0	Pseudo return to initial value by VCLEAR enable.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_HUE_USER_R[6:0]	6:0	Sub window IHC hue adjustment of R.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_HUE_USER_G[6:0]	6:0	Sub window IHC hue adjustment of G.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_HUE_USER_B[6:0]	6:0	Sub window IHC hue adjustment of B.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_HUE_USER_C[6:0]	6:0	Sub window IHC hue adjustment of C.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_HUE_USER_M[6:0]	6:0	Sub window IHC hue adjustment of M.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_HUE_USER_Y[6:0]	6:0	Sub window IHC hue adjustment of Y.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_HUE_USER_F[6:0]	6:0	Sub window IHC hue adjustment of F.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_TEST_EN[1:0]	7:6	Color adaptive test mode enable in horizontal noise-masking.	
	SUB_COLOR_PK_WIN2_EN	5	Sub window color adaptive win2 enable in horizontal noise-masking.	
	SUB_COLOR_PK_WIN1_EN	4	Sub window color adaptive win1 enable in horizontal noise-masking.	
	-	3:2	Reserved.	
	MAIN_COLOR_PK_WIN2_EN	1	Main window color adaptive win2 enable in horizontal noise-masking.	
	MAIN_COLOR_PK_WIN1_EN	0	Main window color adaptive win1 enable in horizontal noise-masking.	
69h	**REG102FD3**	**7:0**	**Default: 0x00**	**Access: R/W**

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FD3h)	-	7:4	Reserved.	
	COLOR_PK_WIN2_TRANSITION _STEP[1:0]	3:2	Color adaptive win2 transition step in horizontal noise-masking.	
	COLOR_PK_WIN1_TRANSITION _STEP[1:0]	1:0	Color adaptive win1 transition step in horizontal noise-masking.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN1_CB_UP[7:0]	7:0	Color adaptive win1 cb up in horizontal noise-masking.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN1_CR_UP[7:0]	7:0	Color adaptive win1 cr up in horizontal noise-masking.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN1_CB_DOWN[7:0]	7:0	Color adaptive win1 cb down in horizontal noise-masking.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN1_CR_DOWN[7:0]	7:0	Color adaptive win1 cr down in horizontal noise-masking.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_CB_UP[7:0]	7:0	Color adaptive win2 cb up in horizontal noise-masking.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_CR_UP[7:0]	7:0	Color adaptive win2 cr up in horizontal noise-masking.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_CB_DOWN[7:0]	7:0	Color adaptive win2 cb down in horizontal noise-masking.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_CR_DOWN[7:0]	7:0	Color adaptive win2 cr down in horizontal noise-masking.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_R2Y_EN	4	Sub window RGB to YCbCr enable.	
	-	3:2	Reserved.	
	R2Y_DITHER_EN	1	RGB to YCbCr dither enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr enable.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_R2Y_EQ_SEL[1:0]	5:4	Sub window RGB to YCbCr equation selection.	
	-	3:2	Reserved.	
	MAIN_R2Y_EQ_SEL[1:0]	1:0	Main window RGB to YCbCr equation selection.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_NM_LOW_Y_EN	4	Sub window mosquito noise low y mode enable.	
	-	3:1	Reserved.	
	MAIN_NM_LOW_Y_EN	0	Main window mosquito noise low y mode enable.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_NM_LOW_Y_TH[7:0]	7:0	Main window mosquito noise low y mode threshold.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_NM_LOW_Y_GAIN[5:0]	5:0	Main window mosquito noise low y mode gain.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_NM_LOW_Y_STEP[1:0]	1:0	Main window mosquito noise low y mode step.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_NM_LOW_Y_TH[7:0]	7:0	Sub window mosquito noise low y mode threshold.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_NM_LOW_Y_GAIN[5:0]	5:0	Sub window mosquito noise low y mode gain.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_NM_LOW_Y_STEP[1:0]	1:0	Sub window mosquito noise low y mode step.	

PEAKING Register (Bank = 102F, Sub-bank = 19)

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	VPS_SRAM_ACT	7	2D peaking line-buffer SRAM active.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2:1	Reserved.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BAND8_PEAKING_EN	7	Main window band8 peaking enable.	
	MAIN_BAND7_PEAKING_EN	6	Main window band7 peaking enable.	
	MAIN_BAND6_PEAKING_EN	5	Main window band6 peaking enable.	
	MAIN_BAND5_PEAKING_EN	4	Main window band5 peaking enable.	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.	
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.	
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.	
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BAND8_COEF_STEP[1:0]	7:6	Main window band8 coefficient step.	
	MAIN_BAND7_COEF_STEP[1:0]	5:4	Main window band7 coefficient step.	
	MAIN_BAND6_COEF_STEP[1:0]	3:2	Main window band6 coefficient step.	
	MAIN_BAND5_COEF_STEP[1:0]	1:0	Main window band5 coefficient step.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_V_NOISE_MASKING_EN	7	Main window vertical Y noise-masking enable.	
	MAIN_V_COLOR_NOISE_ MASKING_EN	6	Main window vertical Y noise-masking color adaptive enable.	
	MAIN_V_NOISE_MASK_GAIN[5:0]	5:0	Main window vertical Y noise-masking gain.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_V_LPF_COEF_2[2:0]	6:4	Main window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_V_LPF_COEF_1[2:0]	2:0	Main window vertical up-down pixel Y LPF coefficient.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_OSD_SHARPNESS_CTRL[5:0]	5:0	Main window user sharpness adjust.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_Y_LPF_COEF[2:0]	6:4	Sub window horizontal Y LPF coefficient.	
	MAIN_SUB_EXCHANGE_EN	3	Main/Sub window swap enable.	
	-	2:1	Reserved.	
	SUB_POST_PEAKING_EN	0	Sub window 2D peaking enable.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BAND8_PEAKING_EN	7	Sub window band8 peaking enable.	
	SUB_BAND7_PEAKING_EN	6	Sub window band7 peaking enable.	
	SUB_BAND6_PEAKING_EN	5	Sub window band6 peaking enable.	
	SUB_BAND5_PEAKING_EN	4	Sub window band5 peaking enable.	
	SUB_BAND4_PEAKING_EN	3	Sub window band4 peaking enable.	
	SUB_BAND3_PEAKING_EN	2	Sub window band3 peaking enable.	
	SUB_BAND2_PEAKING_EN	1	Sub window band2 peaking enable.	
	SUB_BAND1_PEAKING_EN	0	Sub window band1 peaking enable.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BAND4_COEF_STEP[1:0]	7:6	Sub window band4 coefficient step.	
	SUB_BAND3_COEF_STEP[1:0]	5:4	Sub window band3 coefficient step.	
	SUB_BAND2_COEF_STEP[1:0]	3:2	Sub window band2 coefficient step.	
	SUB_BAND1_COEF_STEP[1:0]	1:0	Sub window band1 coefficient step.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BAND8_COEF_STEP[1:0]	7:6	Sub window band8 coefficient step.	
	SUB_BAND7_COEF_STEP[1:0]	5:4	Sub window band7 coefficient step.	
	SUB_BAND6_COEF_STEP[1:0]	3:2	Sub window band6 coefficient step.	
	SUB_BAND5_COEF_STEP[1:0]	1:0	Sub window band5 coefficient step.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_V_NOISE_MASKING_EN	7	Sub window vertical Y noise-masking enable.	
	SUB_V_COLOR_NOISE_MASKING_EN	6	Sub window vertical Y noise-masking color adaptive enable.	
	SUB_V_NOISE_MASK_GAIN[5:0]	5:0	Sub window vertical Y noise-masking gain.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_V_LPF_COEF_2[2:0]	6:4	Sub window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	
	SUB_V_LPF_COEF_1[2:0]	2:0	Sub window vertical up-down pixel Y LPF coefficient.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CORING_THRD_2[3:0]	7:4	Sub window coring threshold 2.	
	SUB_CORING_THRD_1[3:0]	3:0	Sub window coring threshold 1.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_OSD_SHARPNESS_CTRL[5:0]	5:0	Sub window user sharpness adjust.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND5_COEF[5:0]	5:0	Main window band5 coefficient.	
1Ah	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F35h)	-	7:6	Reserved.	
	MAIN_BAND6_COEF[5:0]	5:0	Main window band6 coefficient.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND7_COEF[5:0]	5:0	Main window band7 coefficient.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND8_COEF[5:0]	5:0	Main window band8 coefficient.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM2_SELECT[2:0]	6:4	Main window peaking term2 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM1_SELECT[2:0]	2:0	Main window peaking term1 select.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM4_SELECT[2:0]	6:4	Main window peaking term4 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM3_SELECT[2:0]	2:0	Main window peaking term3 select.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM6_SELECT[2:0]	6:4	Main window peaking term6 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM5_SELECT[2:0]	2:0	Main window peaking term5 select.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM8_SELECT[2:0]	6:4	Main window peaking term8 select.	
	-	3	Reserved.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_PEAKING_TERM7_ SELECT[2:0]	2:0	Main window peaking term7 select.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM10_ SELECT[2:0]	6:4	Main window peaking term10 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM9_ SELECT[2:0]	2:0	Main window peaking term9 select.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM12_ SELECT[2:0]	6:4	Main window peaking term12 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM11_ SELECT[2:0]	2:0	Main window peaking term11 select.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM14_ SELECT[2:0]	6:4	Main window peaking term14 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM13_ SELECT[2:0]	2:0	Main window peaking term13 select.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM16_ SELECT[2:0]	6:4	Main window peaking term16 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM15_ SELECT[2:0]	2:0	Main window peaking term15 select.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND1_OVERSHOOT_LIMIT[7:0]	7:0	Main window band1 overshoot limit.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND2_OVERSHOOT_LIMIT[7:0]	7:0	Main window band2 overshoot limit.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND3_OVERSHOOT_LIMIT[7:0]	7:0	Main window band3 overshoot limit.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND4_OVERSHOOT_LIMIT[7:0]	7:0	Main window band4 overshoot limit.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND5_OVERSHOOT_LIMIT[7:0]	7:0	Main window band5 overshoot limit.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND6_OVERSHOOT_LIMIT[7:0]	7:0	Main window band6 overshoot limit.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND7_OVERSHOOT_LIMIT[7:0]	7:0	Main window band7 overshoot limit.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND8_OVERSHOOT_LIMIT[7:0]	7:0	Main window band8 overshoot limit.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND1_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band1 undershoot limit.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND2_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band2 undershoot limit.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND3_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band3 undershoot limit.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND4_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band4 undershoot limit.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND5_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band5 undershoot limit.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND6_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band6 undershoot limit.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND7_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band7 undershoot limit.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND8_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band8 undershoot limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND1_COEF[5:0]	5:0	Sub window band1 coefficient.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BAND2_COEF[5:0]	5:0	Sub window band2 coefficient.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND3_COEF[5:0]	5:0	Sub window band3 coefficient.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND4_COEF[5:0]	5:0	Sub window band4 coefficient.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND5_COEF[5:0]	5:0	Sub window band5 coefficient.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND6_COEF[5:0]	5:0	Sub window band6 coefficient.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND7_COEF[5:0]	5:0	Sub window band7 coefficient.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND8_COEF[5:0]	5:0	Sub window band8 coefficient.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM2_SELECT[2:0]	6:4	Sub window peaking term2 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM1_SELECT[2:0]	2:0	Sub window peaking term1 select.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM4_SELECT[2:0]	6:4	Sub window peaking term4 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM3_SELECT[2:0]	2:0	Sub window peaking term3 select.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM6_SELECT[2:0]	6:4	Sub window peaking term6 select.	
	-	3	Reserved.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_PEAKING_TERM5_SELECT[2:0]	2:0	Sub window peaking term5 select.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM8_SELECT[2:0]	6:4	Sub window peaking term8 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM7_SELECT[2:0]	2:0	Sub window peaking term7 select.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM10_SELECT[2:0]	6:4	Sub window peaking term10 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM9_SELECT[2:0]	2:0	Sub window peaking term9 select.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM12_SELECT[2:0]	6:4	Sub window peaking term12 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM11_SELECT[2:0]	2:0	Sub window peaking term11 select.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM14_SELECT[2:0]	6:4	Sub window peaking term14 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM13_SELECT[2:0]	2:0	Sub window peaking term13 select.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM16_SELECT[2:0]	6:4	Sub window peaking term16 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM15_SELECT[2:0]	2:0	Sub window peaking term15 select.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_COLOR_PEAKING_EN	7	Main window color adaptive peaking enable.	
	-	6:4	Reserved.	
	SUB_COLOR_PEAKING_EN	3	Sub window color adaptive peaking enable.	
	-	2:0	Reserved.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x33**	**Access: R/W**
	MAIN_COLOR_CORING_EN	7	Main window color adaptive coring enable.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6	Reserved.	
	MAIN_CORING_THRD_STEP[1:0]	5:4	Main window coring step.	
	SUB_COLOR_CORING_EN	3	Sub window color adaptive coring enable.	
	-	2	Reserved.	
	SUB_CORING_THRD_STEP[1:0]	1:0	Sub window coring step.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BAND2_CORING_THRD[3:0]	7:4	Main window band2 coring threshold.	
	MAIN_BAND1_CORING_THRD[3:0]	3:0	Main window band1 coring threshold.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BAND4_CORING_THRD[3:0]	7:4	Main window band4 coring threshold.	
	MAIN_BAND3_CORING_THRD[3:0]	3:0	Main window band3 coring threshold.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BAND6_CORING_THRD[3:0]	7:4	Main window band6 coring threshold.	
	MAIN_BAND5_CORING_THRD[3:0]	3:0	Main window band5 coring threshold.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BAND8_CORING_THRD[3:0]	7:4	Main window band8 coring threshold.	
	MAIN_BAND7_CORING_THRD[3:0]	3:0	Main window band7 coring threshold.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BAND2_CORING_THRD[3:0]	7:4	Sub window band2 coring threshold.	
	SUB_BAND1_CORING_THRD[3:0]	3:0	Sub window band1 coring threshold.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BAND4_CORING_THRD[3:0]	7:4	Sub window band4 coring threshold.	
	SUB_BAND3_CORING_THRD[3:0]	3:0	Sub window band3 coring threshold.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BAND6_CORING_THRD[3:0]	7:4	Sub window band6 coring threshold.	
	SUB_BAND5_CORING_THRD[3:0]	3:0	Sub window band5 coring threshold.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BAND8_CORING_THRD[3:0]	7:4	Sub window band8 coring threshold.	
	SUB_BAND7_CORING_THRD[3:0]	3:0	Sub window band7 coring threshold.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_CORING_THRD_SEC[5:0]	5:0	Main window color coring limit.	
37h	**REG102F6F**	**7:0**	**Default: 0x00**	**Access: R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Fh)	-	7:6	Reserved.	
	SUB_CORING_THRD_SEC[5:0]	5:0	Sub window color coring limit.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0xFF**	**Access: R/W**
	MAIN_Y_V_NM_MIN_THRD[3:0]	7:4	Main window vertical Y mosquito noise remove min value threshold.	
	MAIN_Y_V_NM_MAX_THRD[3:0]	3:0	Main window vertical Y mosquito noise remove max value threshold.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: 0xFF**	**Access: R/W**
	SUB_Y_V_NM_MIN_THRD[3:0]	7:4	Sub window vertical Y mosquito noise remove min value threshold.	
	SUB_Y_V_NM_MAX_THRD[3:0]	3:0	Sub window vertical Y mosquito noise remove max value threshold.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CR_DELAY_NUM[1:0]	7:6	Sub window cr delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
	MAIN_CR_DELAY_NUM[1:0]	5:4	Main window cr delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
	-	3:2	Reserved.	
	SUB_YC_DELAY_EN	1	Sub window yc delay enable.	
	MAIN_YC_DELAY_EN	0	Main window yc delay enable.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CB_DELAY_NUM[1:0]	7:6	Sub window cb delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
	SUB_Y_DELAY_NUM[1:0]	5:4	Sub window y delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_CB_DELAY_NUM[1:0]	3:2	Main window cb delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
	MAIN_Y_DELAY_NUM[1:0]	1:0	Main window y delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_GAUSS_LUT_STEP[1:0]	5:4	Main window Gaussian SNR LUT step.	
	-	3:1	Reserved.	
	MAIN_GAUSS_NR_EN	0	Main window Gaussian SNR enable.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	MAIN_GAUSS_THRD[4:0]	4:0	Main window Gaussian SNR threshold.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_GAUSS_LUT_STEP[1:0]	5:4	Sub window Gaussian SNR LUT step.	
	-	3:1	Reserved.	
	SUB_GAUSS_NR_EN	0	Sub window green Gaussian SNR bypass enable.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_GAUSS_THRD[4:0]	4:0	Sub window Gaussian SNR threshold.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_DERING_REF_WIDTH[1:0]	5:4	Main window dering reference width. 0: 5-pixel. 1: 4-pixel. 2: 3-pixel. 3: 2-pixel.	
	-	3	Reserved.	
	MAIN_DERING_INT_MUX[1:0]	2:1	Main window dering intensity mux.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_DERING_EN	0	Main window dering enable.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_DERING_REF_WIDTH[1:0]	5:4	Sub window dering reference width. 0: 5-pixel. 1: 4-pixel. 2: 3-pixel. 3: 2-pixel.	
	-	3	Reserved.	
	SUB_DERING_INT_MUX[1:0]	2:1	Sub window dering intensity mux.	
	SUB_DERING_EN	0	Sub window dering enable.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x88**	**Access: R/W**
	SUB_DERING_BRIGHT_GAIN[3:0]	7:4	Sub window dering bright strength gain (x.xxx).	
	MAIN_DERING_BRIGHT_GAIN[3:0]	3:0	Main window dering bright strength gain (x.xxx).	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x88**	**Access: R/W**
	SUB_DERING_DARK_GAIN[3:0]	7:4	Sub window dering dark strength gain (x.xxx).	
	MAIN_DERING_DARK_GAIN[3:0]	3:0	Main window dering dark strength gain (x.xxx).	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_LUT_0[7:0]	7:0	Gaussian SNR Table 0.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_LUT_1[7:0]	7:0	Gaussian SNR Table 1.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_LUT_2[7:0]	7:0	Gaussian SNR Table 2.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_LUT_3[7:0]	7:0	Gaussian SNR Table 3.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_LUT_4[7:0]	7:0	Gaussian SNR Table 4.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_LUT_5[7:0]	7:0	Gaussian SNR Table 5.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_LUT_6[7:0]	7:0	Gaussian SNR Table 6.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_LUT_7[7:0]	7:0	Gaussian SNR Table 7.	
7Bh	**REG102FF6**	**7:0**	**Default: 0x00**	**Access: R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FF6h)	-	7:5	Reserved.	
	SUB_V_NM_LOW_Y_EN	4	Sub window vertical mosquito noise low y mode enable.	
	-	3:1	Reserved.	
	MAIN_V_NM_LOW_Y_EN	0	Main window vertical mosquito noise low y mode enable.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_V_NM_LOW_Y_TH[7:0]	7:0	Main window vertical mosquito noise low y mode threshold.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_V_NM_LOW_Y_GAIN[5:0]	5:0	Main window vertical mosquito noise low y mode gain.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_V_NM_LOW_Y_STEP[1:0]	1:0	Main window vertical mosquito noise low y mode step.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_V_NM_LOW_Y_TH[7:0]	7:0	Sub window vertical mosquito noise low y mode threshold.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_V_NM_LOW_Y_GAIN[5:0]	5:0	Sub window vertical mosquito noise low y mode gain.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_V_NM_LOW_Y_STEP[1:0]	1:0	Sub window vertical mosquito noise low y mode step.	

DLC Register (Bank = 102F, Sub-bank = 1A)

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F02h)	MAIN_STATISTIC_V_START[7:0]	7:0	Main window histogram vertical start.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_STATISTIC_V_END[7:0]	7:0	Main window histogram vertical end.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_PRE_Y_GAIN_LSB[3:0]	7:4	Main window pre Y gain LSB. PRE_Y_GAIN_NEW(2.10) = {PRE_Y_GAIN, PRE_Y_GAIN_LSB}.	
	MAIN_Y_GAIN_LSB[3:0]	3:0	Main window Y gain LSB. Y_GAIN_NEW(2.10) = {Y_GAIN, Y_GAIN_LSB}.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_PRE_Y_GAIN_LSB[3:0]	7:4	Sub window pre Y gain LSB. PRE_Y_GAIN_NEW(2.10) = {PRE_Y_GAIN, PRE_Y_GAIN_LSB}.	
	SUB_Y_GAIN_LSB[3:0]	3:0	Sub window Y gain LSB. Y_GAIN_NEW(2.10) = {Y_GAIN, Y_GAIN_LSB}.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_STATISTIC_V_START[7:0]	7:0	Sub window histogram vertical start.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_STATISTIC_V_END[7:0]	7:0	Sub window histogram vertical end.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	MAIN_CURVE_FIT_EN	7	Main window Luma curve enable.	
	SUB_CURVE_FIT_EN	6	Sub window Luma curve enable.	
	-	5	Reserved.	
	HISTOGRAM_MODE	4	0: 3 section. 1: 8 section.	
	STATISTIC_ACK	3	Histogram Acknowledge.	
	STATISTIC_REQUEST	2	Histogram Request.	
	MAIN_STATISTIC_EN	1	Main window statistic enable.	
	SUB_STATISTIC_EN	0	Sub window statistic enable.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	STATISTIC_LOCATE[1:0]	7:6	Statistic locate. 00: Original location, before Y_CURVE_FIT. 01: Before LCE.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: Before H_CORING. 11: After PRE_YGAIN, before 2D_PEAKING.	
	MAIN_CURVE_FIT_RGB_EN	5	Main window Luma curve enable as PC (RGB) mode enable.	
	SUB_CURVE_FIT_RGB_EN	4	Sub window Luma curve enable as PC (RGB) mode enable.	
	PRE_BRI_DITHER_EN	3	Pre-y gain dither bit enable.	
	HIS_Y_RGB_MODE_EN	2	Histogram Y report as PC (RGB) mode enable.	
	ACC_COUNTER22_EN	1	Histogram report sum accumulator add 1 bit.	
	VARIABLE_RANGE_EN	0	Variable 8 section of histogram enable.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	HIS_ACCELERATE_EN	0	Histogram Accelerate Enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: -**	**Access: RO**
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximum pixel.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: -**	**Access: RO**
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: -**	**Access: RO**
	SUB_MAX_PIXEL[7:0]	7:0	Sub window maximum pixel.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: -**	**Access: RO**
	SUB_MIN_PIXEL[7:0]	7:0	Sub window minimum pixel.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_WHITE_SLOP_LSB[2:0]	6:4	Main window white slope LSB. SLOPE_NEW(1.10) = {slope, SLOPE_LSB}.	
	-	3	Reserved.	
	MAIN_BLACK_SLOP_LSB[2:0]	2:0	Main window black slope LSB. SLOPE_NEW(1.10) = {slope, SLOPE_LSB}.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_WHITE_SLOP_LSB[2:0]	6:4	Sub window white slope LSB. SLOPE_NEW(1.10) = {slope, SLOPE_LSB}.	
	-	3	Reserved.	
	SUB_BLACK_SLOP_LSB[2:0]	2:0	Sub window black slope LSB.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			SLOPE_NEW(1.10) = {slope, SLOPE_LSB}.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_BRI_ADJUST_LSB[1:0]	1:0	Sub window Y adjust low bit.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BRI_ADJUST[7:0]	7:0	Sub window Y adjust.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x40**	**Access: R/W**
	MAIN_Y_GAIN[7:0]	7:0	Main window Y gain.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x40**	**Access: R/W**
	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x40**	**Access: R/W**
	SUB_Y_GAIN[7:0]	7:0	Sub window Y gain.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x40**	**Access: R/W**
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x40**	**Access: R/W**
	MAIN_PRE_Y_GAIN[7:0]	7:0	Main window pre-Y gain.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x40**	**Access: R/W**
	SUB_PRE_Y_GAIN[7:0]	7:0	Sub window pre-Y gain.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_SECOND_POST_BRI_ADJUST_LSB[1:0]	3:2	Main window second post Y adjust low bit (2's complement).	
	MAIN_POST_BRI_ADJUST_LSB[1:0]	1:0	Main window post Y adjust low bit (2's complement).	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_SECOND_POST_BRI_ADJUST_LSB[1:0]	3:2	Sub window second post Y adjust low bit (2's complement).	
	SUB_POST_BRI_ADJUST_LSB[1:0]	1:0	Sub window post Y adjust low bit (2's complement).	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_POST_BRI_ADJUST[7:0]	7:0	Main window post Y adjust.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_POST_BRI_ADJUST[7:0]	7:0	Sub window post Y adjust.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_SECOND_POST_BRI_ADJUST[7:0]	7:0	Main window second post Y adjust.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SECOND_POST_BRI_ADJUST[7:0]	7:0	Sub window second post Y adjust.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x20**	**Access: R/W**
	HISTOGRAM_RANGE1[7:0]	7:0	Variable 8 section of histogram range 1.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x40**	**Access: R/W**
	HISTOGRAM_RANGE2[7:0]	7:0	Variable 8 section of histogram range 2.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x60**	**Access: R/W**
	HISTOGRAM_RANGE3[7:0]	7:0	Variable 8 section of histogram range 3.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x80**	**Access: R/W**
	HISTOGRAM_RANGE4[7:0]	7:0	Variable 8 section of histogram range 4.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0xA0**	**Access: R/W**
	HISTOGRAM_RANGE5[7:0]	7:0	Variable 8 section of histogram range 5.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0xC0**	**Access: R/W**
	HISTOGRAM_RANGE6[7:0]	7:0	Variable 8 section of histogram range 6.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0xE0**	**Access: R/W**
	HISTOGRAM_RANGE7[7:0]	7:0	Variable 8 section of histogram range 7.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_1F_00[7:0]	7:0	Histogram report section1.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_1F_00[15:8]	7:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_3F_20[7:0]	7:0	Histogram report section2.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_3F_20[15:8]	7:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_5F_40[7:0]	7:0	Histogram report section3.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_5F_40[15:8]	7:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_7F_60[7:0]	7:0	Histogram report section4.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_7F_60[15:8]	7:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_9F_80[7:0]	7:0	Histogram report section5.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_9F_80[15:8]	7:0	See description of '102F58h'.	
2Dh	**REG102F5A**	**7:0**	**Default: -**	**Access: RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F5Ah)	TOTAL_BF_A0[7:0]	7:0	Histogram report section6.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_BF_A0[15:8]	7:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_DF_C0[7:0]	7:0	Histogram report section7.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_DF_C0[15:8]	7:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_FF_E0[7:0]	7:0	Histogram report section8.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_FF_E0[15:8]	7:0	See description of '102F5Eh'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x08**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x18**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x28**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x38**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x48**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x58**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x68**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x78**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x88**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x98**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0xA8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0xC8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0xD8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0xE8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default: 0xF8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: 0x08**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_0[7:0]	7:0	Sub window curve table 0.	
38h (102F71h)	**REG102F71**	**7:0**	**Default: 0x18**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_1[7:0]	7:0	Sub window curve table 1.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x28**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_2[7:0]	7:0	Sub window curve table 2.	
39h (102F73h)	**REG102F73**	**7:0**	**Default: 0x38**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_3[7:0]	7:0	Sub window curve table 3.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: 0x48**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_4[7:0]	7:0	Sub window curve table 4.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default: 0x58**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_5[7:0]	7:0	Sub window curve table 5.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x68**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_6[7:0]	7:0	Sub window curve table 6.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x78**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_7[7:0]	7:0	Sub window curve table 7.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0x88**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_8[7:0]	7:0	Sub window curve table 8.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default: 0x98**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_9[7:0]	7:0	Sub window curve table 9.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0xA8**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_10[7:0]	7:0	Sub window curve table 10.	
3Dh	**REG102F7B**	**7:0**	**Default: 0x00**	**Access: R/W**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F7Bh)	SUB_CURVE_FIT_TABLE_11[7:0]	7:0	Sub window curve table 11.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: 0xC8**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_12[7:0]	7:0	Sub window curve table 12.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default: 0xD8**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_13[7:0]	7:0	Sub window curve table 13.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: 0xE8**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_14[7:0]	7:0	Sub window curve table 14.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default: 0xF8**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_15[7:0]	7:0	Sub window curve table 15.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_0[7:0]	7:0	Histogram report section 32_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_1[7:0]	7:0	Histogram report section 32_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_4[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_5[15:8]	7:0	See description of '102F8Ah'.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_6[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_7[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_8[15:8]	7:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_9[15:8]	7:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_10[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_11[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_12[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_13[15:8]	7:0	See description of '102F9Ah'.	
4Eh	**REG102F9C**	**7:0**	**Default: -**	**Access: RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F9Ch)	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_14[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_15[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_16[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_17[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_18[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_19[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_20[15:8]	7:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_21[15:8]	7:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_22[15:8]	7:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_23[15:8]	7:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_24[15:8]	7:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_25[15:8]	7:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_26[15:8]	7:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_27[7:0]	7:0	Histogram report section 32_27.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_27[15:8]	7:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_28[7:0]	7:0	Histogram report section 32_28.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_28[15:8]	7:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_29[7:0]	7:0	Histogram report section 32_29.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_29[15:8]	7:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_30[7:0]	7:0	Histogram report section 32_30.	
5Eh	**REG102FBD**	**7:0**	**Default: -**	**Access: RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FBDh)	TOTAL_32_30[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_31[7:0]	7:0	Histogram report section 32_31.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_32_31[15:8]	7:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_PIXEL_SAT_WEIGHT[7:0]	7:0	Histogram saturation report sum of total saturation.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: -**	**Access: RO**
	TOTAL_PIXEL_SAT_WEIGHT[15:8]	7:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: -**	**Access: RO**
	MAIN_MAX_PIXEL_SAT[7:0]	7:0	Main window minimum pixel saturation.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: -**	**Access: RO**
	MAIN_MIN_PIXEL_SAT[7:0]	7:0	Main window maximum pixel saturation.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: -**	**Access: RO**
	SUB_MAX_PIXEL_SAT[7:0]	7:0	Sub window minimum pixel saturation.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: -**	**Access: RO**
	SUB_MIN_PIXEL_SAT[7:0]	7:0	Sub window maximum pixel saturation.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default: 0x08**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_N0[7:0]	7:0	Main window curve table left point, MSB is sign bit.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_N0[8]	0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default: 0x08**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_16[7:0]	7:0	Main window curve table 16.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_16[8]	0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_LSB_2[1:0]	7:6	Main window curve table 2 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_1[1:0]	5:4	Main window curve table 1 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_0[1:0]	3:2	Main window curve table 0 LSB.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_CURVE_FIT_TABLE_LSB_N0[1:0]	1:0	Main window curve table n0 LSB.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_LSB_6[1:0]	7:6	Main window curve table 6 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_5[1:0]	5:4	Main window curve table 5 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_4[1:0]	3:2	Main window curve table 4 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_3[1:0]	1:0	Main window curve table 3 LSB.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_LSB_10[1:0]	7:6	Main window curve table 10 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_9[1:0]	5:4	Main window curve table 9 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_8[1:0]	3:2	Main window curve table 8 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_7[1:0]	1:0	Main window curve table 7 LSB.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_LSB_14[1:0]	7:6	Main window curve table 14 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_13[1:0]	5:4	Main window curve table 13 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_12[1:0]	3:2	Main window curve table 12 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_11[1:0]	1:0	Main window curve table 11 LSB.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_CURVE_FIT_TABLE_LSB_16[1:0]	3:2	Main window curve table 16 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_15[1:0]	1:0	Main window curve table 15 LSB.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_LSB_2[1:0]	7:6	Sub window curve table 2 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_1[1:0]	5:4	Sub window curve table 1 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_0[1:0]	3:2	Sub window curve table 0 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_N0[1:0]	1:0	Sub window curve table n0 LSB.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_LSB_6[1:0]	7:6	Sub window curve table 6 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_5[1:0]	5:4	Sub window curve table 5 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_4[1:0]	3:2	Sub window curve table 4 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_3[1:0]	1:0	Sub window curve table 3 LSB.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_LSB_10[1:0]	7:6	Sub window curve table 10 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_9[1:0]	5:4	Sub window curve table 9 LSB.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_CURVE_FIT_TABLE_LSB_8[1:0]	3:2	Sub window curve table 8 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_7[1:0]	1:0	Sub window curve table 7 LSB.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_LSB_14[1:0]	7:6	Sub window curve table 14 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_13[1:0]	5:4	Sub window curve table 13 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_12[1:0]	3:2	Sub window curve table 12 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_11[1:0]	1:0	Sub window curve table 11 LSB.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_CURVE_FIT_TABLE_LSB_16[1:0]	3:2	Sub window curve table 16 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_15[1:0]	1:0	Sub window curve table 15 LSB.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default: 0x08**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_N0[7:0]	7:0	Sub window curve table left point, MSB is sign bit.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:1	Reserved.	
	SUB_CURVE_FIT_TABLE_N0[8]	0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default: 0x08**	**Access: R/W**
	SUB_CURVE_FIT_TABLE_16[7:0]	7:0	Sub window curve table 16.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:1	Reserved.	
	SUB_CURVE_FIT_TABLE_16[8]	0	See description of '102FFEh'.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)

DLC2 Register (Bank = 102F, Sub-bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	VIP_MAIN_CLAMP_EN	0	VIP main window clamp enable.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	VIP_SUB_CLAMP_EN	0	VIP sub window clamp enable.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	MAIN_Y_MAX_CLAMP[7:0]	7:0	Main window y maximum clamp.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_Y_MAX_CLAMP[9:8]	1:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_MIN_CLAMP[7:0]	7:0	Main window y minimum clamp.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_Y_MIN_CLAMP[9:8]	1:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0xFF**	**Access: R/W**
	MAIN_CB_MAX_CLAMP[7:0]	7:0	Main window cb maximum clamp.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_CB_MAX_CLAMP[9:8]	1:0	See description of '102FE8h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CB_MIN_CLAMP[7:0]	7:0	Main window cb minimum clamp.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_CB_MIN_CLAMP[9:8]	1:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	MAIN_CR_MAX_CLAMP[7:0]	7:0	Main window cr maximum clamp.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_CR_MAX_CLAMP[9:8]	1:0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CR_MIN_CLAMP[7:0]	7:0	Main window cr minimum clamp.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_CR_MIN_CLAMP[9:8]	1:0	See description of '102FEEh'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	SUB_Y_MAX_CLAMP[7:0]	7:0	Sub window y maximum clamp.	
7Ah	**REG102FF5**	**7:0**	**Default: 0x03**	**Access: R/W**

DLC2 Register (Bank = 102F, Sub-bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FF5h)	-	7:2	Reserved.	
	SUB_Y_MAX_CLAMP[9:8]	1:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_MIN_CLAMP[7:0]	7:0	Sub window y minimum clamp.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_Y_MIN_CLAMP[9:8]	1:0	See description of '102FF6h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default: 0xFF**	**Access: R/W**
	SUB_CB_MAX_CLAMP[7:0]	7:0	Sub window cb maximum clamp.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_CB_MAX_CLAMP[9:8]	1:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CB_MIN_CLAMP[7:0]	7:0	Sub window cb minimum clamp.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_CB_MIN_CLAMP[9:8]	1:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	SUB_CR_MAX_CLAMP[7:0]	7:0	Sub window cr maximum clamp.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_CR_MAX_CLAMP[9:8]	1:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CR_MIN_CLAMP[7:0]	7:0	Sub window cr minimum clamp.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_CR_MIN_CLAMP[9:8]	1:0	See description of '102FFEh'.	

LCE Register (Bank = 102F, Sub-bank = 1E)

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F20h)	-	7:5	Reserved.	
	MAIN_LCE_Y_AVE_SEL	4	Main window LCE y ave selection. 1: 5x7. 0: 5x11.	
	MAIN_LCE_COLOR_ALPHA_EN	3	Main window LCE color adaptive alpha blending enable.	
	MAIN_LCE_DERING_ALPHA_EN	2	Main window LCE de-ring alpha blending enable.	
	MAIN_LCE_SODC_ALPHA_EN	1	Main window LCE slop of DLC curve alpha blending enable.	
	MAIN_LCE_EN	0	Main window LCE enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_STD_SLOP2[3:0]	7:4	Main window LCE std slop2: 0.00xxxx format.	
	MAIN_LCE_STD_SLOP1[3:0]	3:0	Main window LCE std slop1: 0.00xxxx format.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_STD_TH1[7:0]	7:0	Main window LCE std threshold 1: 8 bit precision.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_STD_TH2[7:0]	7:0	Main window LCE std threshold 2: 8 bit precision.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_LCE_GAIN_MIN[6:0]	6:0	Main window LCE std gain minimum: x.xxxxxx format.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_GAIN_MAX[7:0]	7:0	Main window LCE std gain maximum: xx.xxxxxx format.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_LCE_SODC_LOW_ALPHA[5:0]	5:0	Main window LCE slop of DLC curve low alpha.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_SODC_LOW_TH[7:0]	7:0	Main window LCE slop of DLC curve low threshold: 8 bit precision.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_LCE_SODC_SLOP[3:0]	3:0	Main window LCE slop of DLC curve slop: 0.000xxxx format.	

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_LCE_DIFF_GAIN[5:0]	5:0	Main window LCE diff gain: xx.xxxx format.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_STRENGTH_LCE[3:0]	7:4	Main window color adaptive for LCE of G.	
	MAIN_R_STRENGTH_LCE[3:0]	3:0	Main window color adaptive for LCE of R.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_STRENGTH_LCE[3:0]	7:4	Main window color adaptive for LCE of C.	
	MAIN_B_STRENGTH_LCE[3:0]	3:0	Main window color adaptive for LCE of B.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_STRENGTH_LCE[3:0]	7:4	Main window color adaptive for LCE of Y.	
	MAIN_M_STRENGTH_LCE[3:0]	3:0	Main window color adaptive for LCE of M.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_NC_STRENGTH_LCE[3:0]	7:4	Main window color adaptive for LCE of other Color.	
	MAIN_F_STRENGTH_LCE[3:0]	3:0	Main window color adaptive for LCE of F.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_CURVE_A[7:0]	7:0	Main window LCE curve threshold a; a<b<c<d; 8 bit precision.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_CURVE_B[7:0]	7:0	Main window LCE curve threshold b; a<b<c<d; 8 bit precision.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_CURVE_C[7:0]	7:0	Main window LCE curve threshold c; a<b<c<d; 8 bit precision.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_CURVE_D[7:0]	7:0	Main window LCE curve threshold d; a<b<c<d; 8 bit precision.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_LCE_GAIN_COMPLEX[7:0]	7:0	Main window LCE std gain complex: xx.xxxxxx format.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_LCE_Y_AVE_SEL	4	Main window LCE y ave selection. 1: 5x7.	

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: 5x11.	
	SUB_LCE_COLOR_ALPHA_EN	3	Sub window LCE color adaptive alpha blending enable.	
	SUB_LCE_DERING_ALPHA_EN	2	Sub window LCE dering alpha blending enable.	
	SUB_LCE_SODC_ALPHA_EN	1	Sub window LCE slop of DLC curve alpha blending enable.	
	SUB_LCE_EN	0	Sub window LCE enable.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_STD_SLOP2[3:0]	7:4	Sub window LCE std slop2: 0.00xxxx format.	
	SUB_LCE_STD_SLOP1[3:0]	3:0	Sub window LCE std slop1: 0.00xxxx format.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_STD_TH1[7:0]	7:0	Sub window LCE std threshold 1: 8 bit precision.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_STD_TH2[7:0]	7:0	Sub window LCE std threshold 2: 8 bit precision.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_LCE_GAIN_MIN[6:0]	6:0	Sub window LCE std gain minimum: x.xxxxxx format.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_GAIN_MAX[7:0]	7:0	Sub window LCE std gain maximum: xx.xxxxxx format.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_LCE_SODC_LOW_ALPHA[5:0]	5:0	Sub window LCE slop of DLC curve low alpha.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_SODC_LOW_TH[7:0]	7:0	Sub window LCE slop of DLC curve low threshold: 8 bit precision.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_LCE_SODC_SLOP[3:0]	3:0	Sub window LCE slop of DLC curve slop: 0.000xxxx format.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_LCE_DIFF_GAIN[5:0]	5:0	Sub window LCE diff gain xx.xxxx format.	

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_STRENGTH_LCE[3:0]	7:4	Sub window color adaptive for LCE of G.	
	SUB_R_STRENGTH_LCE[3:0]	3:0	Sub window color adaptive for LCE of R.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_C_STRENGTH_LCE[3:0]	7:4	Sub window color adaptive for LCE of C.	
	SUB_B_STRENGTH_LCE[3:0]	3:0	Sub window color adaptive for LCE of B.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_STRENGTH_LCE[3:0]	7:4	Sub window color adaptive for LCE of Y.	
	SUB_M_STRENGTH_LCE[3:0]	3:0	Sub window color adaptive for LCE of M.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_NC_STRENGTH_LCE[3:0]	7:4	Sub window color adaptive for LCE of other Color.	
	SUB_F_STRENGTH_LCE[3:0]	3:0	Sub window color adaptive for LCE of F.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_CURVE_A[7:0]	7:0	Sub window LCE curve threshold a; a<b<c<d; 8 bit precision.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_CURVE_B[7:0]	7:0	Sub window LCE curve threshold b; a<b<c<d; 8 bit precision.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_CURVE_C[7:0]	7:0	Sub window LCE curve threshold c; a<b<c<d; 8 bit precision.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_CURVE_D[7:0]	7:0	Sub window LCE curve threshold d; a<b<c<d; 8 bit precision.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_LCE_GAIN_COMPLEX[7:0]	7:0	Sub window LCE std gain complex: xx.xxxxxx format.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_08_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x08 8 MSBs.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_08_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x08 2 LSBs.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_18_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x18 8 MSBs.	

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_18_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x18 2 LSBs.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_28_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x28 8 MSBs.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_28_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x28 2 LSBs.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_38_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x38 8 MSBs.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_38_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x38 2 LSBs.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_48_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x48 8 MSBs.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_48_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x48 2 LSBs.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_58_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x58 8 MSBs.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_58_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x58 2 LSBs.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_68_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x68 8 MSBs.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_68_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x68 2 LSBs.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_78_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x78 8 MSBs.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_78_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x78 2 LSBs.	

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (102F70h)	**REG102F70**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_88_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x88 8 MSBs.	
38h (102F71h)	**REG102F71**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_88_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x88 2 LSBs.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_98_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0x98 8 MSBs.	
39h (102F73h)	**REG102F73**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_98_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0x98 2 LSBs.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_A8_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0xa8 8 MSBs.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_A8_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0xa8 2 LSBs.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_B8_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0xb8 8 MSBs.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_B8_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0xb8 2 LSBs.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_C8_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0xc8 8 MSBs.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_C8_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0xc8 2 LSBs.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_D8_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0xd8 8 MSBs.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_D8_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0xd8 2 LSBs.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_E8_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0xe8 8 MSBs.	
3Eh	**REG102F7D**	**7:0**	**Default: 0x00**	**Access: R/W**

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F7Dh)	-	7:2	Reserved.	
	LCE_CURVE_LUT1_E8_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0xe8 2 LSBs.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT1_F8_8MSB[7:0]	7:0	LCE curve LUT1 Luma equal to 0xf8 8 MSBs.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT1_F8_2LSB[1:0]	1:0	LCE curve LUT1 Luma equal to 0xf8 2 LSBs.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_08_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x08 8 MSBs.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_08_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x08 2 LSBs.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_18_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x18 8 MSBs.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_18_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x18 2 LSBs.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_28_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x28 8 MSBs.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_28_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x28 2 LSBs.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_38_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x38 8 MSBs.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_38_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x38 2 LSBs.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_48_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x48 8 MSBs.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_48_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x48 2 LSBs.	
45h	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: R/W**

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F8Ah)	LCE_CURVE_LUT2_58_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x58 8 MSBs.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_58_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x58 2 LSBs.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_68_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x68 8 MSBs.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_68_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x68 2 LSBs.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_78_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x78 8 MSBs.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_78_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x78 2 LSBs.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_88_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x88 8 MSBs.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_88_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x88 2 LSBs.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_98_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0x98 8 MSBs.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_98_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0x98 2 LSBs.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_A8_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0xa8 8 MSBs.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_A8_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0xa8 2 LSBs.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_B8_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0xb8 8 MSBs.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LCE_CURVE_LUT2_B8_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0xb8 2 LSBs.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_C8_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0xc8 8 MSBs.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_C8_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0xc8 2 LSBs.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_D8_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0xd8 8 MSBs.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_D8_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0xd8 2 LSBs.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_E8_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0xe8 8 MSBs.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_E8_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0xe8 2 LSBs.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT2_F8_8MSB[7:0]	7:0	LCE curve LUT2 Luma equal to 0xf8 8 MSBs.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT2_F8_2LSB[1:0]	1:0	LCE curve LUT2 Luma equal to 0xf8 2 LSBs.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_08_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x08 8 MSBs.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_08_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x08 2 LSBs.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_18_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x18 8 MSBs.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_18_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x18 2 LSBs.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_28_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x28 8 MSBs.	

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_28_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x28 2 LSBs.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_38_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x38 8 MSBs.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_38_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x38 2 LSBs.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_48_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x48 8 MSBs.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_48_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x48 2 LSBs.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_58_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x58 8 MSBs.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_58_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x58 2 LSBs.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_68_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x68 8 MSBs.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_68_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x68 2 LSBs.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_78_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x78 8 MSBs.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_78_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x78 2 LSBs.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_88_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x88 8 MSBs.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_88_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x88 2 LSBs.	

LCE Register (Bank = 102F, Sub-bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_98_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0x98 8 MSBs.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_98_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0x98 2 LSBs.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_A8_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0xa8 8 MSBs.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_A8_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0xa8 2 LSBs.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_B8_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0xb8 8 MSBs.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_B8_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0xb8 2 LSBs.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_C8_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0xc8 8 MSBs.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_C8_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0xc8 2 LSBs.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_D8_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0xd8 8 MSBs.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_D8_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0xd8 2 LSBs.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_E8_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0xe8 8 MSBs.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LCE_CURVE_LUT3_E8_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0xe8 2 LSBs.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0x00**	**Access: R/W**
	LCE_CURVE_LUT3_F8_8MSB[7:0]	7:0	LCE curve LUT3 Luma equal to 0xf8 8 MSBs.	
5Fh	**REG102FBF**	**7:0**	**Default: 0x00**	**Access: R/W**

LCE Register (Bank = 102F, Sub-bank = 1E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(102FBFh)	-	7:2	Reserved.
	LCE_CURVE_LUT3_F8_2LSB[1:0]	1:0	LCE curve LUT3 Luma equal to 0xf8 2 LSBs.

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_IDX_DEPTH[7:0]	7:0	The number of menuload data. 0: Disable menuload.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_IDX_DEPTH[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_EN	7	Menuload enable.	
	-	6:4	Reserved.	
	MLOAD_REQ_LEN[3:0]	3:0	Length of menuload DMA's request. 0: Disable menuload.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_BASE_ADR[7:0]	7:0	Base address of allocated memory for menuload.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_BASE_ADR[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_BASE_ADR[23:16]	7:0	See description of '102F06h'.	
08h ~ 0Bh (102F10h ~ 102F17h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_REQ_LEN[3:0]	7:4	Length of dynamic scaling DMA's request. 0: Disable dynamic scaling.	
	DS_REQ_TH[3:0]	3:0	Threshold for one dynamic scaling DMA request.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_IPM2MI_SEL	7	Main IP dynamic scaling MIU selection.	
	DS_IPS2MI_SEL	6	Sub IP dynamic scaling MIU selection.	

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DS_OP2MI_SEL	5	OP dynamic scaling MIU selection.	
	DS_RIU_WE	4	Enable write register through RIU.	
	IPM_DS_EN	3	Enable main IP2 dynamic scaling.	
	IPS_DS_EN	2	Enable sub IP2 dynamic scaling.	
	OP_DS_EN	1	Enable OP dynamic scaling.	
	DS_REQ_PRI	0	User specified priority of MIU.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_BASE_ADR[7:0]	7:0	Base address of allocated memory for dynamic scaling.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_BASE_ADR[15:8]	7:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_BASE_ADR[23:16]	7:0	See description of '102F22h'.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_IDX_DEPTH[7:0]	7:0	The number of dynamic scaling data per index. 0: Disable dynamic scaling.	
13h (102F26h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
14h ~ 1Fh (102F28h ~ 102F39h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_V_BASEADDR[7:0]	7:0	DRAM base address for keystone vertical parameter.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_V_BASEADDR[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_V_BASEADDR[23:16]	7:0	See description of '102F40h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_H_BASEADDR[7:0]	7:0	DRAM base address for keystone horizontal parameter.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_H_BASEADDR[15:8]	7:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_H_BASEADDR[23:16]	7:0	See description of '102F44h'.	
24h	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F48h)	-	7:2	Reserved.	
	KST_V_NONLINEAR_EN	1	Keystone vertical nonlinear enable.	
	KST_EN	0	Keystone enable.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x01**	**Access: R/W**
	KST_TRIG_DLY[7:0]	7:0	Generate keystone trigger pulse from delayed line of Vsync.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	SEL_KST[1:0]	7:6	Select the source to trigger menuload. 0: Falling edge of VFDE. 1: Rising edge of Vsync. 2: Falling edge of Vsync. 3: Delay line set by REG_KST_TRIG_DLY.	
	-	5:4	Reserved.	
	KST_TRIG_DLY[11:8]	3:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_VSF_INI[7:0]	7:0	Initial vertical scaling ratio for keystone vertical nonlinear function.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_VSF_INI[15:8]	7:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_VSF_INI[23:16]	7:0	See description of '102F4Ch'.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	-	1	Reserved.	
	MAIN_EN	0	Enable main window shown on the screen.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)

Index (Absolute)	Mnemonic	Bit	Description
	-	5:3	Reserved.
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.
	-	1:0	Reserved.
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00** **Access: R/W**
	SCLB_BASE_F2[7:0]	7:0	The starting address of F2 stored at line buffer.
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00** **Access: R/W**
	-	7:4	Reserved.
	SCLB_BASE_F2[11:8]	3:0	See description of '102F24h'.
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0xFF** **Access: R/W**
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x0F** **Access: R/W**
	-	7:4	Reserved.
	VLEN_F2[11:8]	3:0	See description of '102F2Ah'.
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00** **Access: R/W**
	-	7:4	Reserved.
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional border.
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0xB8** **Access: R/W**
	-	7	Reserved.
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter. 0: Vsync of SC_TOP. 1: Delay one line of VFDE.
	SEL_DISP[1:0]	5:4	Select the trigger point to start OP1 engine. 0: DOWN_EQ7. 1: DOWN_EQ8. 2: DOWN_EQ9. 3: Delay lines set by DISP_TRIG_DLY.
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. 0: Falling edge of Vsync. 1: Nearly rising edge of Vsync. 2: Delay line set by ATP_TRIG_DLY. 3: Manual triggered by setting ATP_EN.
	SEL_SYNC[1:0]	1:0	Select the trigger point for sync to initial engine. 0: Falling edge of Vsync. 1: Rising edge of Vsync.

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2: Reserved. 3: Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x03**	**Access: R/W**
	ATP_TRIG_DLY[7:0]	7:0	Generate TRAIN_TRIG_P from delayed line of Vsync.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	ATP_TRIG_DLY[11:8]	3:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x05**	**Access: R/W**
	DISP_TRIG_DLY[7:0]	7:0	Generate DISP_TRIG_P from delayed line of Vsync.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0xC2**	**Access: R/W**
	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. 0: 2 pixel. 1: 4 pixel. 2: 8 pixel. 3: 16 pixel.	
	DISP_START_MODE	5	Select the display line buffer start mode. 0: Start at advance 1 display line. 1: Start at falling edge of VSYNC_INIT.	
	DISP_LB_MODE	4	Select the trigger mode. 0: Line base. 1: Fill line buffer.	
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. 0: Before 8 pixels. 1: Before 16 pixels. 2: Before 32 pixels. 3: Before 64 pixels.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DISP_RLN_MODE[1:0]	1:0	Select the UNDER_RUN value of display level. 0: Update by Hsync (not optimum performance). 1: Update when session is done (subject to error). 2: Update when line is done (DISP_TRIG_MODE = 0). 3: Reserved.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DISP_UNDER_MODE	3	Select the UNDER_RUN value of display level. 0: 16'h0000. 1: 16'hffff.	
	DISP_PAT_EN	2	Enable internal pattern of OP1_DISP.	
	DISP_LB_WEZ	1	Disable WEN of display line buffer.	
	DISP_TRIG_MODE	0	Select the trigger mode. 0: Trigged by SELF_COUNTER. 1: Trigged by OP2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0xFF**	**Access: R/W**
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x07**	**Access: R/W**
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x01**	**Access: R/W**
	DS_TRIG_DLY[7:0]	7:0	Generate DS_TRIG_P from delayed line of Vsync.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DS_TRIG_DLY[11:8]	3:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x01**	**Access: R/W**
	MLOAD_TRIG_DLY[7:0]	7:0	Generate MLOAD_TRIG_P from delayed line of Vsync.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MLOAD_TRIG_DLY[11:8]	3:0	See description of '102F44h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: -**	**Access: RO**
	-	7:1	Reserved.	
	DISPLAY_UNDERRUN	0	Indicate whether the display line buffer is underrun in previous frame.	
41h	**REG102F82**	**7:0**	**Default: -**	**Access: RO**

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F82h)	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line count of first display position.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: -**	**Access: RO**
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line count of minimum display level occurred.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	MIN_DISP_LINE[11:8]	3:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: -**	**Access: RO**
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: -**	**Access: RO**
	MIN_DISP_CNT[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: -**	**Access: RO**
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: -**	**Access: RO**
	MAX_DISP_CNT[15:8]	7:0	See description of '102F88h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: -**	**Access: RO**
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '102FA2h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: -**	**Access: RO**
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_BF_LEN[11:8]	3:0	See description of '102FAAh'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: -**	**Access: RO**
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '102FC2h'.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: -**	**Access: RO**
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default: -**	**Access: RO**
	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '102FC8h'.	
65h ~ 67h (102FCAh ~ 102FCFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

ELA Register (Bank = 102F, Sub-bank = 21)

ELA Register (Bank = 102F, Sub-bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 02h (102F02h ~ 102F04h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. 1: Enable. 0: Disable.	
7Fh ~ 7Fh (102FFEh ~ 102FFFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

TDDI Register (Bank = 102F, Sub-bank = 22)

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x04**	**Access: R/W**
	RATIO_DIV_YCSEP_F2	7	Main window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F2[2:0]	2:0	Main window ratio divide mode when Y/C separate.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F2[2:0]	5:3	Main window ratio divide mode.	
	RATIO_MD_F2[2:0]	2:0	Main window ratio filter mode.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x80**	**Access: R/W**
	RATIO_C_INDEP_F2	7	Main window C ratio independent mode. 0: Disable C ratio filter. 1: Enable C ratio filter.	
	RSV_02_2_F2[2:0]	6:4	Reserved.	
	RATIO_C_MIN_F2[3:0]	3:0	Main window C minimum ratio in independent mode.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:2	Reserved.	
	RATIO_C_YMAX_SEL_F2	1	Main window C ratio takes Y ratio mode. 0: Select Y ratio before SST. 1: Select Y ratio after SST.	
	RATIO_C_YMAX_DIS_F2	0	Main window C ratio takes Y ratio mode disable. 0: Enable. 1: Disable.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	FILM_EODIW_EN_F2	7	Main window EODi weight compensation enable in film mode.	
	-	6:0	Reserved.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	PRE_MOT_FILTER_EN_F2	7	Main Window LPF enable of DNR motion calculation.	
	-	6	Reserved.	
	PRE_MOT_OFFSET_F2[5:0]	5:0	Main Window pre-memory motion offset for motion calculation.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:4	Reserved.	

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PRE_MOT_GAIN_F2[3:0]	3:0	Main Window pre-memory motion gain for motion calculation.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F2[5:0]	5:0	Main Window post-memory motion offset for motion calculation.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x88**	**Access: R/W**
	POST_MOT_CGAIN_F2[3:0]	7:4	Main Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F2[3:0]	3:0	Main Window post-memory motion gain for C motion calculation.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x86**	**Access: R/W**
	POST_MOT_YMAX_EN_F2	7	Main Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F2[2:0]	2:0	Main Window history weighting.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x04**	**Access: R/W**
	HIS_FILTER_MODE_F2	7	Main Window history filter mode.	
	-	6:4	Reserved.	
	HIS_RATIO_OFFSET_F2[3:0]	3:0	Main Window history ratio offset.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x07**	**Access: R/W**
	RSV_STAT_0_F2[1:0]	7:6	Reserved.	
	STAT_INC_MODE_F2	5	Main window ratio statistics: ratio incremental mode.	
	STAT_SEL_C_F2	4	Main window ratio statistics: ratio selection.	
	STAT_CORE_F2[3:0]	3:0	Main window ratio statistics: coring threshold.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: -**	**Access: RO**
	MOTION_STATUS_F2[7:0]	7:0	Main window ratio statistics: motion status.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: -**	**Access: RO**
	MOTION_STATUS_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: -**	**Access: RO**
	MOTION_STATUS_F2[23:16]	7:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x4A**	**Access: R/W**
	ADAPT_MED_EN_F2	7	Main window adaptive DFK enable.	
	WEGT_MED_EN_F2	6	Main window weighted DFK enable.	

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RSV_MED_0_F2	5	Reserved.	
	MED_MANUAL_EN_F2	4	Main window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F2[3:0]	3:0	Main window DFK manual weighting.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F2[4:0]	4:0	Main window weighted DFK low-frequency begin.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F2[3:0]	3:0	Main window weighted DFK low-frequency slope adjustment.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:5	Reserved.	
	MED_HF_BEGIN_F2[4:0]	4:0	Main window weighted DFK high-frequency begin.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F2[3:0]	3:0	Main window weighted DFK high-frequency slope adjustment.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x30**	**Access: R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F2[5:0]	5:0	Main window adaptive DFK motion threshold.	
14h ~ 15h (102F28h ~ 102F2Ah)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x13**	**Access: R/W**
	SST_EN_F2	7	Main window SST enable.	
	-	6	Reserved.	
	RSV_SST_0_F2	5	Reserved.	
	SST_MOTION_LPF_EN_F2	4	Main window SST low-pass on motion enable.	
	SST_MOTION_TH_F2[3:0]	3:0	Main window SST motion threshold.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x27**	**Access: R/W**
	RSV_SST_1_F2[1:0]	7:6	Reserved.	
	SST_ERODE_MODE_F2[1:0]	5:4	Main window SST motion area erosion mode.	
	RSV_SST_2_F2	3	Reserved.	

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SST_DILATE_MODE_F2[2:0]	2:0	Main window SST motion area dilation mode.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0xDF**	**Access: R/W**
	SST_POSTLPF_EN_F2	7	Main window SST post-LPF enable.	
	SST_POSTLPF_MAX_F2	6	Main window SST post-LPF maximum function enable.	
	SST_DYNAMIC_CORE_TH_F2[5:0]	5:0	Main window SST dynamic motion coring threshold.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x85**	**Access: R/W**
	SST_DYNAMIC_SGAIN_F2[3:0]	7:4	Main window SST dynamic motion spatial difference gain.	
	SST_DYNAMIC_TGAIN_F2[3:0]	3:0	Main window SST dynamic motion temporal difference gain.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	RSV_SST_3_F2[1:0]	7:6	Reserved.	
	SST_STATIC_CORE_TH_F2[5:0]	5:0	Main window SST static motion coring threshold.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x22**	**Access: R/W**
	SST_STATIC_SGAIN_F2[3:0]	7:4	Main window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F2[3:0]	3:0	Main window SST static motion temporal difference gain.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	RSV_SST_4_F2[7:0]	7:0	Reserved.	
1Bh ~ 7Fh (102F37h ~ 102FFFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

HVSP Register (Bank = 102F, Sub-bank = 23)

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '102F02h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '102F06h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '102F0Ah'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '102F0Eh'.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	H_SHIFT_MODE_EN_F2	1	Main window horizontal scaling shift mode enable.	
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '102F12h'.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x80**	**Access: R/W**
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: R/W**
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: R/W**
	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Bilinear.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0xC0**	**Access: R/W**
	FORMAT_422_F2	7	Main window data format is 422.	
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F2	5	Main CR_LOAD initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.	
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.	
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.	
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSP_CORING_TH_Y_F2[7:0]	7:0	Main window horizontal Y coring threshold.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.	
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F2	1	Main window field polarity switch.	
	2_INIFAC_MD_F2	0	Main window two initial factors mode.	

HVSP Register (Bank = 102F, Sub-bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSP_3TAP_EN_F2	7	Main window vertical 3-tap scaling enable.	
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width 2 LSB.	
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width 1 LSB.	
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width 0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width 2 LSB.	
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width 1 LSB.	
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width 0 LSB.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width 0.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width 1.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width 2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width 0.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width 1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width 2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_FACTOR_HO[7:0]	7:0	Dynamic horizontal scaling factor.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_FACTOR_HO[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x10**	**Access: R/W**
	DY_FACTOR_HO[23:16]	7:0	See description of '102F38h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_FACTOR_VE[7:0]	7:0	Dynamic vertical scaling factor.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_FACTOR_VE[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x10**	**Access: R/W**
	DY_FACTOR_VE[23:16]	7:0	See description of '102F3Ch'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	CRAM_RW_EN	1	C SRAM read/write enable.	
	YRAM_RW_EN	0	Y SRAM read/write enable.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	RAM_W_PULSE	0	SRAM write data pulse.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_ADDR[7:0]	7:0	For each C SRAM download: Bit5~0: address (0~63). Bit7,6: 00: C SRAM 0. 01: C SRAM 1. 10: C SRAM 2. 11: C SRAM 3. For each Y SRAM download: Bit6~0: address (0~127). bit7: 0: Y SRAM 0. 1: Y SRAM 1.	
43h	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F86h)	RAM_WDATA[7:0]	7:0	SRAM write data.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_WDATA[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_WDATA[23:16]	7:0	See description of '102F86h'.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_WDATA[31:24]	7:0	See description of '102F86h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_WDATA[39:32]	7:0	See description of '102F86h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: -**	**Access: RO**
	RAM_RDATA[7:0]	7:0	SRAM read data.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: -**	**Access: RO**
	RAM_RDATA[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: -**	**Access: RO**
	RAM_RDATA[23:16]	7:0	See description of '102F8Ch'.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: -**	**Access: RO**
	RAM_RDATA[31:24]	7:0	See description of '102F8Ch'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: -**	**Access: RO**
	RAM_RDATA[39:32]	7:0	See description of '102F8Ch'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x41**	**Access: R/W**
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.	
	FACTOR_MANUAL	6	Vertical factor manual mode.	
	VDOWN_SEL	5	Vertical scaling down selection. 0: Bottom. 1: Top.	
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.	
	-	3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.	
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: DE end.	
	-	6:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x40**	**Access: R/W**
	CTI_AUTO_NO_MED_F2	7	Main window CTI auto no median.	
	CTI_STEP_F2[2:0]	6:4	Main window CTI step.	
	-	3	Reserved.	
	CTI_LPF_COEF_F2[2:0]	2:0	Main window CTI LPF coefficients.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x3F**	**Access: R/W**
	-	7:6	Reserved.	
	CTI_BAND_COEF_F2[5:0]	5:0	Main window CTI BPF coefficients.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x88**	**Access: R/W**
	CTI_MEDIAN_EN_F2	7	Main window CTI Median enable.	
	-	6:4	Reserved.	
	CTI_CORING_THRD_F2[3:0]	3:0	Main window CTI coring threshold.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	CTI_EN_F2	7	Main window CTI enable.	
	-	6:0	Reserved.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	LEVEL_SLOPE_F2[2:0]	2:0	Main window CTI gray patch level slope.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: R/W**
	LEVEL_OFFSET_F2[7:0]	7:0	Main window CTI gray patch level offset.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:2	Reserved.	
	GAIN_ADJ_EN_F2	1	Main window CTI gain adjust enable.	
	-	0	Reserved.	

FRC Register (Bank = 102F, Sub-bank = 24)

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: 0x1B**	**Access: R/W**
	-	7:5	Reserved.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TAILCUT	4	TAILCUT enable.	
	NOISE_DITH_DISABLE	3	PAFRC mixed with noise dither disable. 0: Enable. 1: Disable.	
	DITH_BITS	2	Dithering bits. 0: 2-bit. 1: 4-bit.	
	TCON_OFF_EN	1	TCON FRC_GAMMA function off signal enable. 0: Ignore TCON gamma/dither turn off signal. 1: Gamma/dither function turned off by TCON FRC_GAMMA_OFF signal.	
	FRC_ON	0	PAFRC enable.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_ROTATE_EN	7	Box A/B/C/D relative rotation enable.	
	TOP_BOX_UNIT_FLAG[1:0]	6:5	Top box A/B/C/D swap flag. 00: Per 2x2 box. 01: Per 4x4 box. 1x: Per 8x8 box.	
	TOP_BOX_FREEZE	4	Top box freeze.	
	TOP_BOX_SHRINK	3	Top box shrink to 2x2 from 4x4.	
	FR_C2_BIT	2	Top box frame rotation step bit location for codexx10. 0: Bit[0]. 1: Bit[1].	
	C2X2_ROT_B_DIR_S	1	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	D2X2_ROT_B_DIR_S	0	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	G_V_SWAP	6	Green channel vertical swap, avoid polarity not consistent.	
	G_H_SWAP	5	Green channel horizontal swap, avoid polarity not consistent.	
	B_D_SWAP	4	Blue channel diagonal swap.	
	BOX_FR_SW	3	FRAME_CNT bit [1:0] swap for box rotation.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BOX4X4_FR_SW	2	FRAME_CNT bit [1:0] swap for box4x4 rotation.	
	BOX8X8_ROT_UNIT	1	0: Rotate step under A, B, C or D. 1: Rotate step between A/B/C/D.	
	BOX_FREEZE	0	Box local rotation freeze.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	C2X2_ROT_G_DIR	7	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	D2X2_ROT_G_DIR	6	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	C2X2_ROT_G_DIR_S	5	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	D2X2_ROT_G_DIR_S	4	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	A2X2_ROT_B_DIR	3	A 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	B2X2_ROT_B_DIR	2	B 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	C2X2_ROT_B_DIR	1	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	D2X2_ROT_B_DIR	0	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: R/W**
	A2X2_ROT_R_DIR	7	A 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	B2X2_ROT_R_DIR	6	B 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	C2X2_ROT_R_DIR	5	C 2x2 block rotation direction.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Clockwise. 1: Counterclockwise.	
	D2X2_ROT_R_DIR	4	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	C2X2_ROT_R_DIR_S	3	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	D2X2_ROT_R_DIR_S	2	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	A2X2_ROT_G_DIR	1	A 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	B2X2_ROT_G_DIR	0	B 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_SEQ2[7:0]	7:0	Top box frame 2nd 4 frame rotation step.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_SEQ1[7:0]	7:0	Top box frame 1st 4 frame rotation step.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_SEQ4[7:0]	7:0	Top box frame 4th 4 frame rotation step.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_SEQ3[7:0]	7:0	Top box frame 3rd 4 frame rotation step.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_C2_SEQ34[7:0]	7:0	Top box frame 3rd/4th 4 frame rotation step for codexx10.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_C2_SEQ12[7:0]	7:0	Top box frame 1st/2nd 4 frame rotation step for codexx10.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_A_ROT_DIR	7	Location A frame counter direction. 0: Clockwise. 1: Counterclockwise.	
	BOX_B_ROT_DIR	6	Location B frame counter direction. 0: Clockwise. 1: Counterclockwise.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BOX_C_ROT_DIR	5	Location C frame counter direction. 0: Clockwise. 1: Counterclockwise.	
	BOX_D_ROT_DIR	4	Location D frame counter direction. 0: Clockwise. 1: Counterclockwise.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX8X8_ROT_00[1:0]	7:6	Box 8x8 entity 00 rotation step by reference.	
	BOX8X8_ROT_01[1:0]	5:4	Box 8x8 entity 01 rotation step by reference.	
	BOX8X8_ROT_11[1:0]	3:2	Box 8x8 entity 11 rotation step by reference.	
	BOX8X8_ROT_10[1:0]	1:0	Box 8x8 entity 10 rotation step by reference.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_LU_00[1:0]	7:6	B 2x2 block left up entity.	
	B_RU_01[1:0]	5:4	B 2x2 block right up entity.	
	B_RD_11[1:0]	3:2	B 2x2 block right down entity.	
	B_LD_10[1:0]	1:0	B 2x2 block left down entity.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x00**	**Access: R/W**
	A_LU_00[1:0]	7:6	A 2x2 block left up entity.	
	A_RU_01[1:0]	5:4	A 2x2 block right up entity.	
	A_RD_11[1:0]	3:2	A 2x2 block right down entity.	
	A_LD_10[1:0]	1:0	A 2x2 block left down entity.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	D_LU_00[1:0]	7:6	D 2x2 block left up entity.	
	D_RU_01[1:0]	5:4	D 2x2 block right up entity.	
	D_RD_11[1:0]	3:2	D 2x2 block right down entity.	
	D_LD_10[1:0]	1:0	D 2x2 block left down entity.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: R/W**
	C_LU_00[1:0]	7:6	C 2x2 block left up entity.	
	C_RU_01[1:0]	5:4	C 2x2 block right up entity.	
	C_RD_11[1:0]	3:2	C 2x2 block right down entity.	
	C_LD_10[1:0]	1:0	C 2x2 block left down entity.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	D_LU_00_S[1:0]	7:6	D 2x2 block left up entity, 2nd.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	D_RU_01_S[1:0]	5:4	D 2x2 block right up entity, 2nd.	
	D_RD_11_S[1:0]	3:2	D 2x2 block right down entity, 2nd.	
	D_LD_10_S[1:0]	1:0	D 2x2 block left down entity, 2nd.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	C_LU_00_S[1:0]	7:6	C 2x2 block left up entity, 2nd.	
	C_RU_01_S[1:0]	5:4	C 2x2 block right up entity, 2nd.	
	C_RD_11_S[1:0]	3:2	C 2x2 block right down entity, 2nd.	
	C_LD_10_S[1:0]	1:0	C 2x2 block left down entity, 2nd.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_B_LU_00[1:0]	7:6	Location B block A LSB 2 bits plus value.	
	BOX_B_RU_01[1:0]	5:4	Location B block B LSB 2 bits plus value.	
	BOX_B_RD_11[1:0]	3:2	Location B block C LSB 2 bits plus value.	
	BOX_B_LD_10[1:0]	1:0	Location B block D LSB 2 bits plus value.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_A_LU_00[1:0]	7:6	Location A block A LSB 2 bits plus value.	
	BOX_A_RU_01[1:0]	5:4	Location A block B LSB 2 bits plus value.	
	BOX_A_RD_11[1:0]	3:2	Location A block C LSB 2 bits plus value.	
	BOX_A_LD_10[1:0]	1:0	Location A block D LSB 2 bits plus value.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_D_LU_00[1:0]	7:6	Location D block A LSB 2 bits plus value.	
	BOX_D_RU_01[1:0]	5:4	Location D block B LSB 2 bits plus value.	
	BOX_D_RD_11[1:0]	3:2	Location D block C LSB 2 bits plus value.	
	BOX_D_LD_10[1:0]	1:0	Location D block D LSB 2 bits plus value.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_C_LU_00[1:0]	7:6	Location C block A LSB 2 bits plus value.	
	BOX_C_RU_01[1:0]	5:4	Location C block B LSB 2 bits plus value.	
	BOX_C_RD_11[1:0]	3:2	Location C block C LSB 2 bits plus value.	
	BOX_C_LD_10[1:0]	1:0	Location C block D LSB 2 bits plus value.	

XVYCC Register (Bank = 102F, Sub-bank = 25)

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	-	3:0	Reserved.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_RGB_COMPRESS_SEE_SAT_EN	7	Main window RGB compress by saturation enable.	
	-	6:3	Reserved.	
	XV_YCC_MAIN_RGB_COMPRESS_DITHER_EN	2	Main window RGB compress dither bit enable.	
	XV_YCC_MAIN_RGB_COMPRESS_EN	1	Main window RGB compress enable.	
	-	0	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	
	POST_SUB_BRI_EN	4	Sub window post brightness enable.	
	-	3:0	Reserved.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_RGB_COMPRESS_SEE_SAT_EN	7	Sub window RGB compress by saturation enable.	
	-	6:3	Reserved.	
	XV_YCC_SUB_RGB_COMPRESS_DITHER_EN	2	Sub window RGB compress dither bit enable.	
	XV_YCC_SUB_RGB_COMPRESS_EN	1	Sub window RGB compress function enable.	
	-	0	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post R channel offset.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post G channel offset.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post B channel offset.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post R channel gain.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post G channel gain.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_B_CON_GAIN[7:0]	7:0	Main window post B channel gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_R_BRI_OFFSET[7:0]	7:0	Sub window post R channel offset.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_G_BRI_OFFSET[7:0]	7:0	Sub window post G channel offset.	

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_B_BRI_OFFSET[7:0]	7:0	Sub window post B channel offset.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post R channel gain.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[11:8]	3:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post G channel gain.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_B_CON_GAIN[7:0]	7:0	Sub window post B channel gain.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[11:8]	3:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAIN1_TH[7:0]	7:0	HBC gain1 threshold.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	GAMMA_OD_PIPE_SEL	0	Gamma and OD pipe select. 0: Gamma before OD. 1: Gamma after OD.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY0[7:0]	7:0	Dummy register.	
2Eh	**REG102F5D**	**7:0**	**Default: 0x00**	**Access: R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
(102F5Dh)	DUMMY0[15:8]	7:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY1[7:0]	7:0	Dummy register.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY1[15:8]	7:0	See description of '102F5Eh'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	PAT_SWITCH	4	Initial pattern switch for pixel or dot pattern.	
	AUTO_FIT_EN	3	Enable auto fit window size.	
	SW_FREEZE_IDX	2	Software freeze pattern enable.	
	AUTO_IDX_EN	1	Auto run pattern enable.	
	PG_EN	0	Pattern generate enable.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PAT_DELTA[3:0]	3:0	Pattern increase delta value.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SW_SET_IDX[4:0]	4:0	Software set pattern idx.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	PAT_PERIOD[7:0]	7:0	Per pattern period, unit is frame.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PAT_R[7:0]	7:0	R fix color.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	PAT_R[9:8]	1:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PAT_G[7:0]	7:0	G fix color.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	PAT_G[9:8]	1:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PAT_B[7:0]	7:0	B fix color.	
34h	**REG102F69**	**7:0**	**Default: 0x03**	**Access: R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F69h)	-	7:2	Reserved.	
	PAT_B[9:8]	1:0	See description of '102F68h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_R_BLACK_START[6:0]	6:0	Main window R channel black start.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_R_BLACK_SLOP[7:0]	7:0	Main window R channel black slope.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_R_WHITE_START[6:0]	6:0	Main window R channel white start.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_R_WHITE_SLOP[7:0]	7:0	Main window R channel white slope.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_R_BLACK_START[6:0]	6:0	Sub window R channel black start.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_R_BLACK_SLOP[7:0]	7:0	Sub window R channel black slope.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_R_WHITE_START[6:0]	6:0	Sub window R channel white start.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_R_WHITE_SLOP[7:0]	7:0	Sub window R channel white slope.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_B_BLACK_START[6:0]	6:0	Main window B channel black start.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_B_BLACK_SLOP[7:0]	7:0	Main window B channel black slope.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_B_WHITE_START[6:0]	6:0	Main window B channel white start.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_B_WHITE_SLOP[7:0]	7:0	Main window B channel white slope.	
46h	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F8Ch)	-	7	Reserved.	
	SUB_B_BLACK_START[6:0]	6:0	Sub window B channel black start.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_B_BLACK_SLOP[7:0]	7:0	Sub window B channel black slope.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_B_WHITE_START[6:0]	6:0	Sub window B channel white start.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_B_WHITE_SLOP[7:0]	7:0	Sub window B channel white slope.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_RGB_COMPRESS_SAT_THRD[7:0]	7:0	Main window RGB compress by saturation threshold: 10 bit precision.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_RGB_COMPRESS_START_SLOP[3:0]	7:4	Main window RGB compress by saturation start point slope.	
	-	3:2	Reserved.	
	MAIN_RGB_COMPRESS_SAT_THRD[9:8]	1:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_RGB_COMPRESS_SAT_THRD[7:0]	7:0	Sub window RGB compress by saturation threshold.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_RGB_COMPRESS_START_SLOP[3:0]	7:4	Sub window RGB compress by saturation start point slop.	
	-	3:2	Reserved.	
	SUB_RGB_COMPRESS_SAT_THRD[9:8]	1:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_RGB_COMPRESS_PRMCLR_MN_LIM_EN	2	Main window RGB compress by RGB primary color minimum value limit enable.	
	MAIN_RGB_COMPRESS_PRMCLR_MX_LIM_EN	1	Main window RGB compress by RGB primary color maximum value limit enable.	
	MAIN_RGB_COMPRESS_SEE_	0	Main window RGB compress by RGB primary color	

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PRMCLR_EN		enable.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: 0x00**	**Access: R/W**
	_	7:4	Reserved.	
	MAIN_RGB_COMPRESS_PRMCLR_START_SLOP[3:0]	3:0	Main window RGB compress by RGB primary color start point slope.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_RGB_COMPRESS_PRMCLR_THRD[7:0]	7:0	Main window RGB compress by RGB primary color threshold: 13 bit precision.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: 0x00**	**Access: R/W**
	_	7:5	Reserved.	
	MAIN_RGB_COMPRESS_PRMCLR_THRD[12:8]	4:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x00**	**Access: R/W**
	_	7:3	Reserved.	
	SUB_RGB_COMPRESS_PRMCLR_MN_LIM_EN	2	Sub window RGB compress by RGB primary color minimum value limit enable.	
	SUB_RGB_COMPRESS_PRMCLR_MX_LIM_EN	1	Sub window RGB compress by RGB primary color maximum value limit enable.	
	SUB_RGB_COMPRESS_SEE_PRMCLR_EN	0	Sub window RGB compress by RGB primary color enable.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: 0x00**	**Access: R/W**
	_	7:4	Reserved.	
	SUB_RGB_COMPRESS_PRMCLR_START_SLOP[3:0]	3:0	Sub window RGB compress by RGB primary color start point slope.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_RGB_COMPRESS_PRMCLR_THRD[7:0]	7:0	Sub window RGB compress by RGB primary color threshold: 13 bit precision.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: 0x00**	**Access: R/W**
	_	7:5	Reserved.	
	SUB_RGB_COMPRESS_PRMCLR_THRD[12:8]	4:0	See description of '102F9Ah'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN0_X0[7:0]	7:0	OSD window0 x0 position.	
50h	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FA1h)	-	7:4	Reserved.	
	OSD_WIN0_X0[11:8]	3:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN0_X1[7:0]	7:0	OSD window0 x1 position.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN0_X1[11:8]	3:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN0_Y0[7:0]	7:0	OSD window0 y0 position.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN0_Y0[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN0_Y1[7:0]	7:0	OSD window0 y1 position.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN0_Y1[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN1_X0[7:0]	7:0	OSD window1 x0 position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN1_X0[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN1_X1[7:0]	7:0	OSD window1 x1 position.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN1_X1[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN1_Y0[7:0]	7:0	OSD window1 y0 position.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN1_Y0[11:8]	3:0	See description of '102FACh'.	
57h	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
(102FAEh)	OSD_WIN1_Y1[7:0]	7:0	OSD window1 y1 position.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN1_Y1[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN2_X0[7:0]	7:0	OSD window2 x0 position.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN2_X0[11:8]	3:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN2_X1[7:0]	7:0	OSD window2 x1 position.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN2_X1[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN2_Y0[7:0]	7:0	OSD window2 y0 position.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN2_Y0[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN2_Y1[7:0]	7:0	OSD window2 y1 position.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN2_Y1[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN3_X0[7:0]	7:0	OSD window3 x0 position.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN3_X0[11:8]	3:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN3_X1[7:0]	7:0	OSD window3 x1 position.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OSD_WIN3_X1[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN3_Y0[7:0]	7:0	OSD window3 y0 position.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN3_Y0[11:8]	3:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN3_Y1[7:0]	7:0	OSD window3 y1 position.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN3_Y1[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN4_X0[7:0]	7:0	OSD window4 x0 position.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN4_X0[11:8]	3:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN4_X1[7:0]	7:0	OSD window4 x1 position.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN4_X1[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN4_Y0[7:0]	7:0	OSD window4 y0 position.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN4_Y0[11:8]	3:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_WIN4_Y1[7:0]	7:0	OSD window4 y1 position.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_WIN4_Y1[11:8]	3:0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x00**	**Access: R/W**
	LENGTH[7:0]	7:0	LVDS VBI Tx data length.	

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LENGTH[9:8]	1:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0x00**	**Access: R/W**
	WAIT_CNT[7:0]	7:0	LVDS VBI Tx wait cycle.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default: 0x00**	**Access: R/W**
	TYPE[7:0]	7:0	LVDS VBI Tx type.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	TYPE[9:8]	1:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x00**	**Access: R/W**
	HEADER_PW[7:0]	7:0	LVDS VBI header password.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	HEADER_PW[9:8]	1:0	See description of '102FCEh'.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	OSD_WIN_VALID[4:0]	4:0	OSD window valid bit.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default: 0x00**	**Access: R/W**
	VBI_FIRE	7	LVDS VBI fire.	
	-	6:1	Reserved.	
	LVDS_ VBI_EN	0	LVDS VBI Tx enable.	

DMS Register (Bank = 102F, Sub-bank = 26)

DMS Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	DMS_ALPHA_LPF_EN_F2	1	Alpha low pass filter enable F2.	
	DMS_EN_F2	0	Mosquito noise reduction enable F2.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	

DMS Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DMS_STRENGTH_F2[4:0]	4:0	Mosquito noise reduction strength F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	STD_LOW_THRD_HOR_F2[7:0]	7:0	Horizontal std low threshold F2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	STD_LOW_THRD_CEN_F2[7:0]	7:0	Center std low threshold F2.	
20H ~ 2FH (102F40H ~ 102F5FH)	**-**	**7:0**	**DEFAULT: -**	**ACCESS: -**
	-	-	Reserved.	

SPIKE_NR Register (Bank = 102F, Sub-bank = 26)

SPIKE_NR Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:4	Reserved.	
	SPIKE_NR_MR_EN	3	Spike NR motion ratio enable.	
	-	2	Reserved.	
	V_C_LPF_EN_F2	1	Vertical C Low Pass Filter Enable F2.	
	SPIKE_NR_EN_F2	0	Spike NR Enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SPIKE_NR_COEF[3:0]	3:0	Spike NR Coefficient.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	P_THRD_1[4:0]	4:0	Spike NR P threshold 1.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	P_THRD_2[7:0]	7:0	Spike NR P threshold 2.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	P_THRD_3[7:0]	7:0	Spike NR P threshold 3.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	

SPIKE_NR Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	D_31_STEP[2:0]	6:4	Spike NR D31 Step.	
	-	3	Reserved.	
	D_11_21_STEP[2:0]	2:0	Spike NR D11_21 Step.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	YP_22_STEP[2:0]	2:0	Spike NR YP22 Step.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SPK_MR_LPF_EN_F2	0	Spike NR motion ratio low pass filter enable F2 (LPF is 3x3 mask).	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x10**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_0[7:0]	7:0	Spike NR motion ratio look-up-table 0.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x32**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_1[7:0]	7:0	Spike NR motion ratio look-up-table 1.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x54**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_2[7:0]	7:0	Spike NR motion ratio look-up-table 2.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x76**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_3[7:0]	7:0	Spike NR motion ratio look-up-table 3.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x98**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_4[7:0]	7:0	Spike NR motion ratio look-up-table 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0xBA**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_5[7:0]	7:0	Spike NR motion ratio look-up-table 5.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0xDC**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_6[7:0]	7:0	Spike NR motion ratio look-up-table 6.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0xFE**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_7[7:0]	7:0	Spike NR motion ratio look-up-table 7.	

ACE2 Register (Bank = 102F, Sub-bank = 27)

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_CTI_MEDIAN_EN	5	Sub window CTI median enable.	
	SUB_CTI_EN	4	Sub window CTI enable.	
	-	3:2	Reserved.	
	MAIN_CTI_MEDIAN_EN	1	Main window CTI median enable.	
	MAIN_CTI_EN	0	Main window CTI enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_CTI_STEP[1:0]	5:4	Main window CTI step.	
	-	3	Reserved.	
	MAIN_CTI_LPF_COEF[2:0]	2:0	Main window CTI low pass filter coefficient.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_CTI_CORING_THRD[3:0]	3:0	Main window CTI coring threshold.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_CTI_BAND_COEF[5:0]	5:0	Main window CTI band pass filter coefficient.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_CTI_STEP[1:0]	5:4	Sub window CTI step.	
	-	3	Reserved.	
	SUB_CTI_LPF_COEF[2:0]	2:0	Sub window CTI low pass filter enable.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_CTI_CORING_THRD[3:0]	3:0	Sub window CTI coring threshold.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_CTI_BAND_COEF[5:0]	5:0	Sub window CTI band pass filter coefficient.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CTI_GRAY_THRD[7:0]	7:0	Main window CTI gray patch threshold step.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_CTI_GRAY_STEP[2:0]	2:0	Main window CTI gray patch step.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CTI_GRAY_THRD[7:0]	7:0	Sub window CTI gray patch threshold step.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_CTI_GRAY_STEP[2:0]	2:0	Sub window CTI gray patch step.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x88**	**Access: R/W**
	MAIN_G_STRENGTH[3:0]	7:4	Main window color adaptive for peaking of G.	
	MAIN_R_STRENGTH[3:0]	3:0	Main window color adaptive for peaking of R.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x88**	**Access: R/W**
	MAIN_C_STRENGTH[3:0]	7:4	Main window color adaptive for peaking of C.	
	MAIN_B_STRENGTH[3:0]	3:0	Main window color adaptive for peaking of B.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x88**	**Access: R/W**
	MAIN_Y_STRENGTH[3:0]	7:4	Main window color adaptive for peaking of Y.	
	MAIN_M_STRENGTH[3:0]	3:0	Main window color adaptive for peaking of M.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x88**	**Access: R/W**
	MAIN_NC_STRENGTH[3:0]	7:4	Main window color adaptive for peaking of other color.	
	MAIN_F_STRENGTH[3:0]	3:0	Main window color adaptive for peaking of F.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x88**	**Access: R/W**
	SUB_G_STRENGTH[3:0]	7:4	Sub window color adaptive for peaking of G.	
	SUB_R_STRENGTH[3:0]	3:0	Sub window color adaptive for peaking of R.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x88**	**Access: R/W**
	SUB_C_STRENGTH[3:0]	7:4	Sub window color adaptive for peaking of C.	
	SUB_B_STRENGTH[3:0]	3:0	Sub window color adaptive for peaking of B.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x88**	**Access: R/W**
	SUB_Y_STRENGTH[3:0]	7:4	Sub window color adaptive for peaking of Y.	
	SUB_M_STRENGTH[3:0]	3:0	Sub window color adaptive for peaking of M.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x88**	**Access: R/W**
	SUB_NC_STRENGTH[3:0]	7:4	Sub window color adaptive for peaking of other color.	
	SUB_F_STRENGTH[3:0]	3:0	Sub window color adaptive for peaking of F.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	VIP_FUN_BYPASS_EN	0	Vip all function bypass enable.	

NR Register (Bank = 102F, Sub-bank = 2A)

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**
	MED_AUTO	7	Median auto.	
	MED_EN	6	Median enable.	
	SNR_EN	5	SNR enable.	
	PATCH_W4_EN	4	Patch w4 enable.	
	PATCH_W3_EN	3	Patch w3 enable.	
	PATCH_W2_EN	2	Patch w2 enable.	
	-	1	Reserved.	
	MCNR_EN	0	MCNR enable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	NR_EN	7	NR enable.	
	PDNR_EN	6	PDNR enable.	
	RANDOM_MOTION_CHECK_DIFF	5	Random motion check diff enable.	
	RANDOM_MOTION_EN	4	Random motion enable.	
	DITHER_EN	3	Dither enable.	
	KEEP_DETAIL_EN	2	Keep detail enable.	
	FAVOR_MV0_EN	1	Favor mv0 enable.	
	C_PDNR_EN	0	PDNR c enable.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0xEE**	**Access: R/W**
	NR_LUT_2[7:4]	7:4	NR look up table 2.	
	NR_LUT_3[3:0]	3:0	NR look up table 3.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0xFF**	**Access: R/W**
	NR_LUT_0[15:12]	7:4	NR look up table 0.	
	NR_LUT_1[11:8]	3:0	NR look up table 1.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0xCC**	**Access: R/W**
	NR_LUT_6[7:4]	7:4	NR look up table 6.	
	NR_LUT_7[3:0]	3:0	NR look up table 7.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0xDD**	**Access: R/W**
	NR_LUT_4[15:12]	7:4	NR look up table 4.	
	NR_LUT_5[11:8]	3:0	NR look up table 5.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0xAA**	**Access: R/W**
	NR_LUT_10[7:4]	7:4	NR look up table 10.	

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NR_LUT_11[3:0]	3:0	NR look up table 11.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0xBB**	**Access: R/W**
	NR_LUT_8[15:12]	7:4	NR look up table 8.	
	NR_LUT_9[11:8]	3:0	NR look up table 9.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x88**	**Access: R/W**
	NR_LUT_14[7:4]	7:4	NR look up table 14.	
	NR_LUT_15[3:0]	3:0	NR look up table 15.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x99**	**Access: R/W**
	NR_LUT_12[15:12]	7:4	NR look up table 12.	
	NR_LUT_13[11:8]	3:0	NR look up table 13.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x66**	**Access: R/W**
	NR_LUT_18[7:4]	7:4	NR look up table 18.	
	NR_LUT_19[3:0]	3:0	NR look up table 19.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x77**	**Access: R/W**
	NR_LUT_16[15:12]	7:4	NR look up table 16.	
	NR_LUT_17[11:8]	3:0	NR look up table 17.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x44**	**Access: R/W**
	NR_LUT_22[7:4]	7:4	NR look up table 22.	
	NR_LUT_23[3:0]	3:0	NR look up table 23.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x55**	**Access: R/W**
	NR_LUT_20[15:12]	7:4	NR look up table 20.	
	NR_LUT_21[11:8]	3:0	NR look up table 21.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x22**	**Access: R/W**
	NR_LUT_26[7:4]	7:4	NR look up table 26.	
	NR_LUT_27[3:0]	3:0	NR look up table 27.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x33**	**Access: R/W**
	NR_LUT_24[15:12]	7:4	NR look up table 24.	
	NR_LUT_25[11:8]	3:0	NR look up table 25.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	NR_LUT_30[7:4]	7:4	NR look up table 30.	
	NR_LUT_31[3:0]	3:0	NR look up table 31.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x11**	**Access: R/W**
	NR_LUT_28[15:12]	7:4	NR look up table 28.	

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NR_LUT_29[11:8]	3:0	NR look up table 29.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x88**	**Access: R/W**
	PDNR_LOW_LUT_2[7:4]	7:4	PDNR low look up table 2.	
	PDNR_LOW_LUT_3[3:0]	3:0	PDNR low look up table 3.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x88**	**Access: R/W**
	PDNR_LOW_LUT_0[15:12]	7:4	PDNR low look up table 0.	
	PDNR_LOW_LUT_1[11:8]	3:0	PDNR low look up table 1.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_LOW_LUT_6[7:4]	7:4	PDNR low look up table 6.	
	PDNR_LOW_LUT_7[3:0]	3:0	PDNR low look up table 7.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x51**	**Access: R/W**
	PDNR_LOW_LUT_4[15:12]	7:4	PDNR low look up table 4.	
	PDNR_LOW_LUT_5[11:8]	3:0	PDNR low look up table 5.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_LOW_LUT_10[7:4]	7:4	PDNR low look up table 10.	
	PDNR_LOW_LUT_11[3:0]	3:0	PDNR low look up table 11.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_LOW_LUT_8[15:12]	7:4	PDNR low look up table 8.	
	PDNR_LOW_LUT_9[11:8]	3:0	PDNR low look up table 9.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_LOW_LUT_14[7:4]	7:4	PDNR low look up table 14.	
	PDNR_LOW_LUT_15[3:0]	3:0	PDNR low look up table 15.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_LOW_LUT_12[15:12]	7:4	PDNR low look up table 12.	
	PDNR_LOW_LUT_13[11:8]	3:0	PDNR low look up table 13.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0xDC**	**Access: R/W**
	PDNR_HIGH_LUT_2[7:4]	7:4	PDNR high look up table 2.	
	PDNR_HIGH_LUT_3[3:0]	3:0	PDNR high look up table 3.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0xFE**	**Access: R/W**
	PDNR_HIGH_LUT_0[15:12]	7:4	PDNR high look up table 0.	
	PDNR_HIGH_LUT_1[11:8]	3:0	PDNR high look up table 1.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x98**	**Access: R/W**
	PDNR_HIGH_LUT_6[7:4]	7:4	PDNR high look up table 6.	

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PDNR_HIGH_LUT_7[3:0]	3:0	PDNR high look up table 7.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0xBA**	**Access: R/W**
	PDNR_HIGH_LUT_4[15:12]	7:4	PDNR high look up table 4.	
	PDNR_HIGH_LUT_5[11:8]	3:0	PDNR high look up table 5.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x54**	**Access: R/W**
	PDNR_HIGH_LUT_10[7:4]	7:4	PDNR high look up table 10.	
	PDNR_HIGH_LUT_11[3:0]	3:0	PDNR high look up table 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x76**	**Access: R/W**
	PDNR_HIGH_LUT_8[15:12]	7:4	PDNR high look up table 8.	
	PDNR_HIGH_LUT_9[11:8]	3:0	PDNR high look up table 9.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x10**	**Access: R/W**
	PDNR_HIGH_LUT_14[7:4]	7:4	PDNR high look up table 14.	
	PDNR_HIGH_LUT_15[3:0]	3:0	PDNR high look up table 15.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x32**	**Access: R/W**
	PDNR_HIGH_LUT_12[15:12]	7:4	PDNR high look up table 12.	
	PDNR_HIGH_LUT_13[11:8]	3:0	PDNR high look up table 13.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x88**	**Access: R/W**
	PDNR_C_LUT_2[7:4]	7:4	PDNR c look up table 2.	
	PDNR_C_LUT_3[3:0]	3:0	PDNR c look up table 3.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x88**	**Access: R/W**
	PDNR_C_LUT_0[15:12]	7:4	PDNR c look up table 0.	
	PDNR_C_LUT_1[11:8]	3:0	PDNR c look up table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_C_LUT_6[7:4]	7:4	PDNR c look up table 6.	
	PDNR_C_LUT_7[3:0]	3:0	PDNR c look up table 7.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x51**	**Access: R/W**
	PDNR_C_LUT_4[15:12]	7:4	PDNR c look up table 4.	
	PDNR_C_LUT_5[11:8]	3:0	PDNR c look up table 5.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_C_LUT_10[7:4]	7:4	PDNR c look up table 10.	
	PDNR_C_LUT_11[3:0]	3:0	PDNR c look up table 11.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_C_LUT_8[15:12]	7:4	PDNR c look up table 8.	

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PDNR_C_LUT_9[11:8]	3:0	PDNR c look up table 9.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_C_LUT_14[7:4]	7:4	PDNR c look up table 14.	
	PDNR_C_LUT_15[3:0]	3:0	PDNR c look up table 15.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDNR_C_LUT_12[15:12]	7:4	PDNR c look up table 12.	
	PDNR_C_LUT_13[11:8]	3:0	PDNR c look up table 13.	
34h ~ 7Fh (102F68h ~ 102FFFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
12/10/09		• Created first version.

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