MCP3201

2.7V 12-Bit A/D Converter with SPI™ Serial Interface

Features

- 12-bit resolution
- ±1 LSB max DNL
- ±1 LSB max INL (MCP3201-B)
- ±2 LSB max INL (MCP3201-C)
- On-chip sample and hold
- SPI™ serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100ksps max. sampling rate at V_{DD} = 5V
- 50ksps max. sampling rate at V_{DD} = 2.7V
- Low power CMOS technology
- 500 nA typical standby current, 2 µA max.
- 400 µA max. active current at 5V
- Industrial temp range: -40°C to +85°C
- 8-pin MSOP, PDIP, SOIC and TSSOP packages

Applications

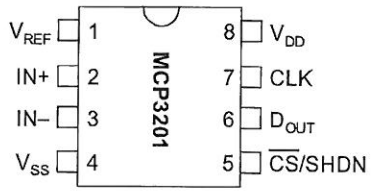
- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

Description

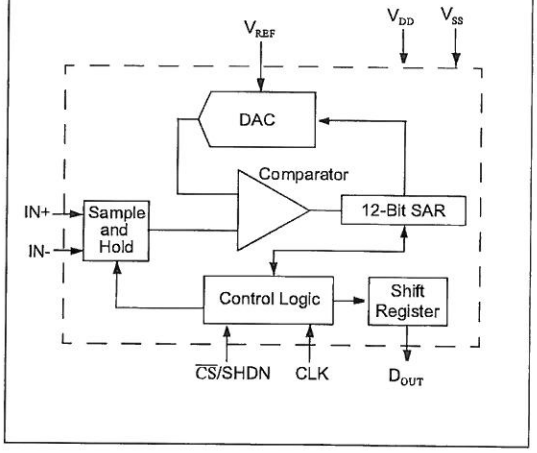
The Microchip Technology Inc. MCP3201 is a successive approximation 12-bit Analog-to-Digital (A/D) Converter with on-board sample and hold circuitry. The device provides a single pseudo-differential input. Differential Nonlinearity (DNL) is specified at ±1 LSB, and Integral Nonlinearity (INL) is offered in ±1 LSB (MCP3201-B) and ±2 LSB (MCP3201-C) versions. Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device is capable of sample rates of up to 100 ksps at a clock rate of 1.6 MHz. The MCP3201 operates over a broad voltage range (2.7V - 5.5V). Low current design permits operation with typical standby and active currents of only 500 nA and 300 µA, respectively. The device is offered in 8-pin MSOP, PDIP, TSSOP and 150 mil SOIC packages.

Package Types

MSOP, PDIP, SOIC, TSSOP



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD}.....7.0V

All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{DD} +0.6V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-65°C to +125°C

ESD protection on all pins (HBM).....> 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{DD}	+2.7V to 5.5V Power Supply
V_{SS}	Ground
IN+	Positive Analog Input
IN-	Negative Analog Input
CLK	Serial Clock
D_{OUT}	Serial Data Out
$\overline{CS}$/SHDN	$\overline{CS}$ Chip Select/Shutdown Input
V_{REF}	Reference Voltage Input

ELECTRICAL CHARACTERISTICS

All parameters apply at V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 5V, T_{AMB} = -40°C to +85°C, f_{SAMPLE} = 100 ksps, and f_{CLK} = 16*f_{SAMPLE} unless otherwise noted.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Conversion Rate:						
Conversion Time	t_{CONV}	—	—	12	clock cycles	
Analog Input Sample Time	t_{SAMPLE}		1.5		clock cycles	
Throughput Rate	f_{SAMPLE}	—	—	100 50	ksps ksps	V_{DD} = V_{REF} = 5V V_{DD} = V_{REF} = 2.7V
DC Accuracy:						
Resolution			12		bits	
Integral Nonlinearity	INL	— —	±0.75 ±1	±1 ±2	LSB LSB	MCP3201-B MCP3201-C
Differential Nonlinearity	DNL	—	±0.5	±1	LSB	No missing codes over temperature
Offset Error		—	±1.25	±3	LSB	
Gain Error		—	±1.25	±5	LSB	
Dynamic Performance:						
Total Harmonic Distortion	THD	—	-82	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Signal to Noise and Distortion (SINAD)	SINAD	—	72	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Spurious Free Dynamic Range	SFDR	—	86	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Reference Input:						
Voltage Range		0.25	—	V_{DD}	V	**Note 2**
Current Drain		— —	100 .001	150 3	µA µA	$\overline{CS}$ = V_{DD} = 5V
Analog Inputs:						
Input Voltage Range (IN+)	IN+	IN-	—	V_{REF}+IN-	V	
Input Voltage Range (IN-)	IN-	V_{SS}-100		V_{SS}+100	mV	
Leakage Current		—	0.001	±1	µA	
Switch Resistance	R_{SS}	—	1K	—	W	See Figure 4-1
Sample Capacitor	C_{SAMPLE}	—	20	—	pF	See Figure 4-1

Note 1: This parameter is established by characterization and not 100% tested.

2: See graph that relates linearity performance to V_{REF} level.

3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.

ELECTRICAL CHARACTERISTICS (CONTINUED)

All parameters apply at V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 5V, T_{AMB} = -40°C to +85°C, f_{SAMPLE} = 100 ksps, and f_{CLK} = 16*f_{SAMPLE} unless otherwise noted.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Digital Input/Output:						
Data Coding Format		Straight Binary				
High Level Input Voltage	V_{IH}	0.7 V_{DD}	—	—	V	
Low Level Input Voltage	V_{IL}	—	—	0.3 V_{DD}	V	
High Level Output Voltage	V_{OH}	4.1	—	—	V	I_{OH} = -1 mA, V_{DD} = 4.5V
Low Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1 mA, V_{DD} = 4.5V
Input Leakage Current	I_{LI}	-10	—	10	µA	V_{IN} = V_{SS} or V_{DD}
Output Leakage Current	I_{LO}	-10	—	10	µA	V_{OUT} = V_{SS} or V_{DD}
Pin Capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	—	10	pF	V_{DD} = 5.0V **(Note 1)** T_{AMB} = 25°C, f = 1 MHz
Timing Parameters:						
Clock Frequency	f_{CLK}	— —	— —	1.6 0.8	MHz MHz	V_{DD} = 5V **(Note 3)** V_{DD} = 2.7V **(Note 3)**
Clock High Time	t_{HI}	312	—	—	ns	
Clock Low Time	t_{LO}	312	—	—	ns	
$\overline{CS}$ Fall To First Rising CLK Edge	t_{SUCS}	100	—	—	ns	
CLK Fall To Output Data Valid	t_{DO}	—	—	200	ns	See Test Circuits, Figure 1-2
CLK Fall To Output Enable	t_{EN}	—	—	200	ns	See Test Circuits, Figure 1-2
$\overline{CS}$ Rise To Output Disable	t_{DIS}	—	—	100	ns	See Test Circuits, Figure 1-2 **(Note 1)**
$\overline{CS}$ Disable Time	t_{CSH}	625	—	—	ns	
D_{OUT} Rise Time	t_R	—	—	100	ns	See Test Circuits, Figure 1-2 **(Note 1)**
D_{OUT} Fall Time	t_F	—	—	100	ns	See Test Circuits, Figure 1-2 **(Note 1)**
Power Requirements:						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Operating Current	I_{DD}	— —	300 210	400 —	µA µA	V_{DD} = 5.0V, D_{OUT} unloaded V_{DD} = 2.7V, D_{OUT} unloaded
Standby Current	I_{DDS}	—	0.5	2	µA	$\overline{CS}$ = V_{DD} = 5.0V
Temperature Ranges:						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistance:						
Thermal Resistance, 8L-PDIP	q_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	q_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	q_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-TSSOP	q_{JA}	—	124	—	°C/W	

Note 1: This parameter is established by characterization and not 100% tested.

2: See graph that relates linearity performance to V_{REF} level.

3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.

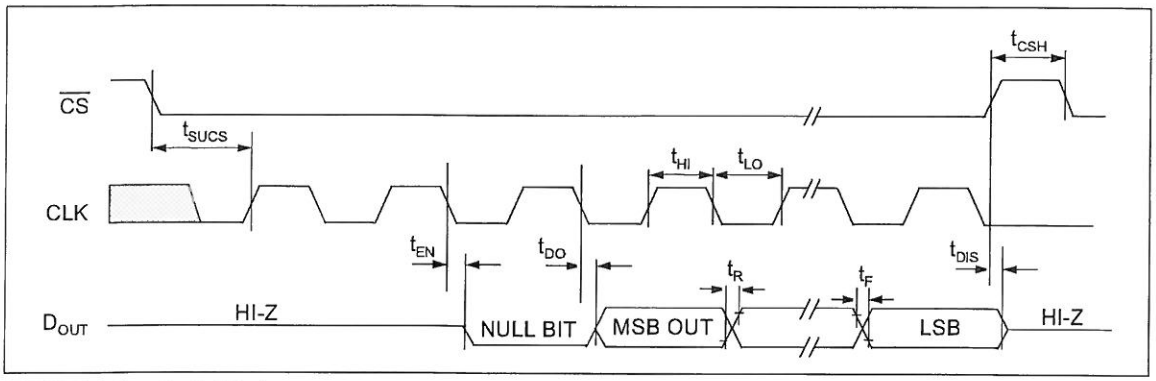


FIGURE 1-1: *Serial Timing.*

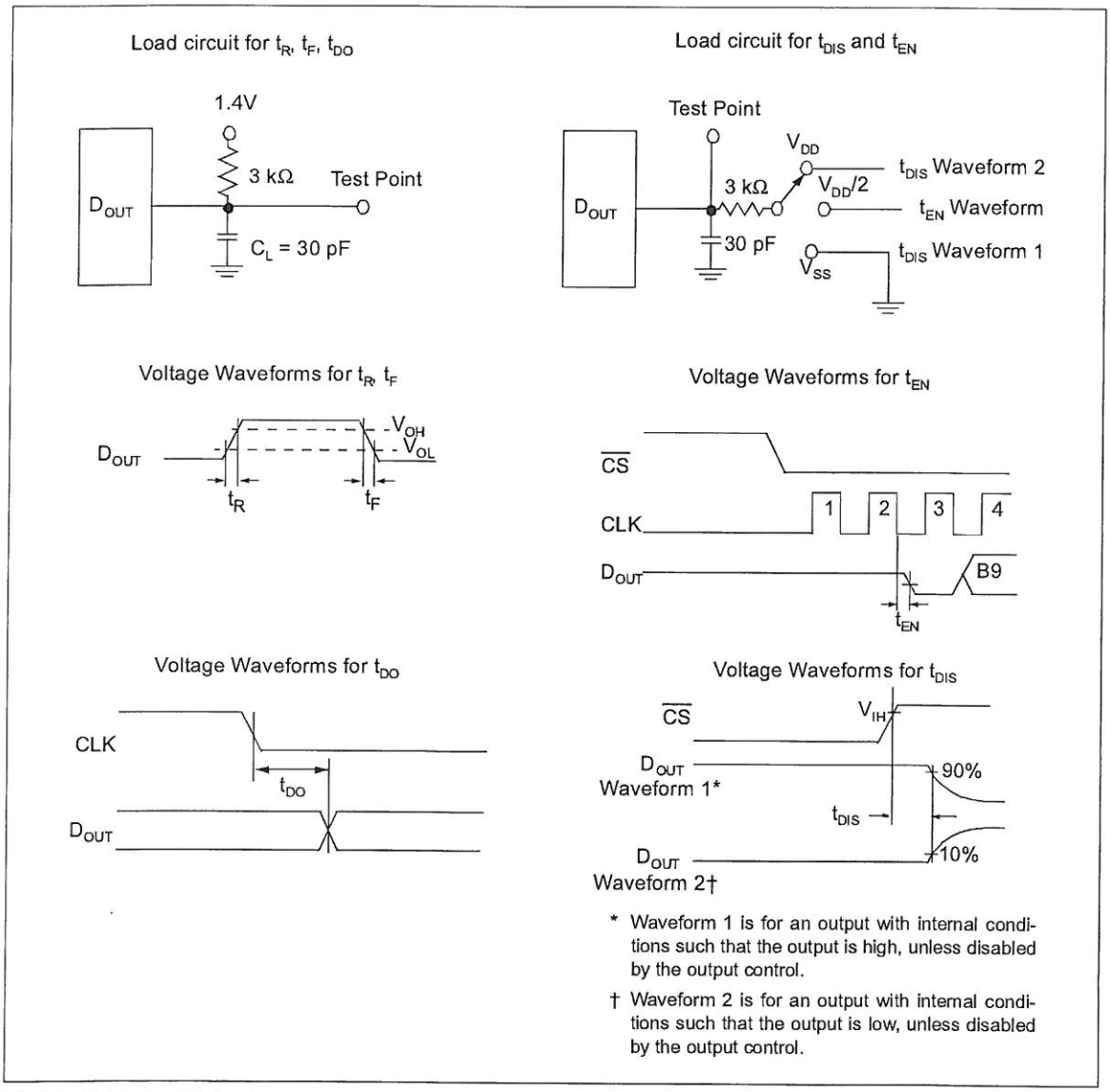


FIGURE 1-2: *Test Circuits.*