EAGLE Style Guide

v1.0

Part Creation

- Symbol
  - Grid
    - 0.1 inches Size
    - 0.01 inches Alt
  - Style
    - Location
      - Center origin of grid on the center of the part
    - Font
      - Vector rendered
      - Ratio 8%, unless made bold for end user benefit
      - Size of 0.07 in
      - Value aligned bottom-left, name on top left of symbol
  - Functionality
    - Pins should be labeled in a way that allows the symbol to be applied to any parts in a similar family
    - For passive elements, pin labels can be disabled for simplicity
      - “Visible - pin” for just the pin label
      - “Visible - pad” for just the pad label
    - Use passive for the pin type; at a minimum, don’t set any to power even if they are power pins
    - For functional layout: Inputs on left, outputs on right, power top-left, ground bottom-right.
    - Pin placement
      - Inputs on left
      - Outputs on right
      - Power on top (optional)
      - Ground on bottom (optional)
    - Decimal value labeling
      - For labeling fractional values, include the decimal point. Eg. 3.3V
      - 4.51k → 4,510 kOhm
      - NOT 3V3, etc.

- Footprint
  - Grid
    - 1 mm Size
    - 0.1 mm Alt
  - Font
    - Font - Vector
    - Ratio - 8%
      - unless made bold for end user benefit
    - Size - 1 mm
  - Functionality
    - Silkscreen
      - Line for alignment on tPlace/bPlace
      - All ICs should have pin one marked with a dot
      - All diodes should have direction or cathode marks
      - Clearly indicate polarity as necessary
      - Try not to overlap pads with silkscreen; although tedious, cut a section out
    - Slots
      - Use the milling layer (46) to draw the outline of the slot
      - Create the pad using the elongated pad
      - Set the hole diameter to the width of the slot
      - Export the milling layer to its own gerber file and attach it with the rest of your gerbers
      - Every manufacturer has its own preferred method, but seems to be accepted widely enough
  - Labeling
    - >NAME label on top
    - >VALUE label on below
    - Outline of package on tDocu/bDocu
- Device
  - Attributes
    - Name should be manufacturer part number
    - Attribute - DKPN should be filled with the Digi-Key part number
  - Descriptions
    - One sentence describes the function of the part
    - Datasheet link if available
  - Prefix
    - Chart for Designators

Letter	Part Type

C	Capacitor
D	Diode, LED
F	Fuse
J	Jack or Connector (least moveable connection part)
JP	Jumper
K	Relay or Contactor
L	Inductor
LS/BZ	Loudspeaker or buzzer
M	Motor
P	Plug (most moveable connection part)
PS	Power Supply
Q	Transistor (all)
R	Resistor
S/SW	Switch
T	Transformer
TP	Test Point
U	Integrated Circuit
X	Crystal

Schematics

- Overall
    - Organize subsystems as follows:
    - Related subsystems should be grouped into a sheet
    - Each subsystem in a sheet should be boxed clearly, and that box labeled
        - Use line tool, width 0.006, shortdash, layer 97 info

        - Label font
            - Font - vector
            - Ratio - 12%
            - Size - 0.25 in
            - Layer - Info
    - Every sheet should have the following:
        - A frame no bigger than 11 x 17" (8½ x 11” preferred), which should have the following info:
            - A name
            - Last edit date
            - Last edit engineer(s)
            - Schematic version
            - Page #
        - Frames within a schematic should all be the same size
- Nets
    - Every net should have a name if possible
        - Use xref tags at 0.05 size
    - Every bus should have a name and description
    - Every power net should be labeled with the acceptable voltage range and max current at the net driver
    - Differentially routed nets should be commented as such as the driver and sink
    - Impedance controlled nets should be commented as such as the driver and sink
    - Power and Ground nets
        - Use symbol with appropriate name
- Configs
    - Any value computed (e.g. varies by application) from a datasheet should be noted
    - Any optional parts should be noted
    - 0ohm isolation resistor and 0ohm jumper resistors should be noted

Boards

- Fab House / Validation
    - Load fab house DRC before place and route
    - RoboJackets has slightly conservative DRCs for 2 and 4 layer boards
- Placement
    - Keep analog electronics far from high power electronics
    - Locate power net status LEDs near power sources
    - Provide adequate spacing for stitching/shielding if needed
    - Verify any mechanical considerations

        - Board mounting holes
        - Component mounting holes/cutouts
        - Use tDoc/bDoc and/or tKeepout/bKeepout for bolt head size to prevent traces near mounting
    - Place decoupling capacitors as close to the power pin of the IC as possible
        - Smallest values should be closest to pin to minimize parasitic inductance
- Routing
    - Avoid minimum trace width where possible
        - Suggestions: 0.2 to 0.3mm for signals, 0.4 to 0.5mm for power (increase as needed for current rating)
    - Avoid minimum trace spacing where possible
    - Avoid minimum drill/via size where possible
        - Suggestions: 0.35mm drill, 0.65mm diameter for vias
    - Do not split differentially routed pairs unless impedance and arrival time can be matched
    - Avoid vias on signals above 1GHz
    - Use the same number of vias on differentially routed traces
    - For two layer boards, try to keep component, signal, and power on the top layer and ground return on the bottom layer
    - High frequency signals should have continuous low impedance return path directly beneath trace.
    - Keep high frequency signals isolated from other signals to minimize crosstalk
    - route signals orthogonally to avoid cross-talk
- Silkscreen
    - This is far more important than most people realize and can take a significant amount of time to get right. A good silkscreen makes a board easier to use, easier to debug, and harder to break.
    - Meta
        - Have at least a "vMAJOR.minor" version label on the board
        - Have your team name and year (optionally month, Ubuntu style) on the board
        - Have your team logo on the board
        - Have a filled white square to write in an instance ID
            - Recommended if more than three boards will be fabricated
            - e.g. can say "board #2 is broken", there is a "2" written on the white square
            - Cover ink with Kapton tape
        - Don’t place them on vias (even tented vias) unless absolutely unavoidable
    - Components & Connectors
        - Set default line width to 0.2mm

        - Label all power inputs with name and voltage (current optional)
        - Label all connectors with name
        - Label all switches with position values
        - Label all debug LEDs
        - Label all fuses with current rating (type optional)
    - Font
        - All font should be vector rendered
        - All font should be ratio 8%, unless made bold for end user benefit
        - Component font size should be "1"
            - e.g. R45, Q1, etc.
        - Layer - t/bPlace