EFR32xG27 2-Layer Hardware Design Example Reference Manual

Silicon Labs provides customers with a reference design for BLE Mesh agricultural applications on a 2-layer PCB in a CR2450 coin cell battery size with EFR32xG27, operational amplifiers and sensors. This document describes this 2-layer reference design including RF test data as well. Also, design files including schematic and layout CAD designs, BOM, PDF and Gerbers, are available under Silicon Labs website at www.silabs.com.

The design example utilizes an EFR32BG27 chip in a QFN32 package utilizing DCDC buck converter.

The design is pre-compliance tested and appeared to be fully compliant with CE and FCC regulatory standards.

The BLE agricultural reference design includes the following circuit components:

- EFR32BG27 radio chip with buck converter for +8 dBm maximum TX power in a QFN32 package
- High- and low-frequency crystals
- Built-in PCB inverted-F antenna
- 10-pin mini-simplicity debug connector
- CR2450 coin cell battery
- Si7021 RH / Temperature sensor
- LMP91000 Analog AFE integrated circuit
- OPA4991 4-channel operational amplifier for EIS measurement capability
- PMOS power switches for the sensors

KEY POINTS

- Brief description of EFR32BG27 QFN32 BLE 2-layer reference design
- RF test data provided, including antenna impedance, gain and efficiency, conducted and radiated fundamental and harmonics EIRP data, radiation patterns
- Design files are available for customers reference at www.silabs.com

1. Introduction

The EFR32xG27 QFN32-based 2-layer BLE reference design is virtually provided for customers, since design files, including schematic and layout CAD design files, BOM, PDF and Gerbers, are available under www.silabs.com but there is no orderable part number for the board design itself.
The design is also pre-tested by Silicon Labs and is compliant with CE and FCC regulatory standards at the TX output power level of +8 dBm.
The module utilizes 2 electrical layers and an on-board printed antenna, and it runs from a CR2450 coin cell battery. The entire module dimension (~ 38 x 32 mm) is not even significantly larger than the size of a coin cell battery holder (mounted on the PCB bottom side).
The module has the so-called 10-pin mini-simplicity header for programming and debugging purposes (see connection details in AN958 application note).
The on-board printed antenna is tuned when the coin cell battery is being inserted into, but no plastic enclosure is considered. So, for design implementations with plastics, Silicon Labs recommends checking the antenna impedance since some fine-tuning (probably only BOM change) might be required in its final environment.
The photo of the reference design (engineering sample, RF parts mounted only) is shown in the Figure 1.1 below.
The reference design is also aiming for agricultural applications, therefore circuit connections with LMP91000 Analog AFE integrated circuit and operational amplifiers with connecting electrodes are also provided for EIS (Electrochemical Impedance Spectroscopy) measurement capabilities. Additionally, the design includes a humidity and temperature sensor as well.
However, this reference manual focuses on the RF circuit connections and test data, so these additional blocks for EIS tests are not detailed here.

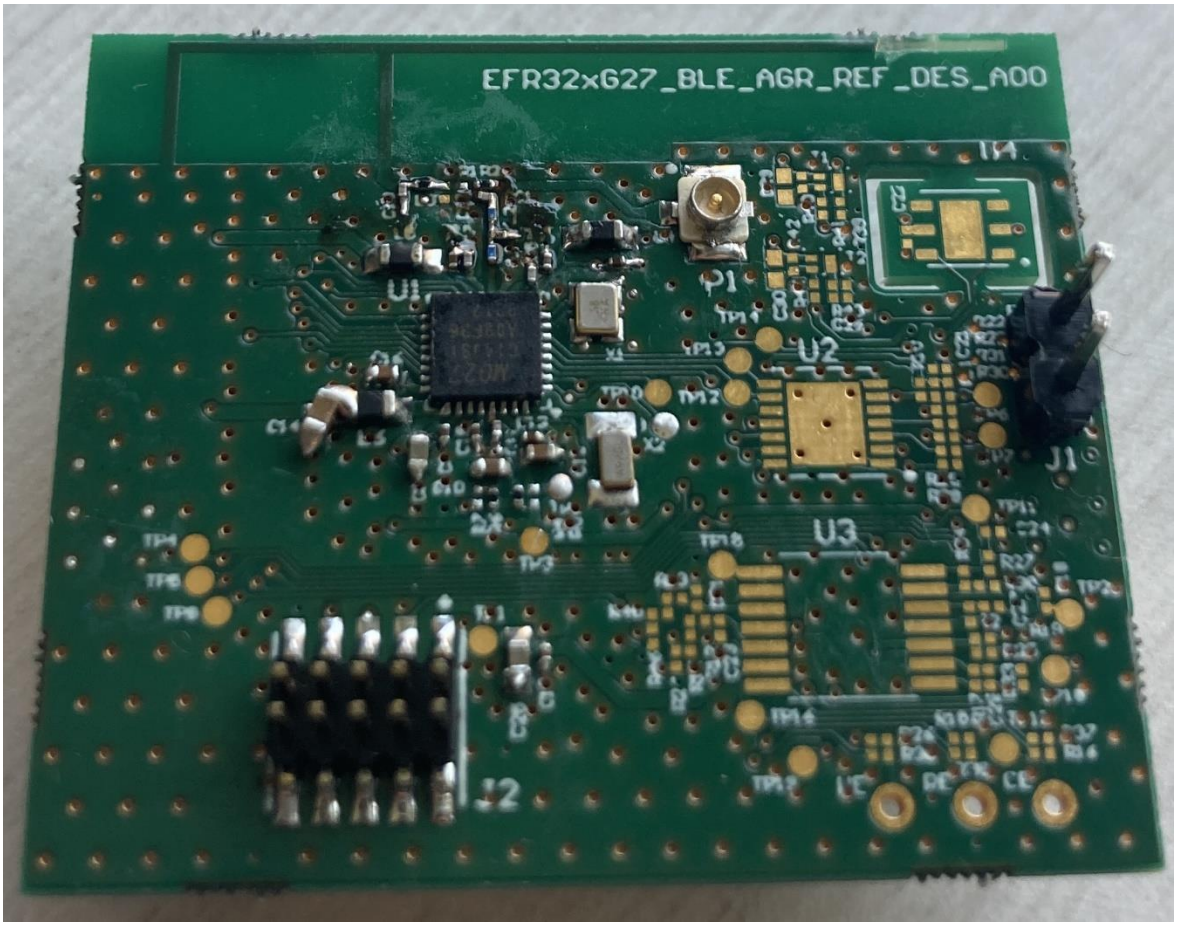


Figure 1.1 EFR32xG27 Low-Cost 2-layer Design (RF engineering sample)

2. Schematic Design

The complete schematic design of the EFR32xG27-based reference module can be found in the full design pack provided by Silicon Labs and is also available under www.silabs.com. Since this reference manual focuses on the RF design part of the module, this section shows the RF focused schematic part of the entire design.
The EFR32xG27 RF part of the schematic is shown in the Figure 2.1 below.

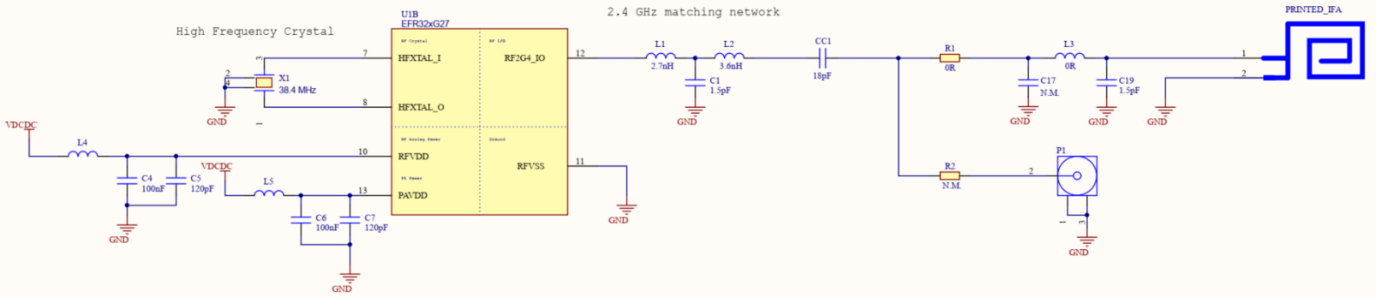


Figure 2.1 RF part of the EFR32xG27 reference schematic design

The design includes both low- and high-frequency crystals and the on-chip DCDC converter is also being utilized. Both RFVDD and PAVDD nets are connected to the internal DCDC converter's output to minimize the current consumption, TX power variation caused by battery draining, and to maximize the battery life as well. The RF front-end path can be divided into two separate parts: EFR32xG27 RF matching network including components L1, L2, C1, while CC1 is an RF-bypass, DC-blocking capacitor; printed antenna and antenna matching network including components L3, C17, C19. The 50-ohm point in the RF-FE path is between the EFR32xG27 and antenna matching networks, i.e., the common point of components CC1, R1 and R2. Conducted measurements can be performed on the u.FL connector by selecting the appropriate RF path by R2 (while R1 not mounted).
The RF matching network elements are realized by SMD 0201-sized components, capacitors from Murata GRM0335C and inductors from Murata LQP03TN series.
The RF matching network is optimized on a 1mm-thick (FR-4) 2-layer PCB for the maximum TX power level of +8 dBm.

3. Layout Design

The complete layout design of the EFR32xG27-based reference module, in CAD format as well, can be found in the full design pack provided by Silicon Labs and is also available under www.silabs.com.
Snapshots from the layout design of EFR32xG27 BLE 2-layer module are shown in the Figure 3.1 below.
The board design follows the generic RF layout recommendations as much as possible on this space-constrained design. The top layer consists of all components, excluding the coin cell battery holder which is placed on the bottom layer of the module. The bottom layer beneath the RF section ensures the low-impedance return path for the RF part of the design by having continuous and unbroken ground pour on it. The printed antenna is an inverted-F design. The antenna has a separate area on the PCB as well as shown in the figures below and placed away from the coin cell battery as much as possible to avoid any possible shielding effects of it.

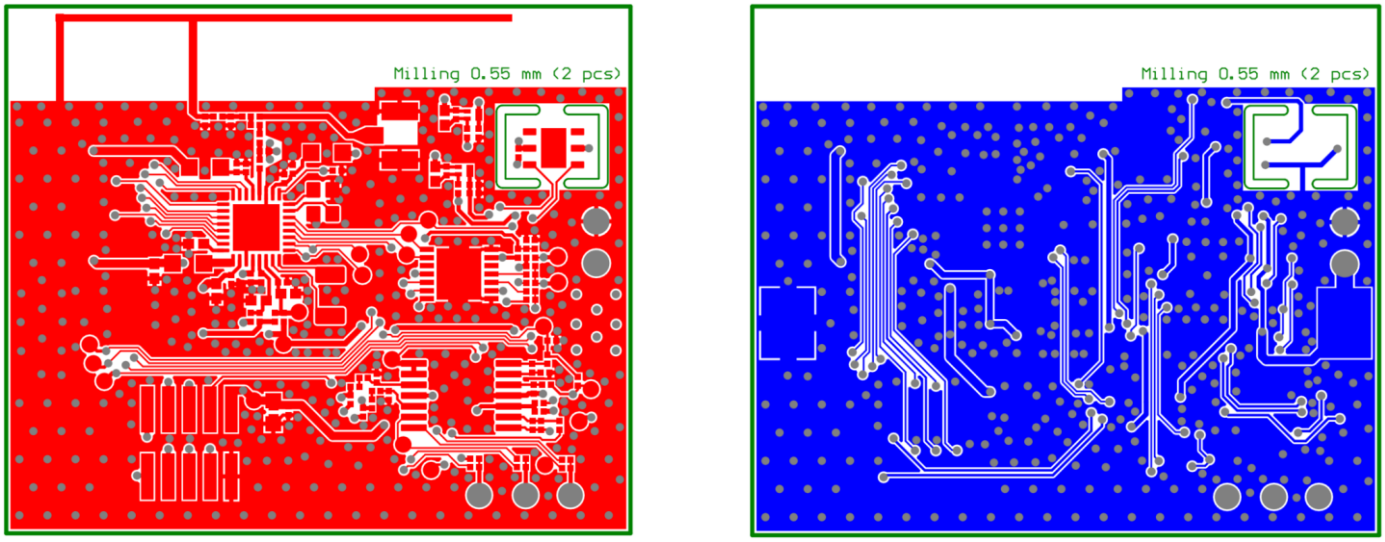


Figure 3.1 EFR32xG27 2-layer reference layout design: top and bottom layers

4. Antenna Simulations

The RF path and antenna designs have been simulated in a 3D EM simulator, in CST. The simplified simulated antenna structure and PCB is shown in Figure 4.1 below.

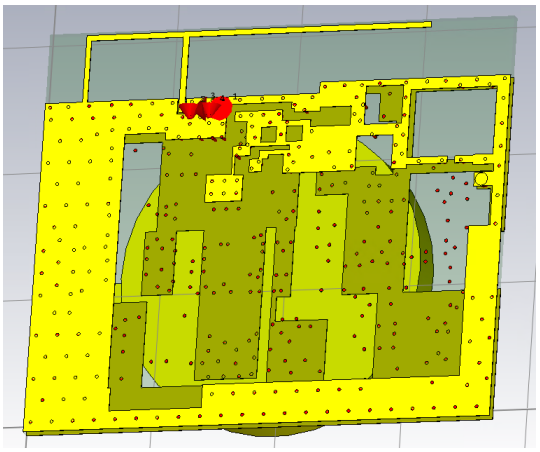


Figure 4.1 EFR32xG27 BLE Design – Simplified Simulated structure in CST

The simulated antenna parameters are plotted in the following figures below.

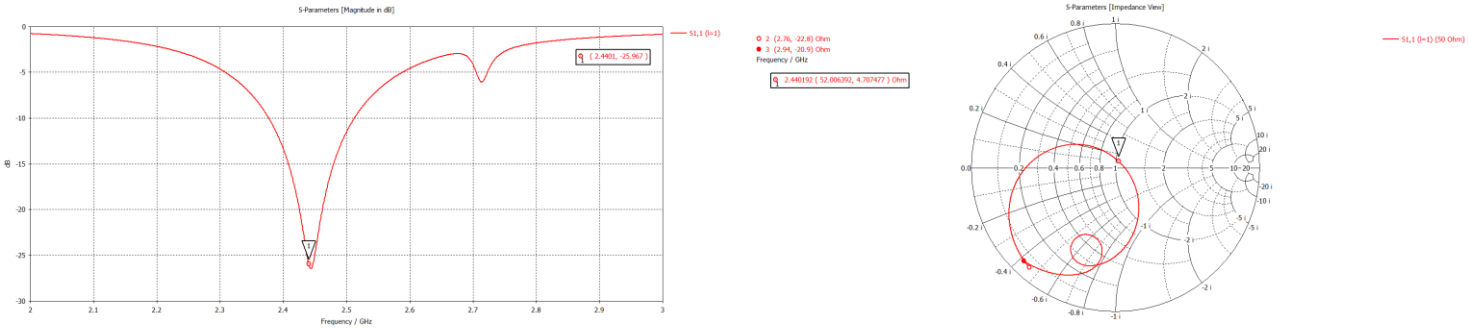


Figure 4.2 Simulated antenna S11

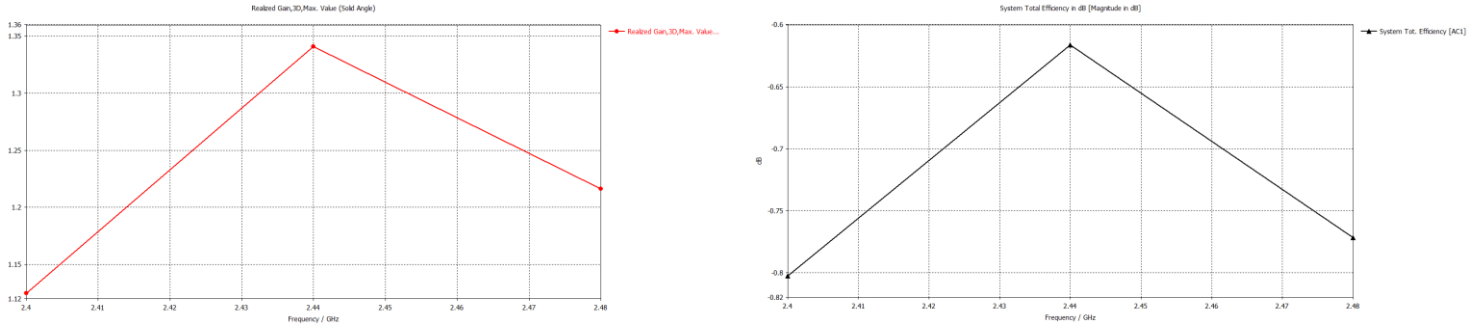


Figure 4.3 Simulated antenna realized gain and total efficiency

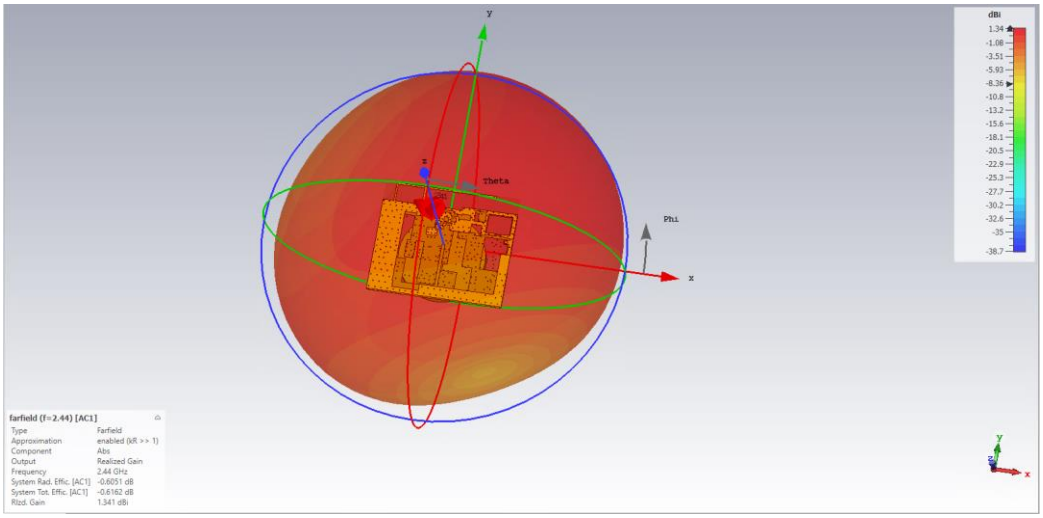


Figure 4.4 Simulated antenna far-field properties

5. Measurement Results

5.1. Conducted TX Performance

The TX conducted performance results are summarized in the table below.

Table 5.1 Conducted TX Performance Results

Power Settings	Frequency	TXP	H2	H3	H4	H5	Current
Setpower 85	2402 MHz	7.6 dBm	-59.8 dBm	-45.8 dBm	< -70 dBm	-59.1 dBm	13.9 mA
	2440 MHz	7.7 dBm	-61.9 dBm	-46.5 dBm	< -70 dBm	-63.1 dBm	14.1 mA
	2480 MHz	7.7 dBm	-63.8 dBm	-45.8 dBm	< -70 dBm	< -70 dBm	14.0 mA

The spectrum plot for these TX conducted measurements listed above are shown in the following figure below.

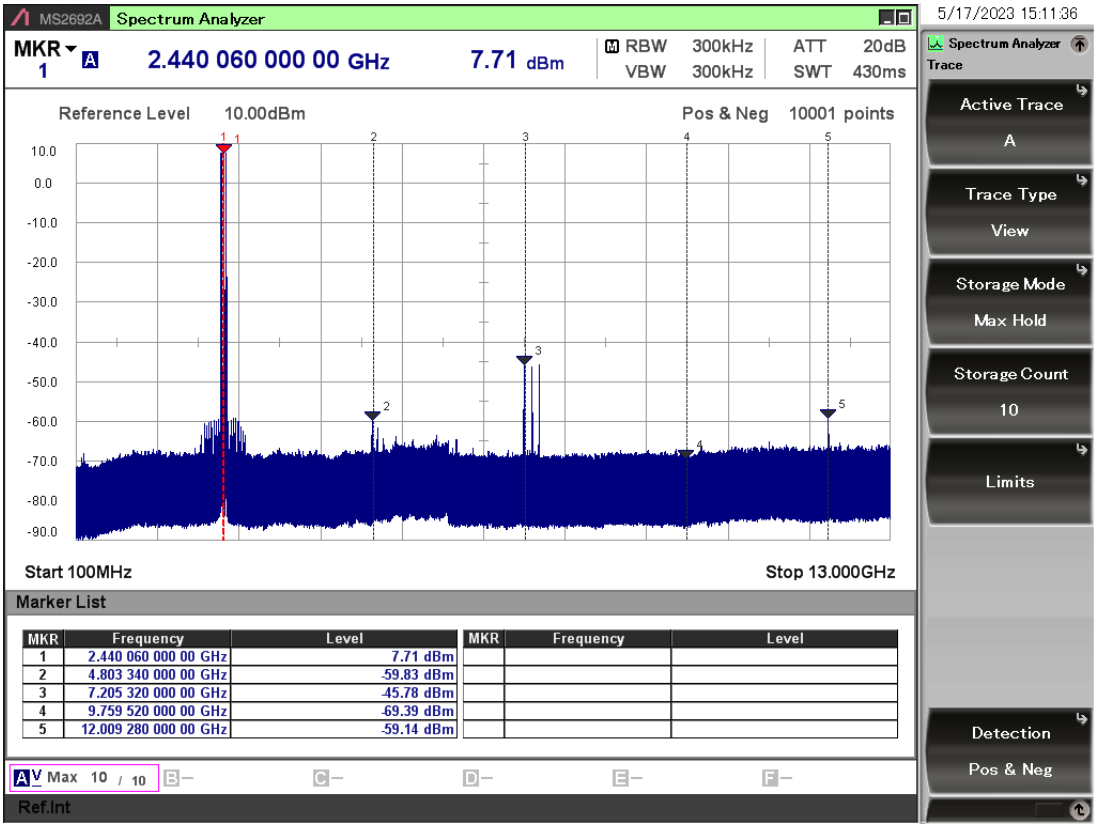


Figure 5.1 Conducted Spectrum, Max Hold for 3 Frequencies Captured

5.2. Conducted RX Performance

The conducted RX measurement results are demonstrated with the following charts. The receiver performance has been checked with Bluetooth LE 1 Mbps and 125 kbps coded PHYs, while the sensitivity limit is PER < 30%, which basically corresponds to BER < 0.1% for the same MSK signal.

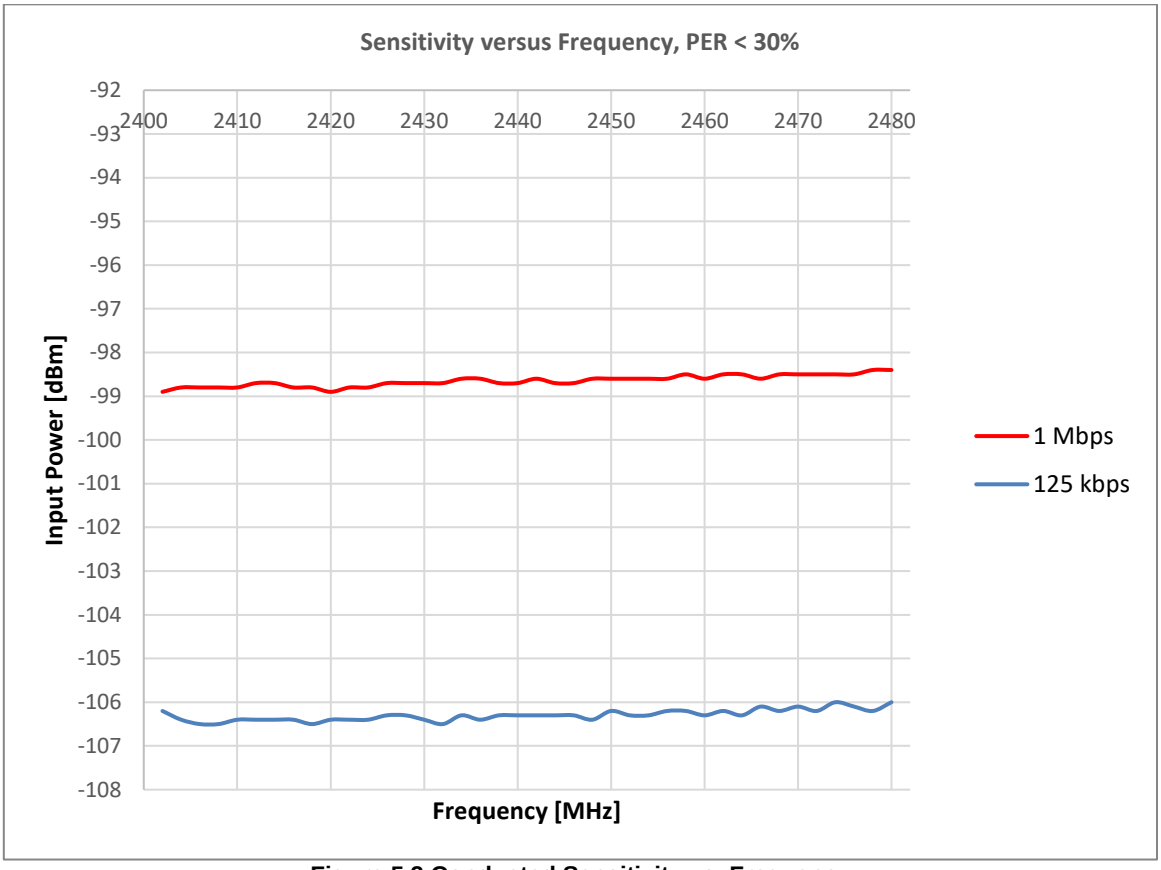


Figure 5.2 Conducted Sensitivity vs. Frequency

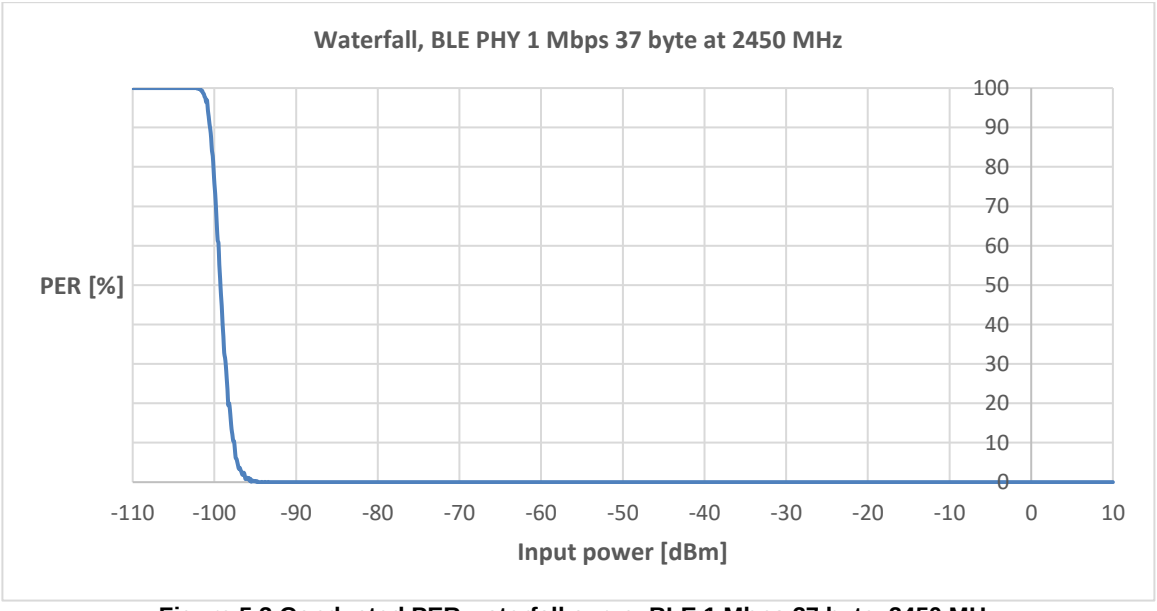


Figure 5.3 Conducted PER waterfall curve, BLE 1 Mbps 37 byte, 2450 MHz

5.3. Antenna Impedance

The measured antenna impedance of the module's printed antenna is shown in the figure below.
The measured S11 of the antenna is below -10dB in the frequency band of interest (2.4 – 2.48 GHz) which is basically acceptable and good for this application also considered the small board size which is a limiting factor in impedance bandwidth. The antenna impedance has been checked by using a sleeve balun connected as well to avoid any current leakage through the connected RF pig-tail cable which would deteriorate the measurement results. Additionally, the antenna impedance tuning has been performed when the coin-cell battery was being inserted into, but without plastic enclosure. So, designs with plastic housing applied might need some further fine-tuning of antenna to achieve the best RF performance.

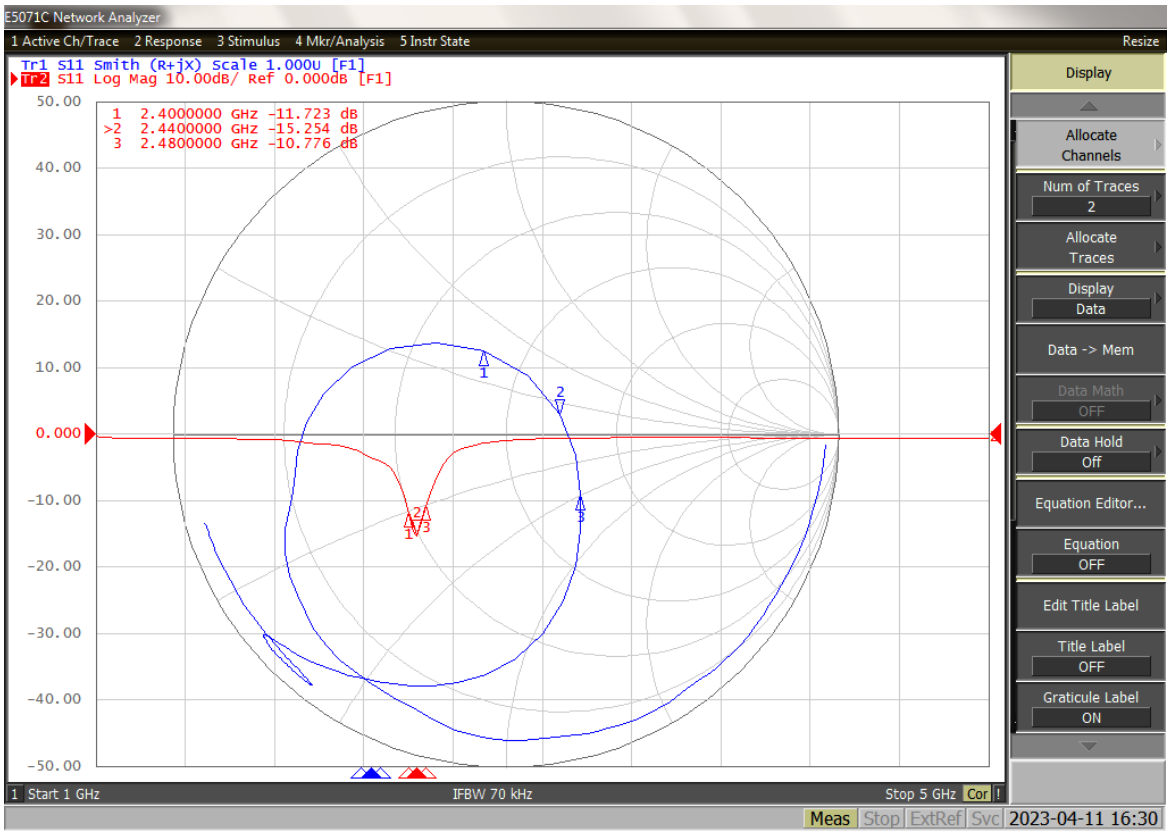


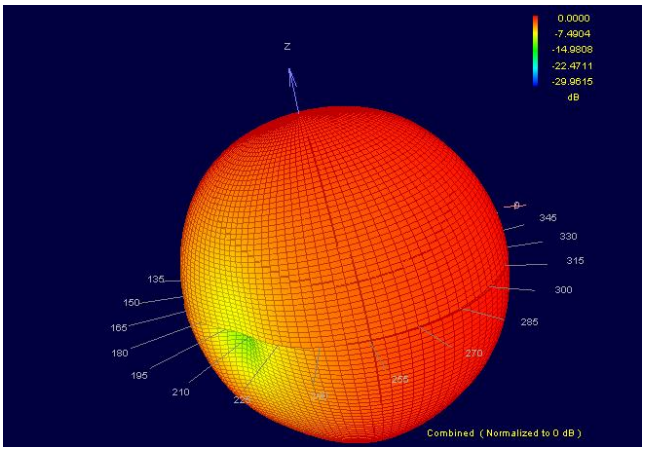
Figure 5.4 Antenna Impedance

5.4. Antenna Efficiency and Radiation Patterns

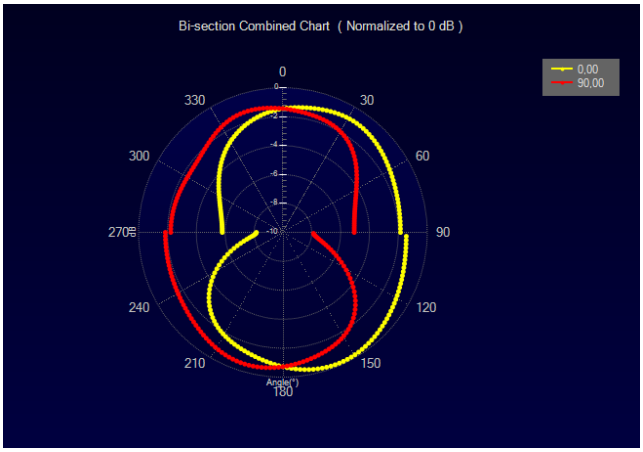
The antenna efficiency, radiation patterns of the on-board printed antenna and the total radiated power of the BLE module have been measured by using the RFxpert measuring equipment. It also plots the realized gain and maximum EIRP values, but these parameters have also been checked in radiated measurements in an anechoic RF chamber and will be presented later in this document.

Table 5.2 RFxpert measurement results

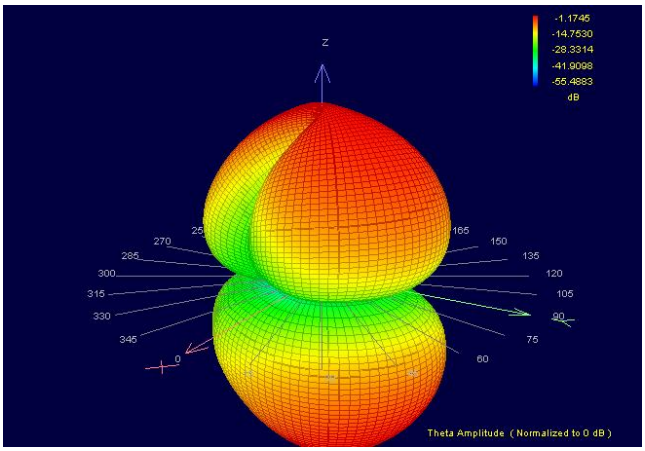
Power Settings	Frequency	Antenna Efficiency	Realized Gain	TRP	EIRP
Setpower 85	2402 MHz	**-2.55 dB**	+0.37 dBi	**+5.05 dBm**	+7.97 dBm
	2440 MHz	**-2.08 dB**	+0.75 dBi	**+5.62 dBm**	+8.45 dBm
	2480 MHz	**-2.45 dB**	+0.58 dBi	**+5.25 dBm**	+8.28 dBm



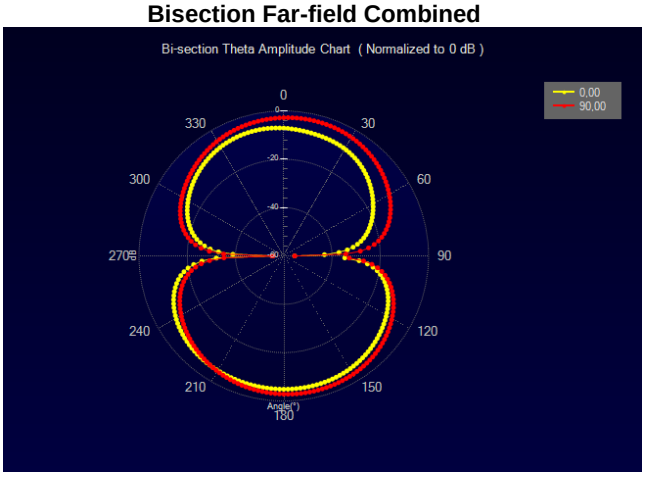
3D Far-field Combined



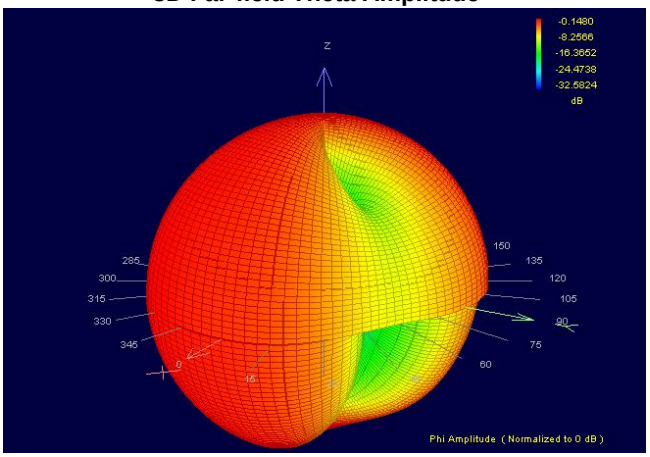
Bisection Far-field Combined



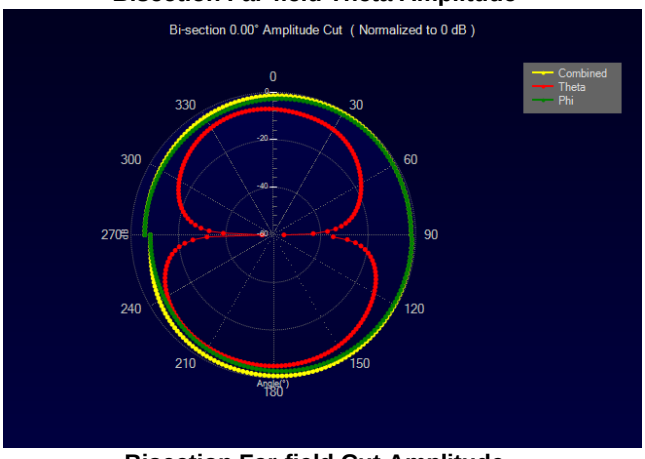
3D Far-field Theta Amplitude



Bisection Far-field Theta Amplitude



3D Far-field Phi Amplitude



Bisection Far-field Cut Amplitude

Figure 5.5 RFxpert Far-field plots at 2440 MHz

5.5. Radiated EIRP and Harmonics

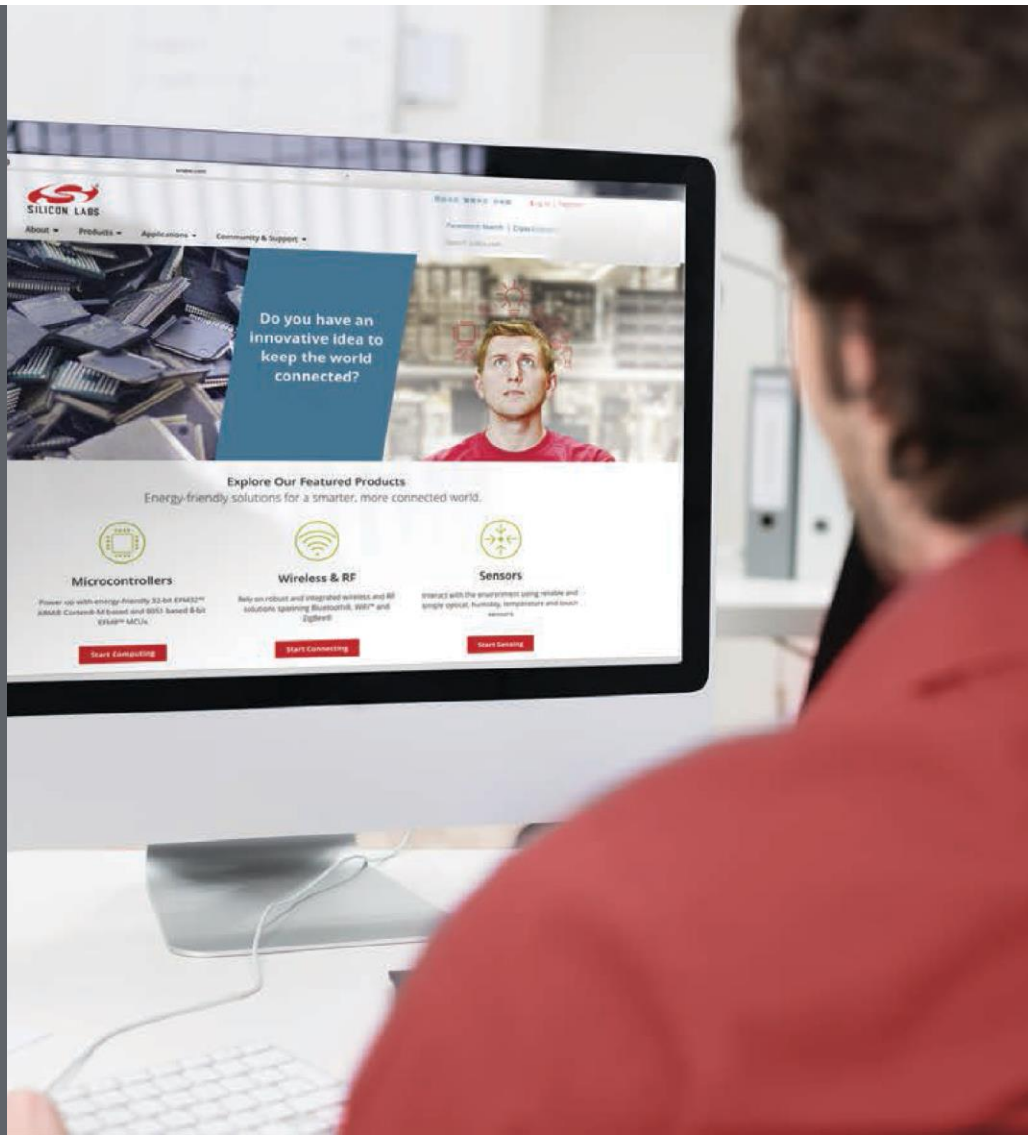
The radiated fundamental EIRP and harmonics of the module have also been measured in an anechoic RF chamber, and the following tables represent the results. The module has been measured in its stand-alone operation mode with a CW tone code running on it. The module was being supplied by a coin cell CR2450 battery.
The reference design module complies with CE and FCC regulatory standards based on the pre-certification tests, but the module does not have any official certification ID owned by Silicon Labs.
The module's maximum antenna gain based on these radiated EIRP measurements is +0.4 dBi.

Table 5.3 Radiated EIRP at 'Setpower 85' full power setting

2440 MHz +8 dBm	Measured maximums of the radiated power in EIRP [dBm]					
	XY		XZ		YZ	
	H	V	H	V	H	V
Fund.	+8.1	-8.1	+0.6	+5.7	+3.5	+7.3
H2	-57.4	-56.6	-53.2	-55.7	-57.9	-53.0
H3	-41.8	-42.6	-42.2	-43.8	-44.0	-44.2
H4	-52.7	-52.2	-52.2	-52.2	-52.2	-52.2
H5	-40.2[1]	-38.3[1]	-42.0	-36.3[1]	-36.6[1]	-41.1[1]

Note 1: Based on the pre-certification testing this fails in CW mode with peak detector but should be compliant with worst-case margins of 1.5 dB when applying modulated signal with AVG detector allowed by FCC.

Smart.
Connected.
Energy-Friendly.



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com