EFR32xG22 Low-Cost Design Reference Manual

Silicon Labs provides customers with a low-cost, stand-alone, battery-powered reference design for EFR32xG22 designs. This document describes the low-cost reference design and provides the RF measurement results for reference. The design files such as the schematic and layout in CAD format, bill-of-material (BOM), PDFs, and Gerbers are available on the Silicon Labs website at https://www.silabs.com/support/resources.
The low-cost reference design utilizes an EFR32xG22 chip in a QFN32 package. It is pre-compliance tested and appears to be compliant with ETSI and FCC regulatory standards.

KEY POINTS

- Brief description of EFR32xG22 low cost reference design
- TX/RX RF performance data that includes conducted and radiated fundamental EIRP and harmonics, antenna impedance, gain, efficiency, and radiation patterns

1. Introduction

To minimize costs at the manufacturing level for EFR32xG22 devices, Silicon Labs designed an EFR32xG22 QFN32-based, 2-layer reference design board that is virtually available to customers at https://www.silabs.com/support/resources since there is no orderable part number for the board design. The minimal BOM solution presented in the application note, AN933.2: EFR32 Series 2 Minimal BOM, is also applicable to the 2- layer EFR32xG22 reference design, so this makes the 2-layer EFR32xG22 reference design with the reduced BOM an effective, low-cost solution for customers to use in their applications. Measurements performed on the 2-layer design with the optimized BOM are also provided in this document.

Note that the schematic design and the measurement results in this document are provided for output power levels up to 6 dBm. The EFR32xG22 part is also capable of transmitting up to +8 dBm output power. However, higher than +6 dBm TX power output will result in higher current consumption and harmonic levels, and the +8 dBm TXP is not guaranteed over temperature and process variations. Contact your local Silicon Labs sales representative to request an AN1353-NDA EFR32xG22 8 dBm Use Case Recommendations application note for more details.

The design utilizes two electrical layers with the minimum number of signal connections required for radio and communication interface, an on-board PCB antenna, a CR2032 coin cell battery for power, and a 10-pin Mini-Simplicity header for programming and debugging purposes (see application note, AN958: Debugging and Programming Interfaces for Custom Designs for pin connections). The board thickness is 0.8 mm and, unlike our typical 4-layer reference designs, the physical size of the 2-layer design is reduced to fit a coin cell battery holder which makes the PCB size approximately 34 x 30 mm.

The default power supply configurations and the power supply filtering follow the EFR32xG22 reference designs (BRD4182A or BRD4183A), whose design files can be found in Simplicity Studio or on the Silicon Labs website.

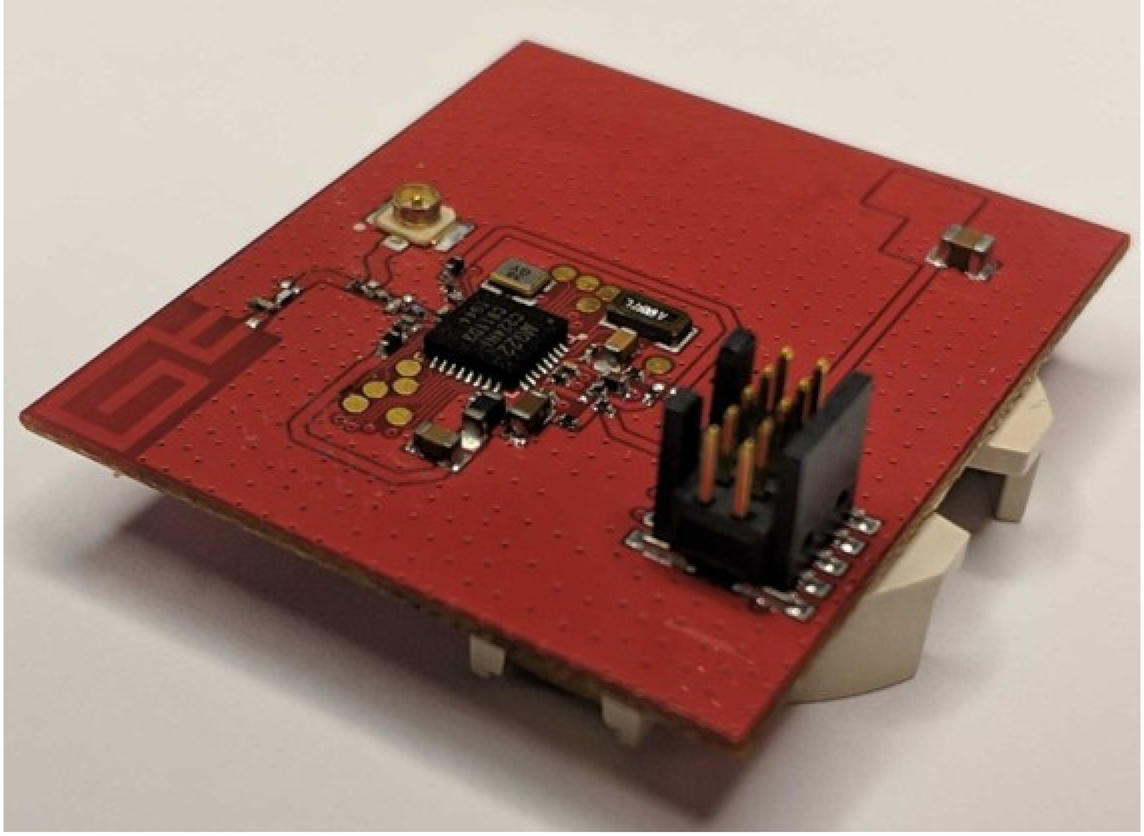


Figure 1.1. EFR32xG22 2-Layer Low-Cost Reference Design

2. Schematic Design

Since this reference manual focuses on the RF design part of the module, this section shows only the RF portion of the entire schematic. The complete design of the EFR32xG22 low-cost reference design is available at https://www.silabs.com/support/resources. The on-chip, dc-dc converter is used to supply both RFVDD and PAVDD to minimize current consumption and maximize battery life. The RF front-end path can be divided into two parts: the EFR32xG22 matching network and the PCB antenna with its antenna matching network placeholder (C17, L4, C19). There are two EFR32xG22 matching network solutions applicable to this design: a 3-element C-L-C Pi network or L-C-L T network plus a series dc-blocking capacitor. Both matching network solutions can be used to achieve up to 6 dBm output power with higher radiated harmonic margins on the latter. The recommended component values for each solution are provided in the table below. For more details regarding matching network approaches and design guidance, see AN930.2: EFR32 Series 2 2.4 GHz Matching Guide.

Table 2.1. RF Matching Network Recommended Component Values

Matching Configuration	Max. Output Power	C1	L1	C2	Z1	Z2
Pi network	6 dBm	1.7 pF	2.7 nH	1.3 pF	18 pF	0 ohm
T network	6 dBm	DNP	2.7 nH	1.2 pF	2.7 nH	18 pF

Although the antenna can achieve a good match to 50 ohms with only a 2-element matching network, the 3-element placeholder allows for flexibility of different matching network topologies (L, C, L-C, C-L), if needed. The design has the option of taking conducted measurements via the U.FL connector (P2 in the figure below) similar to our typical radio boards.

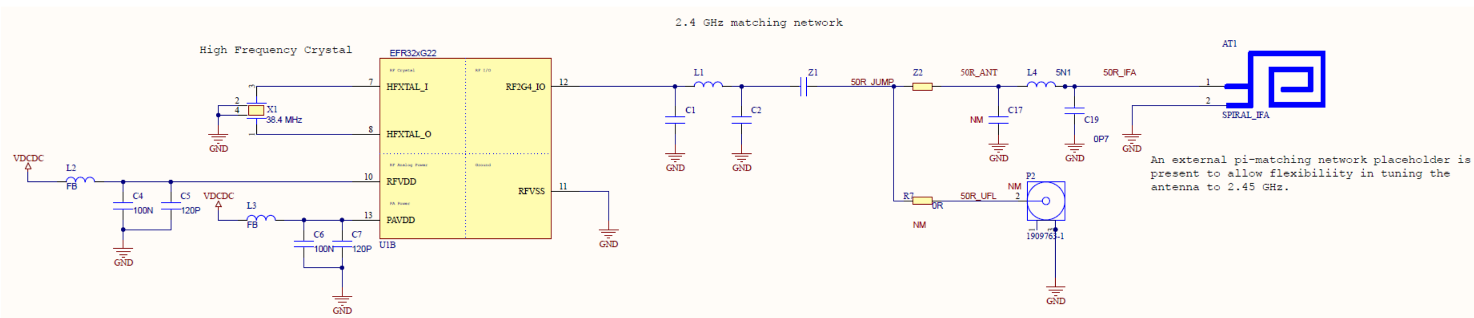


Figure 2.1. RF Portion of the Low-Cost Reference Design

3. Layout Design

The board design follows the generic RF layout recommendations provided in application note, AN928.2: EFR32 Series 2 Layout Design Guide. The top layer consists of all components, excluding the coin cell battery holder, which is placed on the bottom layer of the board. Unlike our typical reference designs which have four electrical layers, this design is comprised of only two electrical layers. So, while dedicating the bottom layer to having a continuous, unbroken ground plane is not possible, a low-impedance return path for currents is ensured on the bottom layer from the antenna and RF match to the RFIC's center ground pad. Additionally, the signals were routed carefully to avoid power supply trace loops on the top layer, minimize traces, and have as much solid ground pour as possible on the bottom layer.

The PCB antenna is a spiral Inverted-F antenna chosen specifically to be used in space-constrained designs. The compact layout shows that the board size can be further reduced in simple designs where the application does not require long RF range and the antenna's performance can be compromised. Note that, although an external antenna matching network is used in this design for antenna tuning, simple dimensional changes such as increasing or decreasing the length of the spiral can be made during the prototyping stage to tune the antenna, if applicable to the design.

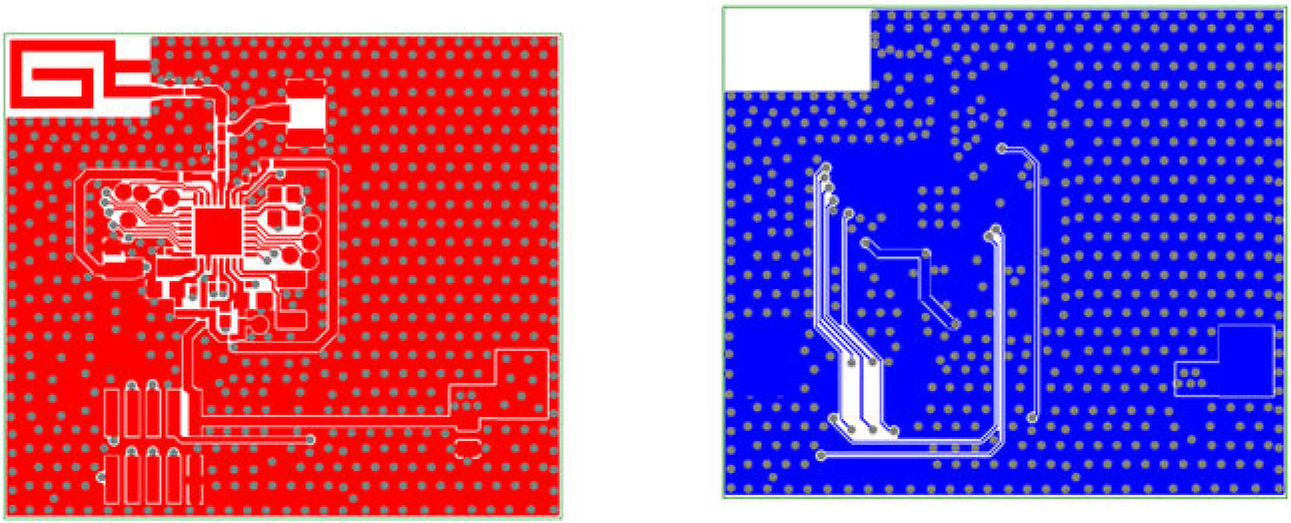


Figure 3.2. 2-Layer Reference Design Layout: Top and Bottom Layer

4. Measurement Results

The TX and RX performance of the 2-layer design was evaluated on two samples – one board with a regular BOM and another board with an optimized BOM for both Pi network and T-network matching configurations. The optimized BOM refers to the minimal BOM presented in AN933.2: EFR32 Series 2 Minimal BOM. The conducted measurements were taken when the EFR32xG22 operated in a stand-alone mode with power supplied using a coin cell battery (CR2032) or via a USB through the WSTK. The radiated measurements were taken only in stand-alone operation mode to avoid unwanted radiation from the cables, which could result in false EIRP or harmonic values.

4.1 Conducted TX Performance

The conducted TX performance results with the regular BOM and the optimized BOM are shown below. For conducted measurements, R6 was removed and R7 was populated with a 0 ohm resistor to take measurements through the U.FL connector. The TX power level was set using RAILtest commands. See UG409: RAILtest User's Guide for more details on how to use RAILtest for testing RF performance. Although the conducted 3rd harmonic looks critical using the Pi network, it should be noted that the radiated 3rd harmonic level complies with the FCC limit, which is only considered for radiated measurements. This will be further discussed in section 4.7 Radiated EIRP and Harmonics of this document.

Table 4.1. Conducted TX Performance Results

Matching Configuration	BOM Configuration	Power Level (raw)	Frequency [MHz]	TXP [dBm]	H2[dBm]	H3 [dBm]	H4 [dBm]	H5 [dBm]
Pi Network	Regular	52	2450	6.20	-68	-35	-56	-42
	Optimized	52	2450	6.00	-65	-36	-56	-43
T Network	Optimized	15	2450	0.5	-59.2	-69.2	-72.7	-72.1
		50		6	-44	-59	-67	-56

4.2 Conducted RX Performance

The conducted receiver sensitivity was checked with Bluetooth LE PHY 1 Mbps 2GFSK at 0.1 % BER (Bit Error Rate).

Table 4.2. Conducted RX Performance Results

Matching Configuration	BOM Configuration	Frequency [MHz]	Sensitivity [dBm]
Pi Network	Regular	2405	-97.70
		2450	-97.90
		2478	-97.80
	Optimized	2405	-97.40
		2450	-97.80
		2478	-96.80
T Network	Regular	2402	-98.1
		2440	-98
		2478	-98.1
	Optimized	2402	-98.2
		240	-97.9
		2478	-98.1

4.3 Antenna Impedance and Return Loss

The measured antenna impedance and return loss of the 2-layer EFR32xG22 design's spiral IFA is shown in the figure below. The measured S11 is considered very good (~-23 dB) at the center frequency 2.45 GHz; however, it is higher than optimal (-10 dB) on the band edges due to the small size of the PCB and antenna reference ground plane being less than quarter wavelength of the 2.4 GHz operating frequency resulting in a narrow bandwidth. Regardless, most of the power from EFR32xG22 is being transferred to the antenna even at the band edges. The antenna impedance has been checked by using a bazooka balun connected as well to avoid current leakage through the connected RF pig-tail cable, which could deteriorate the measurement results. The antenna was tuned on a bare PCB without any assembled components or plastic enclosure, so for custom design implementations with plastics, Silicon Labs recommends checking the antenna impedance as some fine-tuning of the antenna may be needed to achieve the optimal RF performance in its final enclosure.

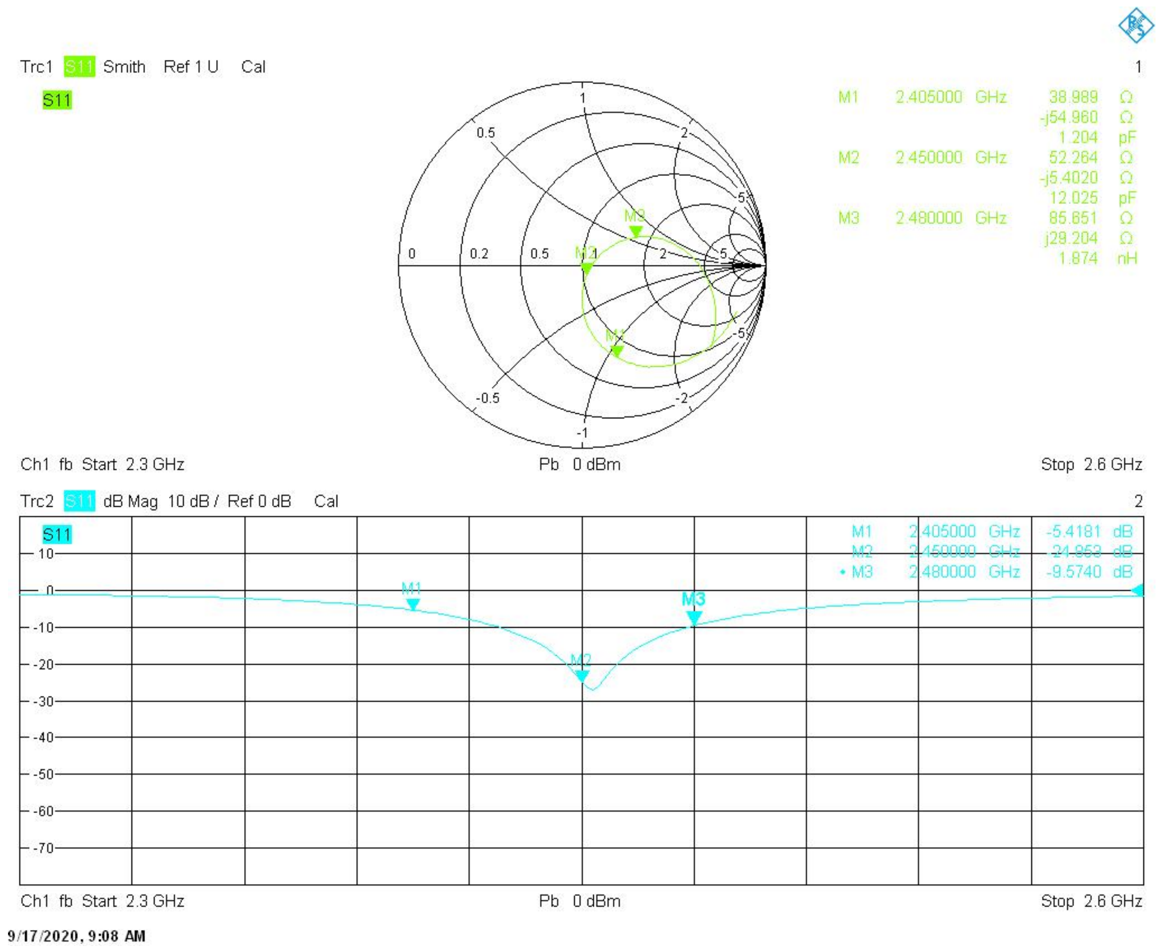


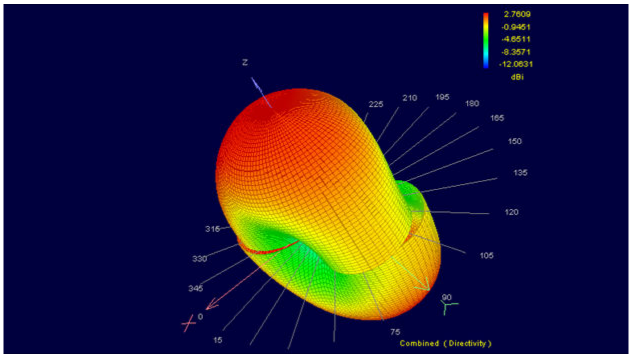
Figure 4.1. Antenna Impedance and Return Loss

4.4 Antenna Efficiency

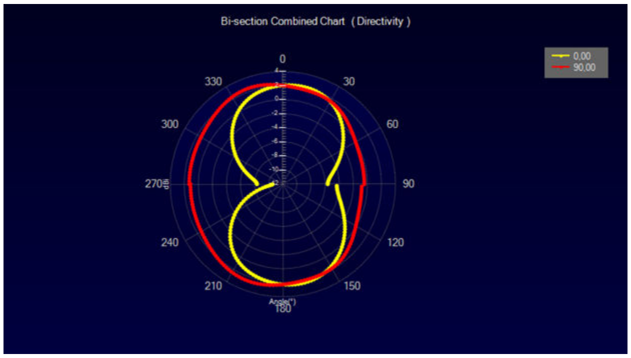
The antenna efficiency of the spiral IFA and the total radiated power of the 2-layer design have been measured using a RFxpert scanner along with the realized gain and the maximum EIRP values. Note that the antenna efficiency at 2405 MHz is lower than the middle and high frequencies of the band, which is reflective of the higher S11 shown in the figure below. This shows that the antenna design or the antenna match network can be further improved for a more consistent performance across the entire frequency band.

Table 4.3. RFxpert Measurement Results

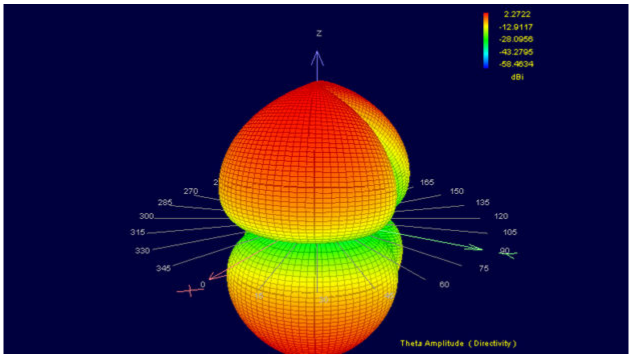
Power Level	Frequency [MHz]	Antenna Efficiency [dB]	Realized Gain [dBi]	TRP [dBm]	EIRP [dBm]
6 dBm PA, 52 raw	2405	-4.6	-2	1.61	4.21
	2450	-2.5	0.25	3.68	6.45
	2480	-2.8	-0.1	3.37	6.1



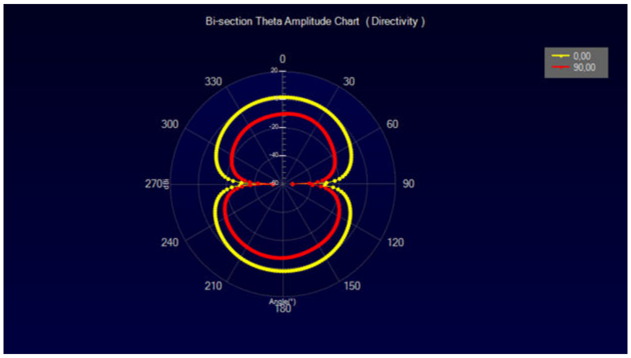
3D Far-Field Combined



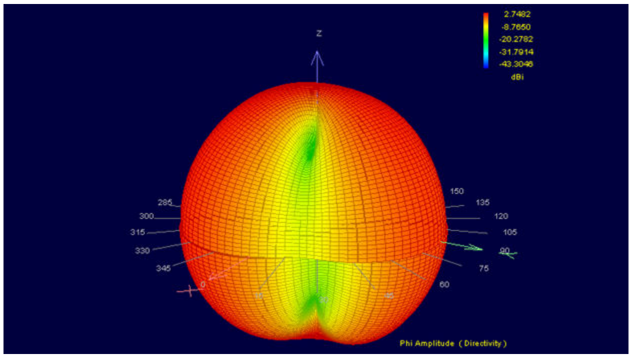
Bisection Far-Field Combined



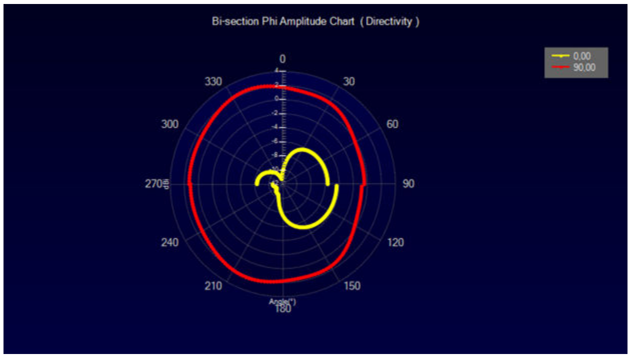
3D Far-Field Theta Amplitude



Bisection Far-Field Theta Amplitude



3D Far-Field Phi Amplitude



Bisection Far-Field Phi Amplitude

Figure 4.2. RFxpert Far-Field Plots at 2450 MHz

4.5 PCB Orientation and Cuts

The following figure shows the orientations and cuts of the PCB used in radiated measurements.

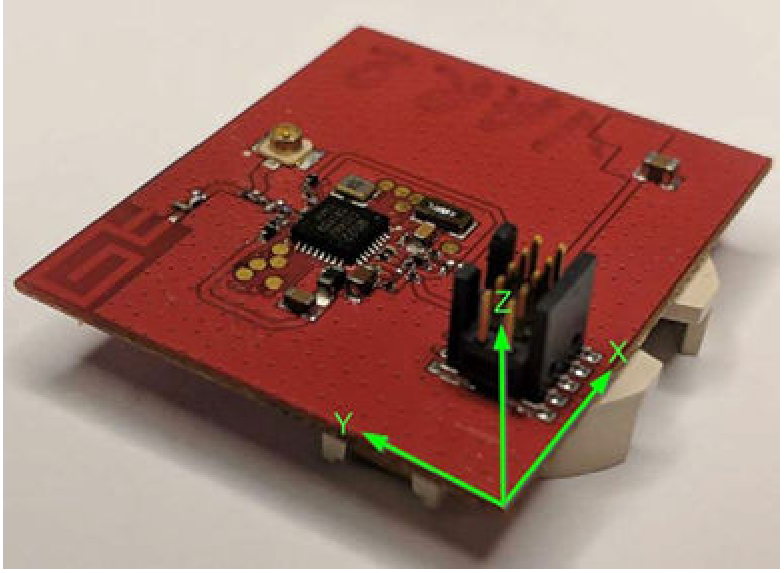


Figure 4.3. PCB Reference Planes used in Radiated Measurements

4.6 Radiation Patterns

The normalized radiation patterns of the reference design have been measured in an anechoic RF chamber and the following plots show the results at 2450 MHz at +6 dBm conducted output power (52 raw power level) using the Pi match.

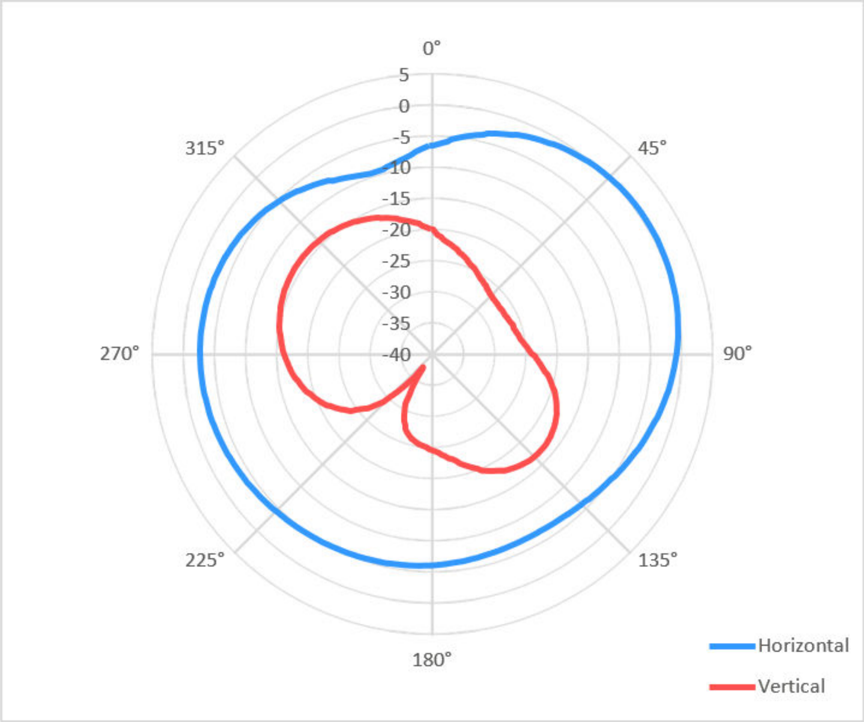


Figure 4.4. Normalized Radiation Pattern, XY Cut, Zero Degree at Y axis, at 2450 MHz

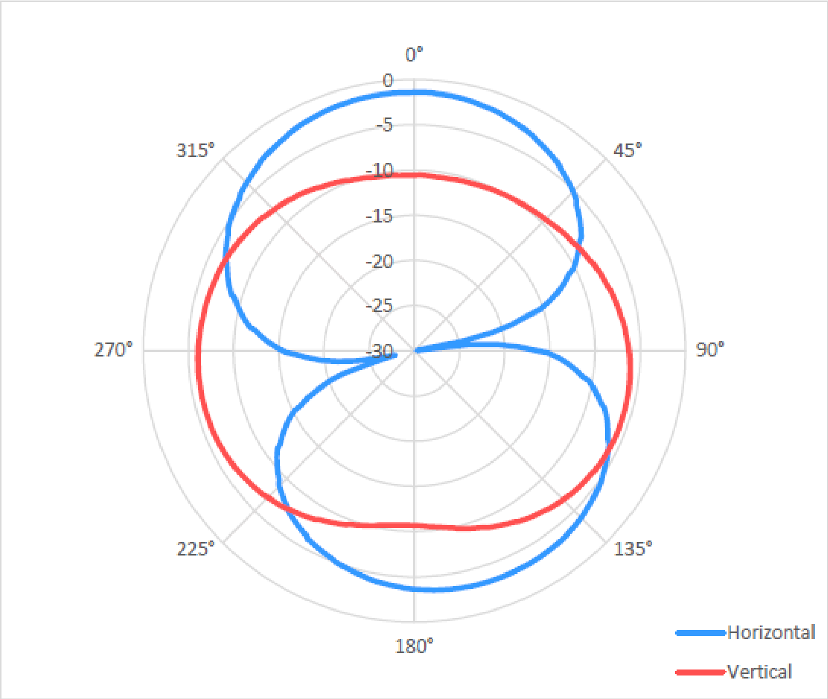


Figure 4.5. Normalized Radiation Pattern, XZ Cut, Zero Degree at Z axis, at 2450 MHz

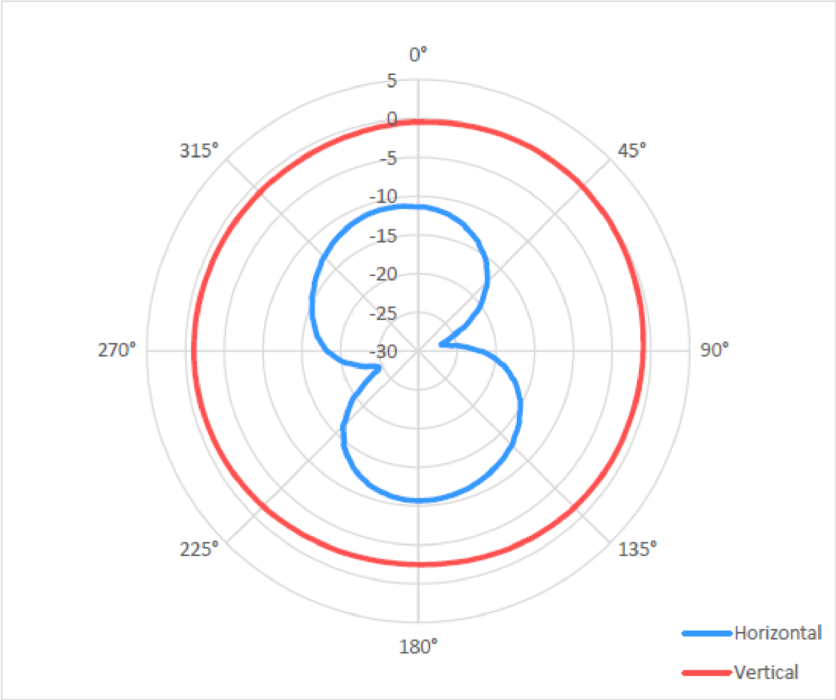


Figure 4.6. Normalized Radiation Pattern, YZ Cut, Zero Degree at Z axis, at 2450 MHz

4.7 Radiated EIRP and Harmonics

The radiated fundamental EIRP and harmonics of the 2-layer reference design using regular and optimized BOM have been measured in an anechoic RF chamber, and the following tables represent the results. The board was operated in a stand-alone mode (power supplied by a coin cell battery) with an unmodulated CW tone transmission at +6 dBm conducted output power setting as determined in section 4.1 Conducted TX Performance of this document.

Table 4.4. Radiated EIRP at + 6 dBm Power Setting using Pi Match

BOM Configuration	Frequency	Measured Maximums of the Radiated Power in EIRP [dBm]					
		XY		XZ		YZ	
		H	V	H	V	H	V
Regular	Fund. (2450 MHz)	4.73	-10.82	5.00	-0.65	-4.68	5.38
	2nd	-55.78	-53.25	-57.26	-49.72	-48.44	-56.44
	3rd	-41.24	-43.34	-45.37	-40.19	-37.91	-45.17
	4th	-50.93	-51.37	-52.08	-51.35	-51.60	-51.63
	5th	-47.11	-46.09	-47.77	-43.92	-44.04	-47.37
Optimized	Fund. (2450 MHz)	5.38	-9.34	4.80	0.38	-4.95	5.80
	2nd	-56.44	-54.51	-57.12	-50.83	-50.18	-56.77
	3rd	-45.17	-43.55	-42.78	-39.56	-37.45	-43.61
	4th	-51.63	-52.03	-50.99	-50.90	-51.09	-51.99
	5th	-47.37	-45.98	-48.01	-45.34	-42.31	-46.75

Table 4.5. Radiated EIRP at + 6 dBm Power Setting using T Match

BOM Configuration	Frequency	Measured Maximums of the Radiated Power in EIRP [dBm]					
		XY		XZ		YZ	
		H	V	H	V	H	V
Regular	Fund. (2450 MHz)	6.38	-13.83	-3.11	6.51	5.3	1.86
	2nd	-47.40	-57.08	-55.39	-47.34	-46.57	-48.76
	3rd	-49.45	-48.94	-43.46	-51.85	-47.88	-45.32
	4th	-52.56	-48.73	-49.80	-49.13	-48.46	-49.97
	5th	-51.38	-44.69	-49.15	-43.31	-42.16	-47.90
Optimized	Fund. (2450 MHz)	7.09	-15.26	-2.28	6.63	4.07	1.69
	2nd	-50.52	-55.05	-51.68	-47.76	-46.17	-51.09
	3rd	-49.33	-48.99	-43.67	-50.88	-49.81	-44.65
	4th	-56.53	-55.15	-53.41	-52.71	-54.10	-54.27
	5th	-48.41	-41.65	-46.90	-39.07	-38.11	-46.19

Although the harmonic values marked in red seem to fail the FCC limit (<-41.2 dBm) in CW mode, they are compliant with at least 1 dB margin when applying a modulated signal and measured using average detector mode in the spectrum analyzer. Additionally, FCC allows the use of duty cycle correction factor (DCCF) on devices with protocol-limited duty cycles, so this gives even more margin on the harmonic levels where the worst case (highest operational) duty cycles for 802.15.4 and BLE are 66% and 98%, respectively.

Based on these results, the 2-layer, low-cost reference design for EFR32xG22 complies with both FCC and ETSI regulatory standards, however, the board does not have any official certification ID owned by Silicon Labs.

5. Revision History

Revision 0.2

August, 2021

- Added measurement results of T match.

Revision 0.1

December, 2020

- Initial release.

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