

# Failsafe ECU through dynamic partial-reconfiguration in FPGAs

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# **1 Introduction**

Brief overview, problem statement and final outcome.

## **1.1 Required Tools and packages**

- Vivado 2018.3
- Vivado 2018.2
- uVision 5 (Windows only)
- ARM Keil (Windows only)
- ARM Cortex M1 IP for Vivado

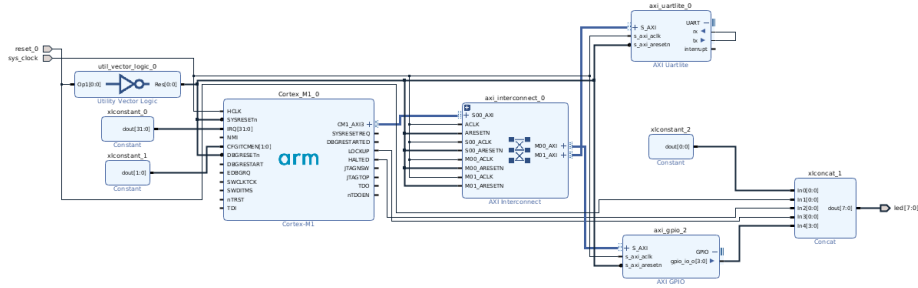


Figure 1: Block Diagram of the partial reconfiguration functionality

## 2 Cortex M1 / M3

Description of the setup of Cortex M1 and Cortex M3 Cores. [1] [2]

### 2.1 Usage of the Keil Toolchain

Link to tutorial enough? Maybe most basic steps (e.g. adaption of arty project for our needs). [3]

### 2.2 Usage of Cortex M1 in Vivado

Only global implementation / synthesis runs are permitted to obtain a working bitstream. If OOC (Out of Context) runs are used, everything except for the Cortex M1 will work fine. The Cortex M1 will enter a hard-fault state which does not allow recovery. This is indicated by a high bit on the *Lockup* port of the processor.

Also trivial, follow tutorial that is provided on ARM Website and adapt to own needs.

#### 2.2.1 Code via Memory Initialization File

File is bound to synthesis process, how to change it...

### 2.3 How to mbed OS

How was the Cortex M1 Project adapted to support the Mbed OS? What is gained through the usage of mbed OS?

## **2.4 Implemented Functionality on the Cortex M1**

How are the UART and IIC peripherals supported in the source code, which libraries are used, interrupt based or not, performance?

Show highlights of the code?

## **3 Bus and Peripherals**

### **3.1 Used Peripherals**

What Peripherals were used (Cortex M1/M3 Boards, which ones).

How to program / use them (only brief).

How are they connected to the Bus?

IIC and UART here or in next section.

### **3.2 Bus**

How is it set up?

Made assumptions?

Document used / invented protocol.

## **4 Partial Reconfiguration**

What is partially reconfigured - Cortex, uart, IIC.

Why not use AXI?

### **4.1 Integration Overview**

[4], [5] Usage of ICAP.

How is the Zynq still used - Loading images and binary blobs from sd card into DDR.

### **4.2 Packaged IP**

Why is the PR IP Packaged, how was it done? [?]

## 5 Organization

### 5.1 Assigned Sub-Tasks

#### 5.1.1 Cortex M1

Evaluation of the provided Cortex-M1 from ARM and adaption of the provided toolchain to our needs.

Creation of a working stand-alone example, creation and integration of working IP-Packages for the Cortex-M1

#### 5.1.2 Partial Reconfiguration

#### 5.1.3 Bus Design

#### 5.1.4 Hardware

### 5.2 Estimated Contribution

Contribution to the project was roughly the same for each group member.

Name	Cortex M1	Partial Reconfiguration	Bus Design	Hardware	mbed OS
Andreas Hirtenlehner	X			X	X
Constantin Schieber	X	X			
Peter Schober	X	X			
Rupert Schorn			X	X	X

## References

- [1] ARM, “Arm® Cortex®-M1 DesignStart™ FPGA-Xilinx edition User Guide,” 2018. [Online]. Available: [https://static.docs.arm.com/100211/0001/arm\\_cortex\\_m1\\_designstart\\_fpga\\_xilinx\\_edition\\_ug\\_100211\\_0001\\_00\\_en.pdf?\\_ga=2.121336076.523725493.1550477241-1711067005.1549732081](https://static.docs.arm.com/100211/0001/arm_cortex_m1_designstart_fpga_xilinx_edition_ug_100211_0001_00_en.pdf?_ga=2.121336076.523725493.1550477241-1711067005.1549732081)
- [2] —, “Cortex-M1 Technical Reference Manual.” [Online]. Available: [https://static.docs.arm.com/ddi0413/d/DDI0413D\\_cortexm1\\_r1p0\\_trm.pdf](https://static.docs.arm.com/ddi0413/d/DDI0413D_cortexm1_r1p0_trm.pdf)
- [3] “Getting Started.” [Online]. Available: <http://www2.keil.com/mdk5/install>
- [4] Xilinx, “Vivado Design Suite User Guide: Partial Reconfiguration (UG909),” 2018. [Online]. Available: [https://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2018\\_3/ug909-vivado-partial-reconfiguration.pdf](https://www.xilinx.com/support/documentation/sw_manuals/xilinx2018_3/ug909-vivado-partial-reconfiguration.pdf)

- [5] —, “Vivado Design Suite Tutorial: Partial Reconfiguration (UG947),” 2018. [Online]. Available: [https://www.xilinx.com/content/dam/xilinx/support/documentation/sw\\_manuals/xilinx2018\\_3/ug947-vivado-partial-reconfiguration-tutorial.pdf](https://www.xilinx.com/content/dam/xilinx/support/documentation/sw_manuals/xilinx2018_3/ug947-vivado-partial-reconfiguration-tutorial.pdf)