

Failsafe ECU through Dynamic Partial Reconfiguration in FPGAs

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Abstract

In this lab, fail-safe mechanisms for Electronic Control Units (ECUs) are explored on the basis of Partial Reconfiguration (PR) in Field Programmable Gate Arrays (FPGAs). The introduced design contains typical characteristics of an automotive system. Communication between the different sub-systems is realized by a specific link (including protocol) and connects the FPGA to the ECUs that handle operations during normal conditions. ECUs are monitored by a bus monitor in the FPGA for nominal operation characteristics and can be replaced by the instantiation of the very same ECU within the FPGA in case of failure.