Clock, and SR, JK, and D Flip-flops

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1 Clock

A "clock" is a signal that periodically tells when a sequential circuit should process an input and adjust the outputs, and when it should remain in the current state. A sequential circuit may be:

- **edge-triggered**: it transitions after reaching a raising OR falling edge
- **level-triggered**: it transitions when signal is low OR high.

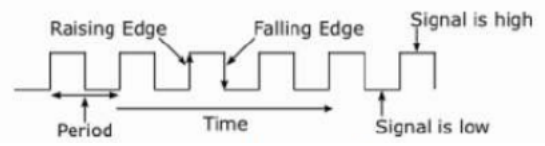
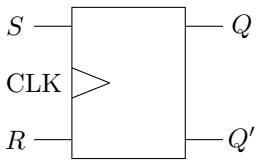


Figure 1: Clock

2 Flip-flops

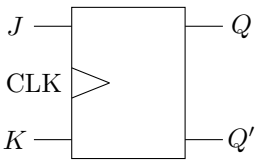
A "flip-flop" is a digital circuit that can store and remember a single bit of information. In ELEC1601, we learn three types of flip-flops: (1) SR flip-flop, (2) JK flip-flop, and (3) D flip-flop. Below are the diagrams and transition tables for each.

SR flip-flop



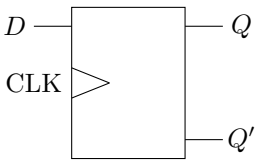
S	R	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	Invalid

JK flip-flop



J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	$(Q_t)'$

D flip-flop



D	Q_{t+1}
0	0
1	1

NOTE: Q_{t+1} denote the future state of Q that the circuit ought to transition to given input values and after reaching a raising edge of the clock.

Flip-flops have the property that its output Q and Q' are (supposedly) opposites of one another at any time. Most flip-flops are **"edge-triggered"**, so its outputs Q and Q' transition under 2 circumstances: (1), we are given input values ie. S & R, J & K, or D, and (2) we have reached the **raising edge of the clock**.

2.1 SR flip-flop architecture

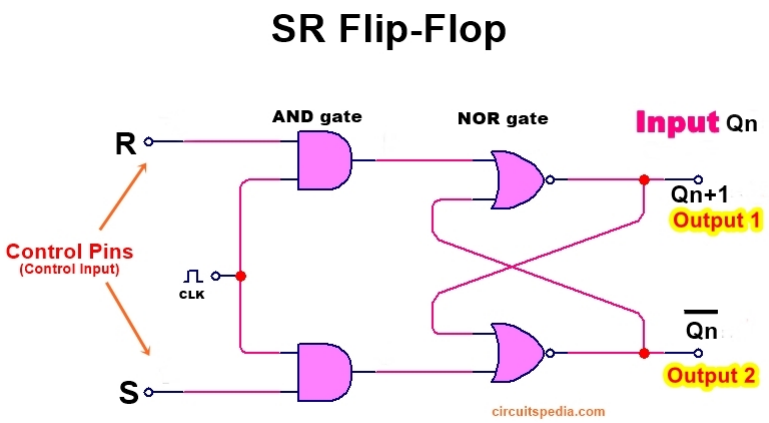


Figure 2: SR flip-flop architecture
Source `https://circuitspedia.com/wp-content/uploads/2021/04/SR-flip-flop-circuit-diagram-1.jpg`

2.2 JK flip-flop architecture

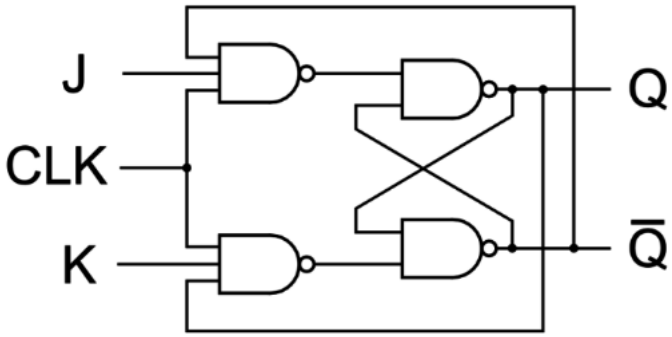


Figure 3: JK flip-flop architecture
Source: `https://i0.wp.com/s3.amazonaws.com/dcaclab.wordpress/wp-content/uploads/2020/01/20202426/JK1.png?fit=532%2C274&ssl=1`

2.3 D flip-flop architecture

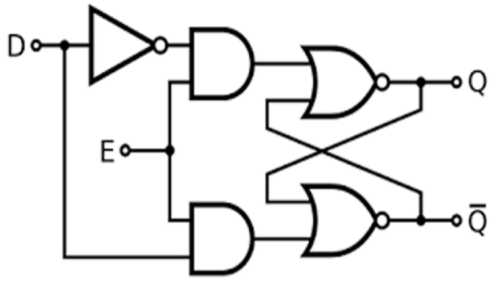


Figure 4: D flip-flop architecture
Source: https://www.knowelectronic.com/wp-content/uploads/2021/11/D-Flip-Flop-Circuit-Truth-Table.png