Cascode Miller-Compensated Three-Stage Amplifier

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Abstract

Silicon technology advancement calls for decrease in transistor size, and as a by-product, the source voltage is also decreasing. Under this circumstance, traditional cascode amplifiers are no longer suitable for achieving high gain and high stability. In the paper, we investigated several historical three-stage amplifier designs and later analyzed the best among them, the CLIA, with manual analysis and numeric simulation.

Introduction

As silicon technology develops, the size of each transistor on a chip decreases by a certain fixed divider every one or two generations. To keep the internal electric field relatively unchanged so that transistors are not so vulnerable to breakdown in case of a sudden voltage spike due to noise and external environmental changes, the source voltage V_{DD} has to decrease according to the size.

However, this brings a problem: As traditional cascode amplifiers have been heavily dependent on a high source voltage to work properly and to provide high voltage gain, those amplifiers have to be redesigned to work under low and ultra-low source voltage. That is where three-stage amplifiers come to the front stage. As [2][3] show, three-stage amplifiers can work better than cascode amplifiers in terms of power efficiency and bandwidth.

As everything has its pros and cons, three-stage amplifiers have its own drawbacks as well. That is, since a three-stage amplifier has three stages, every stage introduces a pole, which makes the whole amplifier a 3-pole system, thus brings about severe potential vulnerabilities concerning stability. Since then, researchers have been actively exploring various frequency compensation techniques to make the most of the advantages brought by three-stage amplifiers, such as power efficiency and bandwidth, but without touching its Achilles' Heel, such as potential instability. The mainstream solutions can be put into the following categories:

- Nested Miller compensation (referred to as NMC), as shown in [4]
- Damping-factor-control frequency compensation (referred to as DFCFC), as shown in [2]
- Simple Miller compensation (referred to as SMC), as shown in [2]
- Cross feed-forward cascode compensation (referred to as CFCC) ,as shown in [3]

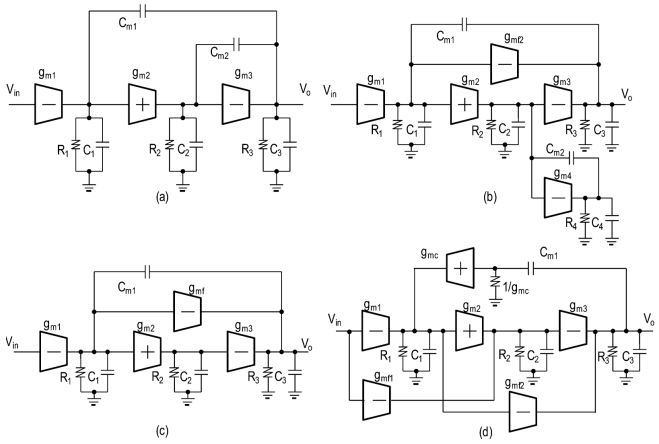

Figure 1: (a) NMC, (b) DFCFC, (c) SMC, (d) CFFC

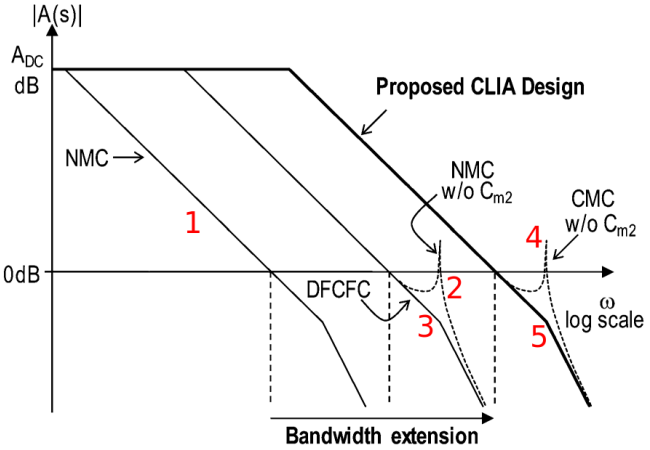

Figure 2: Comparison of the frequency responses of the 4 structures. 1 is NMC, 2 is NMC, 3 is DFCFC, 4 is CMC and 5 is our proposed design CLIA.

As Figure 2 shows, there exists a clear evolution path from NMC to CMC. NMC (shown in Figure 2 as curve 1), which nevertheless has the simplest compensation structure and has a low Q-factor, has a big problem in its unbearably small bandwidth, smaller even than single-stage and two-stage amplifiers. To solve the bandwidth trouble, the inner loop is removed, an inverse amplifying stage is added and parallelled to the previously existing outer loop compensation capacitor C_{m1}, and thus the bandwidth is greatly improved (shown in Figure 2 as curve 2).

However, the evolved structure experiences a high Q-factor and thus introduces instability if not configured properly. To control Q-factor, a damping-factor control unit is parallelled to the output node of the 2nd stage, and thus the structure evolved into DFCFC (shown in Figure 2 as curve 3).

Later, an even higher bandwidth is required, so the outer compensation loop inherited from the ancient SMC has to be replaced with a cascode Miller compensation (CMC) unit to boost bandwidth. Again, the Q-factor introduces vulnerabilities to instability, and it is time to present our proposed design CLIA [1].

CLIA Structure Explained

This section is managed in the following manner: First, the small-signal structure is presented and qualitatively, quantitatively analyzed. Second, the circuit that implements the small-signal structure is presented and quantitatively analyzed.

A. Small-Signal Structure

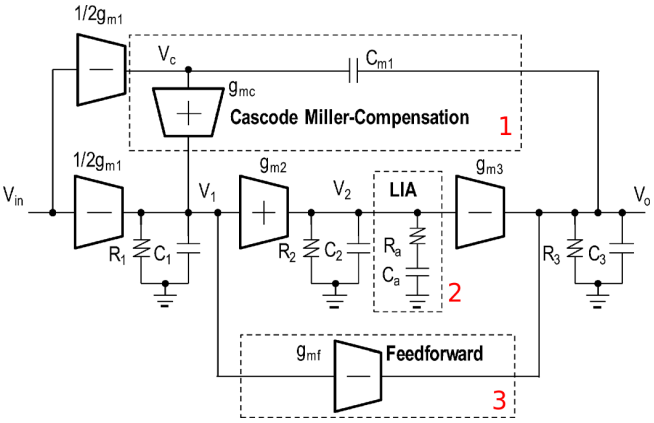

Figure 3: Small signal model of CLIA amplifier. 1 is a cascode Miller compensation unit, 2 is an RC network and 3 is a feed-forward path.

The small-signal structure is presented as Figure 3. The 3 compensation blocks have been marked as 1, 2, 3.

The CMC unit (marked as block 1 in Figure 3), is inherited from CMC amplifiers and is used to eliminate the feed-forward signal path in SMC thus to extend the bandwidth.

The local impedance attenuation (LIA) block (marked as block 2 in Figure 3) is a parallel compensation unit that consists of a series of R_a and C_a. Its purpose is to reduce the high-frequency small-signal output resistance at the 2nd stage, and later in the qualitative analysis, one can see that the complex poles are 'dominated' by this LIA unit, which means that the value of R_a and C_a is the deciding factor in positioning the complex poles.

The feed-forward path (marked as block 3 in Figure 3), made up with an inverse amplifier $-g_\mathrm{mf}$, connecting the output of stage 1 and the final output, improves large-signal performance.

B. Small-Signal Transfer Function

To derive the exact transfer function $H(s)$ is a simple task which we have done a thousand of times: First, convert the small-signal circuit into a system of linear equations; Second, feed the system of equations to some symbolic equation solver such as Python Sympy or Matlab. The Proposed Design CLIAhen a few seconds later, you will be presented with the exact transfer function. What a nice thing.

However, despite the fact that our small-signal circuit looks explicit, the exact transfer function is no way simple. Except that the number of poles and zeros can be seen from the greatest exponent, that the DC gain can be derived by substituting s with 0, and that the particular frequency response under a specific configuration can be plotted, nothing else valuable, insightful or interpretable can be derived from this symbolic expression, by us or by the computer. For example, the bandwidth, the phase margin and the gain margin, which are the three most important values in stability analysis, can by no means be revealed from this complex expression.

Thus, appropriate approximation to this small-signal transfer function is crucial. Based on the following 2 presumptions, it is believed that our transfer function can be reduced to a reasonable size, but without losing too much accuracy:

- The gain of every single stage is way much greater than 1
- Compensation capacitors $C_\mathrm{m1}, C_\mathrm{a}$ and output node capacitor C_3 are much greater than internal output node capacitor C_1, C_2

$$H(s) \approx \frac{g_\mathrm{m1}\,g_\mathrm{m2}\,g_\mathrm{m3}\,R_1\,R_2\,R_3\,(1+sR_\mathrm{a}C_\mathrm{a})}{(1+sg_\mathrm{m2}\,g_\mathrm{m3}\,R_1\,R_2\,R_3\,C_\mathrm{m1})(1+skR_\mathrm{a}C_\mathrm{a})} \cdot \frac{1+s\frac{C_\mathrm{m1}}{2g_\mathrm{mc}}}{1+s\frac{C_1C_3}{kg_\mathrm{m2}\,g_\mathrm{m3}\,R_\mathrm{a}C_\mathrm{m1}}+s^2\frac{C_1C_3}{kg_\mathrm{m2}\,g_\mathrm{m3}\,g_\mathrm{mc}R_\mathrm{a}}}$$

where k is defined as

$$k = 1 + \frac{C_3}{g_\mathrm{m2}\,g_\mathrm{m3}\,R_1\,R_\mathrm{a}\,C_\mathrm{m1}}$$

from Equation 1, we can derive that the system has 2 zeros z_1, z_2, and 4 poles p_0, p_1, p_{21}, p_{22} with p_{21}, p_{22} paired as conjugate poles (they share the same real value and their imagine values are opposite). We can also conclude that the DC gain is

$$A = g_\mathrm{m1}\,g_\mathrm{m2}\,g_\mathrm{m3}\,R_1\,R_2\,R_3 \tag{2}$$

Ordered by their distance to the real axis, the zeros in their symbolic form are

$$\begin{cases} z_1 = -\dfrac{1}{R_a C_a} \\ z_2 = -\dfrac{2g_{mc}}{C_{m1}} \end{cases} \text{or} \begin{cases} z_2 = -\dfrac{1}{R_a C_a} \\ z_1 = -\dfrac{2g_{mc}}{C_{m1}} \end{cases}$$

Actually, we do not know which zero is closer to the real axis.

For poles, their relative distance to the real axis is more explicit, at least the fact is clear that this system has a pole very close to the real axis.

$$\begin{cases} p_0 = -\dfrac{1}{g_{m2} g_{m3} R_1 R_2 R_3 C_{m1}} \\ p_1 = -\dfrac{1}{k R_a C_a} \\ p_{21}, p_{22} = -\dfrac{g_{mc}}{2C_{m1}} \\ \qquad \pm \sqrt{\dfrac{g_{mc}^2}{4C_{m1}^2} - \dfrac{g_{m2} g_{m3} g_{mc} R_a}{C_1 C_3}} \end{cases}$$

and p_1 and p_{21}, p_{22} seem to be close to each other as well.

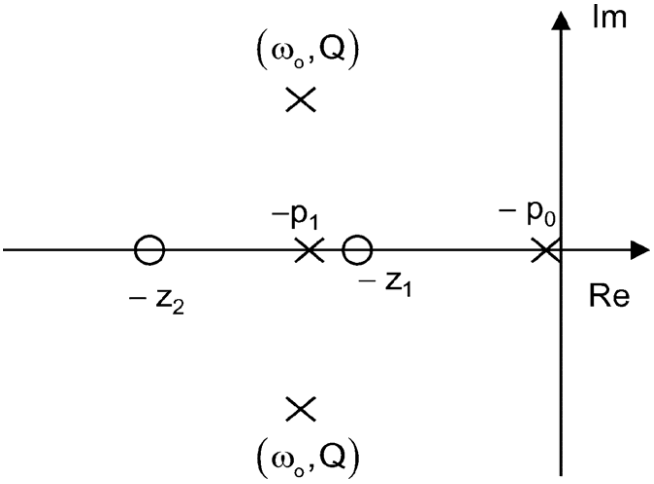

Figure 4: Zeros and poles illusion plot

However, this is not the whole story. Note that z_1 and p_1 differ from each other by only a factor k, and this might give us a hint to perform a pole-zero cancellation approximation, since if $k \approx 1$, z_1 and p_1 can be considered close enough to each other that they almost collide. In fact, we find it feasible, because based on presumption 2, $C_3 \approx C_{m1}$, so they can reduce each other

$$k \approx 1 + \frac{1}{g_{m2} g_{m3} R_1 R_a}$$

and based on presumption 1, $g_{m2} g_{m3} R_1 R_a \gg 1$, so

$$k \approx 1$$

so we removed p_1 and z_1. It is time to update our list of zeros and poles

$$\begin{cases} z_2 = -\dfrac{2g_{mc}}{C_{m1}} \\ p_0 = -\dfrac{1}{g_{m2} g_{m3} R_1 R_2 R_3 C_{m1}} \\ p_{21}, p_{22} = -\dfrac{g_{mc}}{2C_{m1}} \\ \qquad \pm \sqrt{\dfrac{g_{mc}^2}{4C_{m1}^2} - \dfrac{g_{m2} g_{m3} g_{mc} R_a}{C_1 C_3}} \end{cases}$$

so at last our final version of transfer function is given as

$$H(s) \approx \frac{g_{m1} g_{m2} g_{m3} R_1 R_2 R_3}{1 + s g_{m2} g_{m3} R_1 R_2 R_3 C_{m1}} \cdot \frac{1 + s\frac{C_{m1}}{2g_{mc}}}{1 + s\frac{C_1 C_3}{g_{m2} g_{m3} R_a C_{m1}} + s^2 \frac{C_1 C_3}{g_{m2} g_{m3} g_{mc} R_a}}$$

C. Circuit Implementation

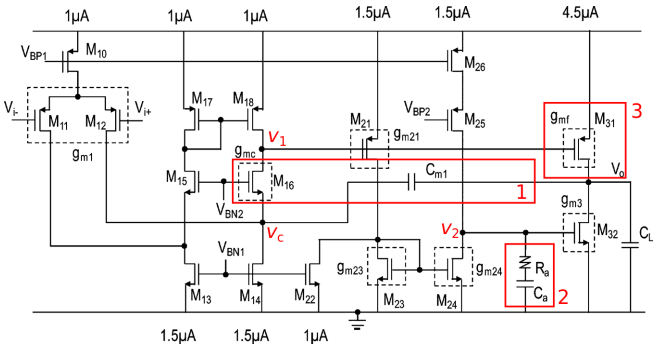

Figure 5: Circuit implementation

The small-signal structure shown in Figure 3 can be implemented by the circuit shown in Figure 5.

M11 and M12 are the input differential pair, and they implement the 1st amplifying stage g_{m1} in the small-signal structure. M16 is the cascode transistor, implementing the non-inverting amplifying stage g_{mc} in the cascode Miller compensation unit. M21, M23 and M24 implement the 2nd stage. Assuming their small-signal transconductance as $g_{m21}, g_{m23}, g_{m24}$, the 2nd stage transconductance in Figure 3 can be expressed as $g_{m24}(g_{m21}/g_{m23})$. M32 implements the 3rd amplifying stage. g_{m3} is just g_{m32}. M31 implements the inverting amplifying stage in the feed-forward path, and its transconductance g_{m31} is g_{mf} in the small-signal structure Figure 3

CLIA Structure in Simulation

A. Under Default Configuration

Paper [1] provides a table of reference sizes for MOSFETs and reference values for compensation components under $0.13\,\mu\text{m}$ CMOS technology. Since in this assignment, we are given a $0.18\,\mu\text{m}$ technology, these reference values may or may not work as

properly as they do in $0.13\,\mu$m technology, but these values can be a good start point for us.

First, we did the AC simulation directly to see if we are fortunate enough to get these values working under a $0.18\,\mu$m technology. However, we are not so lucky. The frequency response is wrong in every way.

So, it is necessary to check each MOSFET, particularly their working region, because if they are working under linear region, they are unable to amplify. After performing the DC simulation, several transistors, including M24, M31 and M32, are identified as not working inside saturation region. After modifying their sizes to force all of them work inside saturation region, the frequency response becomes identifiable.

	size	$g_{\mathrm{m}}(\mu\mathrm{S})$	$g_{\mathrm{ds}}(\mathrm{nS})$	$C_{\mathrm{gd}}(\mathrm{fF})$	$C_{\mathrm{gs}}(\mathrm{fF})$
M10	$2\times(1/2)$	8.80938	619.421	1.17701	22.8149
M11, M12	2/6	3.94907	4.62336	0.648892	67.5331
M17, M18	2/1	12.9689	59.8375	0.654176	11.0746
M15, M16	1/1	17.4262	65.7085	0.363902	3.49798
M13, M14	$3\times(0.4/3)$	17.227	36.4562	0.441493	17.5244
M21	2/0.2	71.4606	1.00908	0.64713	2.38718
M22	$2\times(0.4/3)$	11.4982	22.248	0.292293	11.6797
M23	0.5/0.5	45.158	433.669	0.181136	1.42163
M24	0.5/1.7	15.604	39.5246	0.181004	4.31675
M25	$3\times(1/1)$	18.391	149.558	1.00926	17.0732
M26	$3\times(1/2)$	14.2963	41.5098	0.984962	34.0196
M31	$3\times(4/0.2)$	403.09	7.61647	3.89339	14.2498
M32	4/5	108.471	177.722	1.48874	109.293

Table 1: MOSFET sizes used in simulation, transconductance g_{m} and drain-source small-signal resistance r_{ds} derived from DC simulation

C_{L}	560 pF
R_{a}	250 kΩ
C_{a}	0.3 pF
C_{m1}	0.5 pF

Table 2: Values for compensation components

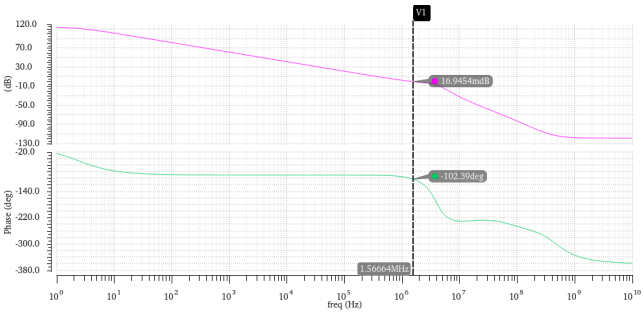

Figure 6: Simulated frequency response

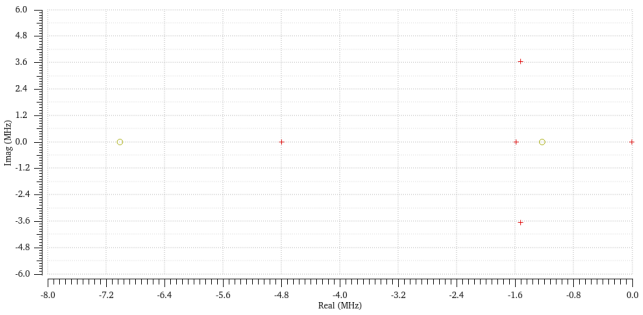

Figure 7: Simulated zeros and poles

From Figure 7, zeros and poles can be seen

$$\begin{cases} p_0 = -2.25\,\mathrm{Hz} \\ z_1 = -1.23\,\mathrm{MHz} \\ p_1 = -1.58\,\mathrm{MHz} \\ p_{21}, p_{22} = -1.52 \pm j3.66\,\mathrm{MHz} \\ z_2 = -7.01\,\mathrm{MHz} \end{cases}$$

Origin	**PM(deg)**	**GM(dB)**	**UGF(Hz)**
This work	77.54	7.535	1.571 M
Paper [1]	56.27	6.549	3.519 M

Table 3: Results from simulation

It is important, however, to compare the simulation results with manual analysis. According to the explanation in circuit implementation section, how each MOSFET contributes to each block in small-signal structure is now quite clear. With

$$\begin{cases} g_{\mathrm{m1}} = g_{11} = 3.94907 \cdot 10^{-6} \\ g_{\mathrm{m2}} = \dfrac{g_{\mathrm{m21}}\, g_{24}}{g_{23}} = 2.46895 \cdot 10^{-5} \\ g_{\mathrm{m3}} = g_{\mathrm{m32}} = 108.471 \cdot 10^{-6} \\ g_{\mathrm{mc}} = g_{\mathrm{m16}} = 17.4262 \cdot 10^{-6} \\ g_{\mathrm{mf}} = g_{\mathrm{m31}} = 403.09 \cdot 10^{-6} \end{cases}$$

and with

$$\begin{cases} R_1 \approx r_{\mathrm{ds18}} // r_{\mathrm{ds16}} = 7.965207 \cdot 10^{6} \\ R_2 \approx r_{\mathrm{ds24}} // r_{\mathrm{ds25}} = 5.288693 \cdot 10^{6} \\ R_3 \approx r_{\mathrm{ds32}} // r_{\mathrm{ds31}} = 5.395533 \cdot 10^{6} \end{cases}$$

and with

$$\begin{cases} C_1 \approx C_{\mathrm{gd16}} + C_{\mathrm{gs21}} + C_{\mathrm{gs31}} = 16.63734 \cdot 10^{-15} \\ C_2 \approx C_{\mathrm{gs32}} = 109.293 \cdot 10^{-15} \\ C_3 \approx C_{\mathrm{L}} = 560 \cdot 10^{-12} \end{cases}$$

so under manual analysis, all zeros and poles are

$$
\begin{cases}
z_2 = -\dfrac{2g_{\mathrm{mc}}}{C_{\mathrm{m1}}} = 69.7048\,\mathrm{MHz} \\
p_0 = -\dfrac{1}{g_{\mathrm{m2}}g_{\mathrm{m3}}R_1R_2R_3C_{\mathrm{m1}}} = 3.28567\,\mathrm{Hz} \\
p_{21}, p_{22} = -\dfrac{g_{\mathrm{mc}}}{2C_{\mathrm{m1}}} \\
\qquad \pm \sqrt{\dfrac{g_{\mathrm{mc}}^2}{4C_{\mathrm{m1}}^2} - \dfrac{g_{\mathrm{m2}}g_{\mathrm{m3}}g_{\mathrm{mc}}R_{\mathrm{a}}}{C_1C_3}} \\
\qquad = -17.426 \pm j30.800\,\mathrm{MHz}
\end{cases}
$$

And the DC gain is

$$A = 2.403812\,\mathrm{M} \approx 127.618\,\mathrm{dB}$$

no surprise at all.

And the unity-gain frequency is

$$f_0 = 8.167\,\mathrm{MHz}$$

at f_0, the phase is -176.5729 deg, which means

$$\mathrm{PM} = 96.818\,\mathrm{deg}$$

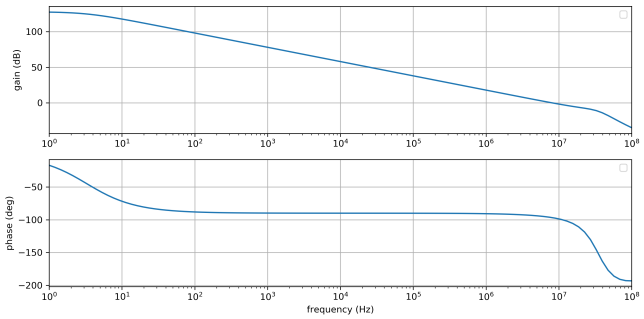

Figure 8: Frequency response from manual analysis

B. C_{L}'s Effect on Frequency Response

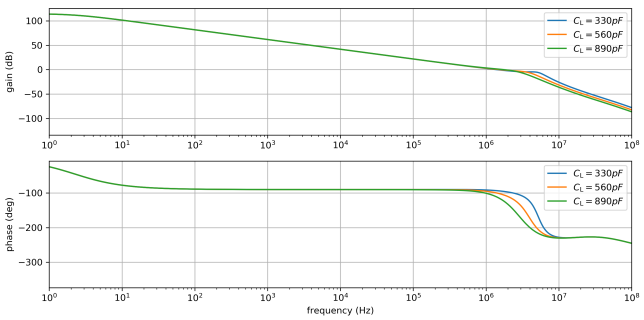

Figure 9: Frequency responses with different C_{L} values

From Figure 9, one can see that greater C_{L} results in smaller PM. Thus, CLIA has a potential vulnerability as well. It does not allow a too big load capacitor, because its stability would otherwise be jeopardized by decreasing PM.

C. R_{a}'s Effect on Frequency Response

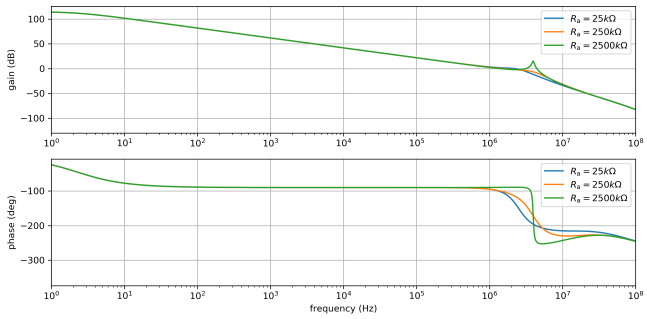

Figure 10: Frequency responses with different R_{a} values

From Figure , one can see that a bigger R_{a} negatively affects PM as well. A bigger R_{a} will boost Q-factor, creating multiple (in this case, 2) unity-gain frequencies f_0.

Conclusion

In this paper, we analyzed the small-signal structure of CLIA amplifier and the circuit that implements CLIA, both in symbolic and simulation. There exist, however, several disagreement between manual analysis and numeric simulation that would require more investigation.

References

[1] M. Tan and W.-H. Ki, "A cascode Miller-compensated three-stage amplifier with local impedance attenuation for optimized complex-pole control," *IEEE J. Solid-State Circuits*

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