

IT7257

Self-Cap Touch Controller for Wearable Device

Preliminary Specification V0.2 (For A Version)

ITE TECH. INC.



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Revision History

Section	Revision	Page No.
_	New package type (32-pin XQFN) added	







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1. Features

Programmable Capacitance-to-digital Converter(CDC)

- 13/22 capacitance sensing pins
- Automatic conversion sequencer
- No external RC components required
- Self-capacitance smart finger detection engine

■ On-chip Automatic Calibration Logic

 Automatic calibration & compensation for environmental change

■ On-chip RAM to Store Calibration Data

- Hardware initialization of SRAM

■ Host Access to SRAM Freely Anytime

■ Powerful Hardware Computer Architecture

- Internal low-power-consumption RISC MCU
- Internal calibrated oscillator
- Internal power-on reset circuit and watch-dog counter

■ Flexible Multi-finger Point Detection

- Supports finger tracking function
- Supports maximum of 2-finger true point detection & gesture

■ Flexible On-Chip Memory

- Internal SRAM for data storage
- Embedded flash for extra program update

Specifications subject to Change without Notice

■ One Dedicated Interrupt Output

■ I2C Compatible Interface

- Compliant to I2C specification v2.1
- Supports slave device only
- Supports standard and fast mode
- Supports immediate read and combined format
- 7-bit device addressing mode

■ Operation Power

- One operation power source 2.8~3.3V
- Provides one internal power regulator for core power generation and sensing driver

■ Low Power Consumption

Active mode: 3mAIdle mode: 200uASleep mode: 2uA

Temperature Range

- -40 °C ~ 85 °C

■ Package

- 24-pin XQFN (3x3x0.55 mm)
- 32-pin XQFN (4x4x0.55 mm)





2. General Description

The IT7257 is a 13/22-channel capacitance sensor detection controller companioned with one ITO film screen module to implement multi-touch functionality. It integrates one single electrode 13/22-channel capacitance-to-digital converter (CDC), one high performance low-power-consumption RISC CPU, flexible memory support, and many powerful hardware functions. The internal CDC has one automatic calibrate and compensates engine to remove effect from environmental change. It also includes one self-learning circuit that can modify the threshold and sensitivity levels automatically to eliminate the impact of different finger sizes so as to optimize the finger touch detection. In addition to one RISC CPU calculating the location of the finger touch and handle all data translation, this chip also includes one special hardware accelerator to speed up the location calculation. The IT7257 supports one interrupt output used to indicate whether the finger location has been changed or some user defined actions. Besides, it supports many flexible internal memory sizes and types, storing the user program and special data to extend special functions in order to meet users' specific requirements.

The IT7257 supports I²C interface only. The serial interface is to communicate with the host. Through these interfaces, the host can program the internal control registers to configure and control the chip to meet users' specific requirements. Additionally, they can help communicate the finger locations and some user specified commands.

The IT7257 is available in 24/32-pad XQFN package. It needs one power 2.8V-3.3V source, and IO voltage level can operate at 1.8V-3.3V.





3. Block Diagram

internal LDO / POR **SRAM** e-flash cache controller Ram OSC Arbiter Interrupt ► INT_N Controller Clock generator Uart 8051 **CPU** Serial IF - SCL Power Mode RESET_N (I2C) Controller data ➤ SDA RAM **Engine** Digital CDC CINs filter Sequence Controller Analog TX Generator Controller IT7257 Watch dog

Figure 3-1. Block Diagram





4. Pin Configuration

Figure 4-1. IT7257 Top View 24-pin XQFN (IT7257AXQN)

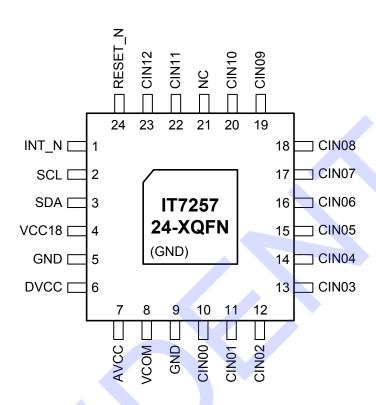


Table 4-1. IT7257AXQN Pins Listed in Numeric Order (24-pin XQFN)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	INT_N	7	AVCC	13	CIN03	19	CIN09
2	SCL	8	VCOM	14	CIN04	20	CIN10
3	SDA	9	GND	15	CIN05	21	NC
4	VCC18	10	CIN00	16	CIN06	22	CIN11
5	GND	11	CIN01	17	CIN07	23	CIN12
6	DVCC	12	CIN02	18	CIN08	24	RESET_N



Figure 4-2. IT7257 Top View 32-pin XQFN (IT7257BXQN)

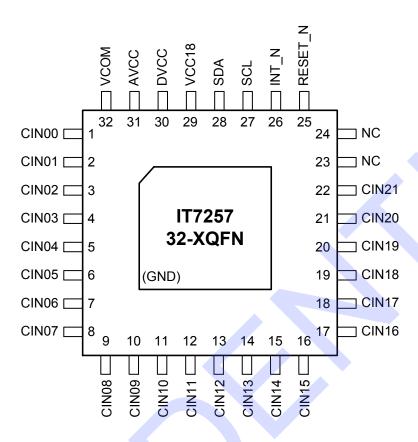


Table 4-2. IT7257BXQN Pins Listed in Numeric Order (32-pin XQFN)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CIN00	9	CIN08	17	CIN16	25	RESET_N
2	CIN01	10	CIN09	18	CIN17	26	INT_N
3	CIN02	11	CIN10	19	CIN18	27	SCL
4	CIN03	12	CIN11	20	CIN19	28	SDA
5	CIN04	13	CIN12	21	CIN20	29	VCC18
6	CIN05	14	CIN13	22	CIN21	30	DVCC
7	CIN06	15	CIN14	23	NC	31	AVCC
8	CIN07	16	CIN15	24	NC	32	VCOM



5. Pin Description

Table 5-1. Description of Capacitance Sensor Related Pins

Pin(s) No.		Signal		Attribute	Description
Capacitance S	Sensor Related	Pins (Analog I/	(F)		
7257AXQN	7257BXQN	7257AXQN	7257BXQN		
10-20, 22-23	1-22	CIN00- CIN12	CIN00- CIN21	AIO	Capacitance Sensor Pin These inputs are used to sense the capacitance values. They can be companioned with capacitance sensors to implement functions such as buttons, scroll bars, and wheels.
8	32	VC	ОМ	AO	Analog Bias Voltage Connected to External 1uF Bypass CAP

Table 5-2. Description of System Control Pins

Pin(s) No.		Signal		Attribute	Description
System Contr	ol Pins (1.8/3.3	V CMOS I/F)			
7257AXQN	7257BXQN	7257AXQN	7257BXQN		
1	26	INT	_N	OD	Interrupt Output This pin is used as the dedicated interrupt output signal.
24	25	RESI	ET_N	IK	Hardware Reset This pin is to reset hardware for this chip.

Table 5-3. Pin Description of I2C Interface

Pin(s	Pin(s) No.		Signal		Description
I2C Interface					
7257AXQN	7257BXQN	7257AXQN	7257BXQN		
2	27	SO	CL	IOKD	I ² C Clock
3	28	SI	DA	IOKD	I ² C Data

Table 5-4. Description of Power/Ground Signals

Pin(s) No.		Signal		Attribute	Description
Power/Ground	d Signals				
7257AXQN	7257BXQN	7257AXQN	7257BXQN		
21	23-24	NC		Al	Not Connected
7	31	AV	CC	Al	Analog VCC (3.3V)
6	30	DV	CC	Al	Digital VCC (3.3V)
4	29	VC	C18	AO	1.8V Regulator Output
					Connected to External 1uF Bypass CAP
0, 5, 9	0	GN	GND		Ground at Thermal PAD

Notes: I/O cell types are described below:

IK: Schmitt Trigger Input PAD.

Al: Analog/Power/Ground Input PAD.

OD: Open-Drain Output PAD.
AO: Analog Output PAD.
AIO: Analog Input/Output PAD.

IOKD: Open-Drain Output/Schmitt Trigger Input PAD.

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6. Serial Interface

6.1 Overview

The IT7257's serial interface supports four transfer types, single write, burst write, single read, and burst read.

6.2 I²C –compatible Interface

The IT7257 supports the industry standard 2-wire I²C serial interface protocol. It is also compatible with System Management Bus (SMBus) protocol.

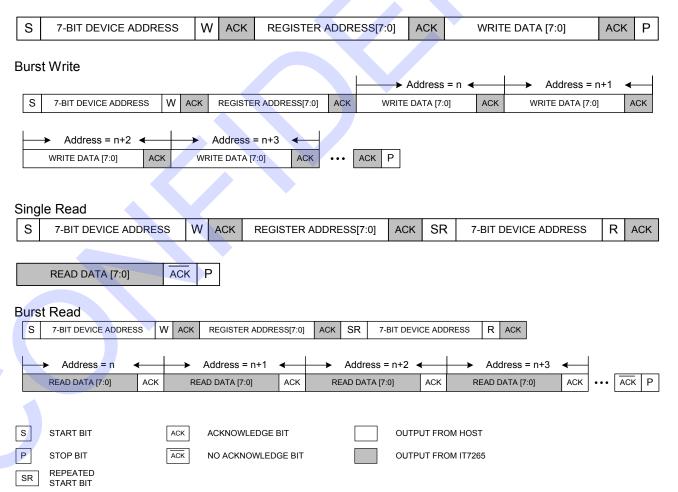
6.2.1 Device Address

The IT7257 supports the default device address (46h), and it can be changed to other address values by CPU.

6.2.2 Data Transfer

Data is transferred over the I²C bus in 8-bit address and 8-bit data. The IT7257 supports the following four types of transfers. The related protocol and timing diagrams are shown below.

Single Write



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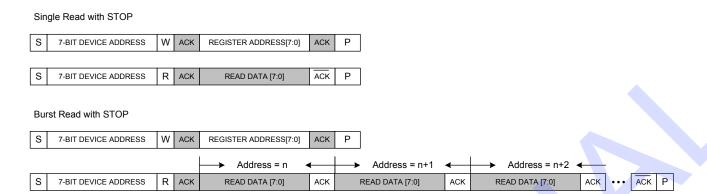


Figure 6-1. Example of I2C Timing for Single Data Write Operation

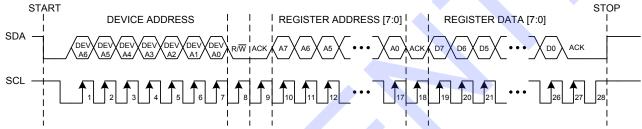
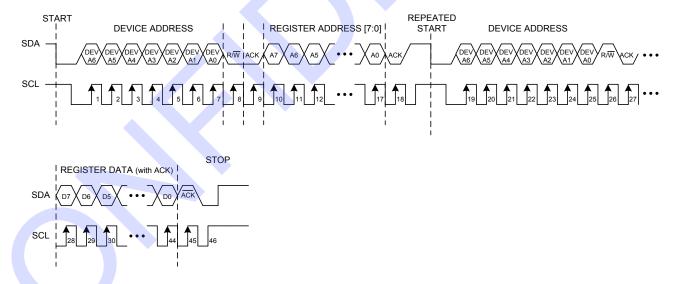


Figure 6-2. Example of I2C Timing for Single Data Read Operation





7. Hardware Reset

The IT7257 supports hardware reset de-glitch function. The reset pulse will be ignored when the pulse width is less than 1us. In addition, the IT7257 will enter the sleep mode when the pulse width is larger than 1ms.

Figure 7-1. Definition of Timing for Hardware Reset

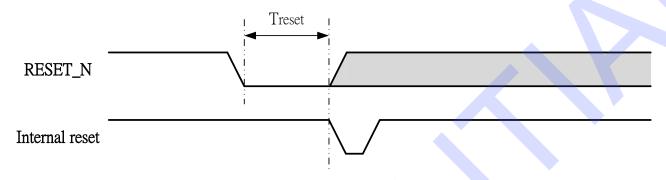


Figure 7-2. Definition of Timing for Sleep Mode

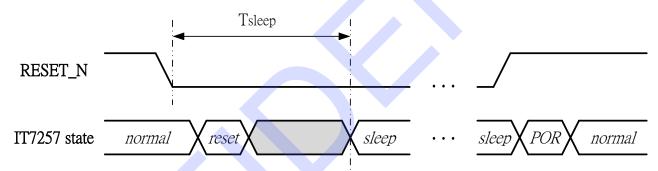


Table 7-1. Hardware Reset Timing

Symbol	Parameter	Min.	Тур.	Max.	Unit
Treset	Hardware Reset Timing	1	2	4	us
Tsleep	Sleep Mode Timing	1	2	-	ms

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8. DC Characteristics

Absolute Maximum Ratings*

Power Supply (AVCC/DVC)	C)0.3V to 3.6V
Input Voltage	0.3V to DVCC + 0.3V
Output Voltage	0.3V to DVCC + 0.3V
Storage Temperature	40°C to 125°C

Comments*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition DVCC=2.6 V -3.6 V, Ta= -40°C~85°C)

Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
V _{IL}	Input Low Voltage	CMOS	-	-	0.5	V
V_{IH}	Input High Voltage	CMOS	1.2	-	-	٧
Vt-	Schmitt trigger negative going threshold voltage	CMOS	ı	1.20	-	V
Vt+	Schmitt trigger positive going threshold voltage	CMOS	,	2.10	-	٧
V_{OL}	Output Low Voltage	I _{OL} =2mA	-	-	0.4	V
V_{OH}	Output High Voltage	I _{OH} =2mA	2.4	-	-	٧
R_{l}	Input Pull-up resistance	V _{IL} =0V or V _{IH} =Vcc	-	75	-	ΚΩ
I _{cc}	Operating current	DVCC=3.3V, Active mode,	-	3	-	mA
I _{CC,IDLE}	Operating current (power save timeout: 50ms)	DVCC=3.3V, Idle mode,	-	200	250	uA
I _{CC,SLEEP}	Operating current	DVCC=3.3V, Sleep mode,	-	2	-	uA
I _{IL}	Input Leakage current	no pull-up	-1	ı	1	uA
l _{oz}	Tri-state leakage current		-1	-	1	mA
C_{IN}	Input capacity		-	10	-	pF
C _{OUT}	Output capacity		-	10	-	pF
C _{BID}	Bi-directional buffer capacity		-	10	-	рF





9. AC Characteristics

Figure 9-1. Definition of Timing for I²C Interface

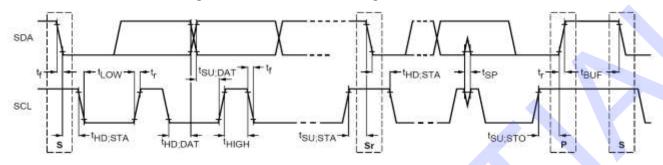


Table 9-1. I2C AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
f _{SCL}	SCL clock frequency	1	400	kHz
t _{HD;STA}	Hold time (repeated) START condition After this period, the first clock pulse is generated.	0.6	-	us
t _{LOW}	LOW period of the SCL clock	1.3	-	us
t _{HIGH}	HIGH period of the SCL clock	0.6	-	us
t _{SU;STA}	Set-up time for a repeated START condition	0.6	-	us
t _{HD;DAT}	Data hold time	0	0.9	us
t _{SU;DAT}	Data setup time	100	-	ns
t _r	Rise time of both SDA and SCL signals	20+0.1C _b	300	ns
t _f	Fall time of both SDA and SCL signals	20+0.1C _b	300	ns
t _{SU;STO}	Set-up time for STOP condition	0.6	-	us
t _{BUF}	Bus free time between a STOP and START condition	1.3	-	us
C _b	Capacitive load for each bus line	-	400	pF
V _{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	0.1V _{DD}	-	V
V _{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2V _{DD}	-	V
t _{timeout}	Cumulative SCL low timeout limit	3	5	ms

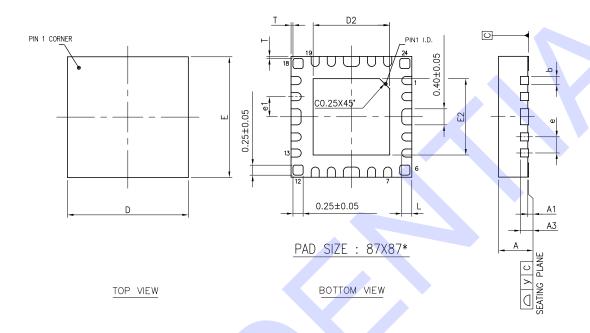




10. Package Information

XQFN 24(3*3) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
Α	0.020	0.022	0.024	0.50	0.55	0.60
A1	0.000	0.001	0.002	0.00	0.02	0.05
A3	0.006 REF			0.150 REF		
b	0.006	0.008	0.010	0.15	0.20	0.25
D/E	0.118 BSC			3.0 BSC		
D2/E2	0.073	0.075	0.077	1.85	1.90	1.95
е	0.016 BSC			0.4 BSC		
e1	0.020 BSC			0.5 BSC		
Г	0.006	0.010	0.014	0.15	0.25	0.35
у			0.003			0.08
T	0.000	0.002	0.004	0.00	0.05	0.10

Notes:

- 1. Controlling dimensions: Millimeter
- 2. Reference document: JEDEC MO-220
- 3. Take SMT into consideration, please use the minimum number of D2's and E2's dimensions.

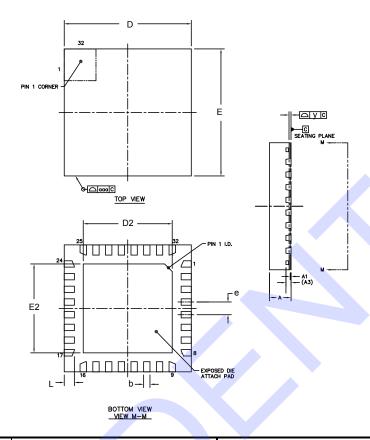
DI-SAW-XQFN24(3*3)v0

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XQFN 32 T1(4*4) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
Α	0.020	0.022	0.024	0.50	0.55	0.60
A1	0.000	1	0.002	0.00	-	0.05
A3	0.008 REF			0.203 REF		
b	0.006	0.008	0.01	0.15	0.20	0.25
D	0.157 BSC			4.00 BSC		
D2	0.102	0.106	0.110	2.60	2.70	2.80
E	0.157 BSC			4.00BSC		
E2	0.102	0.106	0.110	2.60	2.70	2.80
е	0.016 BSC			0.40 BSC		
L	0.010	0.012	0.014	0.25	0.30	0.35
у	-	-	0.003	-	-	0.08

Notes

- 1. Controlling dimensions: Millimeter
- 2. Reference document: JEDEC MO-248
- 3. Take SMT into consideration, please use the minimum number of D2's and E2's dimensions.

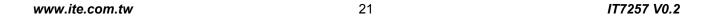
DI-SAW-XQFN32 T1(4*4)v0



11. Ordering Information

Part No.	Channel Number	Package		
IT7257AXQN/AX	13	24-pin 3*3*0.55mm XQFN		
IT7257BXQN/AX	22	32-pin 4*4*0.55mm XQFN		

All green components provided are in compliance with RoHS, and Halogen-Free.

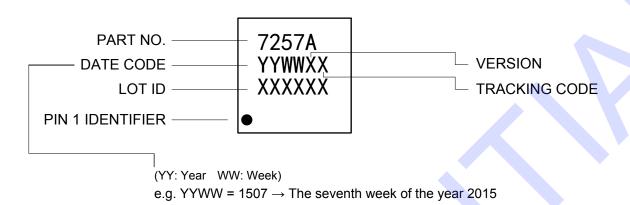




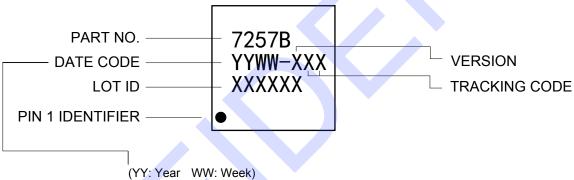


12. Top Marking Information

IT7257AXQN (XQFN24)



IT7257BXQN (XQFN32)



(YY: Year WW: Week) e.g. YYWW = 1507 → The seventh week of the year 2015

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 Seller warrants that the goods sold will be free from defects in material and workmanship
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7. <u>CANCELLATION</u>
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Seller will, at its own expense, assist Buyer with technical support and information in connection with any dairn that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no

liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized

EXCEPT AS EXPRESSIY STATED IN THIS PREFIGURATION OF INTERMINING SUPPLED BY AN ADMINISTRATION OF THE MEMORY AND ADMINISTRATION OF THE

NO CONFIDENTIAL INFORMATION
Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

- 10. ENTIRE AGREEMENT

 (a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
- Buyer is not relying upon any warranty or representation except for those specifically stated

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. <u>JURISDICTION AND VENUE</u>
The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. <u>ATTORNEYS' FEES</u>
Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.