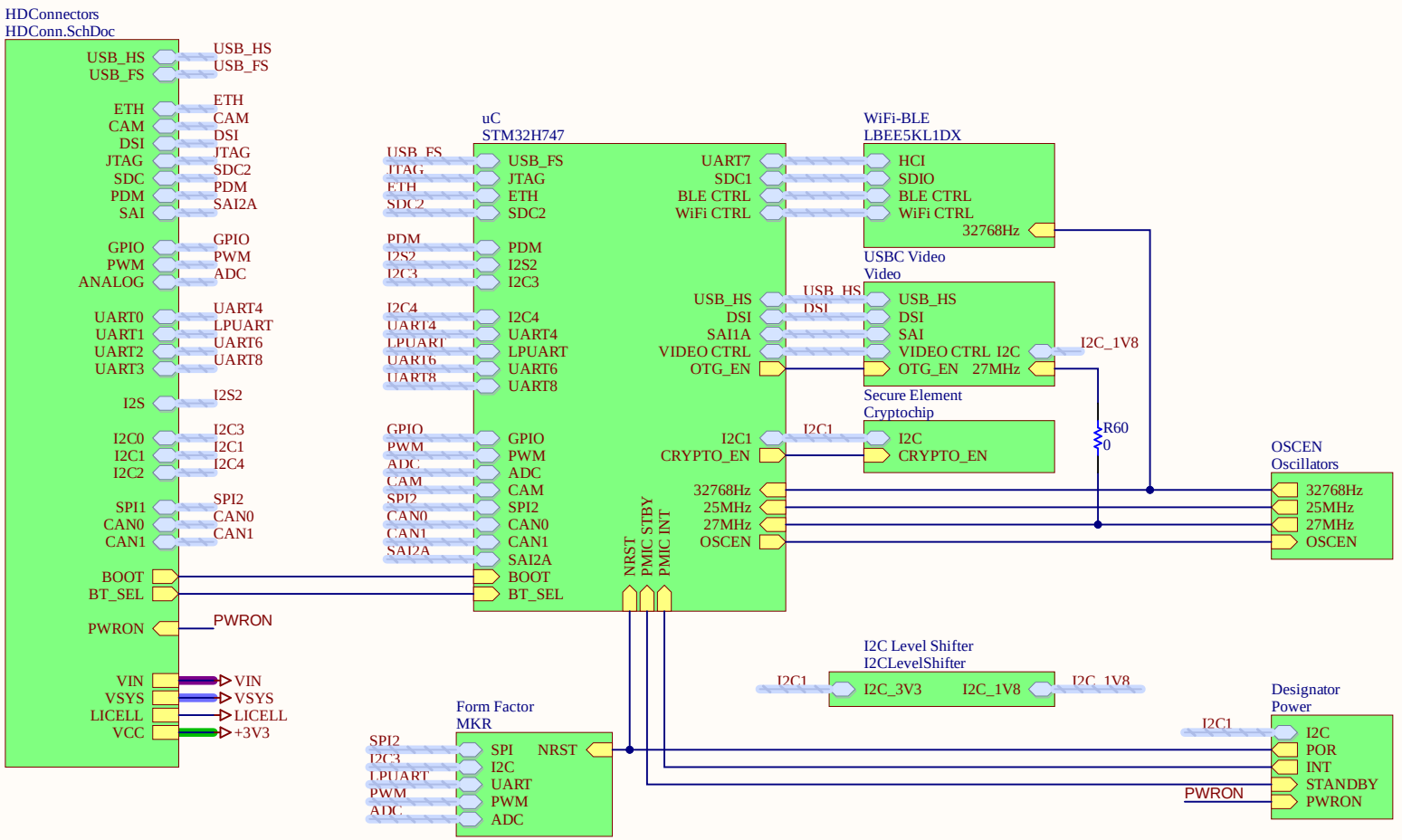

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Title: **PortentaH7**			
ID: SL-ABX00042		Revision: V4.10	
Date: 5/16/2023	Time: 4:55:41 PM	Sheet 1 of 10	
File: TopView.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi

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ARDUINO

U1A
STM32H747XIH6
U1B
STM32H747XIH6
U1C
STM32H747XIH6
SDRAM
U4A
AS4C4M16SA-6BIN
U4B
AS4C4M16SA-6BIN
USB_HS
U3
USB3320C-EZK-TR
ETHERNET
U5
LAN8742AI-CZ-TR
U2
MX25L12833FZ2I-10G
DL1
SMLP34RGB2W3
DISPLAY
DSI
CAMERA
CAM
I2S
I2S2
SAI
SAI1A
SAI2A
CAN
CAN0
CAN1
SDC
SDC1
SDC2
PDM
UART
UART4
LPUART
UART7
UART8
ANALOG
ADC
JTAG
SPI
SPI2
I2C
I2C4
I2C1
I2C3
USB
USB_FS
PWM
BLE CTRL
WiFi CTRL
VIDEO CTRL
GPIO
ETH
BT_SEL
CRYPTO_EN
PMIC STBY
PMIC INT
OTG_EN
OSCEN
NRST
BOOT
PDR_ON
VBUS
USB0_D_P
USB0_D_N
HSU_D_P
HSU_D_N
PJ4
PJ6
PJ7
PJ8
PJ9
PJ10
PJ11
PJ12
PJ13
PJ14
PJ15
PK1
PK2
PK3
PK4
PK5
PK6
PK7
PH0-OSCIN
PH1-OSCOUT
PC13
PC15
PC14-OSC32_IN
PC15-OSC32_OUT
32768Hz
25MHz
27MHz
VBAT
VREF+
VDDA
VDD33USB
VDD50USB
VCAPDSI
VDDDSI
VFBSMPS
VLXSMPS
VSSSMPS
VDDSMPS
VCAP
AREF+
AREF-
SJ6
TP1
TP2
TP3
TP4
TP5
TP29
TP30
TP31
TP32
L1
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L12
R1
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C146
C147
C149
C150
GND
+3V1
+3V1SW
+1V2
+1V8
+VBAT
VDDA
VCAP
VFBSMPS
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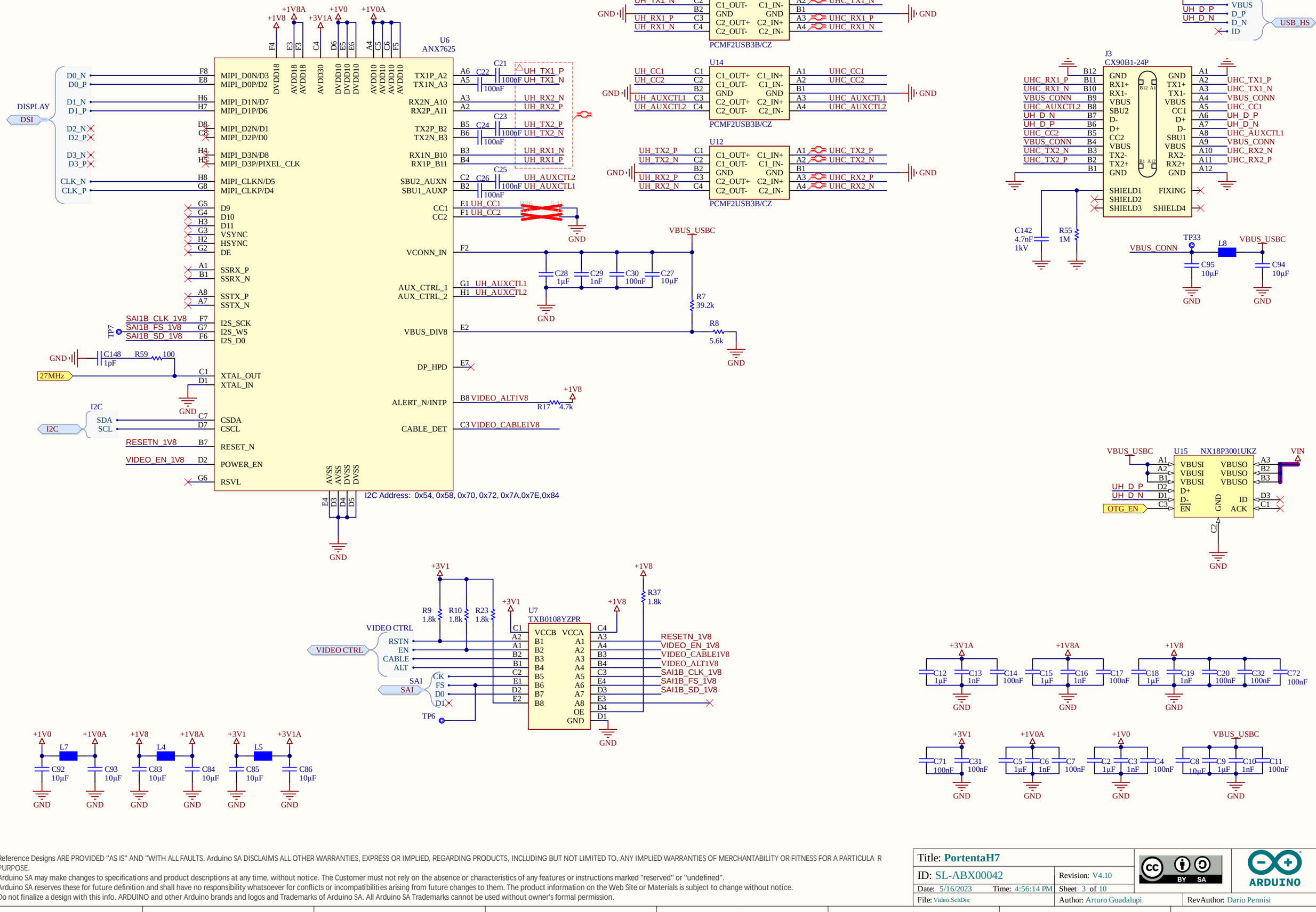
Title: PortentaH7	
ID: SL-ABX00042	Revision: V4.10
Date: 5/16/2023 Time: 4:56:09 PM	Sheet 2 of 10
File: STM32H747.SchDoc	Author: Arturo Guadalupi RevAuthor: Dario Pennisi



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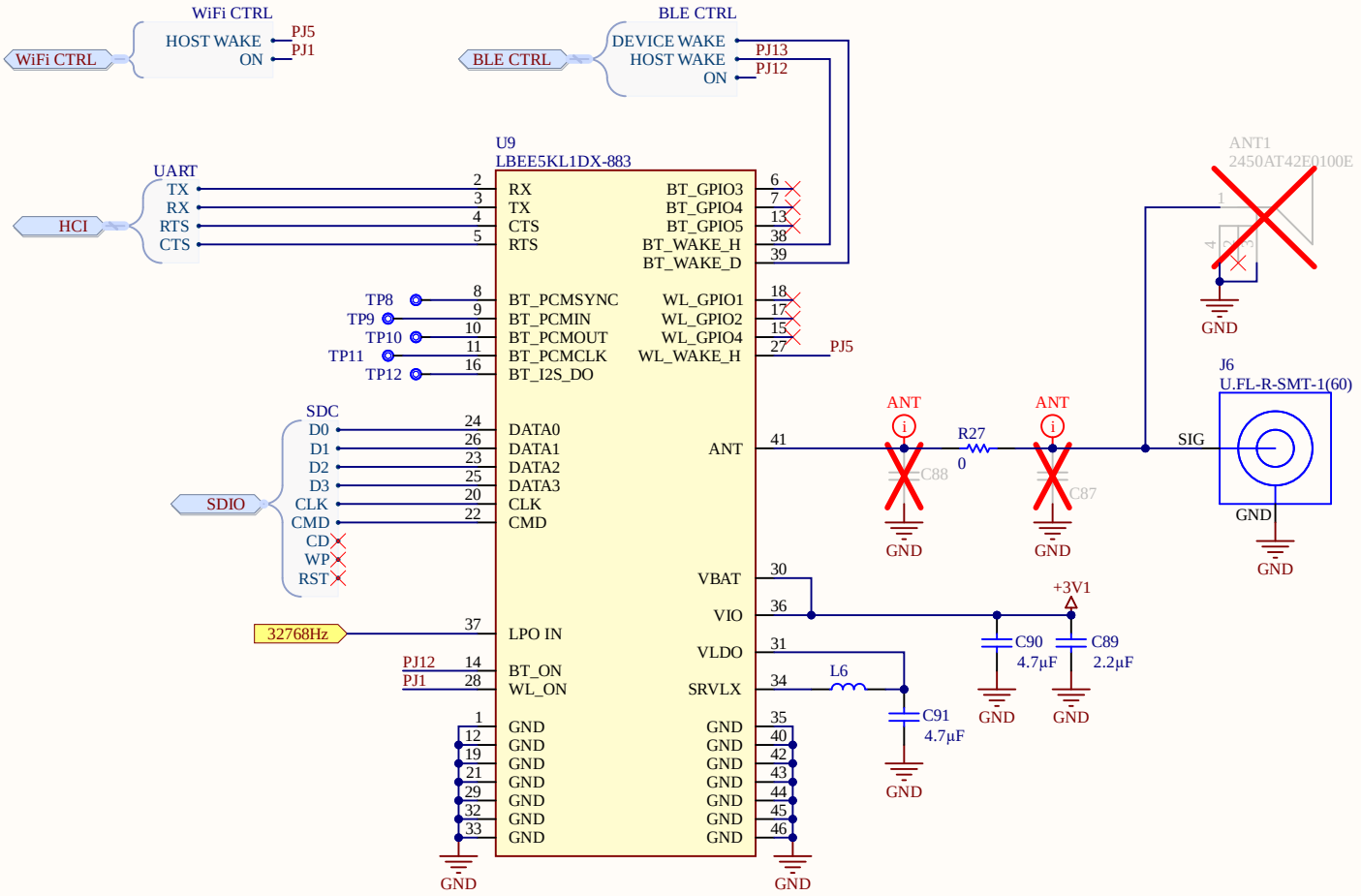
Title: **PortentaH7**			
ID: SL-ABX00042		Revision: V4.10	
Date: 5/16/2023	Time: 4:56:14 PM	Sheet 3 of 10	
File: Video.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi



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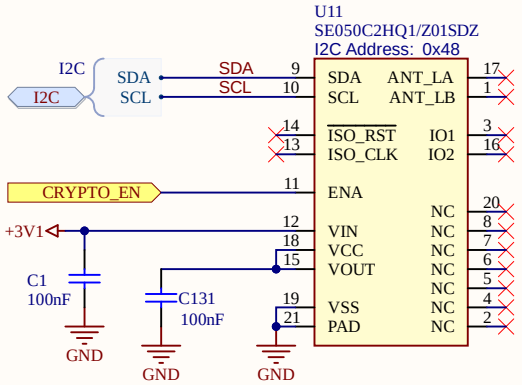
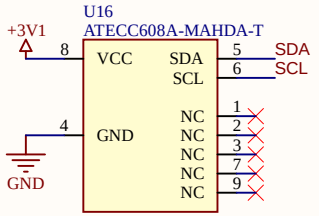
Title: **PortentaH7**			
ID: SL-ABX00042		Revision: V4.10	
Date: 5/16/2023	Time: 4:56:18 PM	Sheet 4 of 10	
File: LBEE5KL1DX.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi





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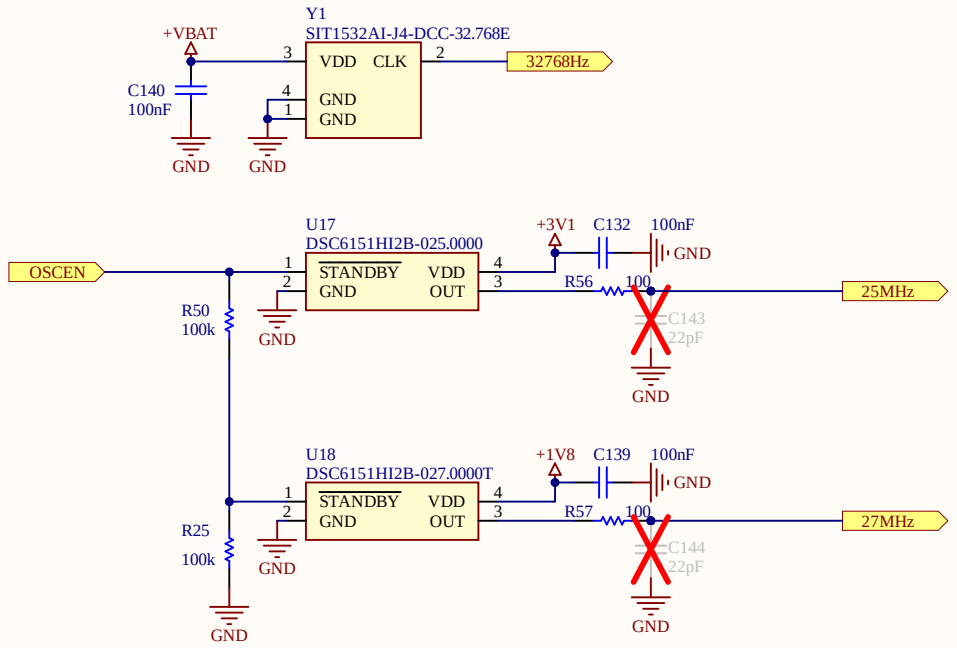
Title: **PortentaH7**			
ID: SL-ABX00042	Revision: V4.10		
Date: 5/16/2023 Time: 4:56:23 PM	Sheet 5 of 10		
File: Cryptochip.SchDoc	Author: ArturoGuadalupi	RevAuthor: Dario Pennisi	



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Title: **PortentaH7**			
ID: SL-ABX00042	Revision: V4.10		
Date: 5/16/2023 Time: 4:56:27 PM	Sheet 6 of 10		
File: Oscillators.SchDoc	Author: Arturo Guadalupi	RevAuthor: Dario Pennisi	

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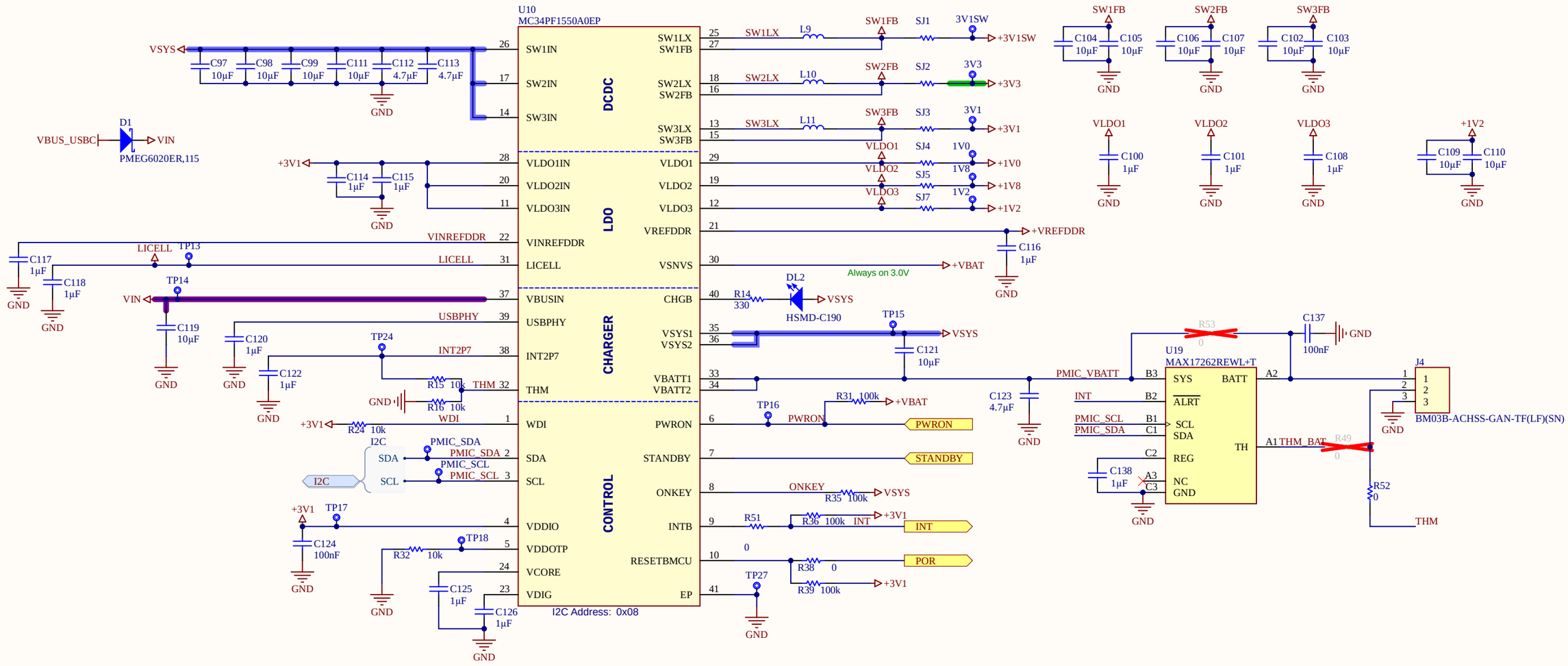

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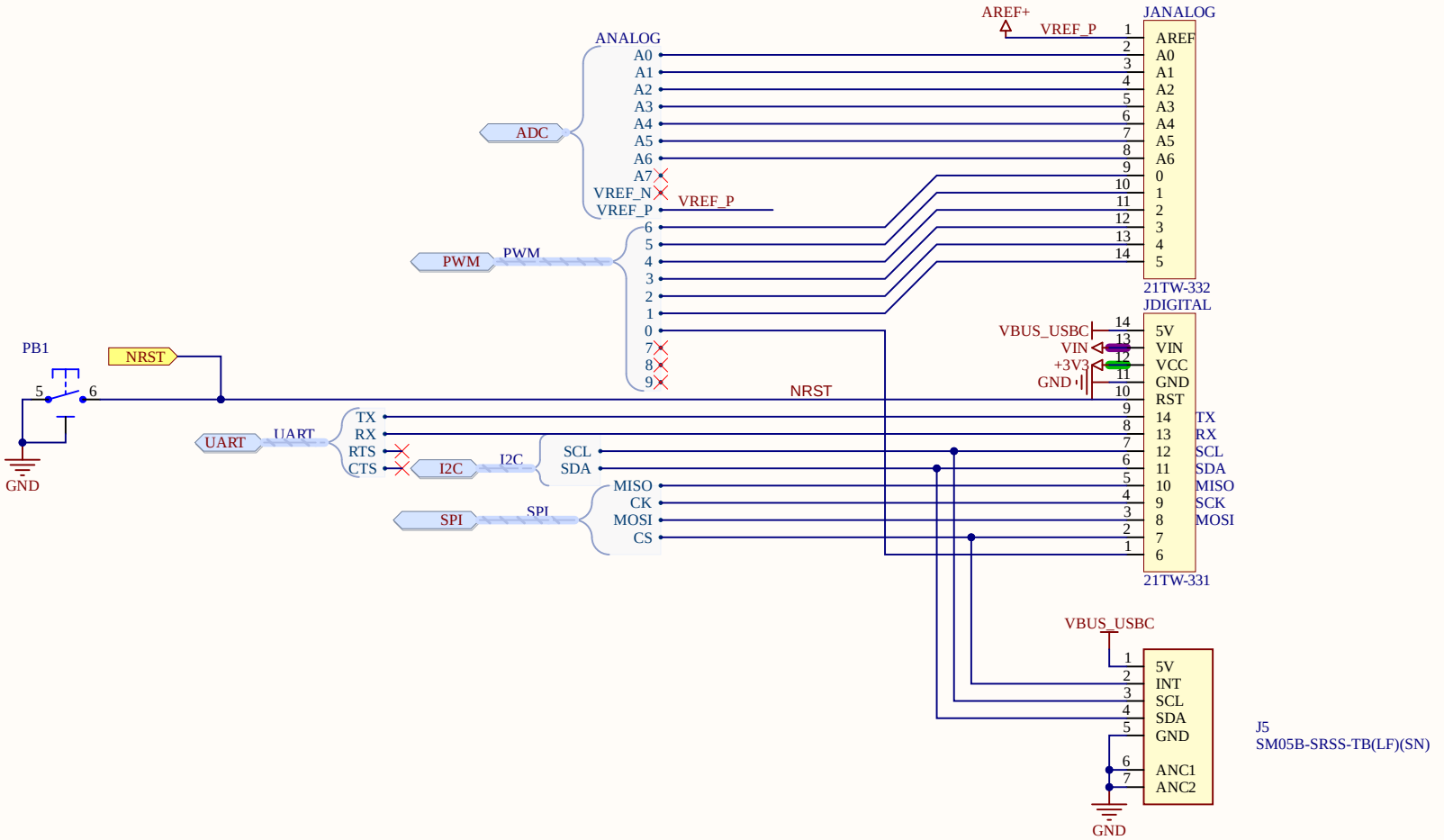
Title: PortentaH7			
ID: SL-ABX00042		Revision: V4.10	
Date: 5/16/2023	Time: 4:56:32 PM	Sheet 7 of 10	
File: Power.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi



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Title: **PortentaH7**			
ID: SL-ABX00042		Revision: V4.10	
Date: 5/16/2023	Time: 4:56:36 PM	Sheet 8 of 10	
File: MKR.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi

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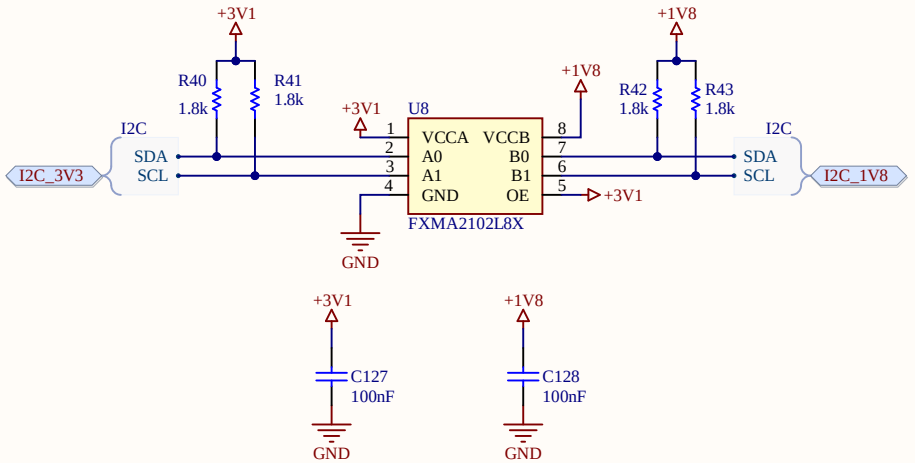

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Title: **PortentaH7**			
ID: SL-ABX00042	Revision: V4.10		
Date: 5/16/2023 Time: 4:56:41 PM	Sheet 9 of 10		
File: I2CLevelShifter.SchDoc	Author: Arturo Guadalupi	RevAuthor: Dario Pennisi	

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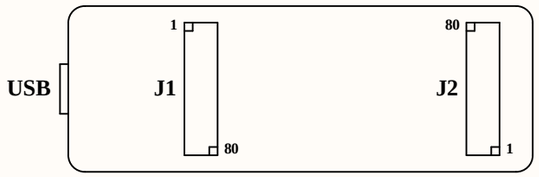
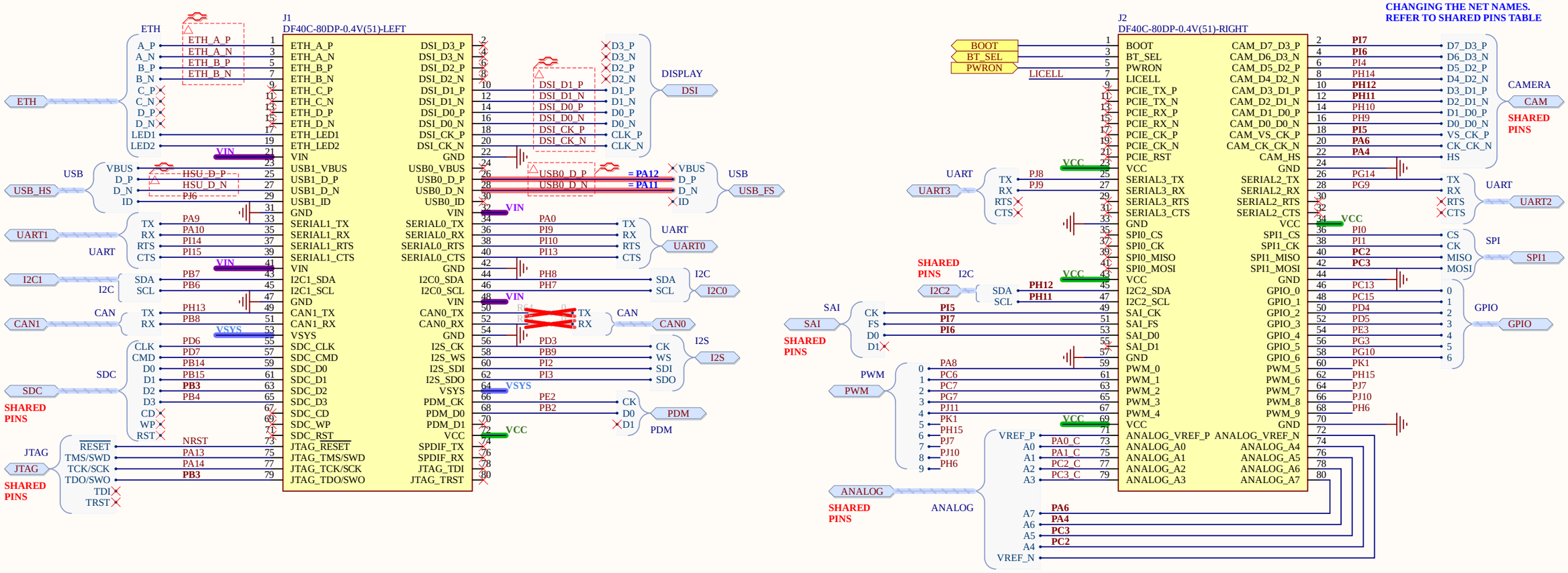
Board side view:

Board BOTTOM view:



IF NECESSARY ROUTE CAMERA WITH DIFFERENTIAL PAIR RULES CHANGING THE NET NAMES. REFER TO SHARED PINS TABLE



SHARED PINS TABLE

NET	BUS 1	BUS 2
PB3	JTAG	SDC2
PH11	CAM	I2C4
PH12	CAM	I2C4
PI5	CAM	SAI2A
PI6	CAM	SAI2A
PI7	CAM	SAI2A
PA4	CAM	ANALOG
PA6	CAM	ANALOG
PC2	ANALOG	SPI2
PC3	ANALOG	SPI2

POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	**PORTENTA INPUT**	4.1V to 6V.	Default 3.3V, PMIC (U10) programmable output.
VCC	***PORTENTA OUTPUT***	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U10) programmable output.
VSYS	***PORTENTA RESERVED OUTPUT***	**RESERVED, DO NOT USE** 3.5V to 4.2V, max 600mA.	Default 4.2V, PMIC (U10) programmable output which is also the input voltage of the bucks inside the PMIC itself.
LICELL	**PORTENTA INPUT**	Coinc cell max 3.6V, max 46uA.	Max 4uA with PMIC (U10) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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Title: **HD Connectors**		
ID: SL-ABX00042	Revision: V4.10	
Date: 5/16/2023 Time: 4:56:46 PM	Sheet 10 of 10	
File: HDConn.SchDoc	Author: Arturo Guadalupi	RevAuthor: Dario Pennisi