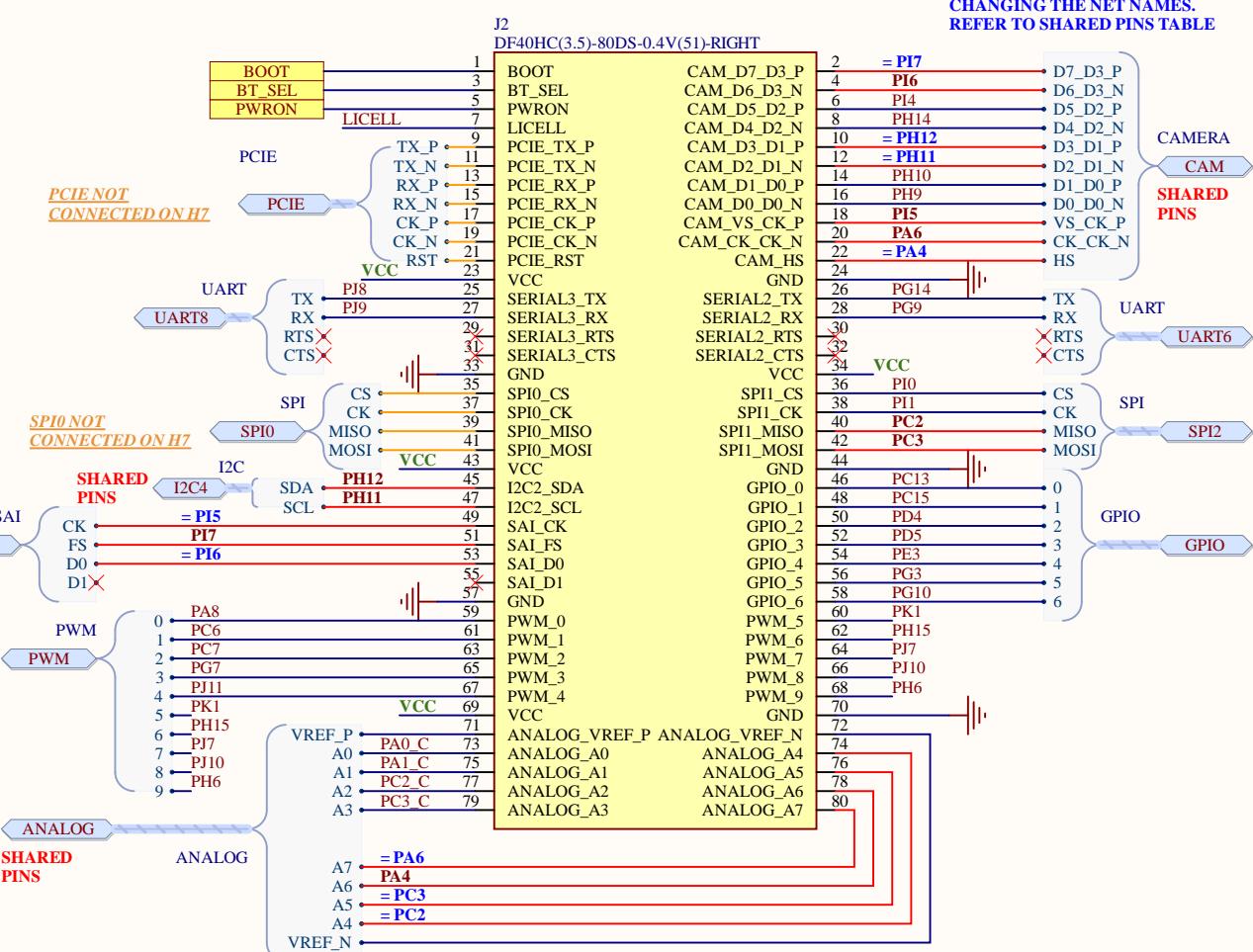
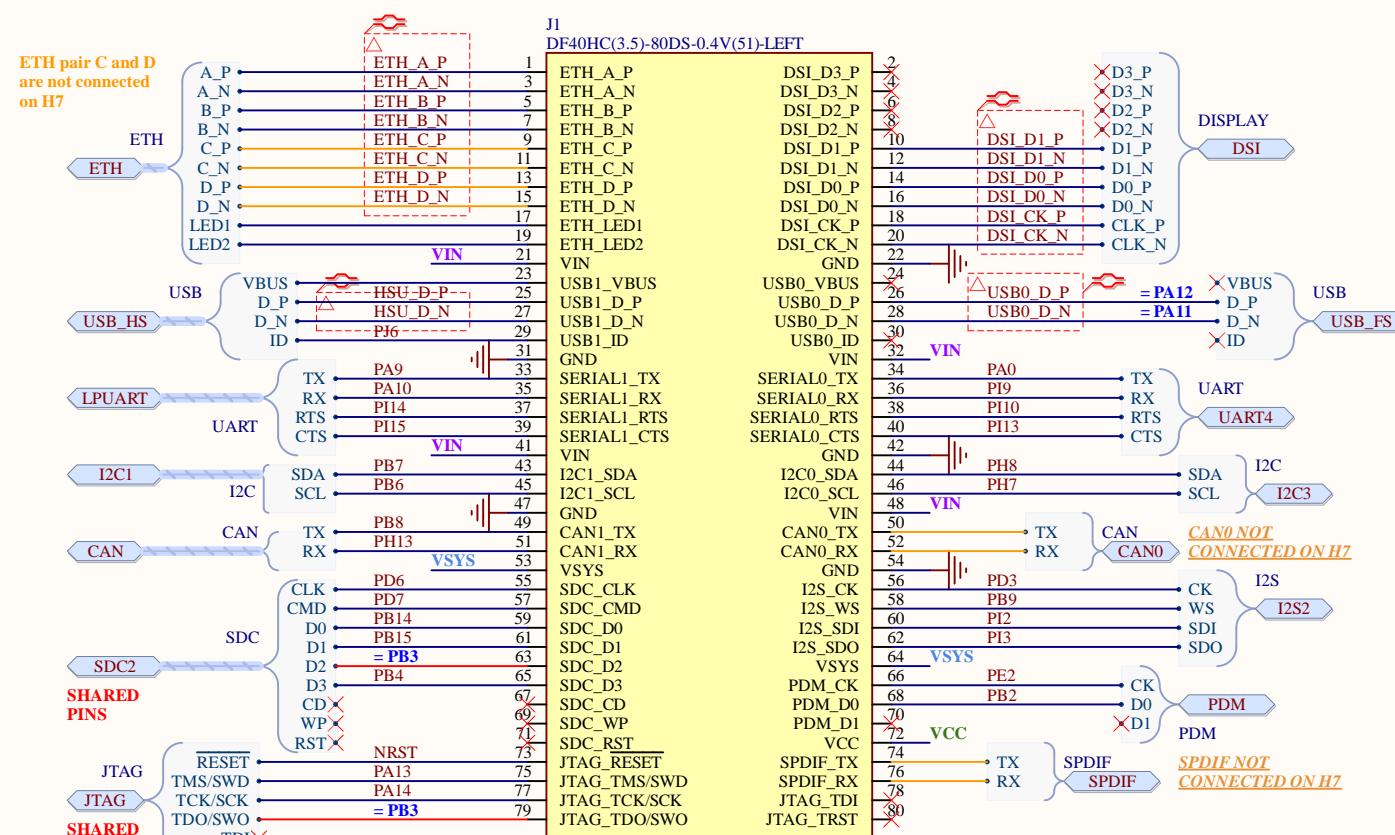
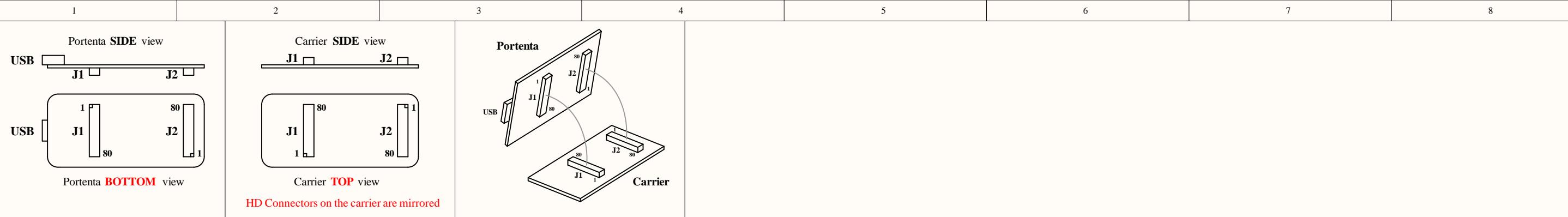


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Title: TOP			
ID: ASX00024	Revision: V1.3		
Date: 2022-08-11	Time: 13:44:10	Sheet 1 of 19	
File: TOP.SchDoc		Author: S.Navaretti	RevAuthor: S.Navaretti



SHARED PINS TABLE

NET	BUS 1	BUS 2
PB3	JTAG	SDC2
PH11	CAM	I2C4
PH12	CAM	I2C4
P15	CAM	SAI2A
P16	CAM	SAI2A
P17	CAM	SAI2A
PA4	CAM	ANALOG
PA6	CAM	ANALOG
PC2	ANALOG	ANALOG
PC3	ANALOG	ANALOG

POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	VIN	4.1V to 6V.	Default 3.3V, PMIC (U10) programmable output.
VCC	VCC	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U10) programmable output.
VSYS	VSYS	RESERVED, DO NOT USE	Default 4.2V, PMIC (U10) programmable output which is also the input voltage of the bucks inside the PMIC itself.
LICELL	LICELL	PORTENTA INPUT	Portenta Input
		3.5V to 4.2V, max 600mA.	
		PORTENTA RESERVED OUTPUT	
		3.5V to 4.2V, max 600mA.	
		PORTENTA INPUT	Portenta Input
		Coin cell max 3.6V, max 46uA.	

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Title: HD Connectors female

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:44:14

Sheet 2 of 19

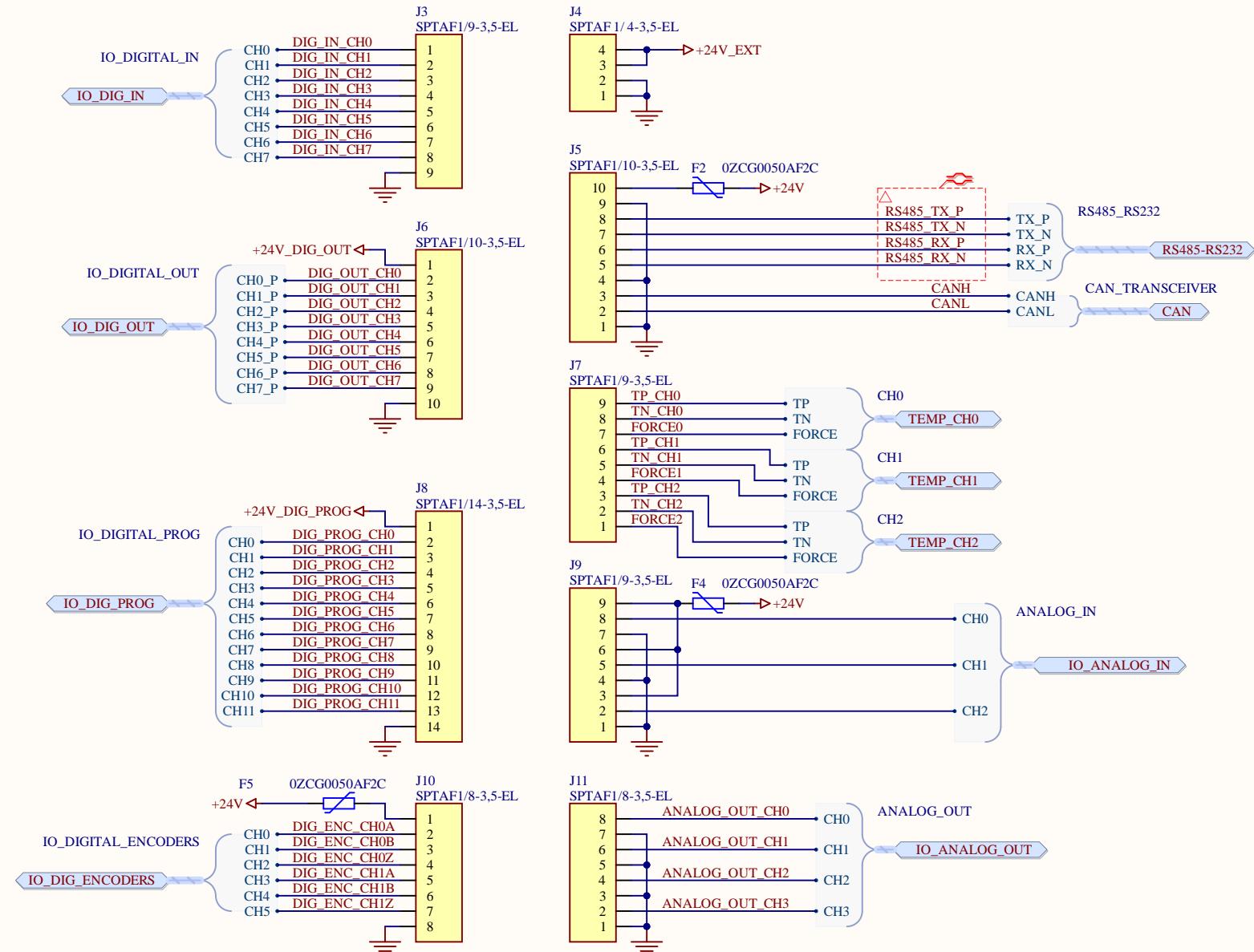
File: HDConn_FEMALE.SchDoc

Author: S.Navaretti

RevAuthor:



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Title: MORSETTIERA

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:44:18

Sheet 3 of 19

File: MORSETTIERA.SchDoc

Author: S.Navaretti



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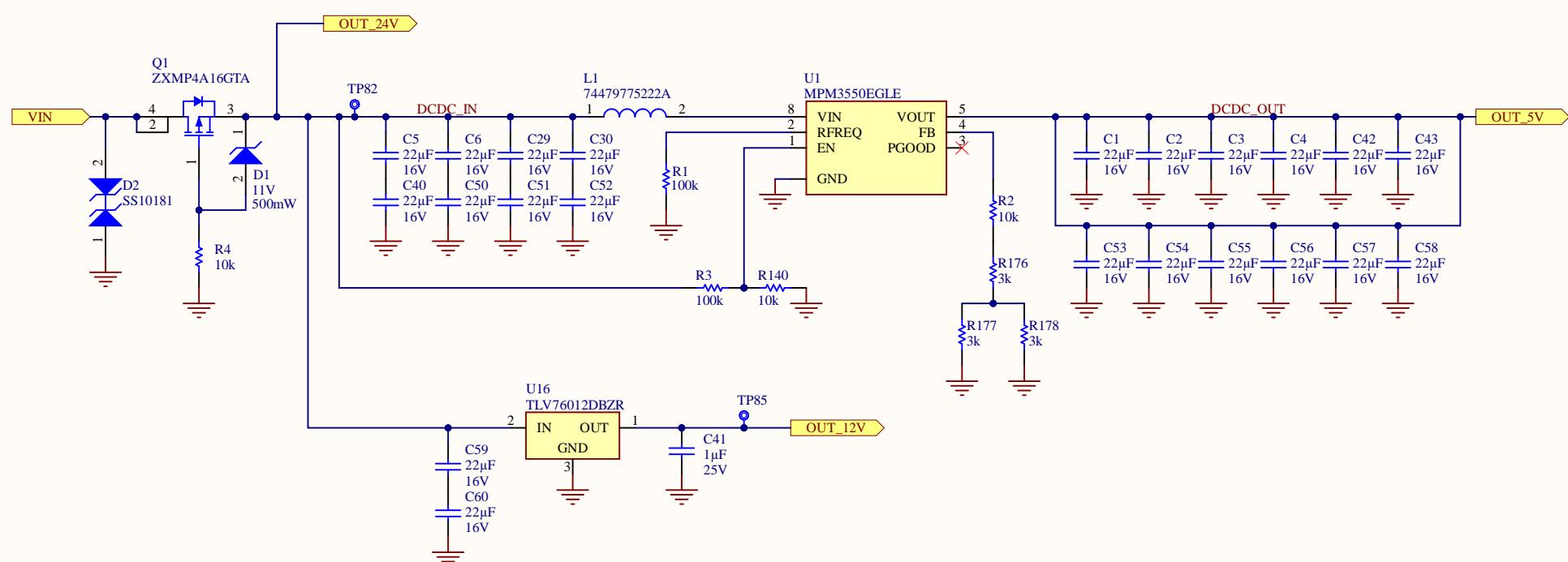
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Title: POWER

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:44:21

Sheet 4 of 19

File: POWER.SchDoc Author: S.Navaretti



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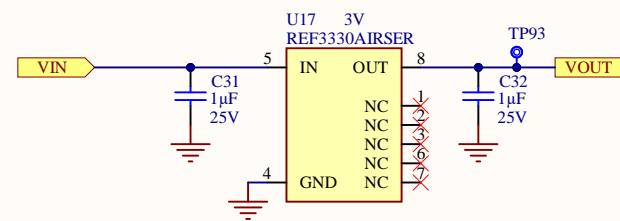
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Title: VOLTAGE REFERENCE

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:44:24

Sheet 5 of 19

File: ADC_VOLTAGE_REFERENCE.SchDoc

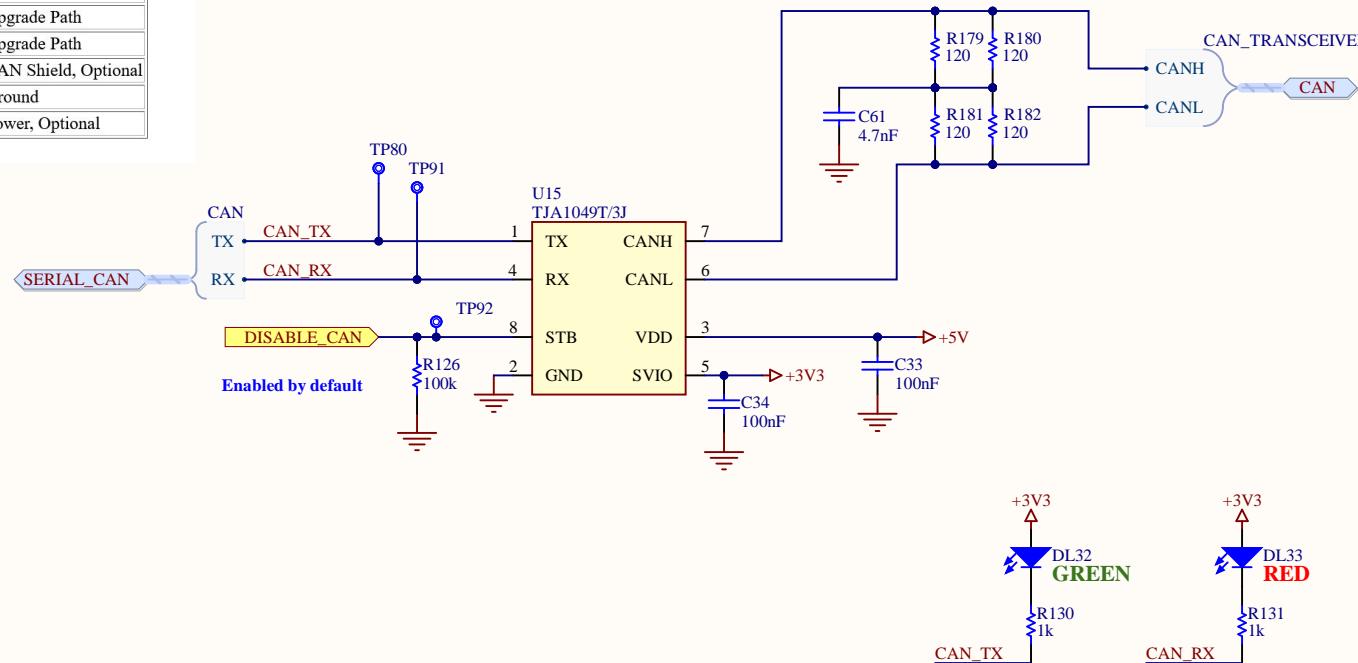
Author: S.Navaretti





RJ10, RJ45 CAN Bus PinOut

RJ45 Pin #	RJ10 Pin #	Signal name	Signal Description
1	2	CAN_H	Dominant High
2	3	CAN_L	Dominant Low
3	4	CAN_GND	Ground
4	-	Reserved	Upgrade Path
5	-	Reserved	Upgrade Path
6	-	CAN_SHLD	CAN Shield, Optional
7	-	CAN_GND	Ground
8	1	CAN_V+	Power, Optional



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Title: CAN

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:44:27

Sheet 6 of 19

File: CAN.SchDoc

Author: S.Navaretti



PIN DESCRIPTIONS

Pin	Name	RS-232	RS-485 Full Duplex	RS-485 Half Duplex
1				
2	GND	Ground		
3	T1OUT, B/Z	Transmitter 1 Output	Z Driver Neg Output	B/Z Neg Input/Output
4	T2OUT, A/Y	Transmitter 2 Output	Y Driver Pos Output	A/Y Pos Input/Output
5				
6	R1OUT	Receiver 1 Output	X	X
7	R2OUT, RO	Receiver 2 Output	Receiver TTL Output	Receiver TTL Output
8				
9				
10	SHDN		Low power shutdown mode when low	
11	SLEW		Data rate limited to 250kbps when low	
12	FD_TX_TERM	X	120Ω Y-Z termination enabled when both TERM and FD_TX_TERM are high	X
13	TERM	X	120Ω A-B termination enabled when high	
14	RS-485/RS-232	0	1	1
15	HALF/FULL	X	0	1
16				
17	GND	Ground		
18	R2IN, A	Receiver 2 Input	A Pos Receiver Input	X
19	R1IN, B	Receiver 1 Input	B Neg Receiver Input	X
20	RE	X	Receiver enabled when low	
21	T2IN, DE	Transmitter 2 Input	Driver enabled when high	
22	T1IN, DI	Transmitter 1 Input	Driver TTL Input	
23				
24	V-	Charge pump negative supply, 0.1µF from ground		
25	C2-	Charge pump cap 2 negative lead		
26	C2+	Charge pump cap 2 positive lead, 0.1µF		
27	V+	Charge pump positive supply, 0.1µF to ground		
28	C1+	Charge pump cap 1 positive lead, 0.1µF		
29	VL	Logic Supply for TTL Inputs and Outputs, $V_L = +1.65V$ to +5.5V or tie to V _{CC}		
30	VCC	Main Supply, $V_{CC} = +3.0V$ to +5.5V, bypass to ground with 1.0µF		
31	C1-	Charge pump cap 1 negative lead		
32				

TABLE 1: RS-232 TX TRUTH TABLE

INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	D/I T1IN, D/E T2IN	Z(B) T1OUT, Y(A) T2OUT
0	X	X	1/8th unit load
1	0	0	1
1	0	1	0
1	1	X	RS-485 Mode

TABLE 2: RS-232 RX TRUTH TABLE

INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	B/R1IN, A/R2IN	R1OUT, R2R2OUT
X	0	0	1
X	0	1	0
X	0	Inputs open	1
X	1	X	R1OUT High-Z, R2R2OUT in RS-485 Mode

TABLE 3: RS-485/422 TX TRUTH TABLE

INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	DE/T2IN	D/I T1IN
0	X	X	X
1	1	0	1/8th unit load
1	1	1	1/8th unit load
1	1	1	0
1	1	1	1
X	0	X	RS-232 Mode

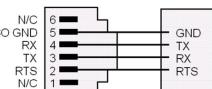
TABLE 4: RS-485/422 RX TRUTH TABLE

INPUTS		OUTPUT	
RS-485/RS-232	SHDN	HALF/FULL	RE
1	0	X	X
1	1	0	$\geq -50mV$
1	1	0	$\leq -200mV$
1	1	0	Floating
1	1	1	$\geq -50mV$
1	1	1	$\leq -200mV$
1	1	X	X
0	X	X	RS-232 Mode

TABLE 5: RS-485/422 TERMINATION TRUTH TABLE

FD_TX_TERM	TERM	RS-485/RS-232	HALF/FULL	TX TERM	RX TERM
Pin 12	Pin 13	Pin 14	Pin 15	Pins 3-4	Pins 15-19
X	0	1	0	-	-
0	1	1	0	-	ON
1	1	1	0	ON	ON
X	0	1	1	-	-
X	1	1	1	ON	-
X	X	0	X	-	-

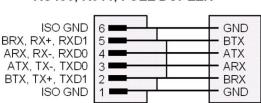
RS232 INTERFACE



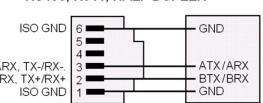
Computer



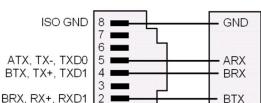
RS485, RJ11, FULL DUPLEX



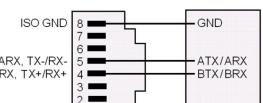
RS485, RJ11, HALF DUPLEX



RS485, RJ45, FULL DUPLEX



RS485, RJ45, HALF DUPLEX



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TABLE 1: RS-232 TX TRUTH TABLE

INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	D/I T1IN, D/E T2IN	Z(B) T1OUT, Y(A) T2OUT
0	X	X	1/8th unit load
1	0	0	1
1	0	1	0
1	1	X	RS-485 Mode

TABLE 2: RS-232 RX TRUTH TABLE

INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	B/R1IN, A/R2IN	R1OUT, R2R2OUT
X	0	0	1
X	0	1	0
X	0	Inputs open	1
X	1	X	R1OUT High-Z, R2R2OUT in RS-485 Mode

TABLE 3: RS-485/422 TX TRUTH TABLE

INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	DE/T2IN	D/I T1IN
0	X	X	X
1	1	0	1/8th unit load
1	1	1	1/8th unit load
1	1	1	0
1	1	1	1
X	0	X	RS-232 Mode

TABLE 4: RS-485/422 RX TRUTH TABLE

INPUTS		OUTPUT	
RS-485/RS-232	SHDN	HALF/FULL	RE
1	0	X	X
1	1	0	$\geq -50mV$
1	1	0	$\leq -200mV$
1	1	0	Floating
1	1	1	$\geq -50mV$
1	1	1	$\leq -200mV$
1	1	X	X
0	X	X	RS-232 Mode

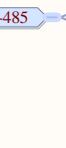
TABLE 5: RS-485/422 TERMINATION TRUTH TABLE

FD_TX_TERM	TERM	RS-485/RS-232	HALF/FULL	TX TERM	RX TERM
Pin 12	Pin 13	Pin 14	Pin 15	Pins 3-4	Pins 15-19
X	0	1	0	-	-
0	1	1	0	-	ON
1	1	1	0	ON	ON
X	0	1	1	-	-
X	1	1	1	ON	-
X	X	0	X	-	-

SERIAL-485



UART



485_RX



485_TX



R128 DNP



R168

TP86

TP87

TP88

TP89

TP90

U19

SP335ECR1-L

RS485_RS232

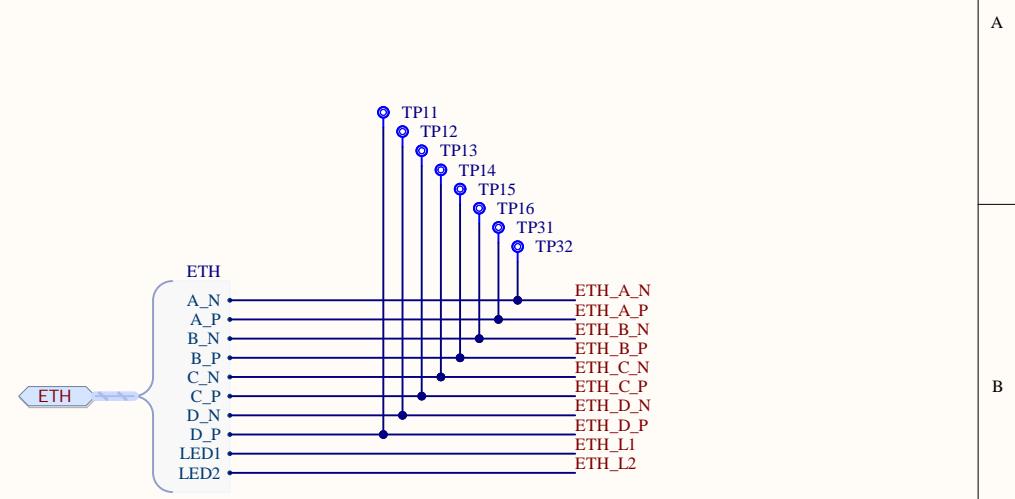
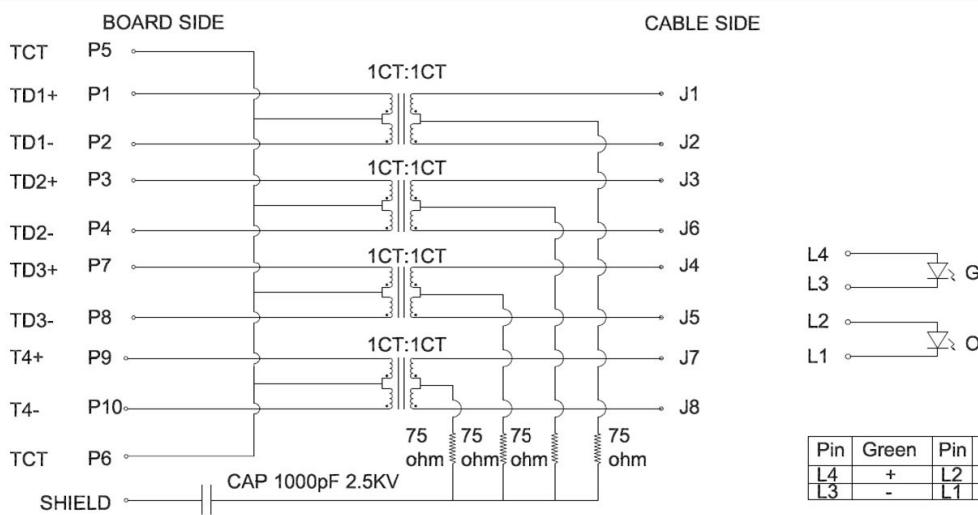
RS422_RS232

RS232_RS232

RS485_RS232

RS422_RS232

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Title: ETHERNET

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:44:34

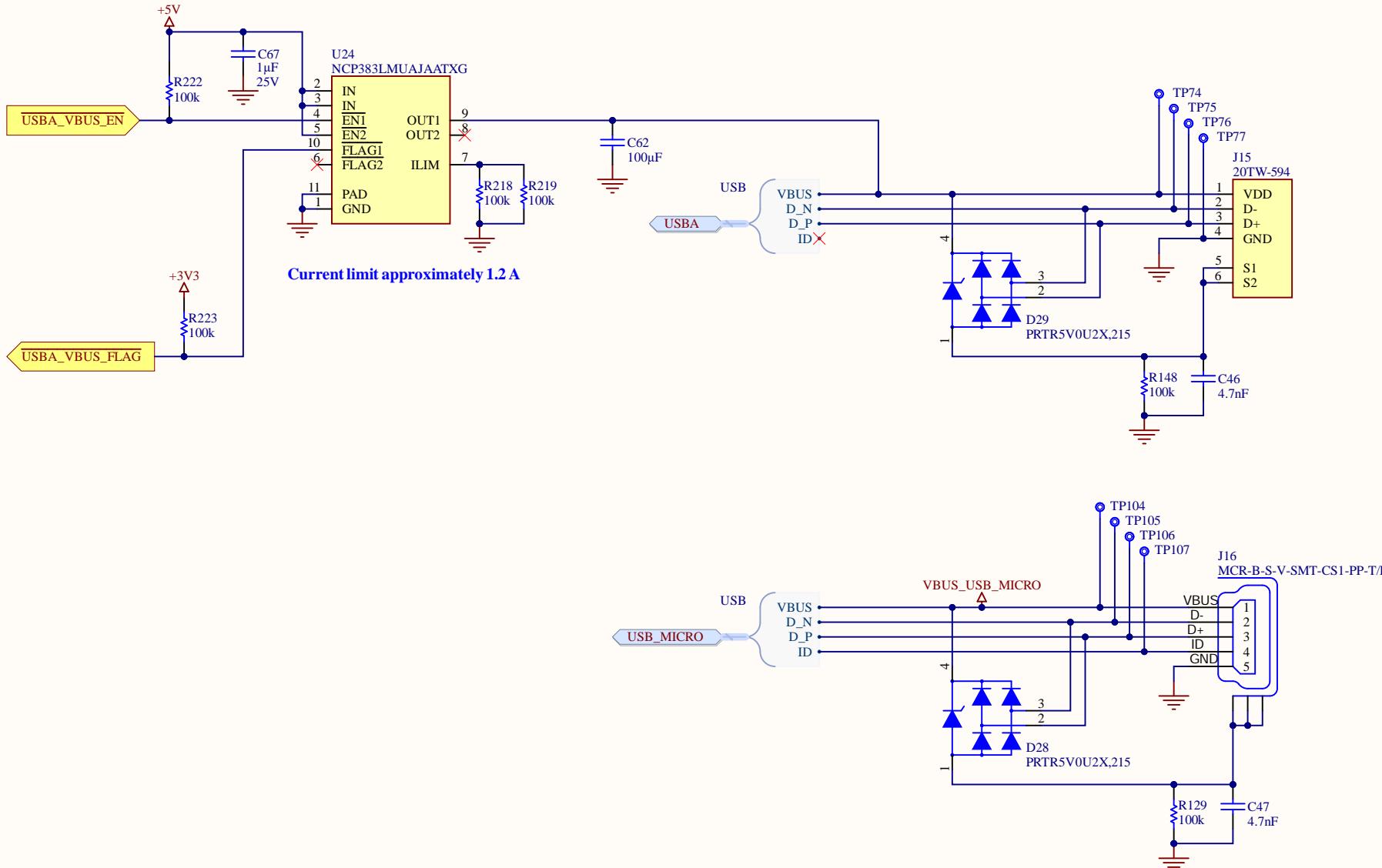
Sheet 8 of 19

File: ETHERNET.SchDoc

Author: S.Navaretti

RevAuthor: S.Navaretti





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Title: USB

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:44:37

Sheet 9 of 19

File: USB.SchDoc

Author: S.Navaretti



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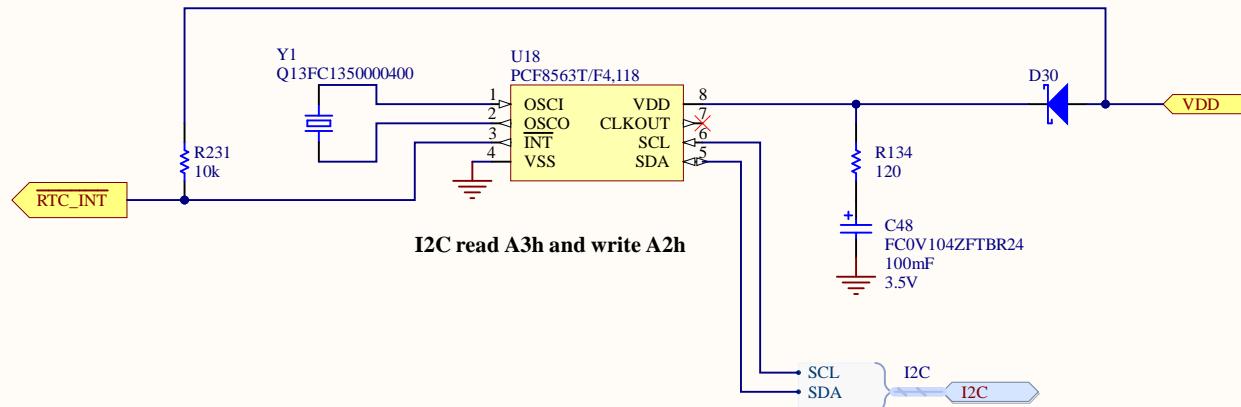
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Title: RTC

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:44:40

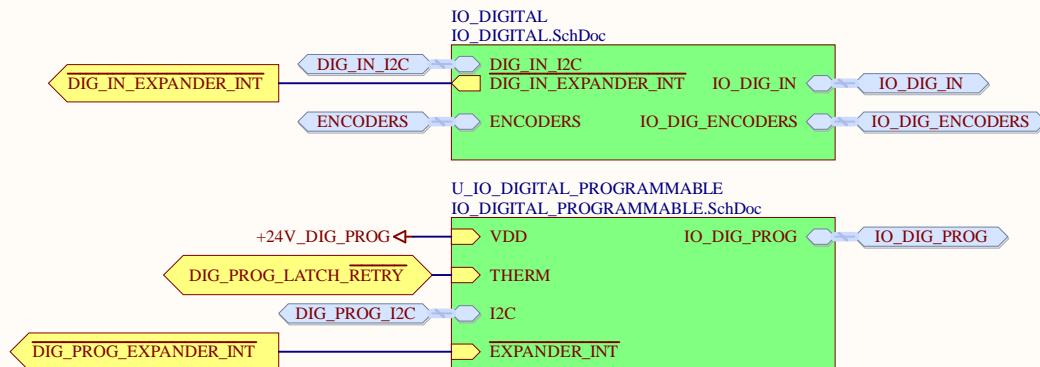
Sheet 10 of 19

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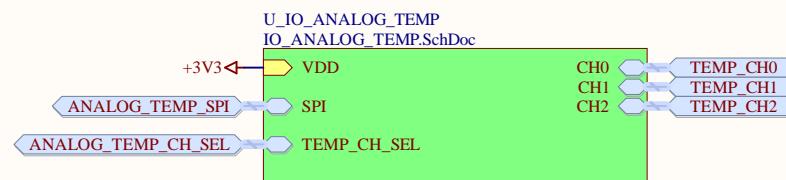
Author: S.Navaretti



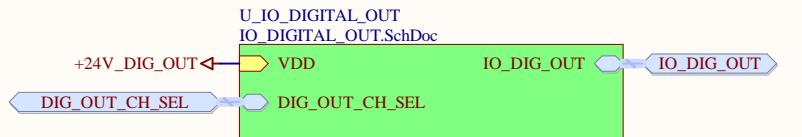
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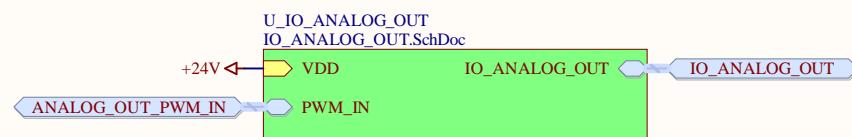
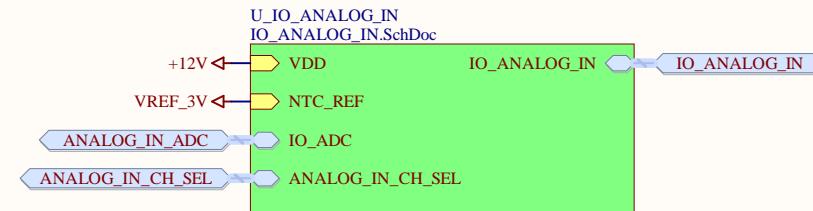
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Title: IO TOP

ID: ASX00024

Revision: V1.3

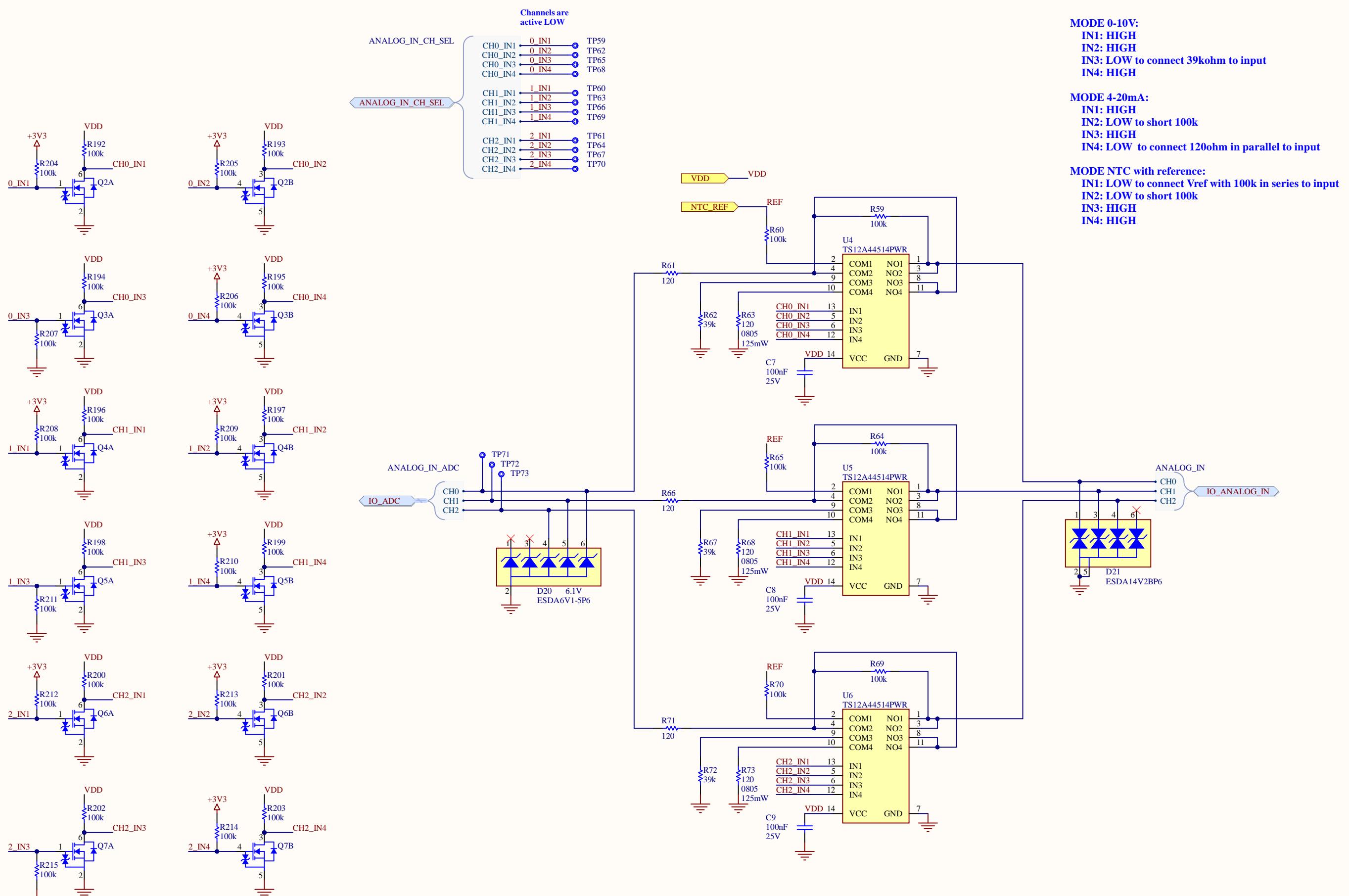
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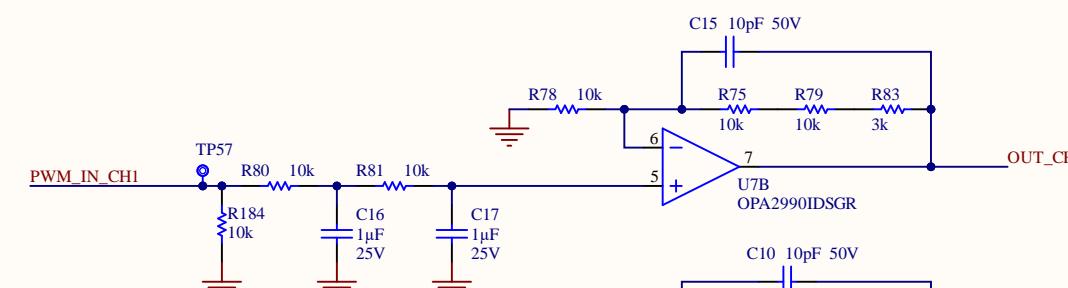
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Author: S.Navaretti

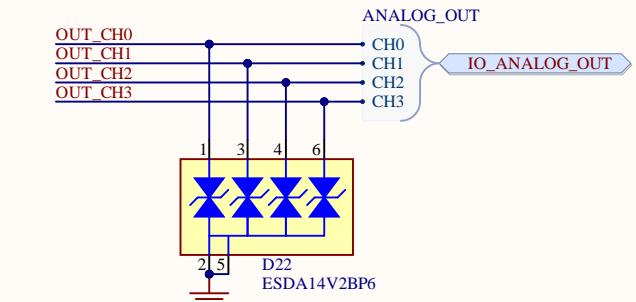
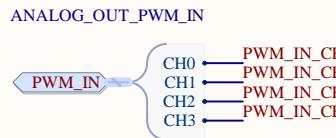
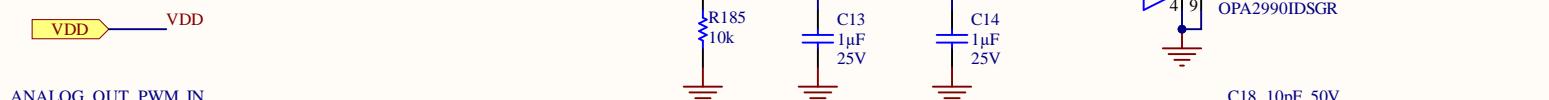




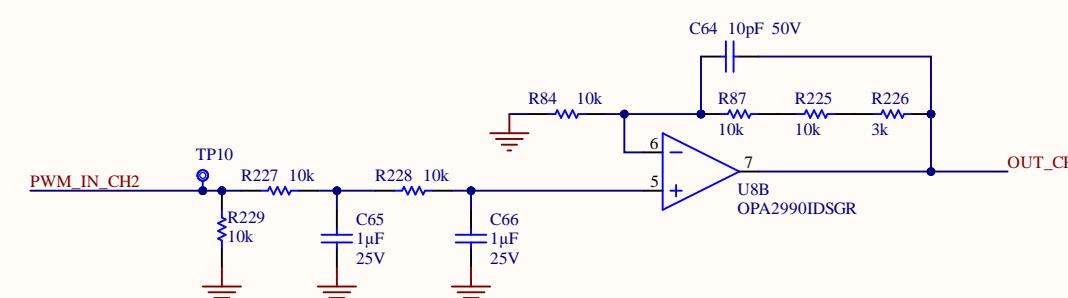
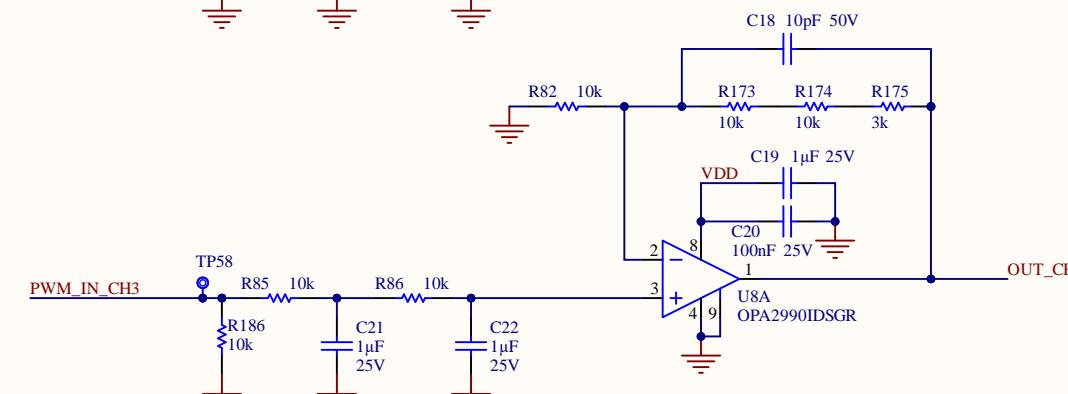
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Title: **ANALOG OUT**

ID: **ASX00024**

Revision: **V1.3**



Date: **2022-08-11**

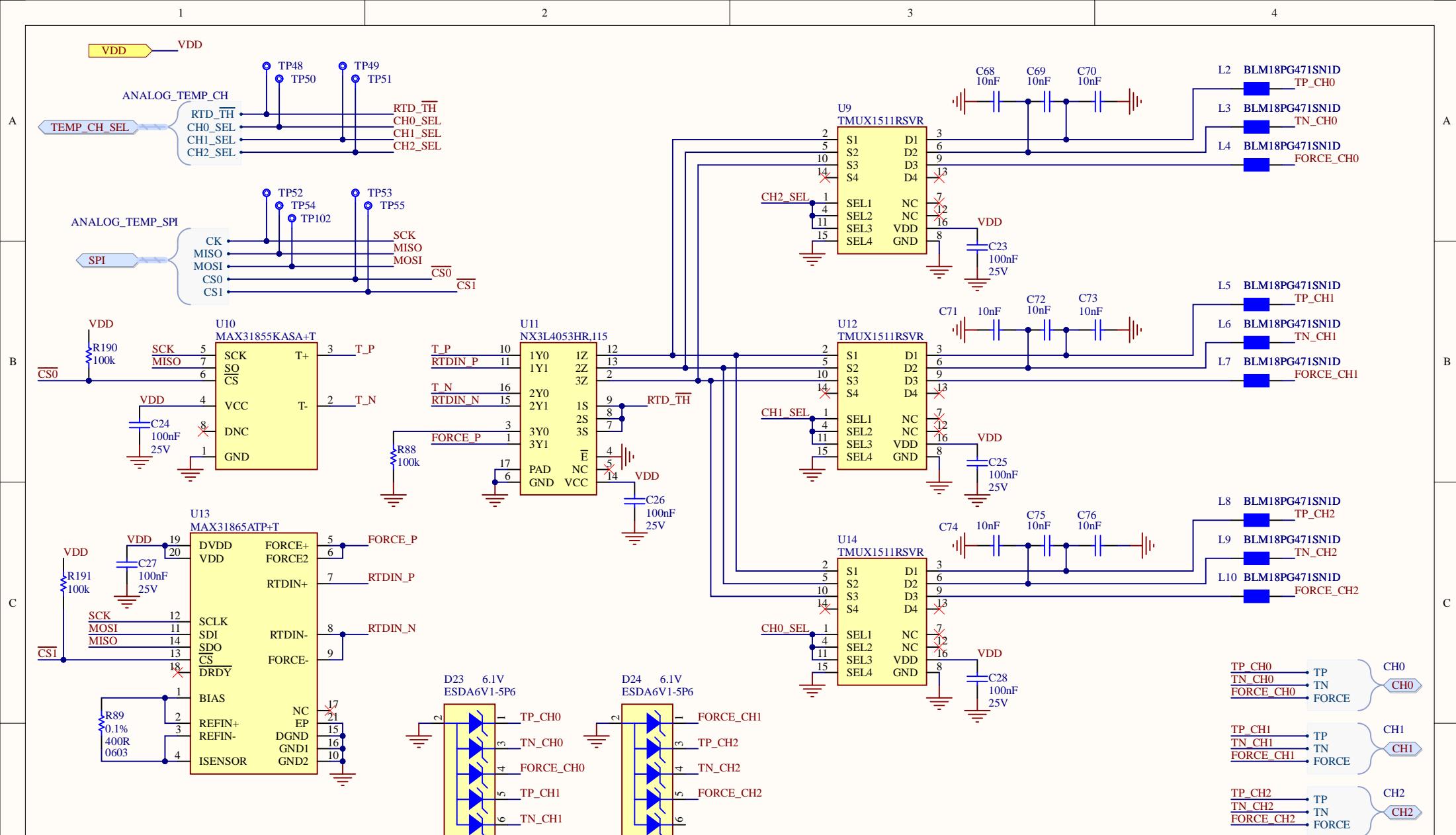
Time: **13:44:49**

Sheet **13 of 19**

File: **IO_ANALOG_OUT.SchDoc**

Author: **S.Navaretti**

RevAuthor: **S.Navaretti**



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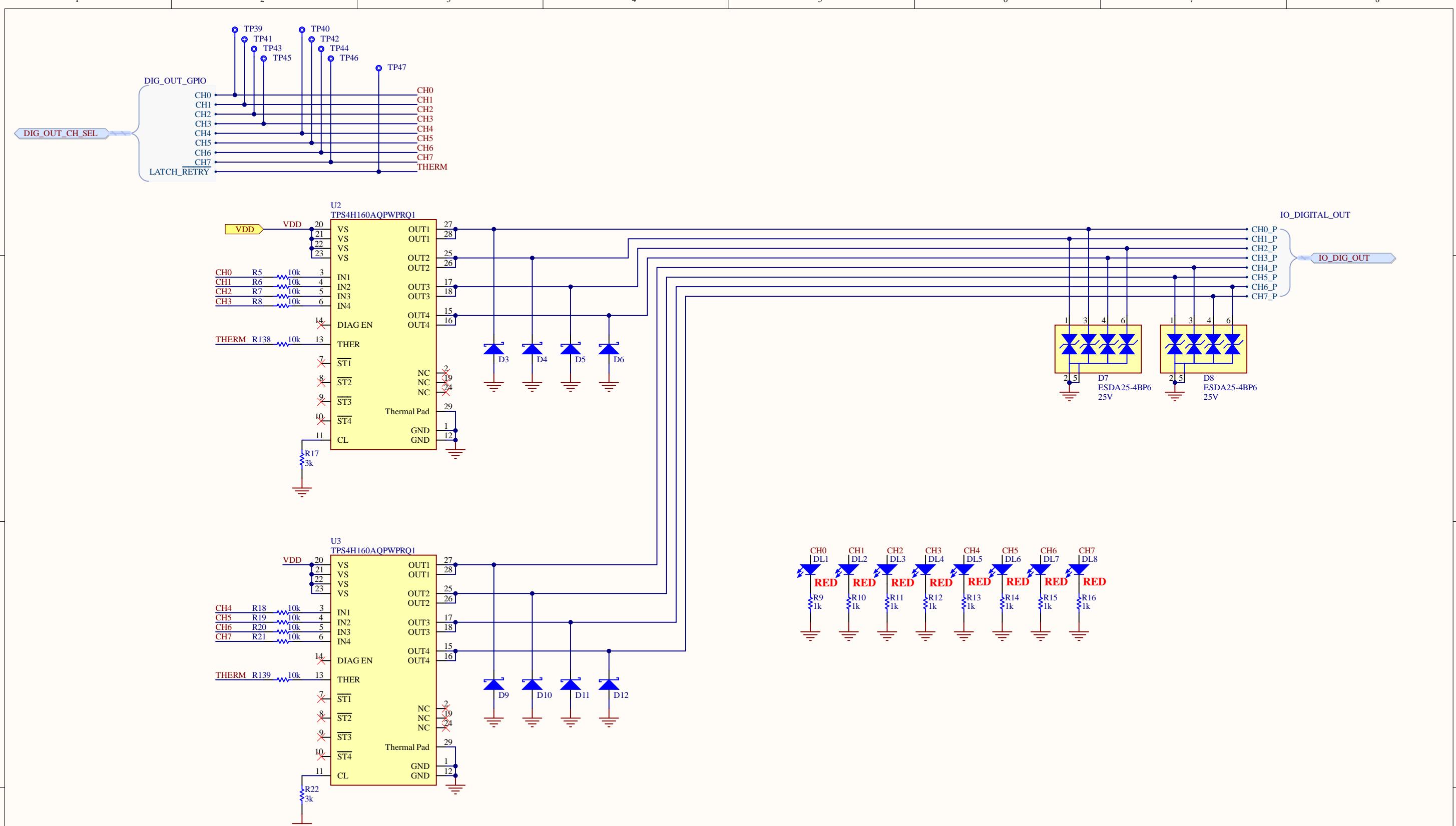
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Title: ANALOG TEMP

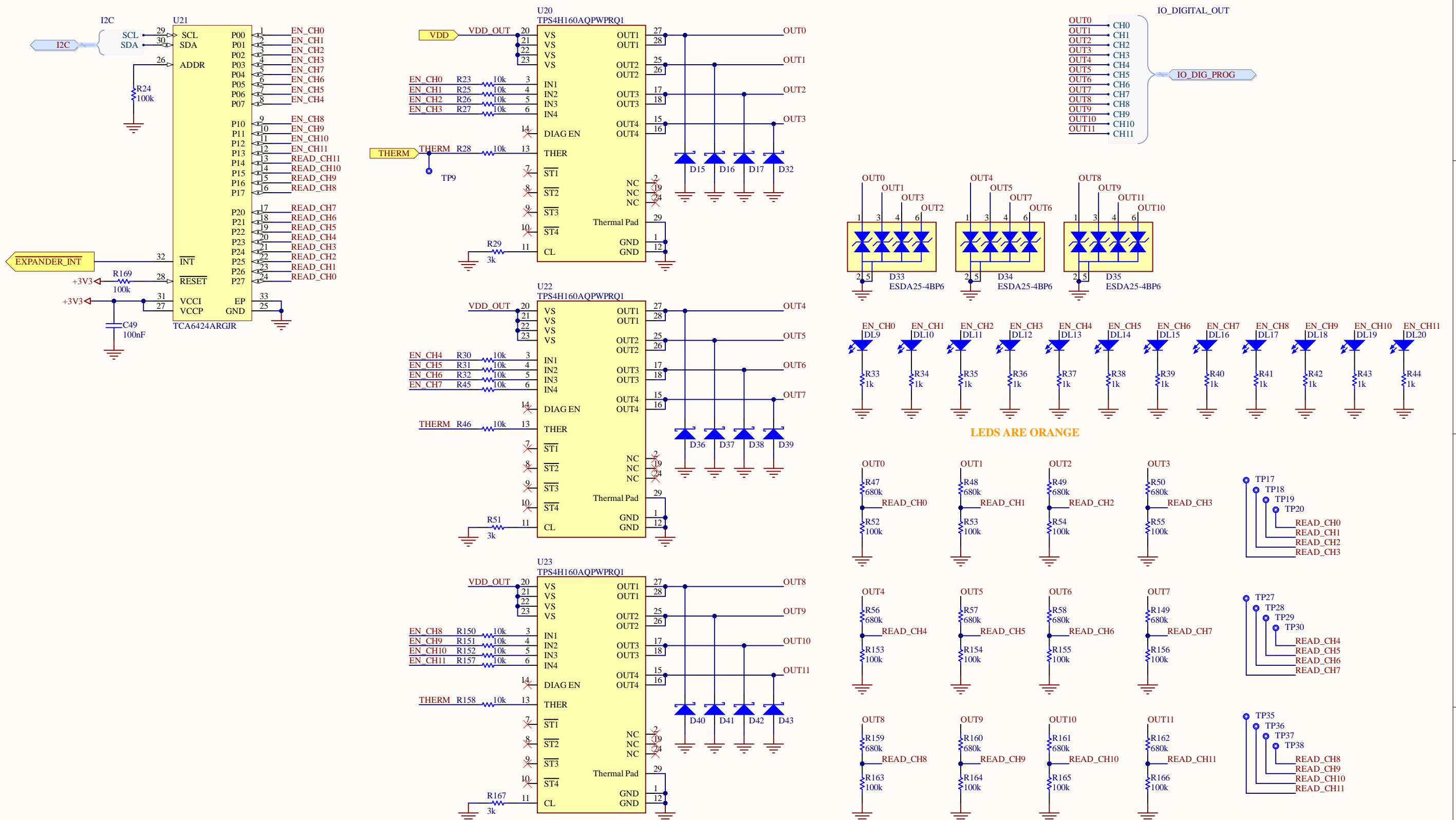
Title: ANALOG TEMP
 ID: ASX00024 Revision: V1.3
 Date: 2022-08-11 Time: 13:44:52 Sheet 14 of 19
 File: IO_ANALOG_TEMP.SchDoc Author: S.Navaretti RevAuthor: S.Navaretti

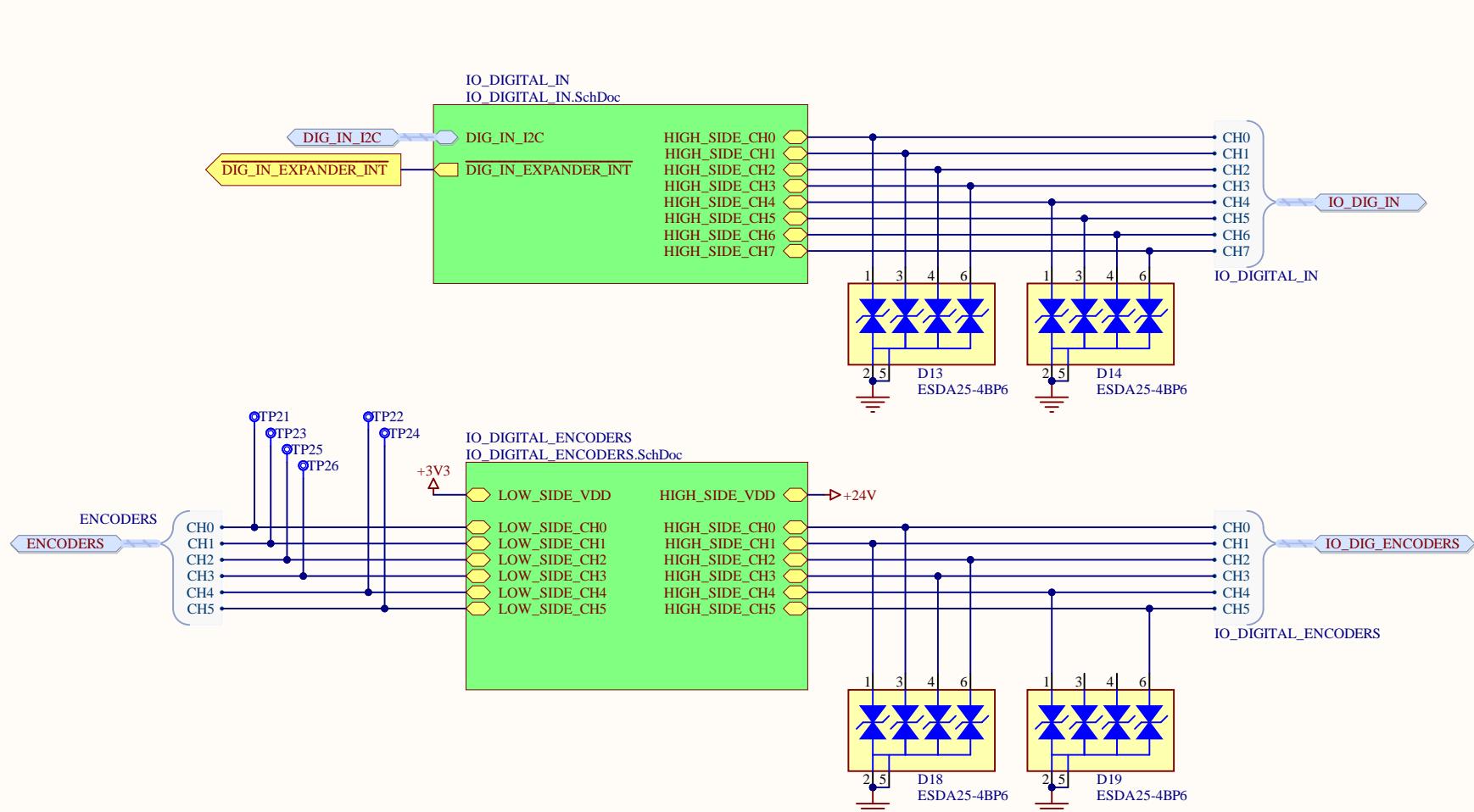


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Title: DIGITAL OUT			
ID: ASX00024	Revision: V1.3		
Date: 2022-08-11	Time: 13:44:55	Sheet 15 of 19	
File: IO_DIGITAL_OUT.SchDoc	Author: S.Navaretti		
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Title: TOP DIGITAL IN / ENCODERS

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:45:01

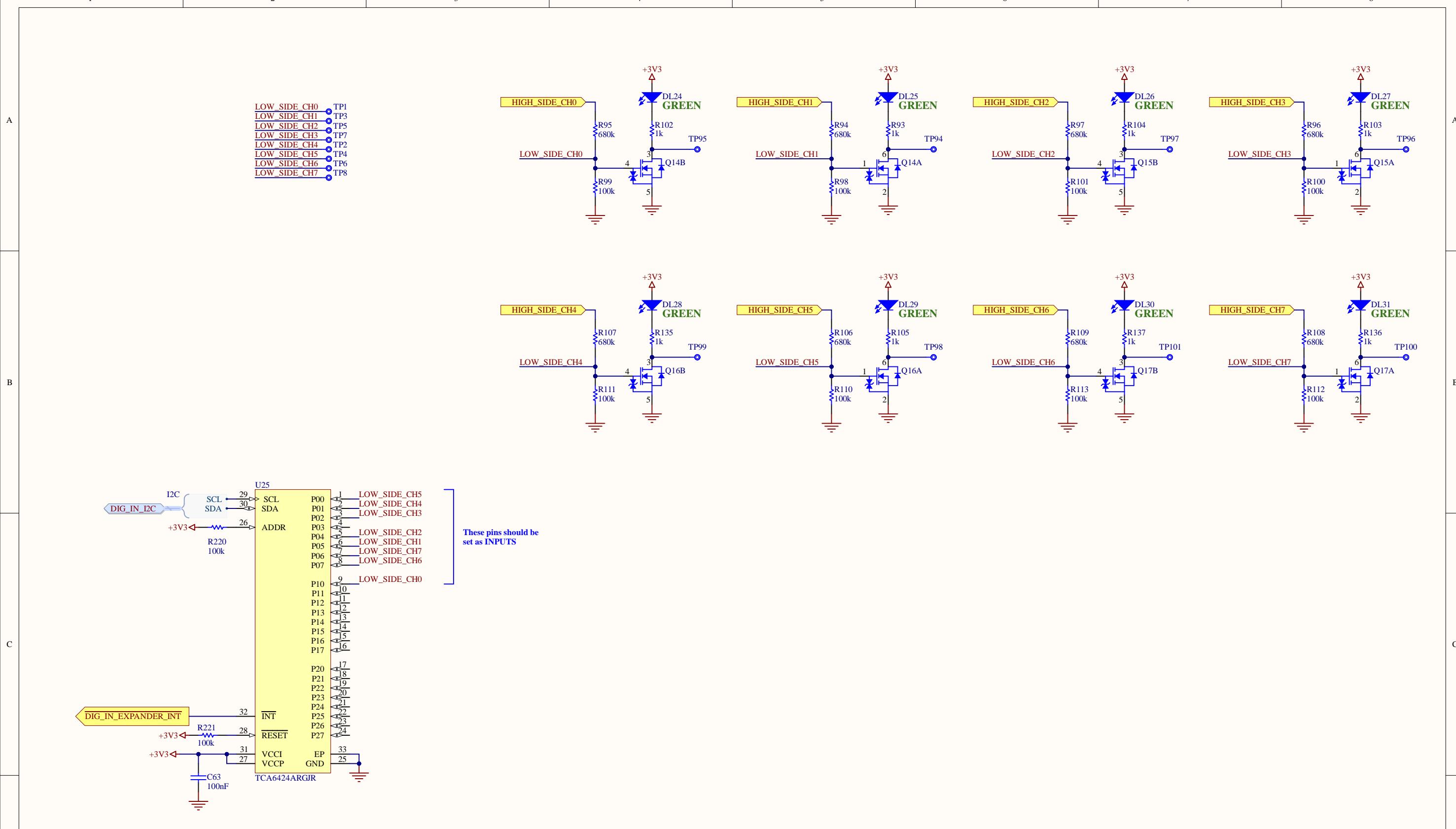
Sheet 17 of 19

File: IO_DIGITAL.SchDoc

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RevAuthor: S.Navaretti





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Title: **DIGITAL IN**

ID: **ASX00024**

Revision: **V1.3**



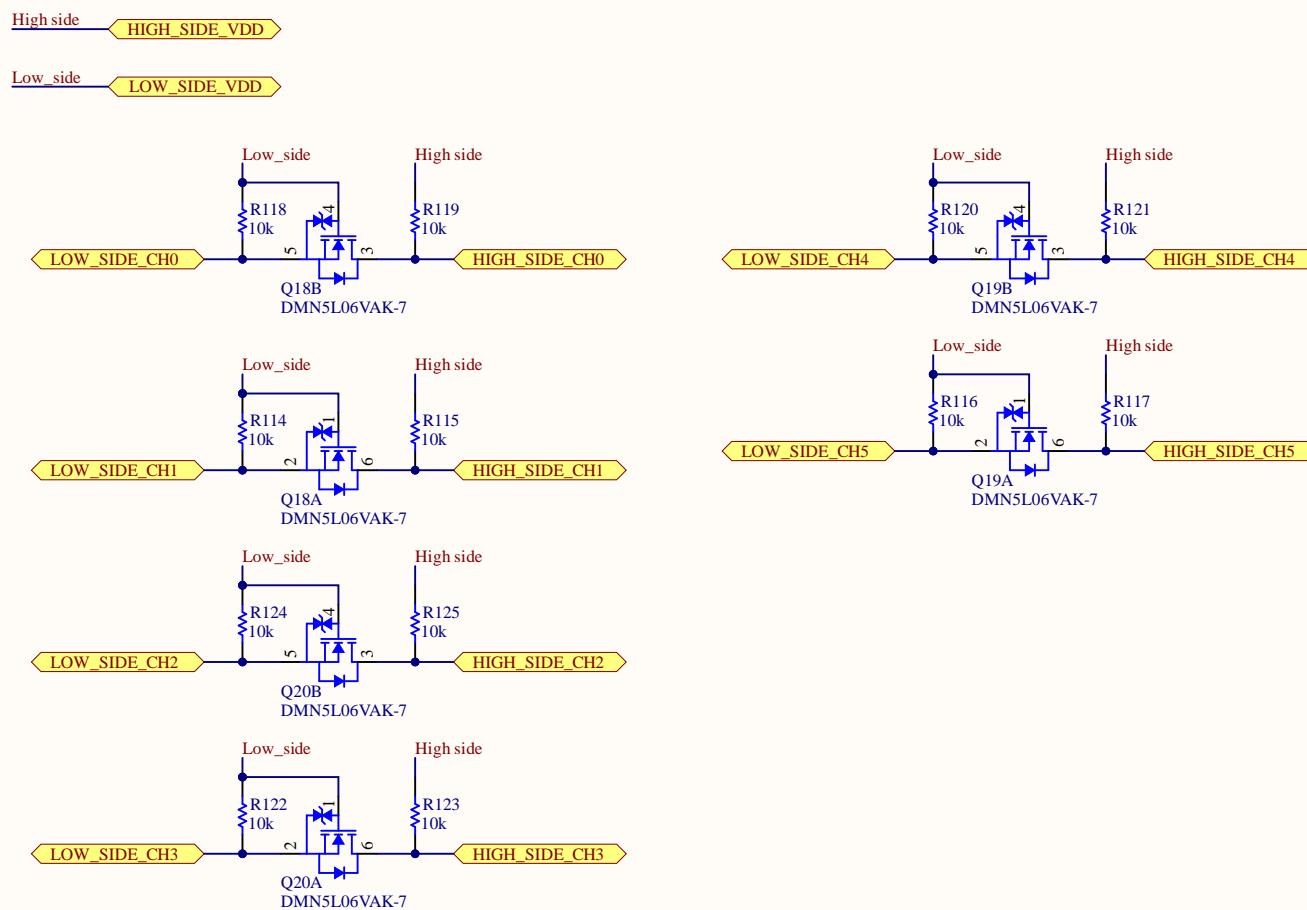
Date: **2022-08-11** Time: **13:45:04** Sheet **18 of 19**

File: **IO_DIGITAL_IN.SchDoc**

Author: **S.Navaretti**

RevAuthor: **S.Navaretti**

A



B

C

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A

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D

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Title: DIGITAL ENCODERS

ID: ASX00024

Revision: V1.3

Date: 2022-08-11 Time: 13:45:07

Sheet 19 of 19

File: IO_DIGITAL_ENCODERS.SchDoc

Author: S.Navaretti

