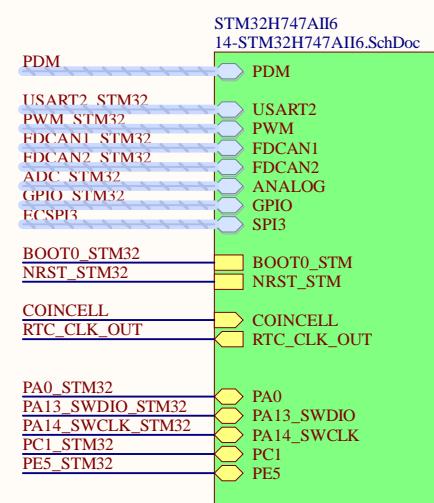
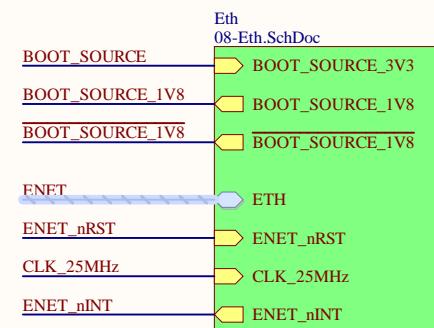
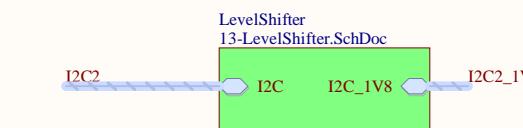
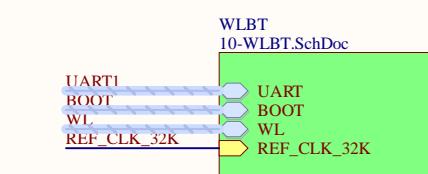
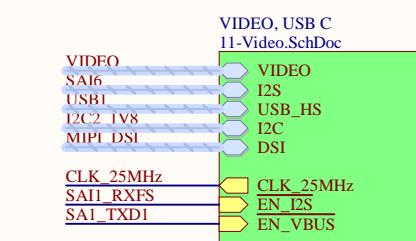
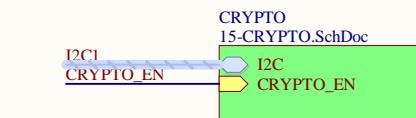
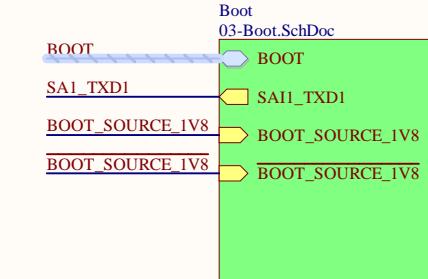
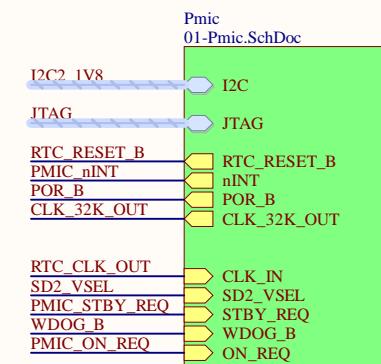
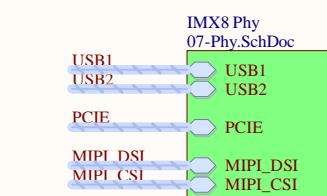
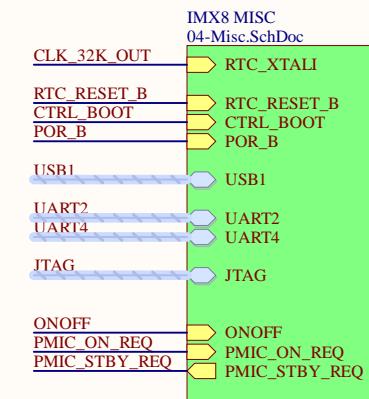
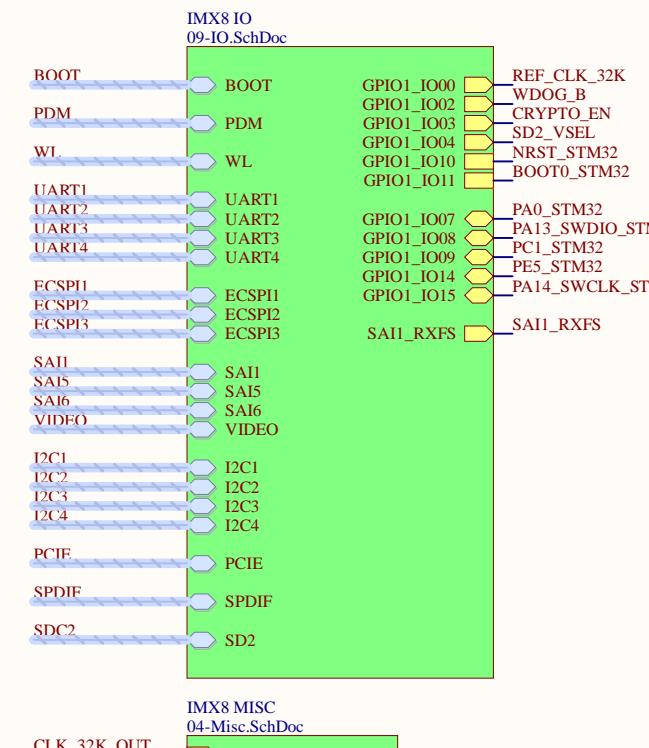
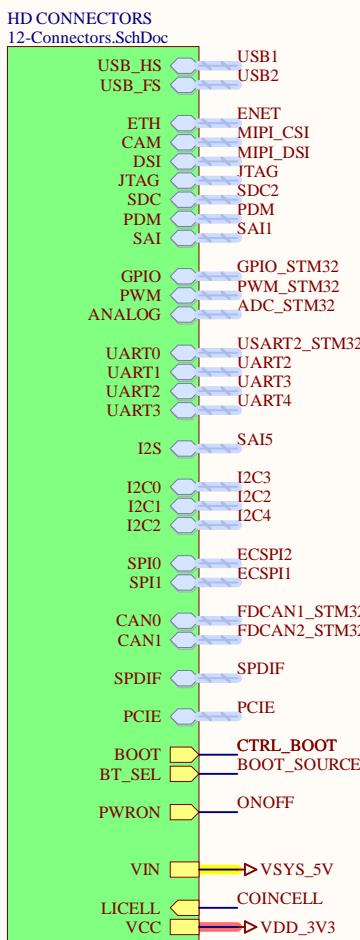


A



Title: TOP

ID: 1

Revision: V4.5

Date: 6/3/2025 Time: 3:40:06 PM Sheet 1 of 16

File: 00-TOP.SchDoc



B

C

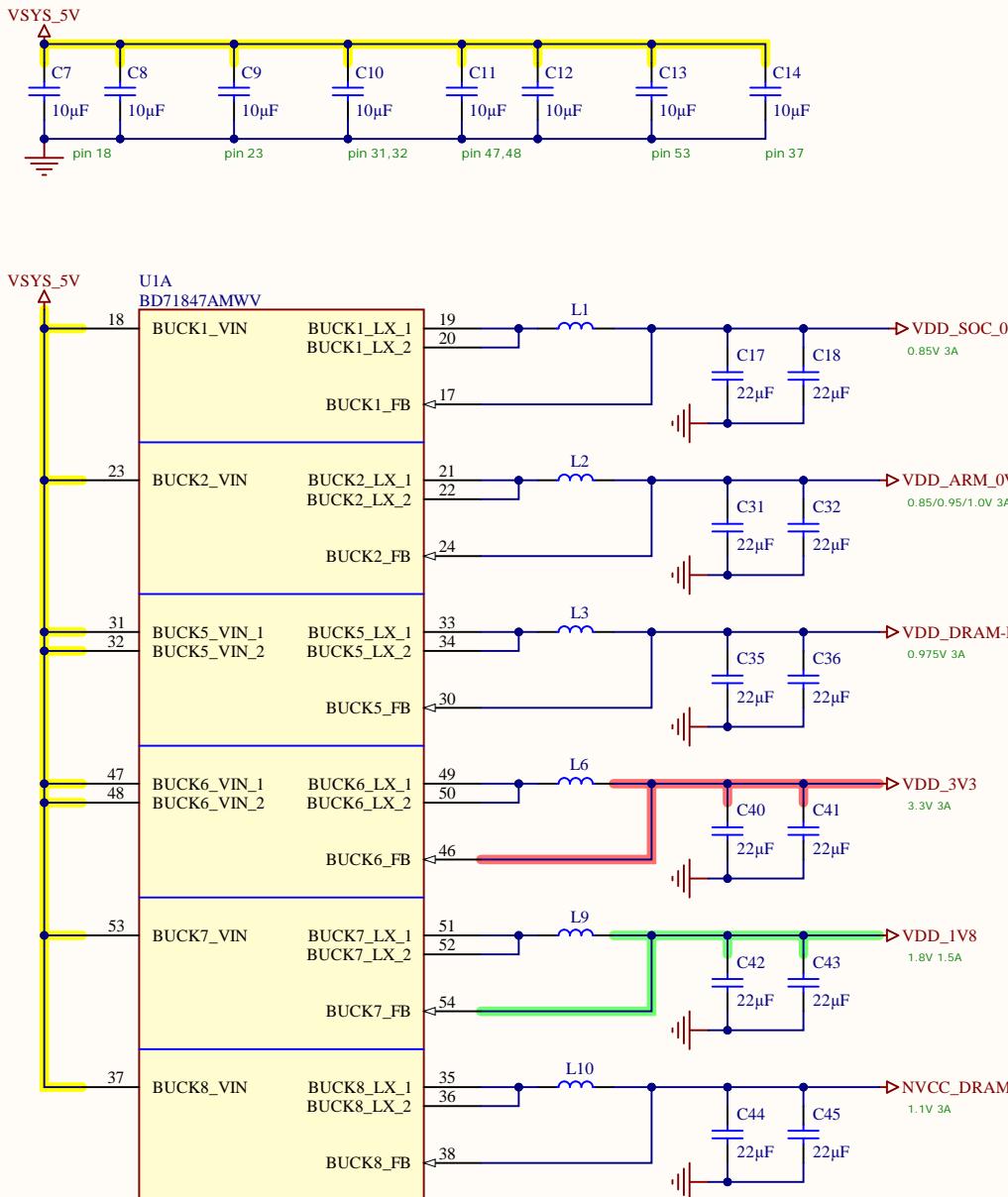
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A

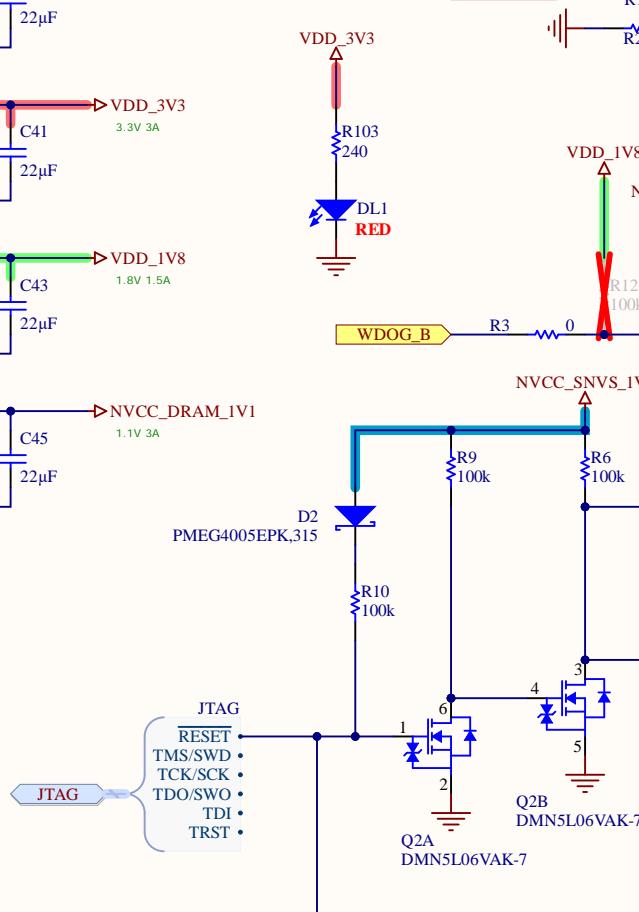
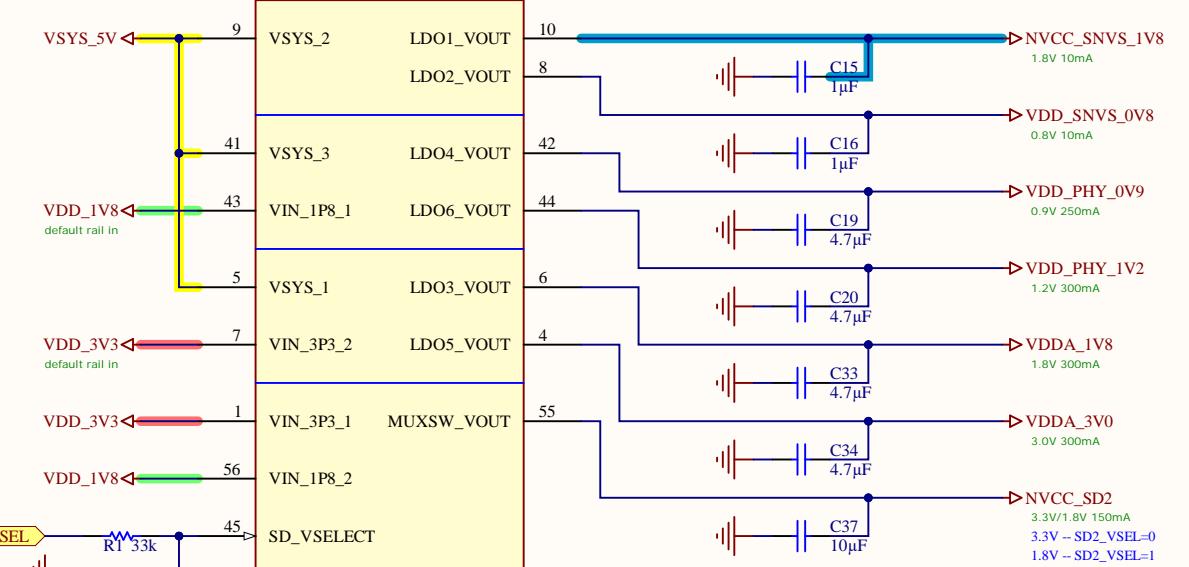
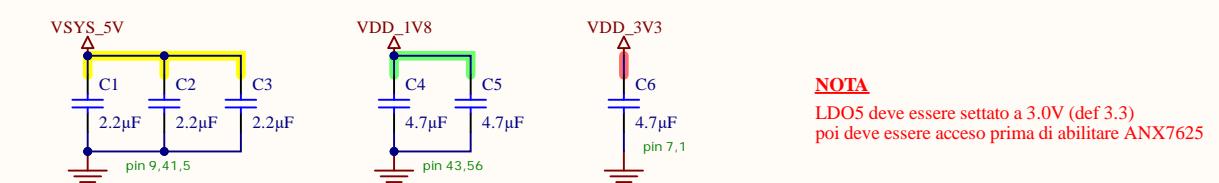
B

C

D

IMX8Mmini PMIC

VDD_SOC_0V8 → VDD_SOC_0V8
 VDD_ARM_0V9 → VDD_ARM_0V9
 VDD_DRAM_PU_0V9 → VDD_DRAM_PU_0V9
 VDD_3V3 → VDD_3V3
 VDD_1V8 → VDD_1V8
 NVCC_DRAM_1V1 → NVCC_DRAM_1V1
 NVCC_SNVS_1V8 → NVCC_SNVS_1V8
 VDD_SNVS_0V8 → VDD_SNVS_0V8
 VDD_PHY_0V9 → VDD_PHY_0V9
 VDD_PHY_1V2 → VDD_PHY_1V2
 VDDA_1V8 → VDDA_1V8
 NVCC_SD2 → NVCC_SD2
 VSYS_5V → VSYS_5V



NOTA
 LDO5 deve essere settato a 3.0V (def 3.3)
 poi deve essere acceso prima di abilitare ANX7625

A

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B

B

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D

D

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ID: 2

Revision: V4.5

Date: 6/3/2025

Time: 3:40:07 PM

Sheet 2 of 16

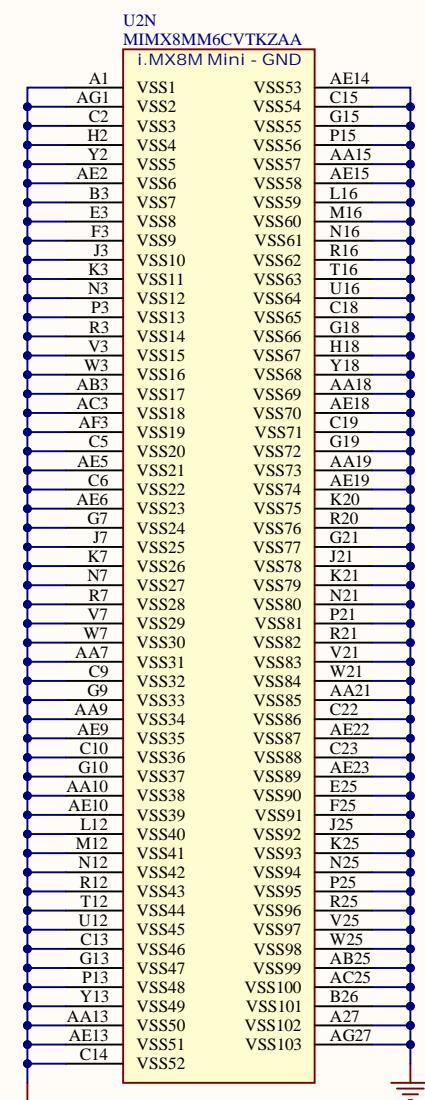
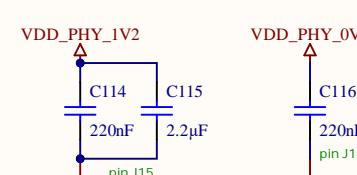
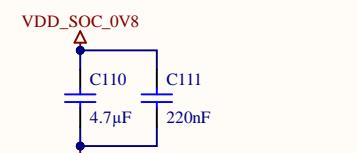
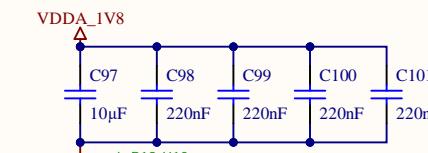
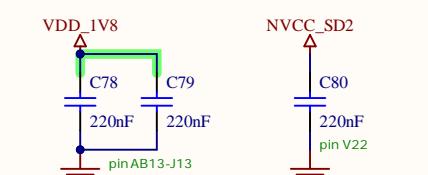
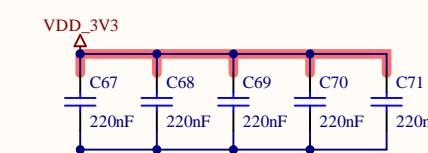
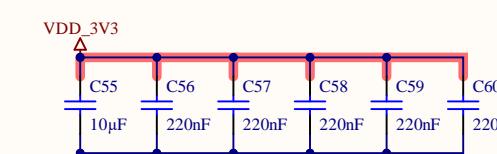
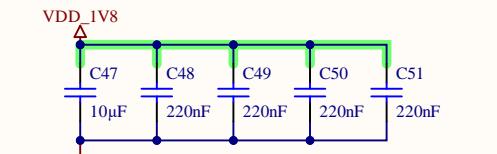
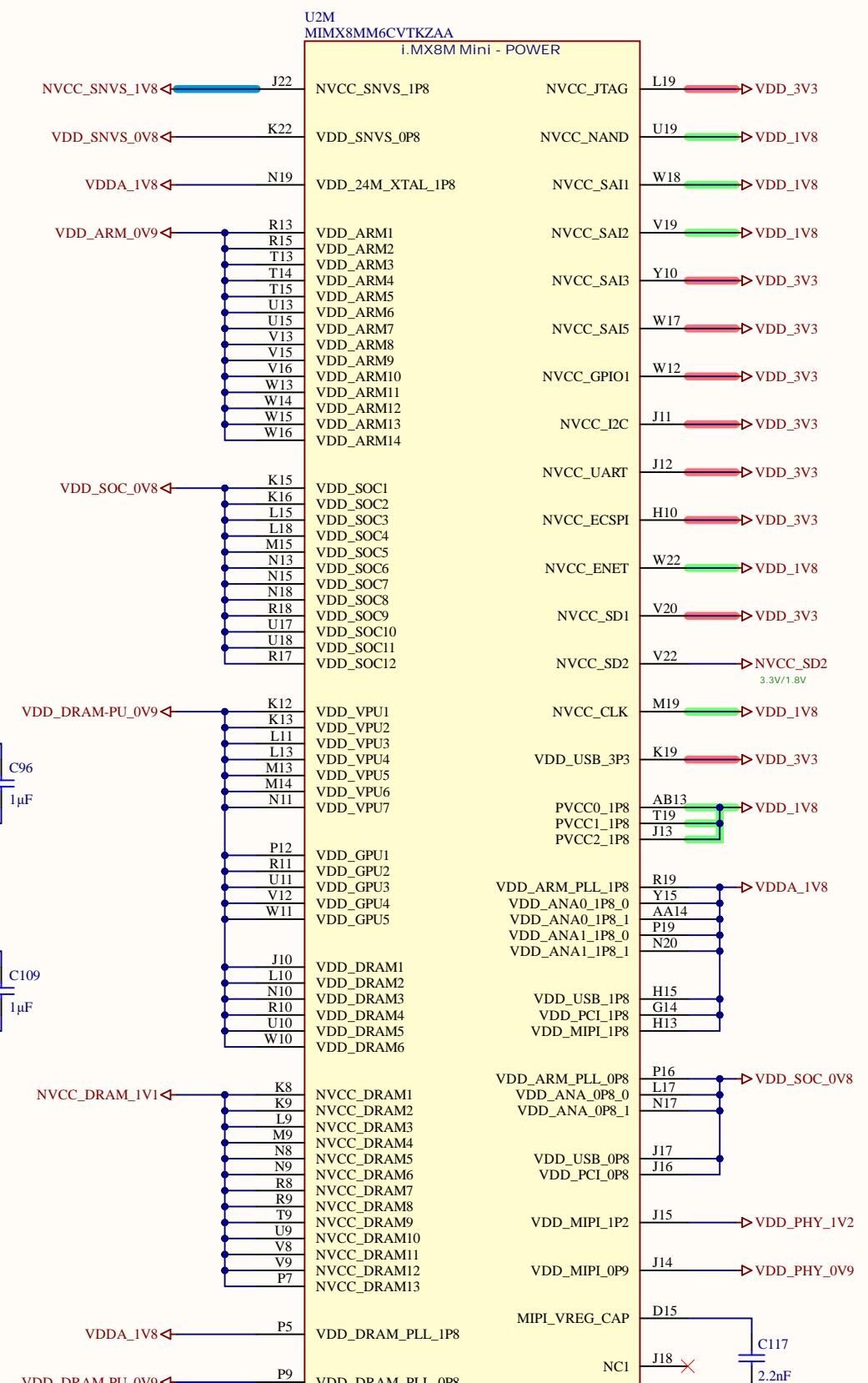
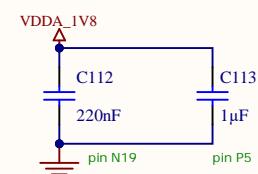
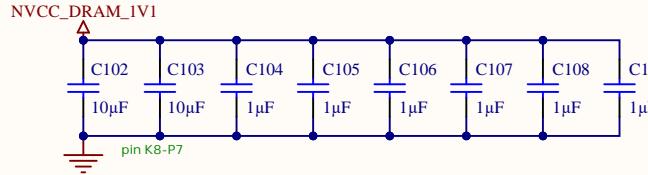
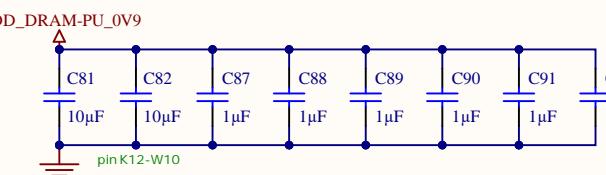
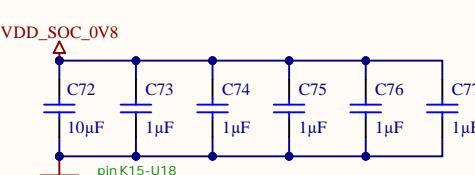
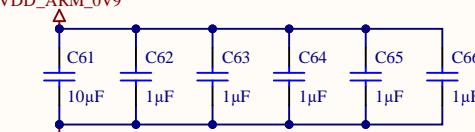
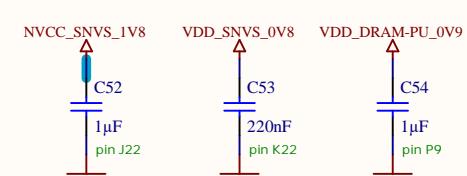
File: 01-Pmic.SchDoc

Author: Dario Pennisi



RevAuthor: Silvio Navaretti

IMX8Mmini POWER



IMX8Mmini BOOT

Boot Pins:							
BOOT_MODE0				BOOT_MODE1			
SAI1_TXD7	BT0_CFG15	SAI1_RXD7	BT0_CFG07				
SAI1_TXD6	BT0_CFG14	SAI1_RXD6	BT0_CFG06				
SAI1_TXD5	BT0_CFG13	SAI1_RXD5	BT0_CFG05				
SAI1_TXD4	BT0_CFG12	SAI1_RXD4	BT0_CFG04				
SAI1_TXD3	BT0_CFG11	SAI1_RXD3	BT0_CFG03				
SAI1_TXD2	BT0_CFG10	SAI1_RXD2	BT0_CFG02				
SAI1_TXD1	BT0_CFG09	SAI1_RXD1	BT0_CFG01				
SAI1_TXD0	BT0_CFG08	SAI1_RXD0	BT0_CFG00				

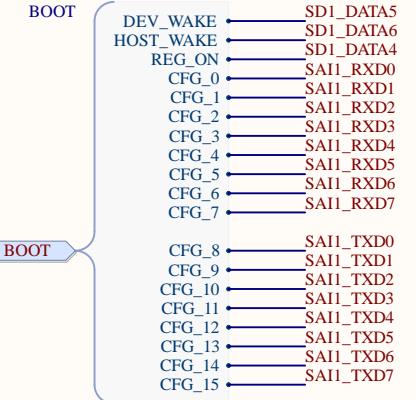
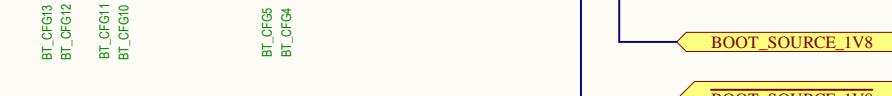
default --> 0 0 1 0 1 0 1 0							
BT_CFG15	BT_CFG14	BT_CFG13	BT_CFG12	BT_CFG11	BT_CFG10	BT_CFG9	BT_CFG8
Infinit-Loop 0 - Disable 1 - Enable	Boot device type 001 - SD/eSD 010 - MMC/eMMC	Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3	Power Cycle Enable '0' - No power cycle '1' - Enabled	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct			

default --> 0 0 0 1 0 0 1 1							
SD		Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50		Reserved
MMC	Fast Boot: 0 - Regular 1 - Fast Boot			Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4)	Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved	USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V

Default boot device: eMMC/SDHC3 - BT_CFG[15:0] = 0 010 10 10 0 010 00 1 1

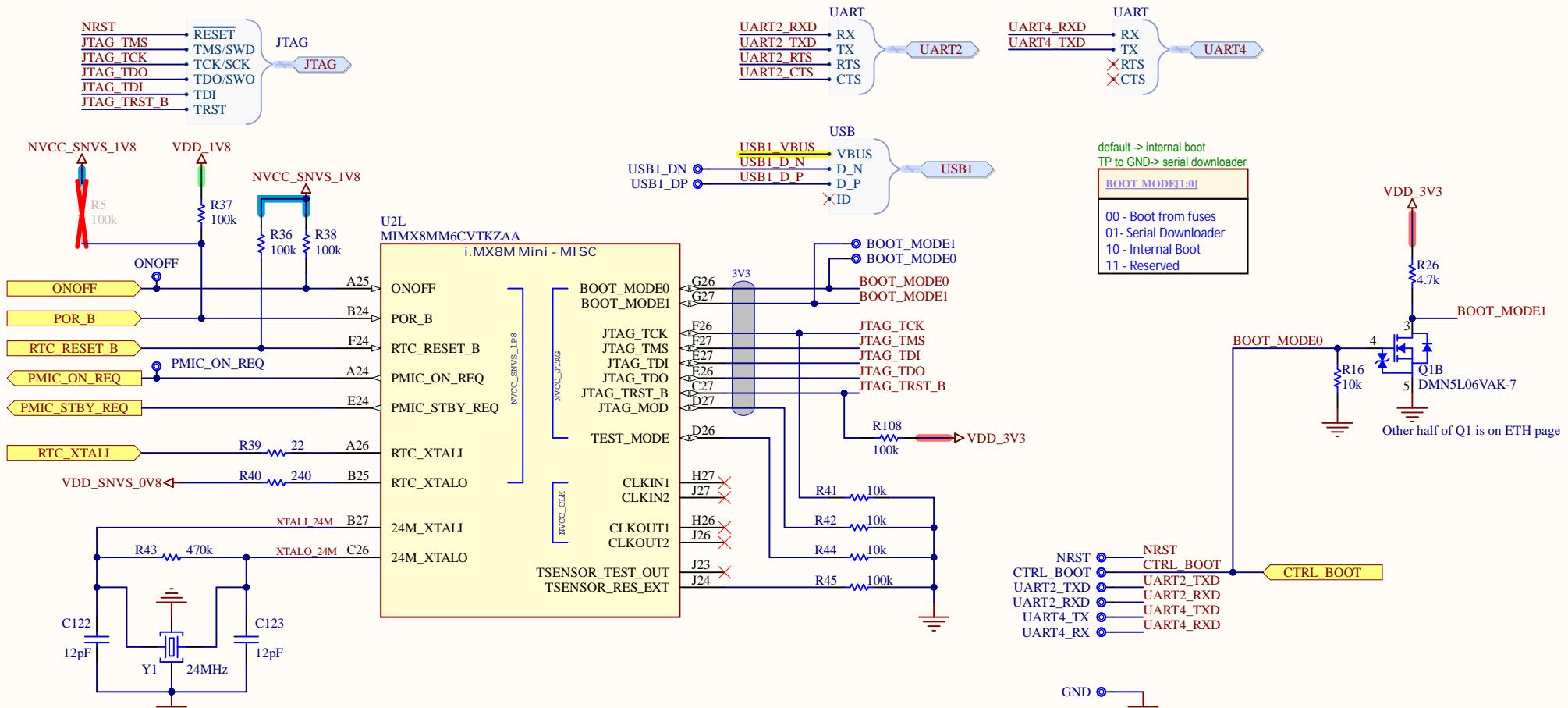


Alternative boot device: uSD/SDHC2 - BT_CFG[15:0] = 0 001 01 10 0 001 00 1 1



ROOT MODE[1:0]	
00	Boot from fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

IMX8Mmini MISC



Mfg Tool

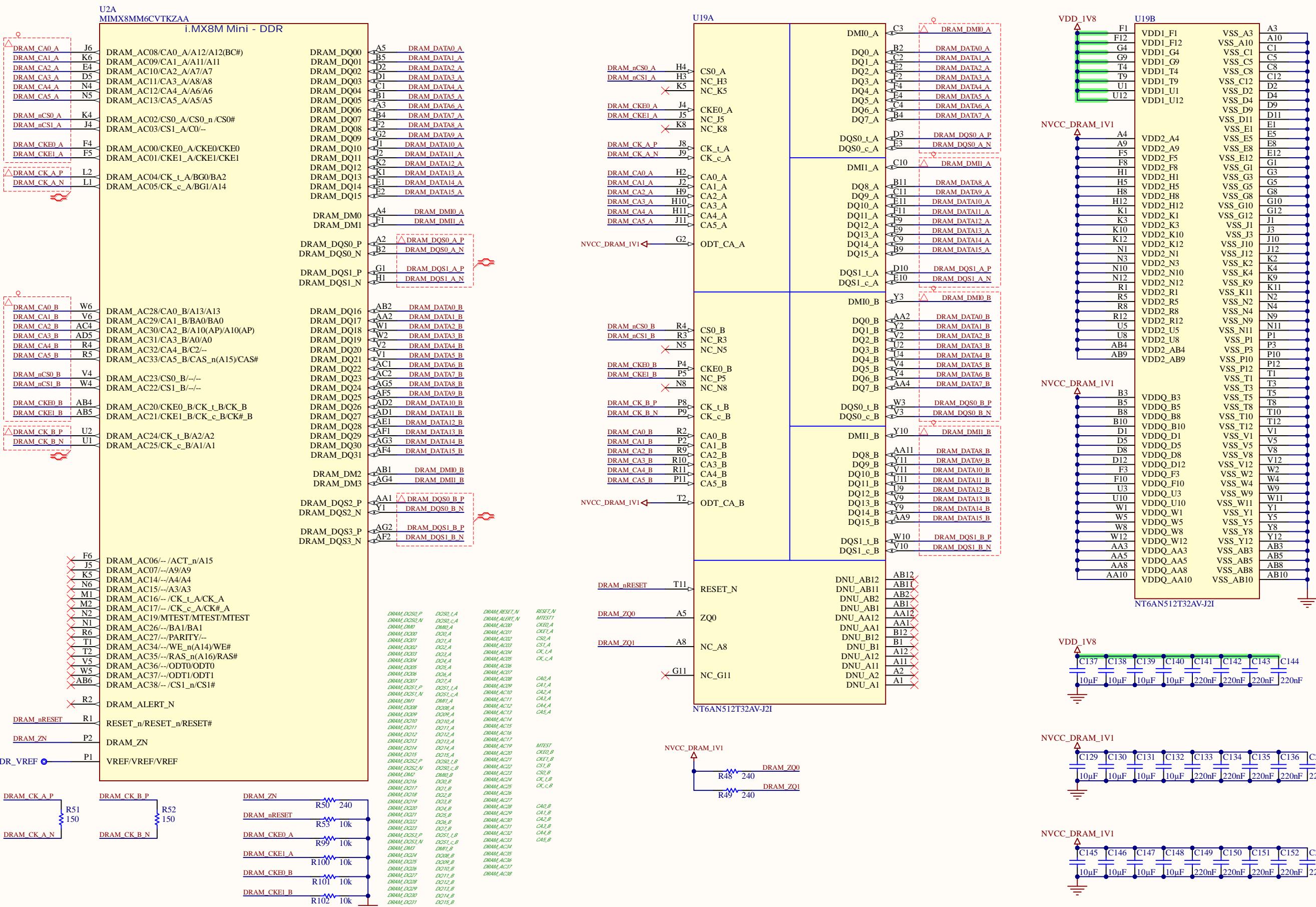
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Title: MISCELLANEOUS

ID: 5	Revision: V4.5
Date: 6/3/2025	Time: 3:40:13 PM
Sheet 5 of 16	
File: 04-Misc.SchDoc	Author: Dario Pennisi RevAuthor: *



IMX8Mmini DDR



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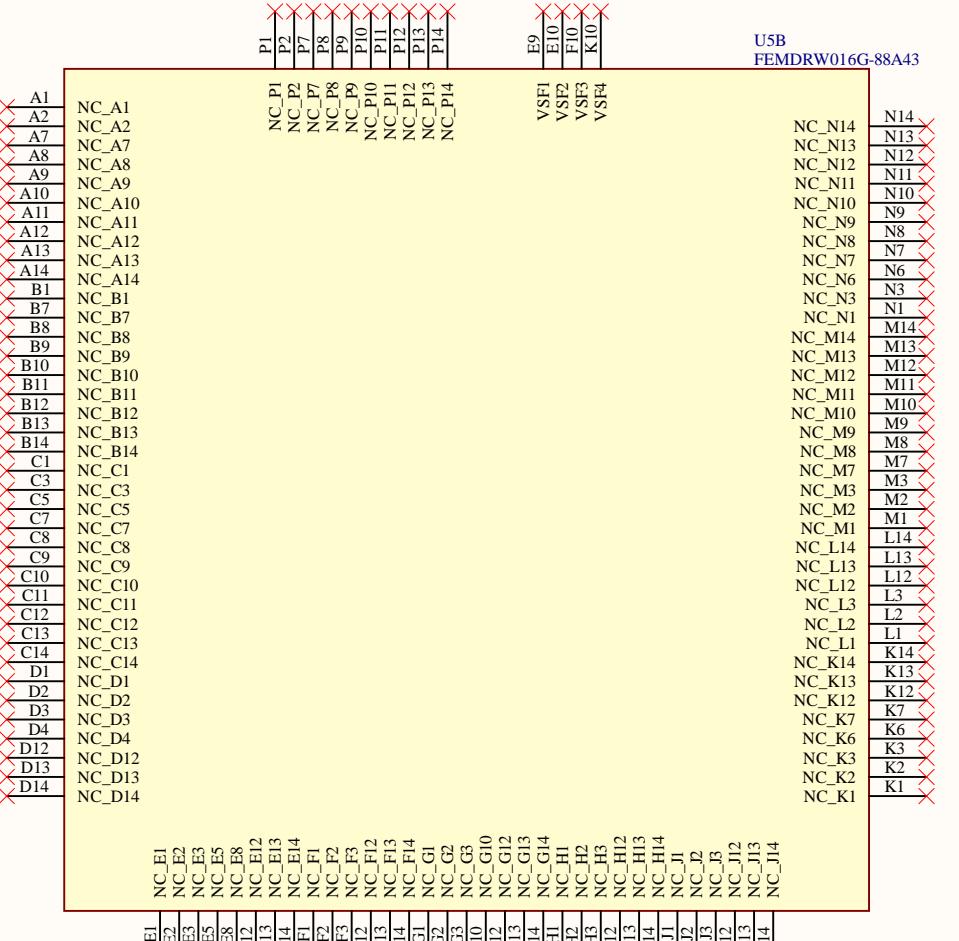
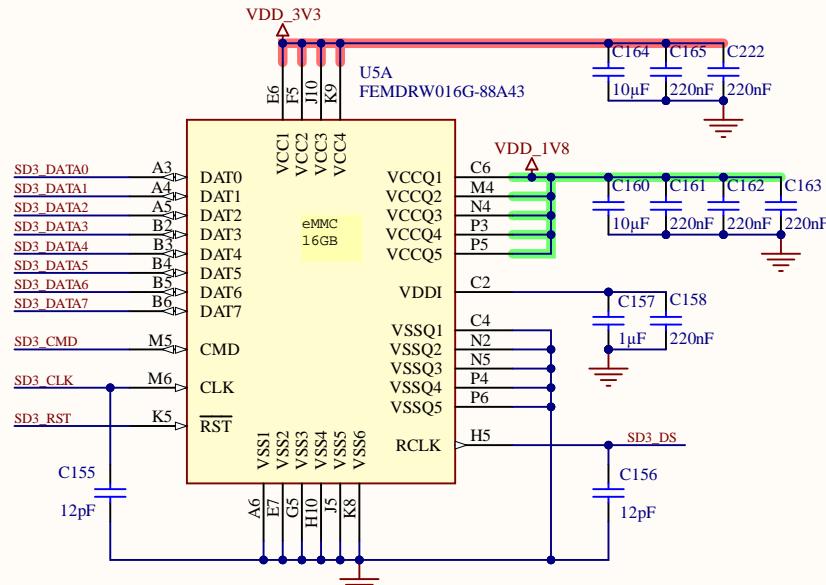
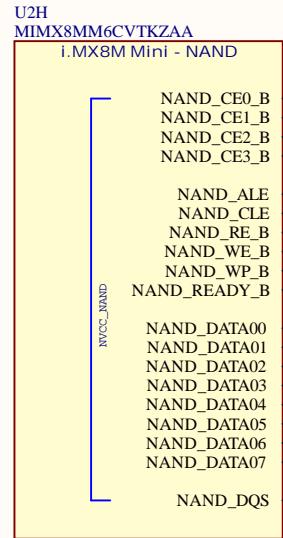
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Title: DDR			
ID: 6	Revision: V4.5		
Date: 6/3/2025	Time: 3:40:15 PM	Sheet 6 of 16	
File: 05-DDr.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti	

IMX8Mmini Memory



A

A

B

B

C

C

D

D

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Title: **MEMORY**

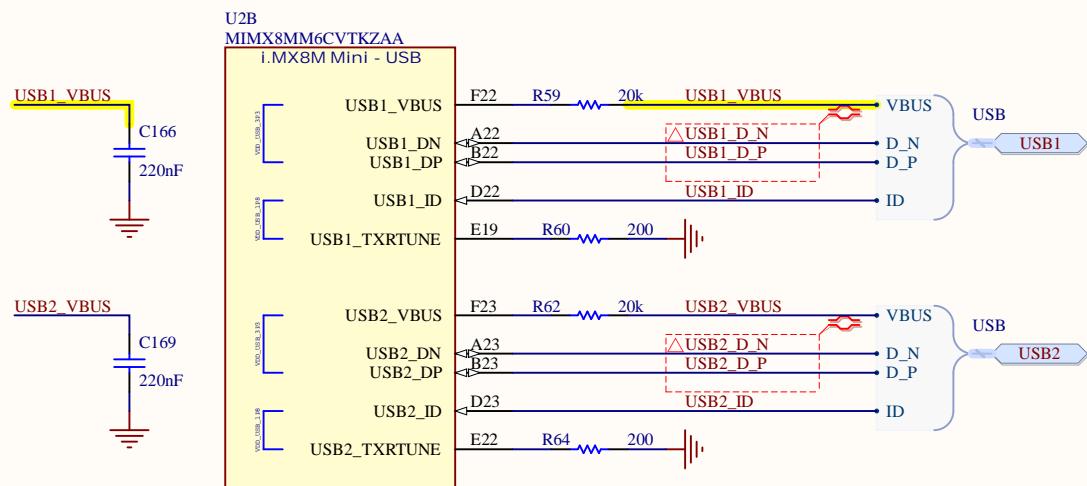
ID: 7	Revision: V4.5
Date: 6/3/2025	Time: 3:40:17 PM
Sheet 7 of 16	



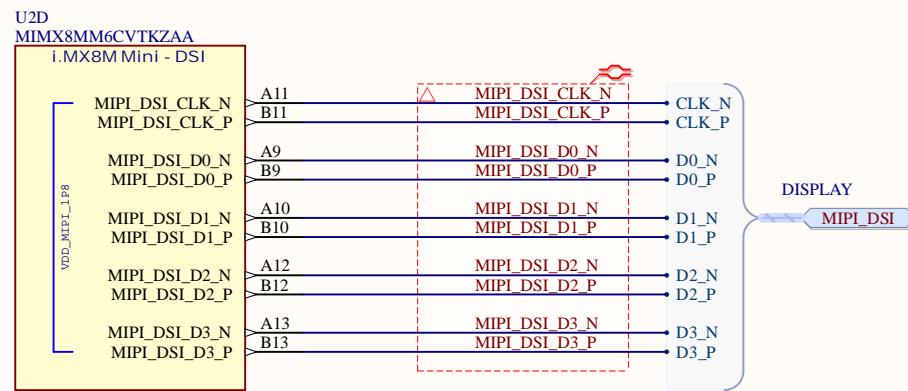
RevAuthor: **Silvio Navaretti**

IMX8Mmini PHY

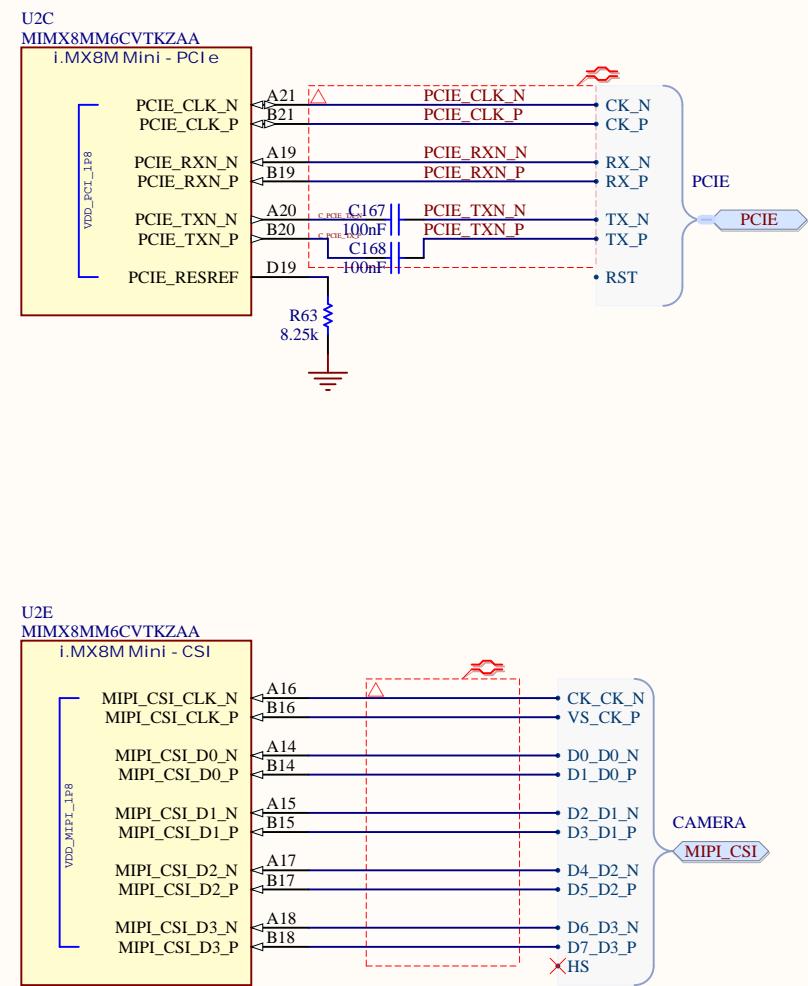
A



B



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D

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Title: **PHY**

ID: **8**

Revision: **V4.5**

Date: **6/3/2025**

Time: **3:40:19 PM**

Sheet **8** of 16

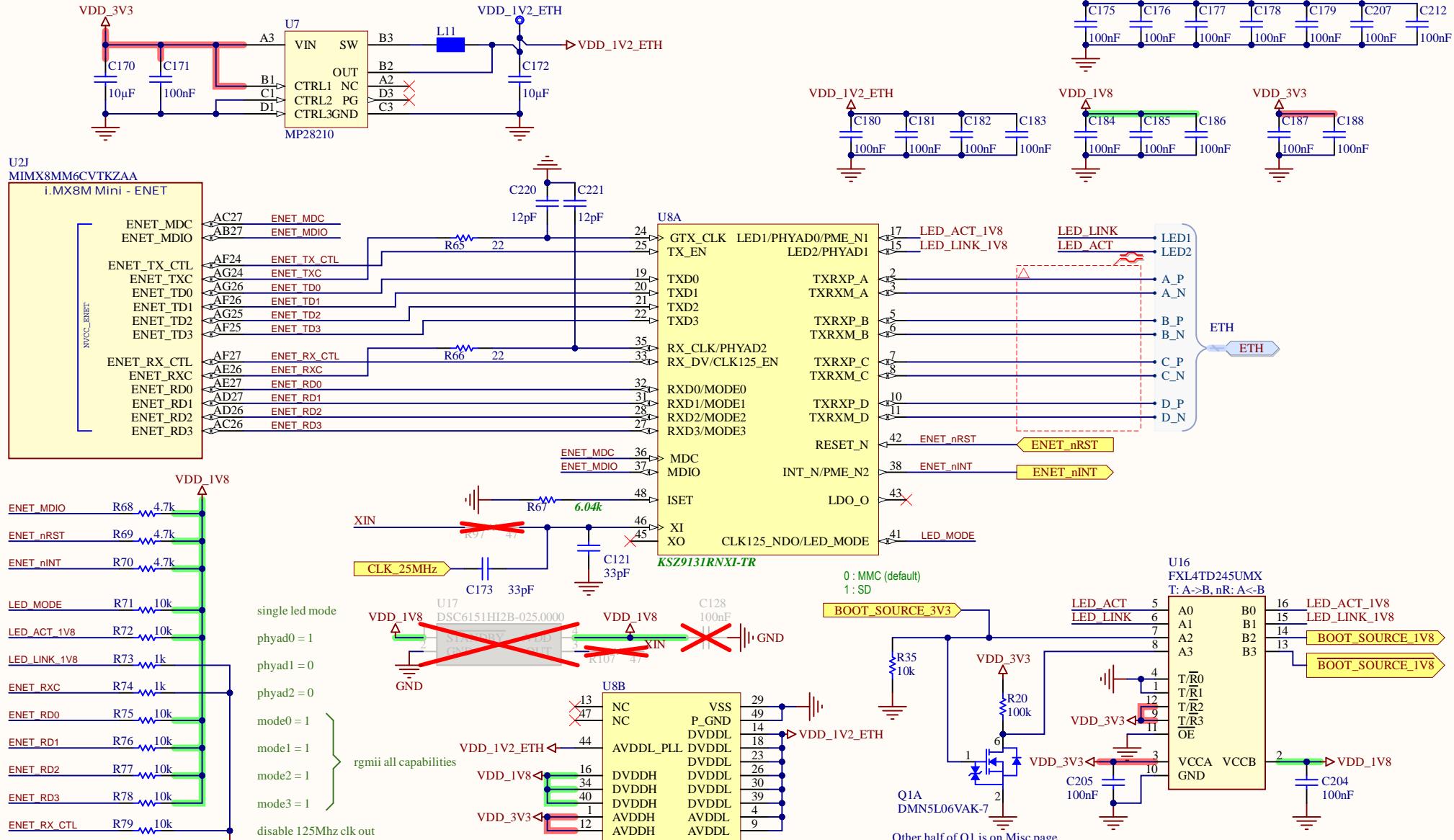
File: **07-Phy.SchDoc**

Author: **Dario Pennisi**



RevAuthor: **Silvio Navaretti**

IMX8Mmini ETH



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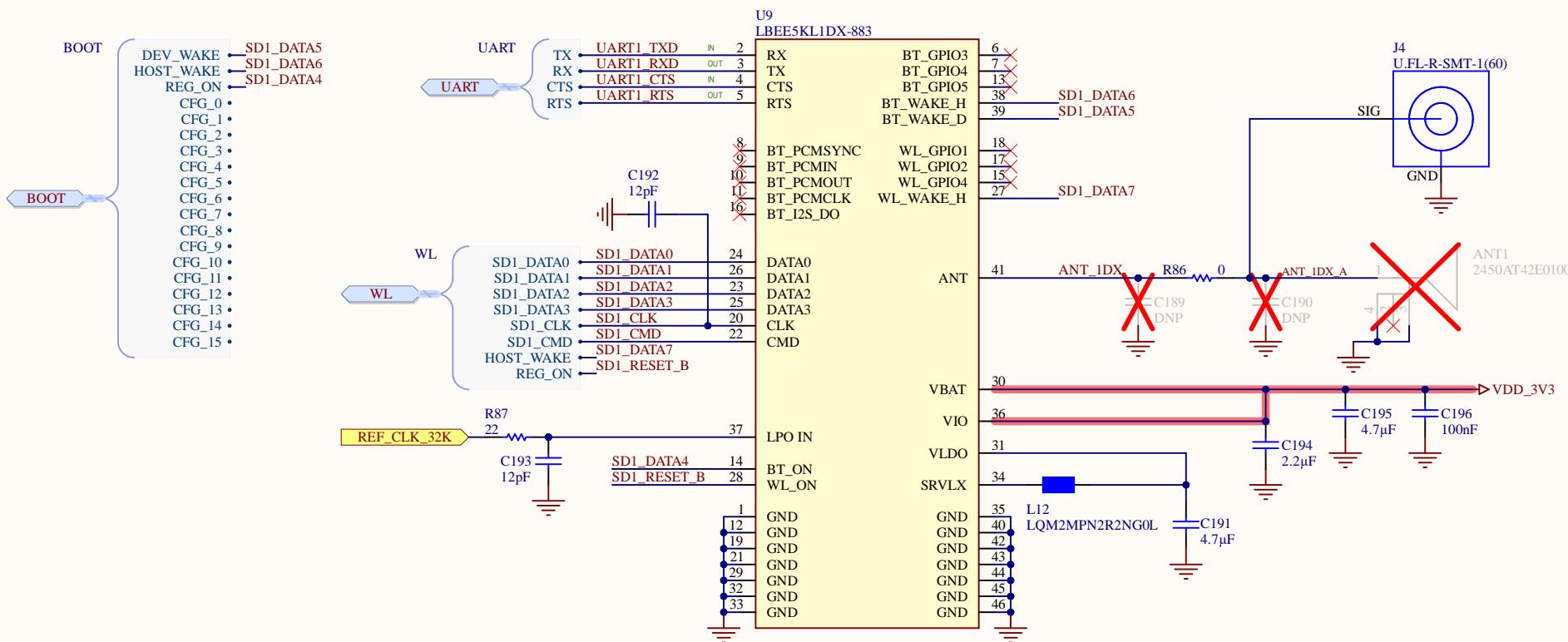
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Title: ETHERNET

ID: 9	Revision: V4.5
Date: 6/3/2025	Time: 3:40:20 PM
File: 08-Eth.SchDoc	Author: Dario Pennisi



IMX8Mmini WL/BT



A

A

B

B

C

C

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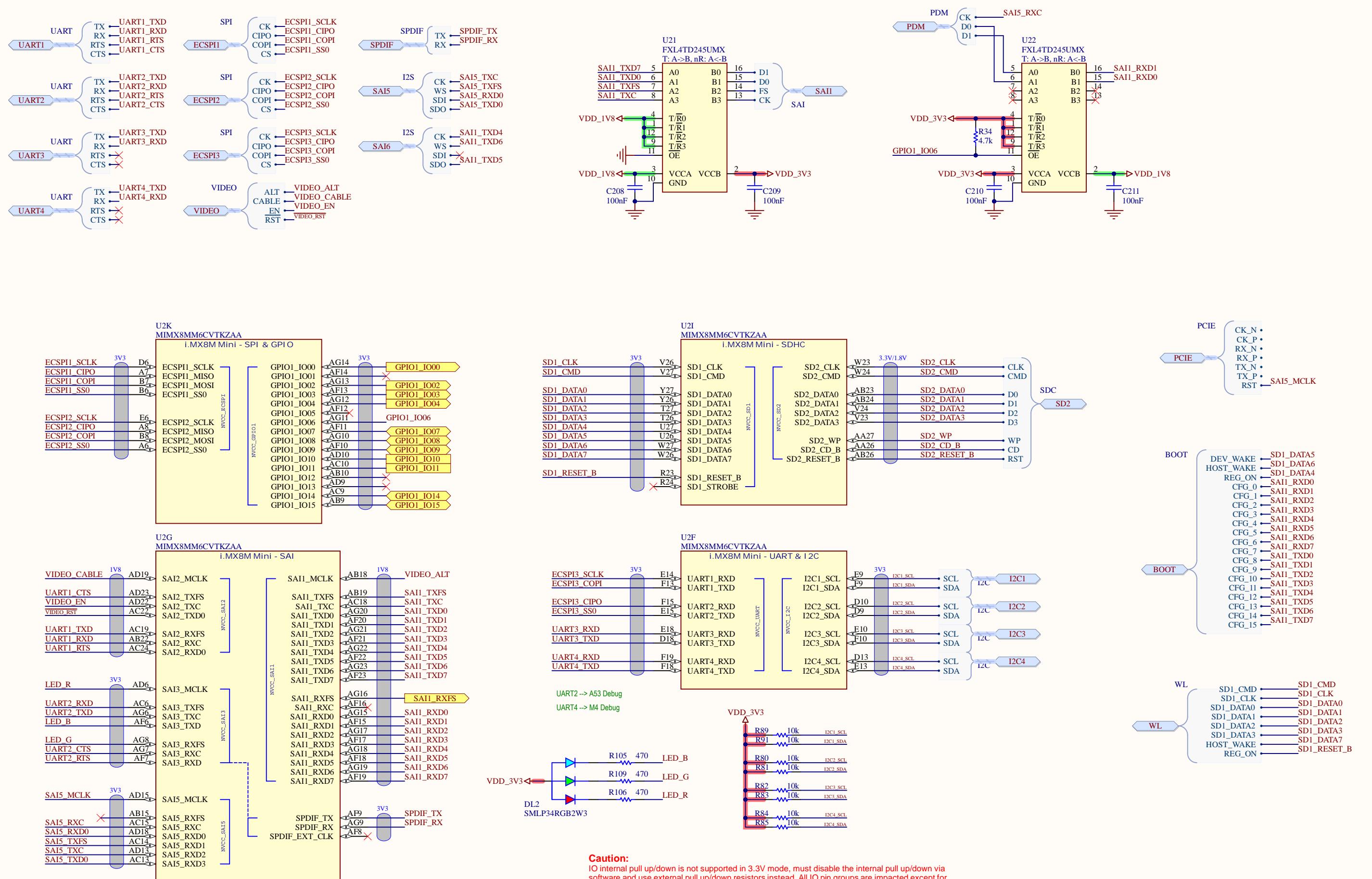
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Title: WLBT

ID: 11	Revision: V4.5
Date: 6/3/2025	Time: 3:40:22 PM
Sheet 10 of 16	



IMX8Mmini IO



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Title: IO

ID: 10

Revision: V4.5

Date: 6/3/2025

Time: 3:40:24 PM

Sheet 11 of 16

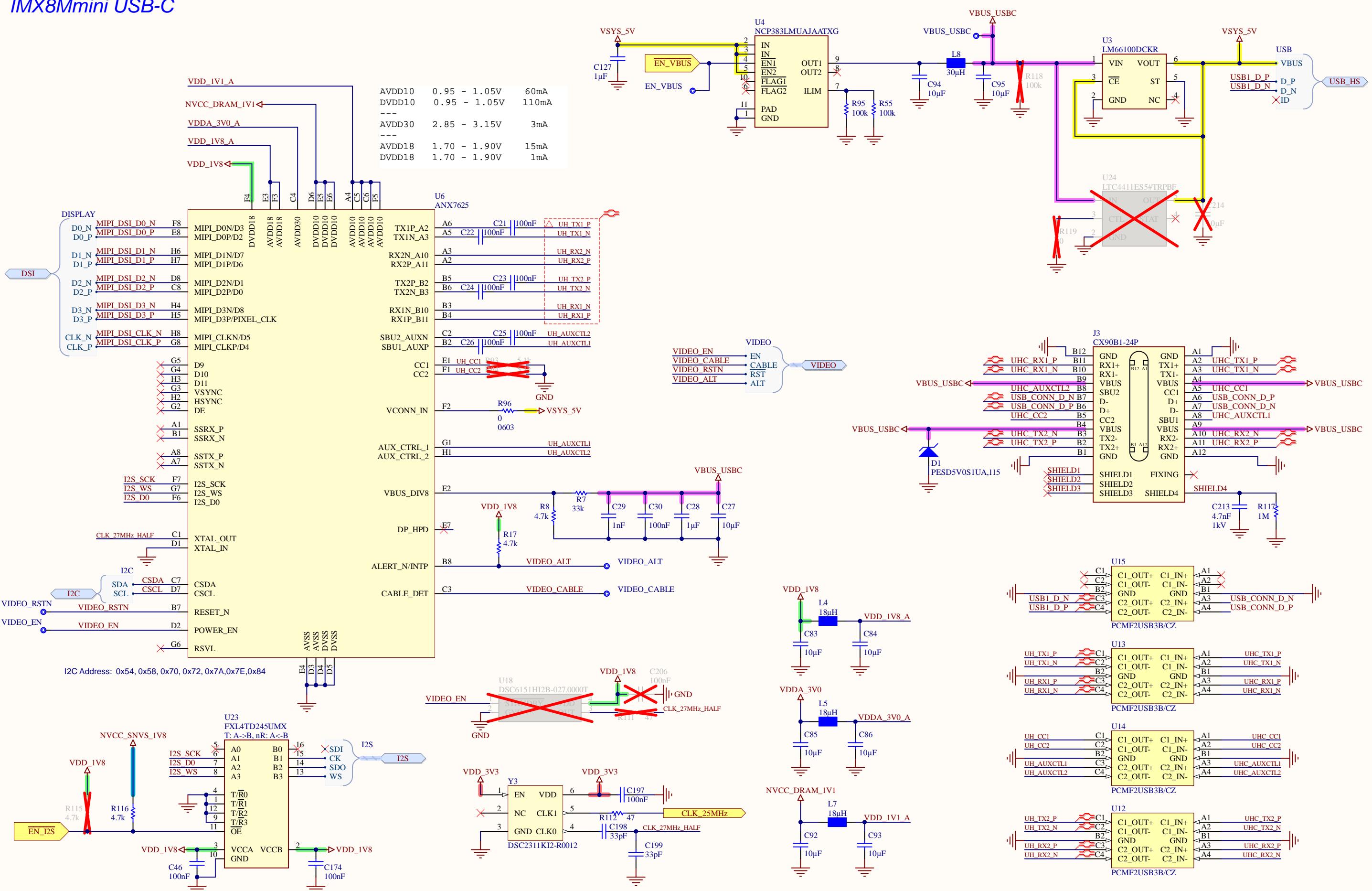
File: 09-IO.SchDoc

Author: Dario Pennisi



RevAuthor: Silvio Navaretti

IMX8Mmini USB-C



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Title: VIDEO

ID: 12

Revision: V4.5

Date: 6/3/2025

Time: 3:40:26 PM

Sheet 12 of 16

File: 11-Video.SchDoc

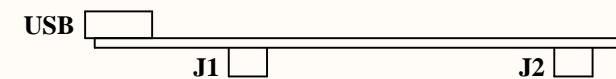
Author: Dario Pennisi



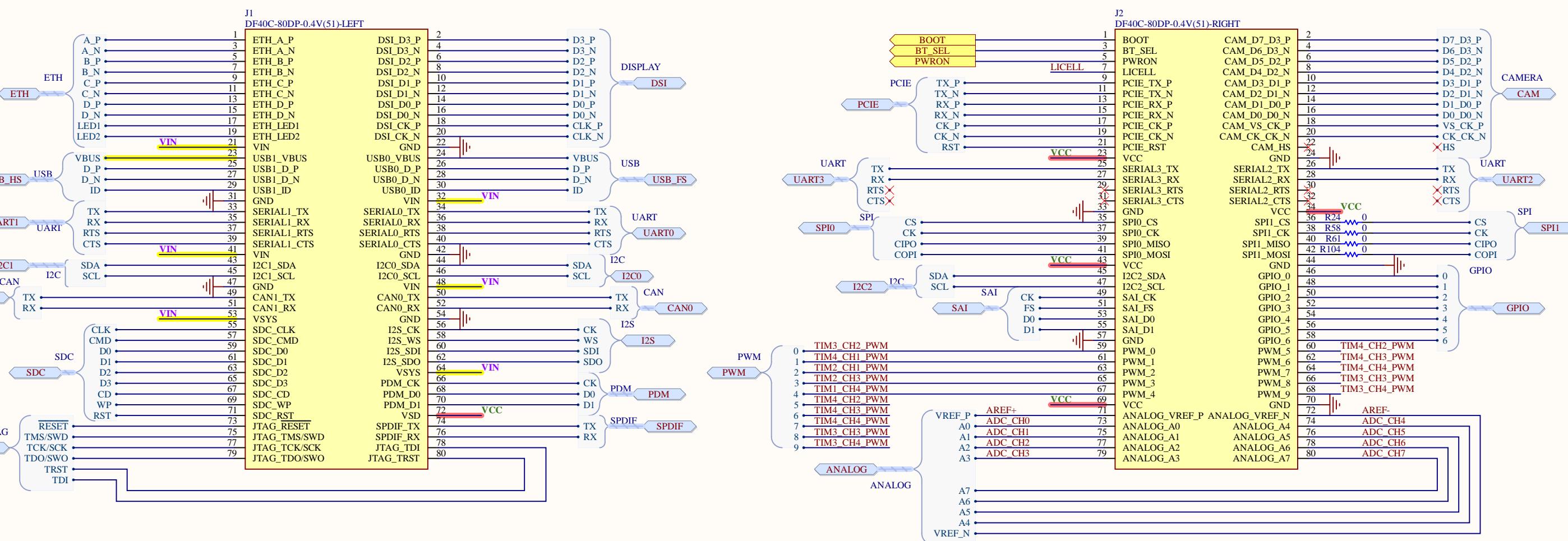
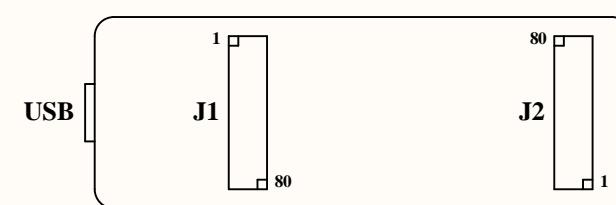
RevAuthor: Silvio Navaretti

IMX8Mmini Connectors

Board side view:



Board BOTTOM view:



POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U1) programmable output.
VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U1) programmable output.
LICELL	PORTENTA INPUT		Max 4uA with PMIC (U1) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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Title: CONNECTORS

ID: 13

Revision: V4.5

Date: 6/3/2025 Time: 3:40:27 PM

Sheet 13 of 16

File: 12-Connectors.SchDoc

Author: Dario Pennisi



IMX8Mmini LevelShifter

A

A

B

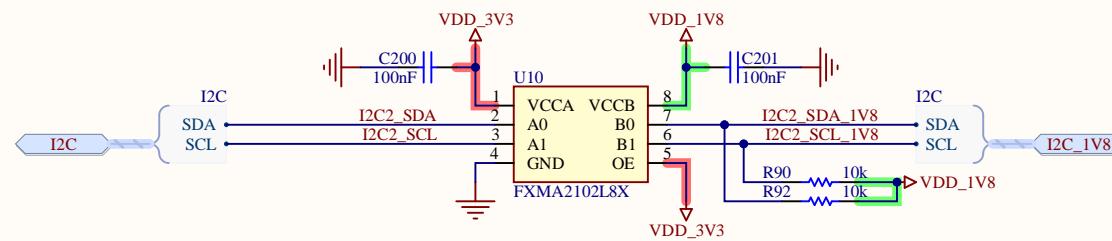
B

C

C

D

D



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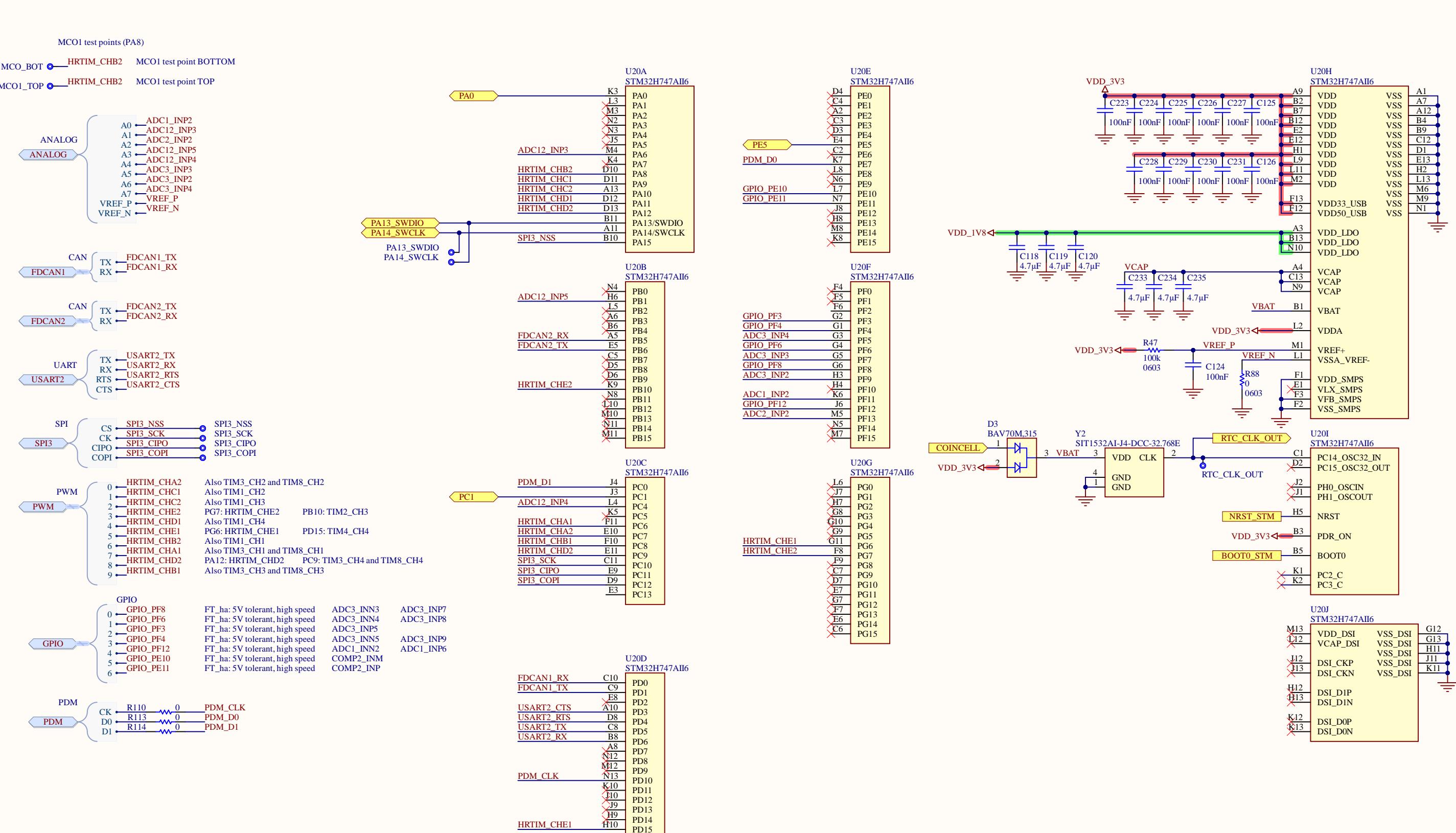
Title: LEVEL SHIFTER

ID: 14	Revision: v4.5
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Date: 6/3/2025	Time: 3:40:29 PM	Sheet 14 of 16
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File: 13-LevelShifter.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti
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A

B

C

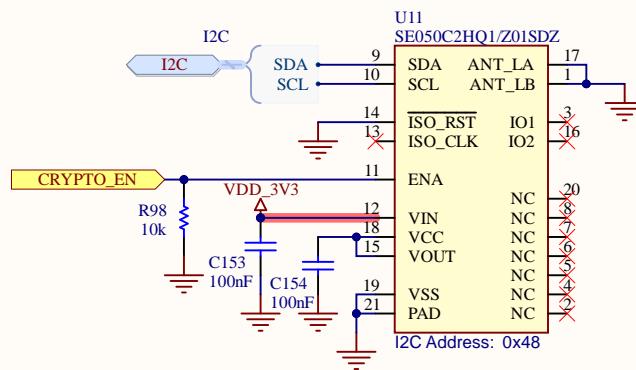
D

A

B

C

D



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Title: CRYPTO

ID: 16 Revision: v4.5

Date: 6/3/2025 Time: 3:40:33 PM Sheet 16 of 16

File: 15-CRYPTO.SchDoc Author: Dario Pennisi

