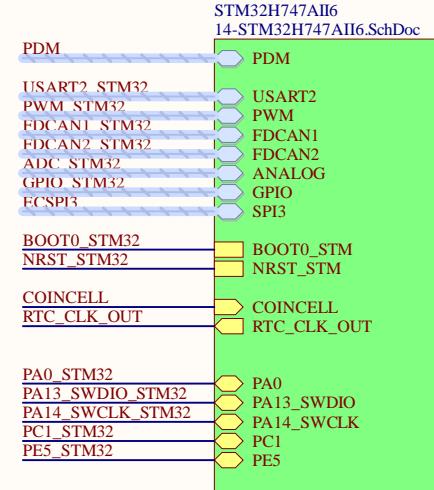
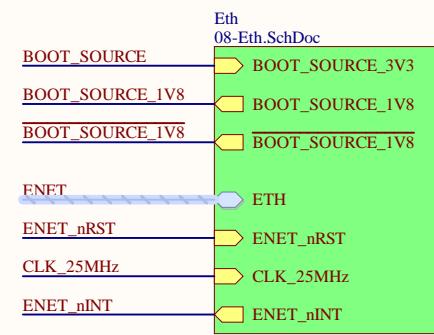
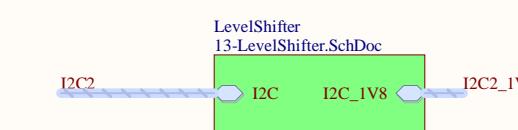
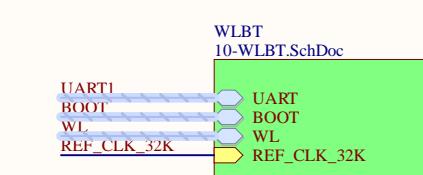
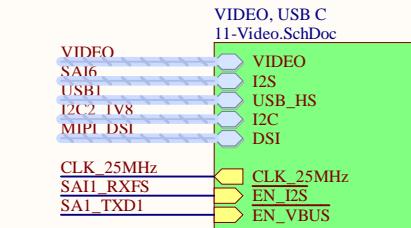
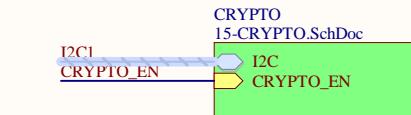
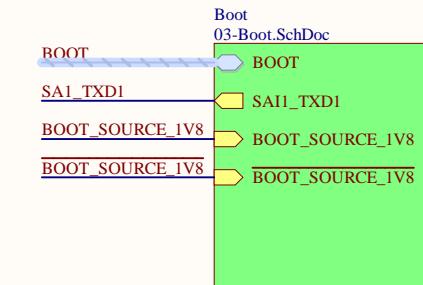
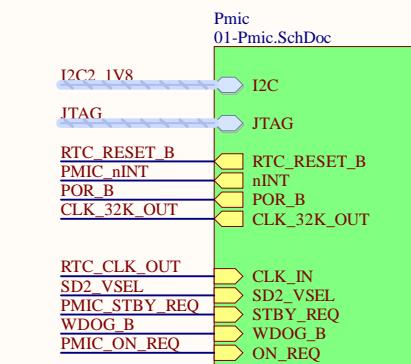
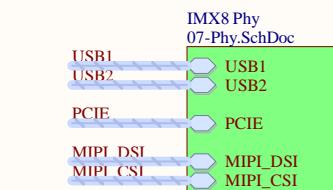
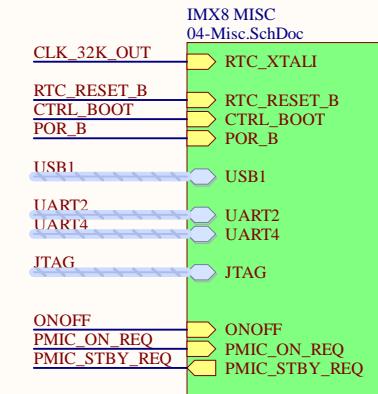
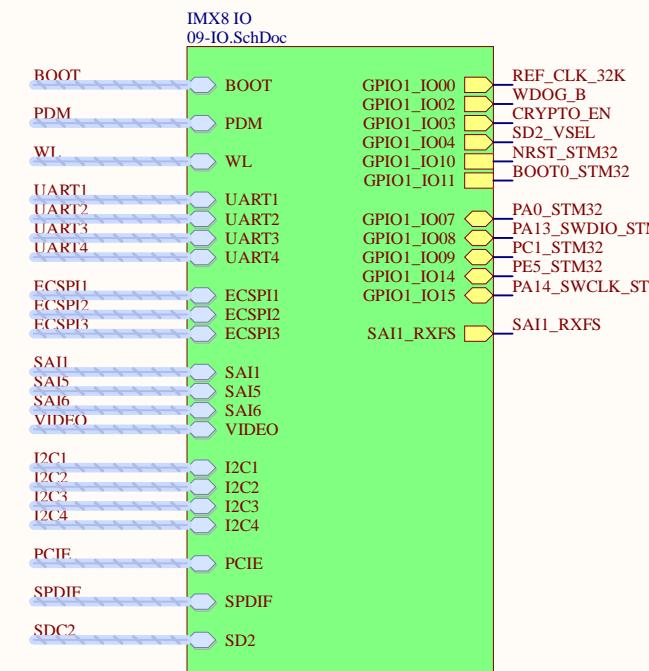
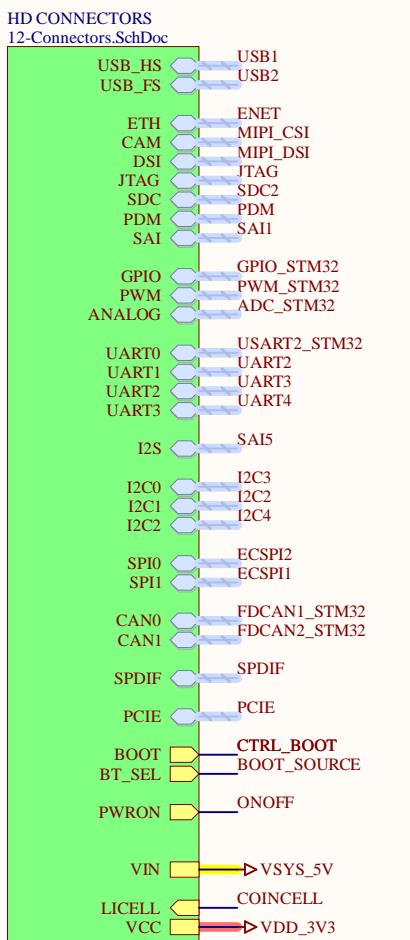


A



Title: TOP

ID: 1

Revision: V4.5

Date: 6/3/2025 Time: 3:40:06 PM Sheet 1 of 16

File: 00-TOP.SchDoc



B

C

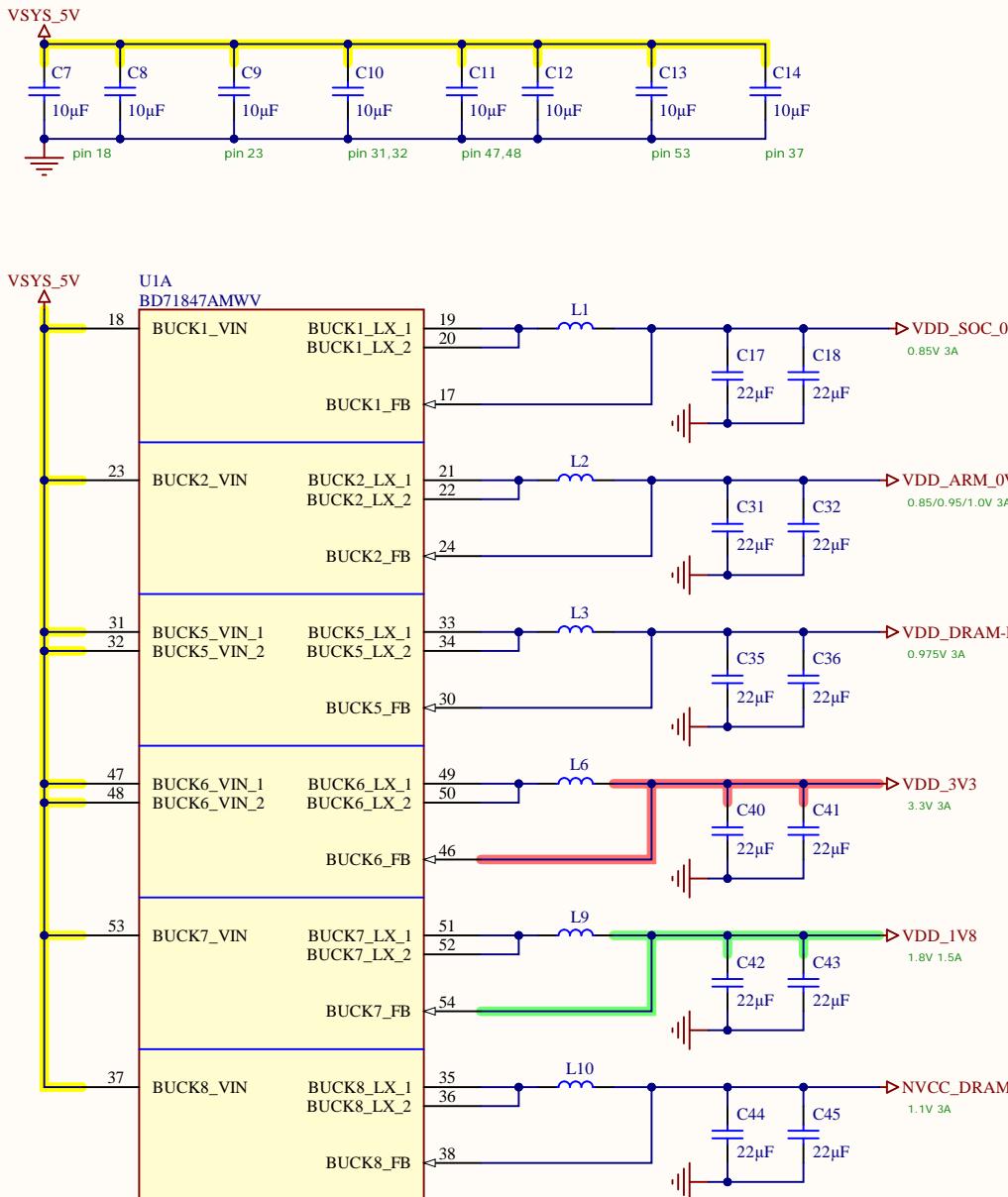
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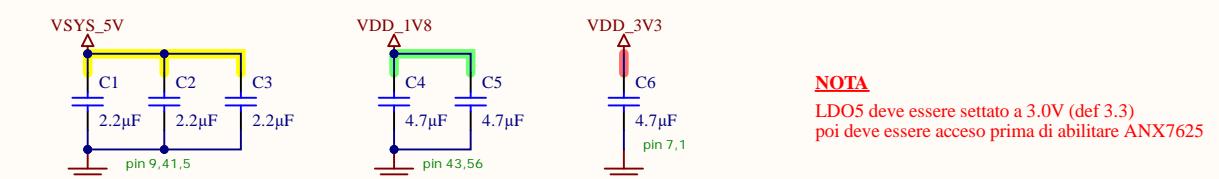
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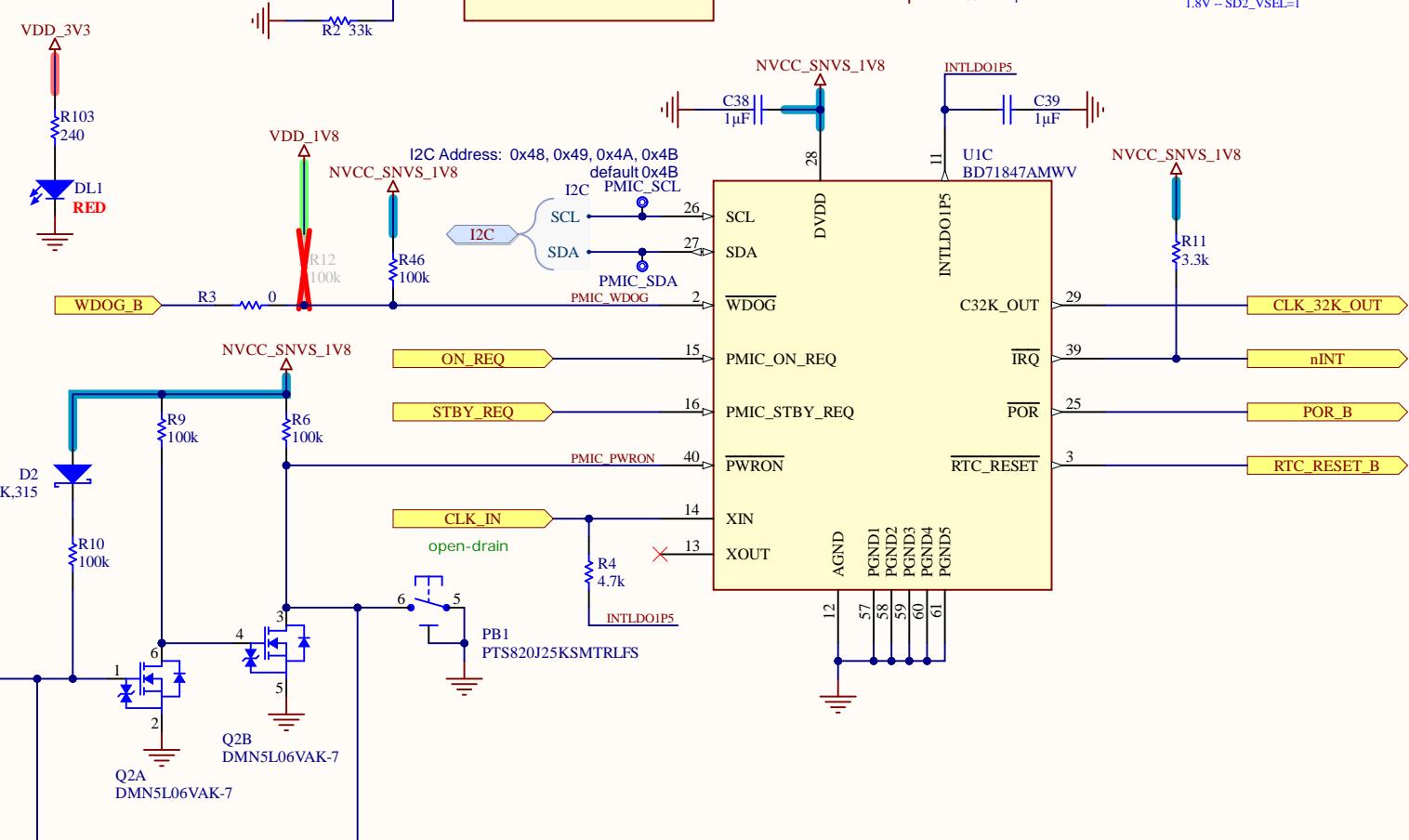
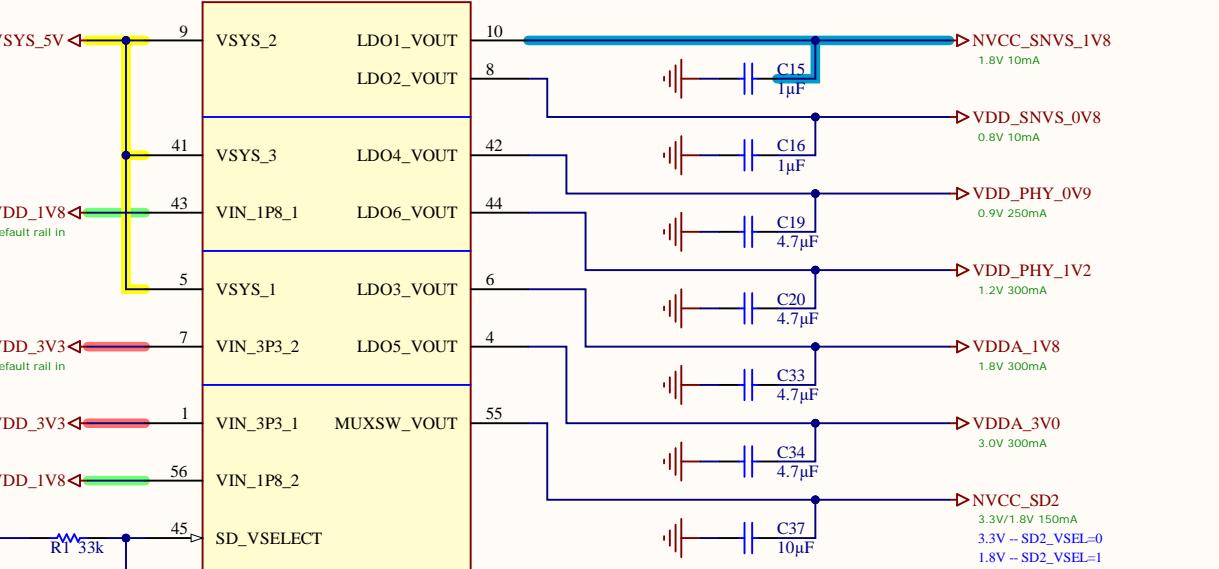
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**IMX8Mmini PMIC**

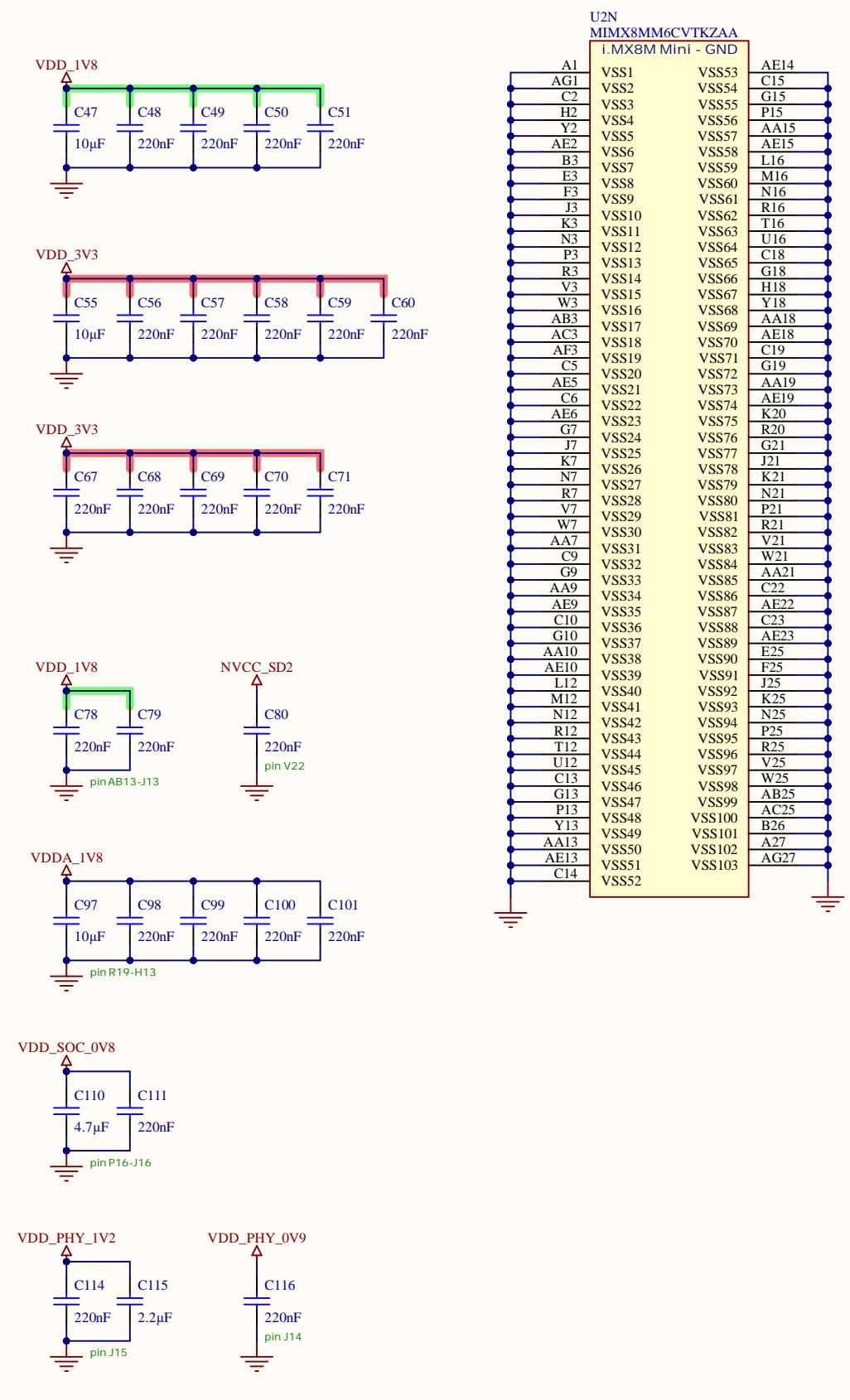
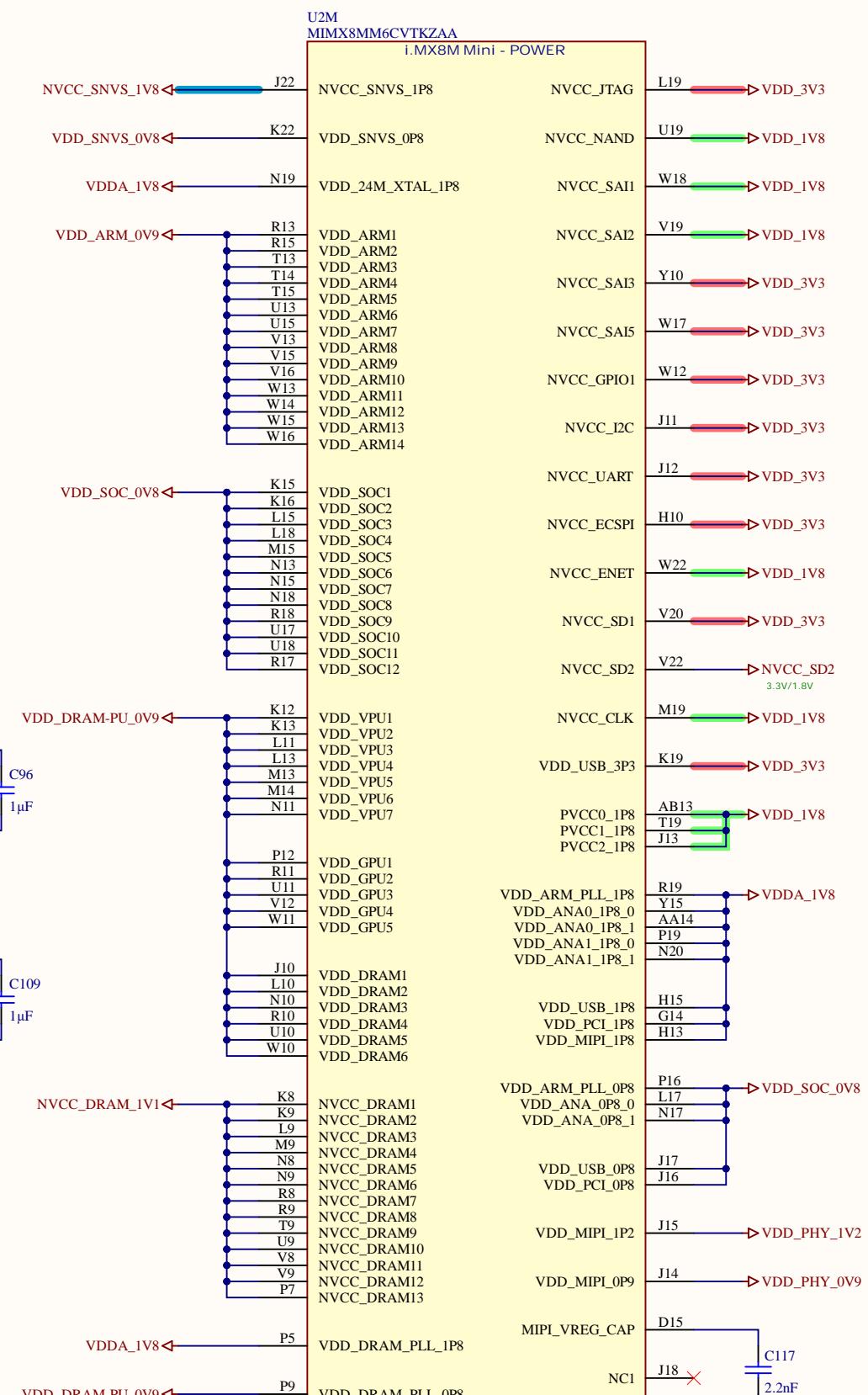
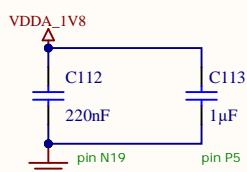
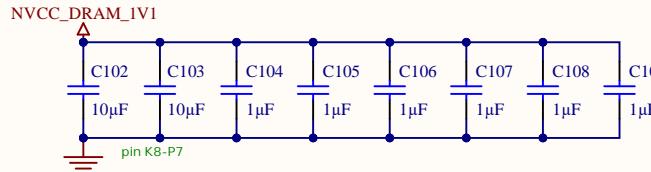
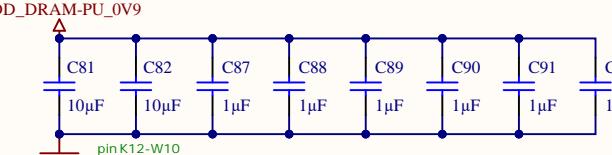
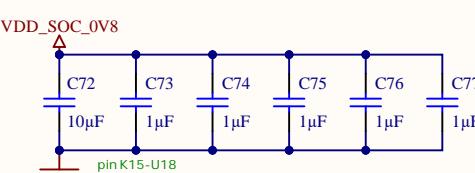
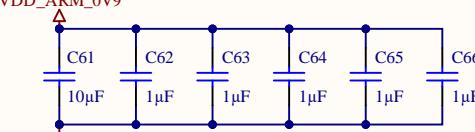
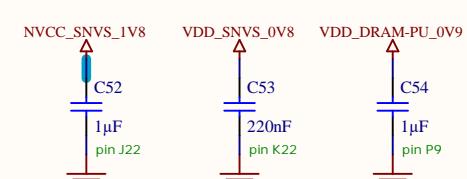
VDD\_SOC\_0V8 → VDD\_SOC\_0V8  
 VDD\_ARM\_0V9 → VDD\_ARM\_0V9  
 VDD\_DRAM\_PU\_0V9 → VDD\_DRAM\_PU\_0V9  
 VDD\_3V3 → VDD\_3V3  
 VDD\_1V8 → VDD\_1V8  
 NVCC\_DRAM\_1V1 → NVCC\_DRAM\_1V1  
 NVCC\_SNVS\_1V8 → NVCC\_SNVS\_1V8  
 VDD\_SNVS\_0V8 → VDD\_SNVS\_0V8  
 VDD\_PHY\_0V9 → VDD\_PHY\_0V9  
 VDD\_PHY\_1V2 → VDD\_PHY\_1V2  
 VDDA\_1V8 → VDDA\_1V8  
 NVCC\_SD2 → NVCC\_SD2  
 VSYS\_5V → VSYS\_5V



**NOTA**  
 LDO5 deve essere settato a 3.0V (def 3.3)  
 poi deve essere acceso prima di abilitare ANX7625



# IMX8Mmini POWER



*IMX8Mmini BOOT*

Boot Pins:			
BOOT_MODE0			
BOOT_MODE1			
SAI1_TxD7	BT0_CFG15	SAI1_RxD7	BT0_CFG07
SAI1_TxD6	BT0_CFG14	SAI1_RxD6	BT0_CFG06
SAI1_TxD5	BT0_CFG13	SAI1_RxD5	BT0_CFG05
SAI1_TxD4	BT0_CFG12	SAI1_RxD4	BT0_CFG04
SAI1_TxD3	BT0_CFG11	SAI1_RxD3	BT0_CFG03
SAI1_TxD2	BT0_CFG10	SAI1_RxD2	BT0_CFG02
SAI1_TxD1	BT0_CFG09	SAI1_RxD1	BT0_CFG01
SAI1_TxD0	BT0_CFG08	SAI1_RxD0	BT0_CFG00

default --> 0 0 1 0 1 0 1

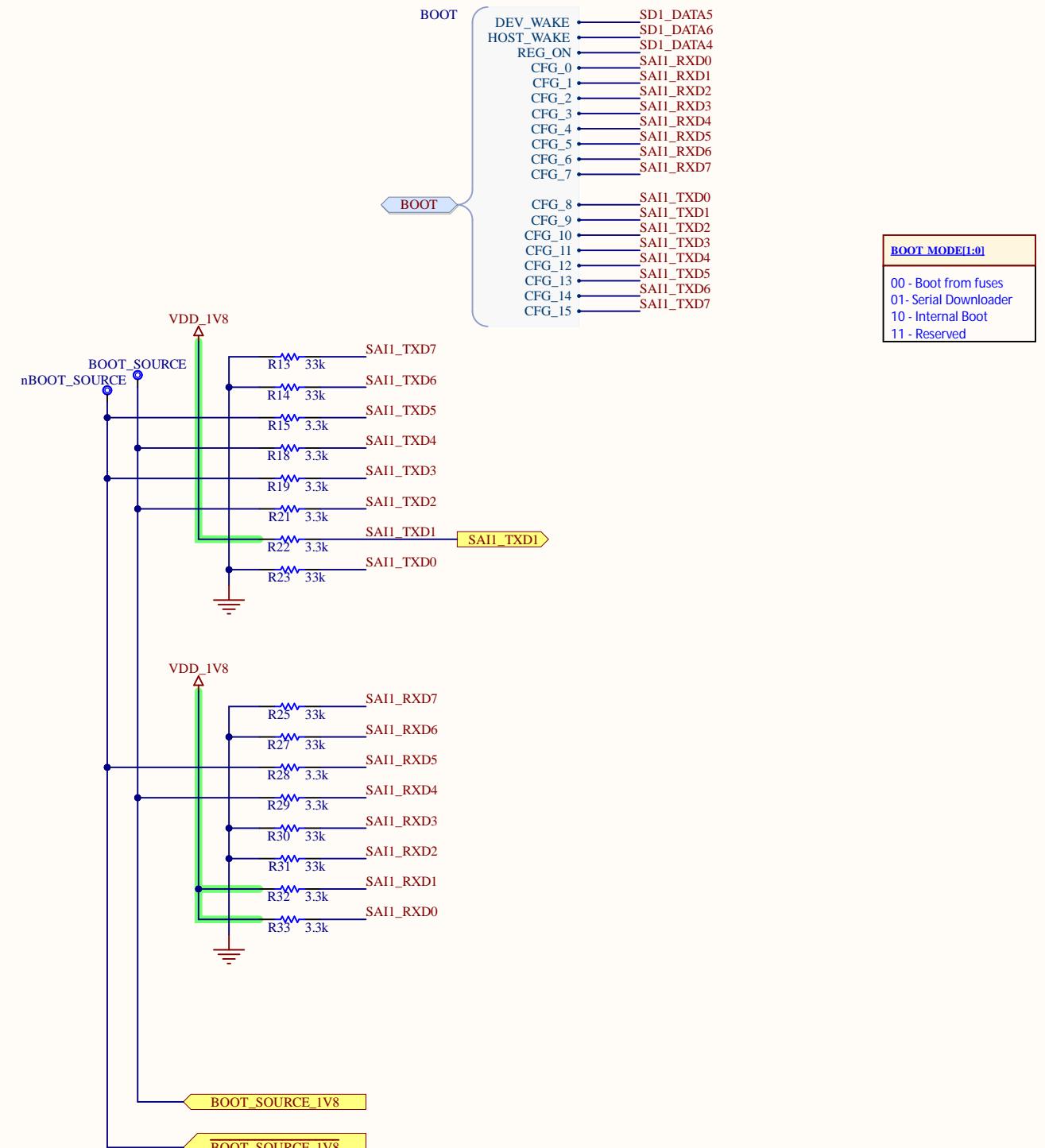
BT_CFG15	BT_CFG14	BT_CFG13	BT_CFG12	BT_CFG11	BT_CFG10	BT_CFG9	BT_CFG8
Infinit-Loop 0 - Disable 1 - Enable	Boot device type 001 - SD/eSD 010 - MMC/eMMC			Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled	SD Loopback Clock Source Sel (for SDR5 and SDR10 only) '0' - through SD pad '1' - direct

default --> 0 0 0 1 0 0 1

	BT_CFG7	BT_CFG6	BT_CFG5	BT_CFG4	BT_CFG3	BT_CFG2	BT_CFG1	BT_CFG0
SD	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50			Reserved
		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4)		Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved	USDHCI IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHCI IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V		

Default boot device: eMMC/SDHC3 - BT\_CFG[15:0] = 0 010 10 10 0 010 00 1 1

Alternative host devices SD/SDHQS PT QEG[15:6] 2 201 21 16 2 201 22 1 1



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Title: **BOOT**

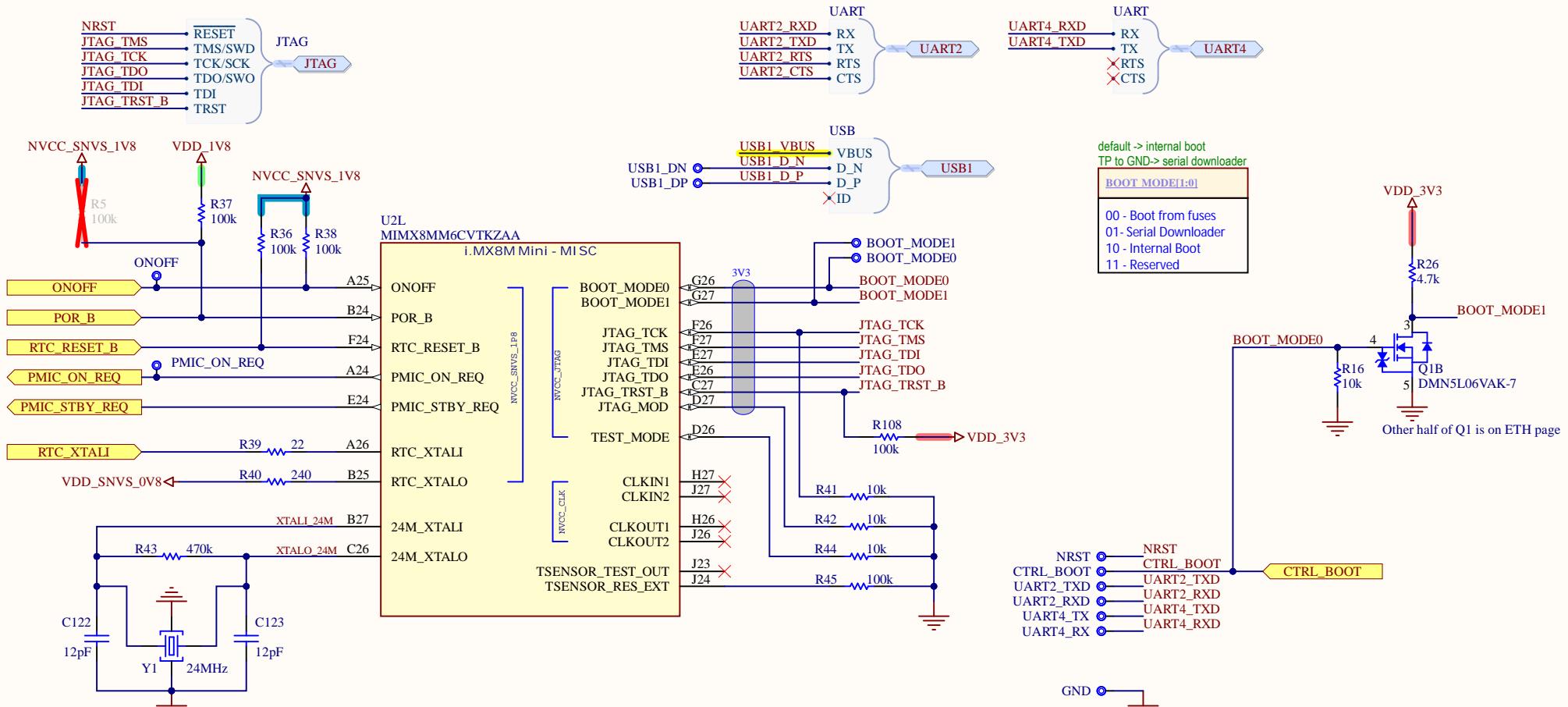
ID: 4

Revision: V4.5

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# IMX8Mmini MISC



Mfg Tool

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Title: MISCELLANEOUS

ID: 5

Revision: V4.5

Date: 6/3/2025 Time: 3:40:13 PM

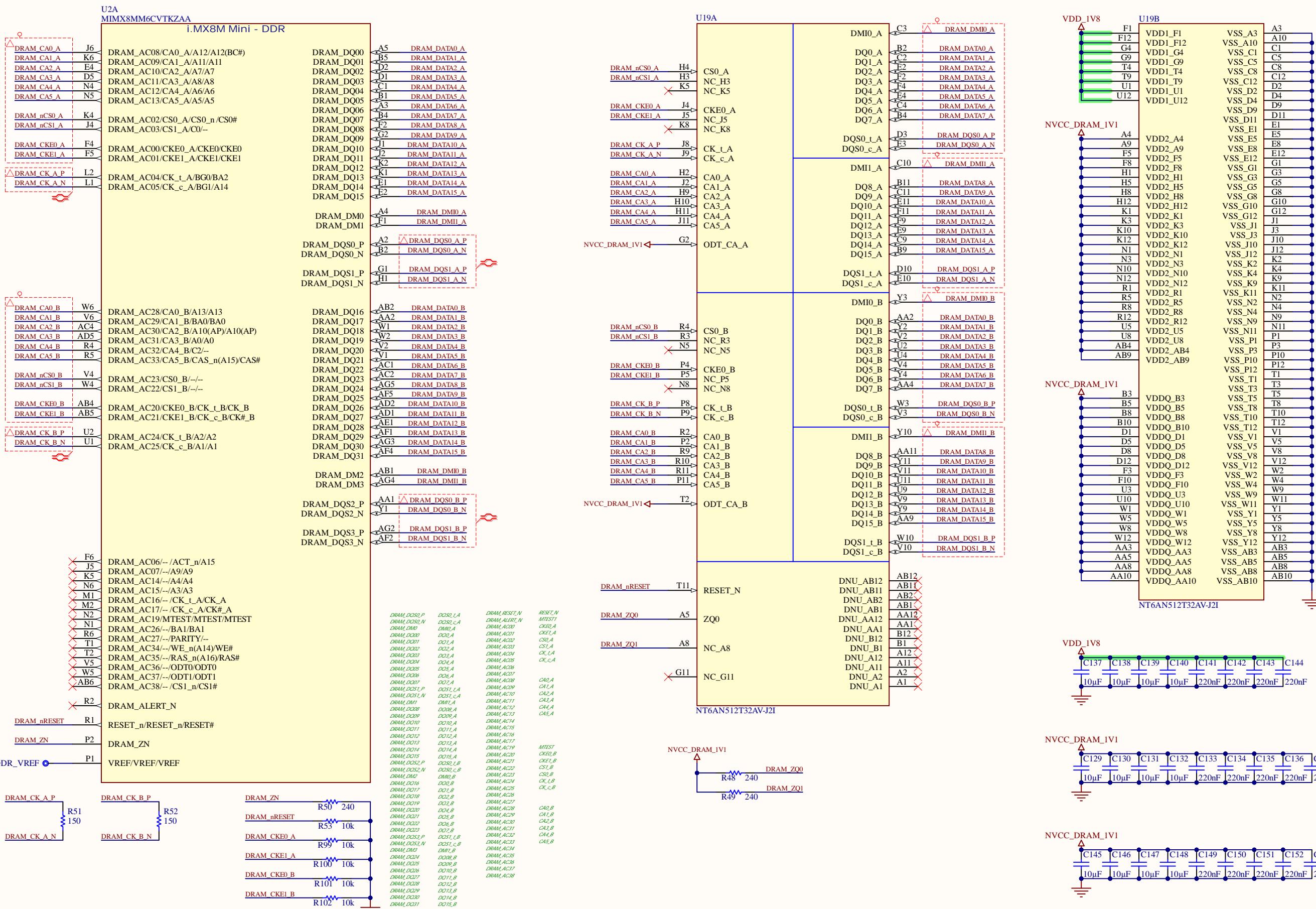
Sheet 5 of 16

File: 04-Misc.SchDoc

Author: Dario Pennisi



*IMX8Mmini DDR*

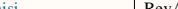


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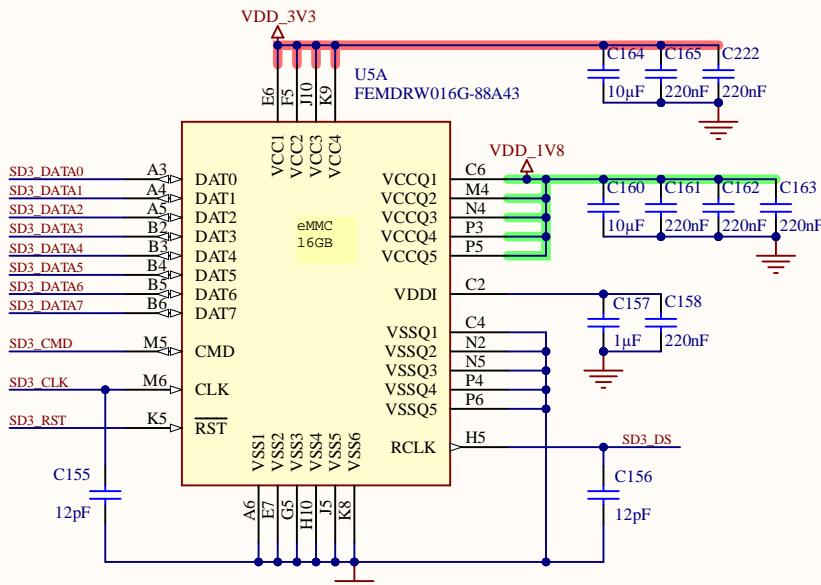
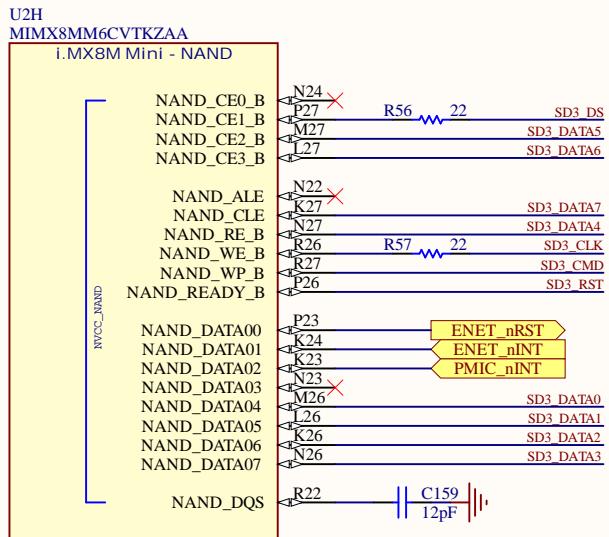
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Title: DDR		
ID: 6	Revision: V4.5	
Date: 6/3/2025	Time: 3:40:15 PM	Sheet 6 of 16
File: 05-Ddr.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti

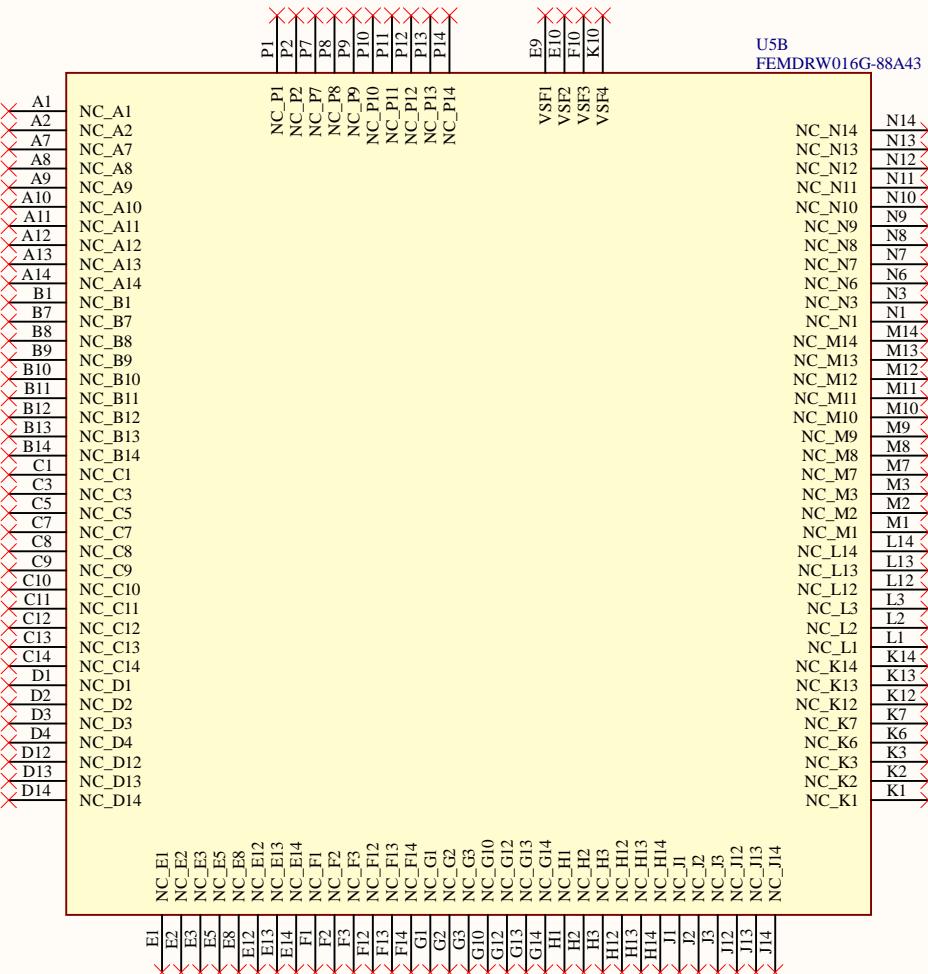
## *IMX8Mmini Memory*



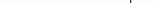
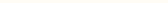
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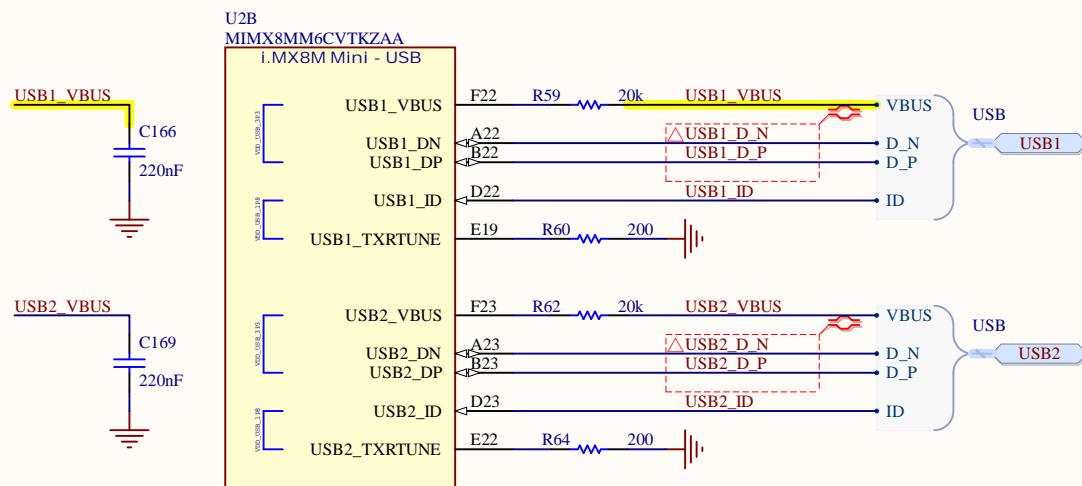


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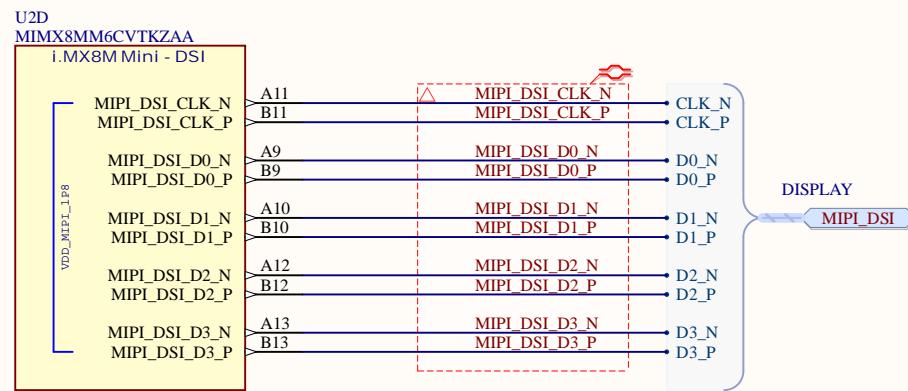
**ID:** 7 **Revision:** V4.5 **Date:** 6/3/2025 **Time:** 3:40:17 PM **Sheet:** 7 of 16    
**File:** 06-Memory.SchDoc **Author:** Dario Pennisi **RevAuthor:** Silvio Navaretti

# IMX8Mmini PHY

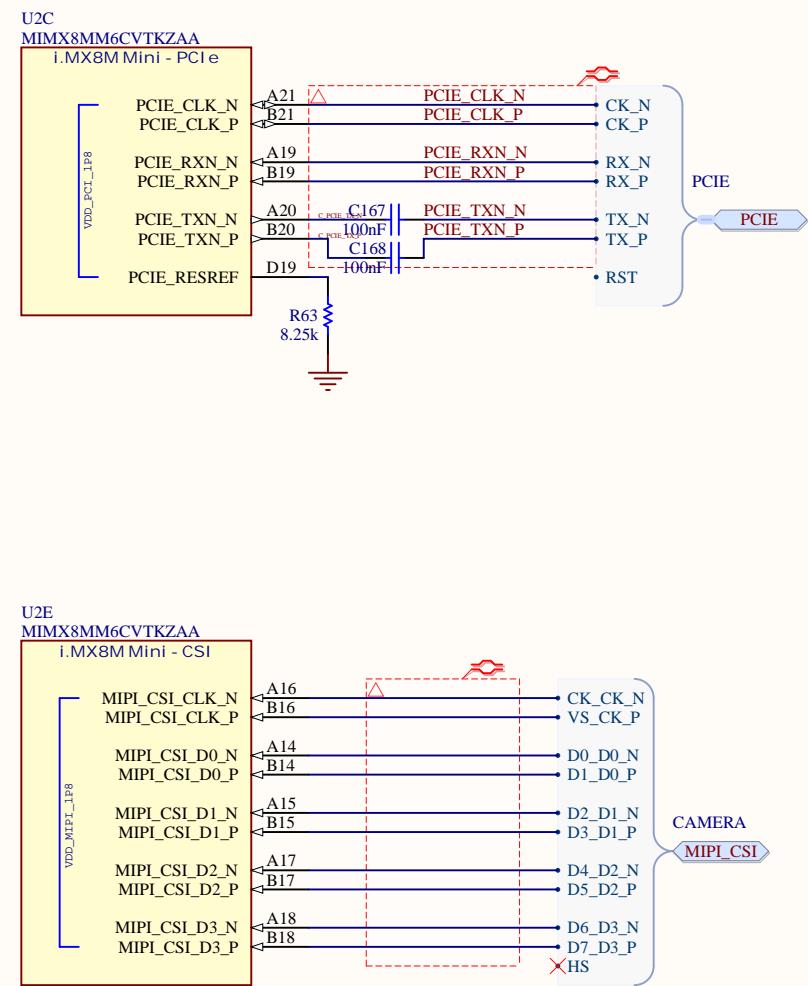
A



B



C



D

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Title: **PHY**

ID: **8**

Revision: **V4.5**

Date: **6/3/2025**

Time: **3:40:19 PM**

Sheet **8** of 16

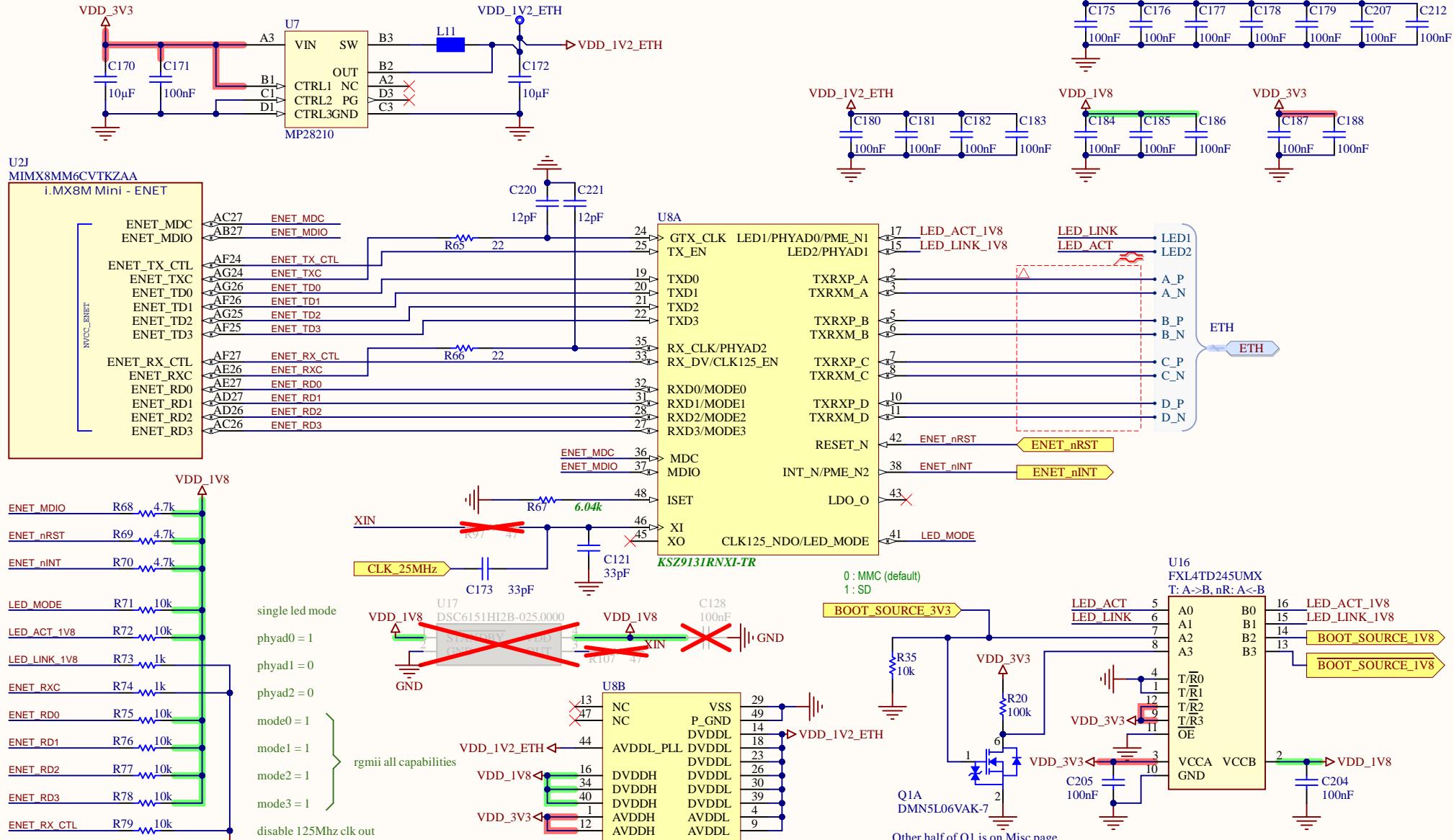
File: **07-Phy.SchDoc**

Author: **Dario Pennisi**



RevAuthor: **Silvio Navaretti**

# IMX8Mmini ETH



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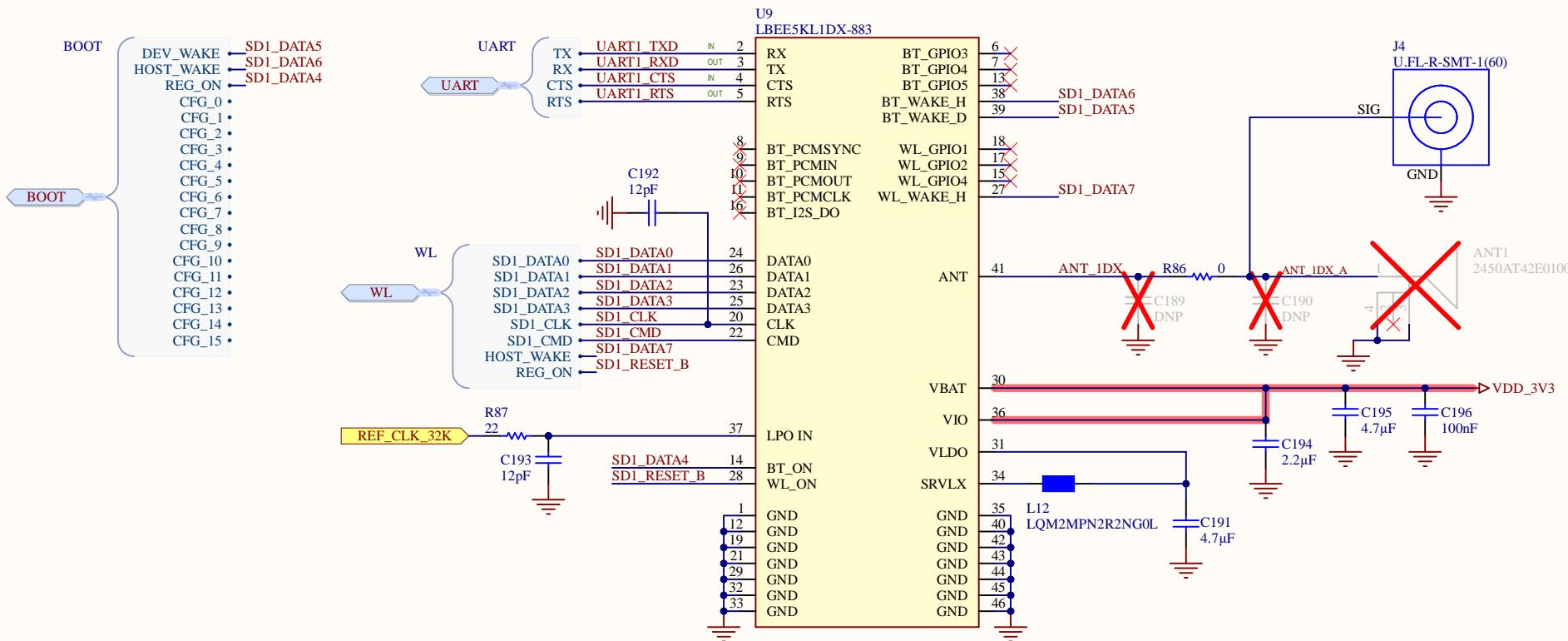
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## Title: ETHERNET

ID: 9	Revision: V4.5
Date: 6/3/2025	Time: 3:40:20 PM
File: 08-Eth.SchDoc	Author: Dario Pennisi



# IMX8Mmini WL/BT



A

A

B

B

C

C

D

D

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Title: **WLBT**

ID: **11** Revision: **V4.5**

Date: **6/3/2025** Time: **3:40:22 PM** Sheet **10 of 16**

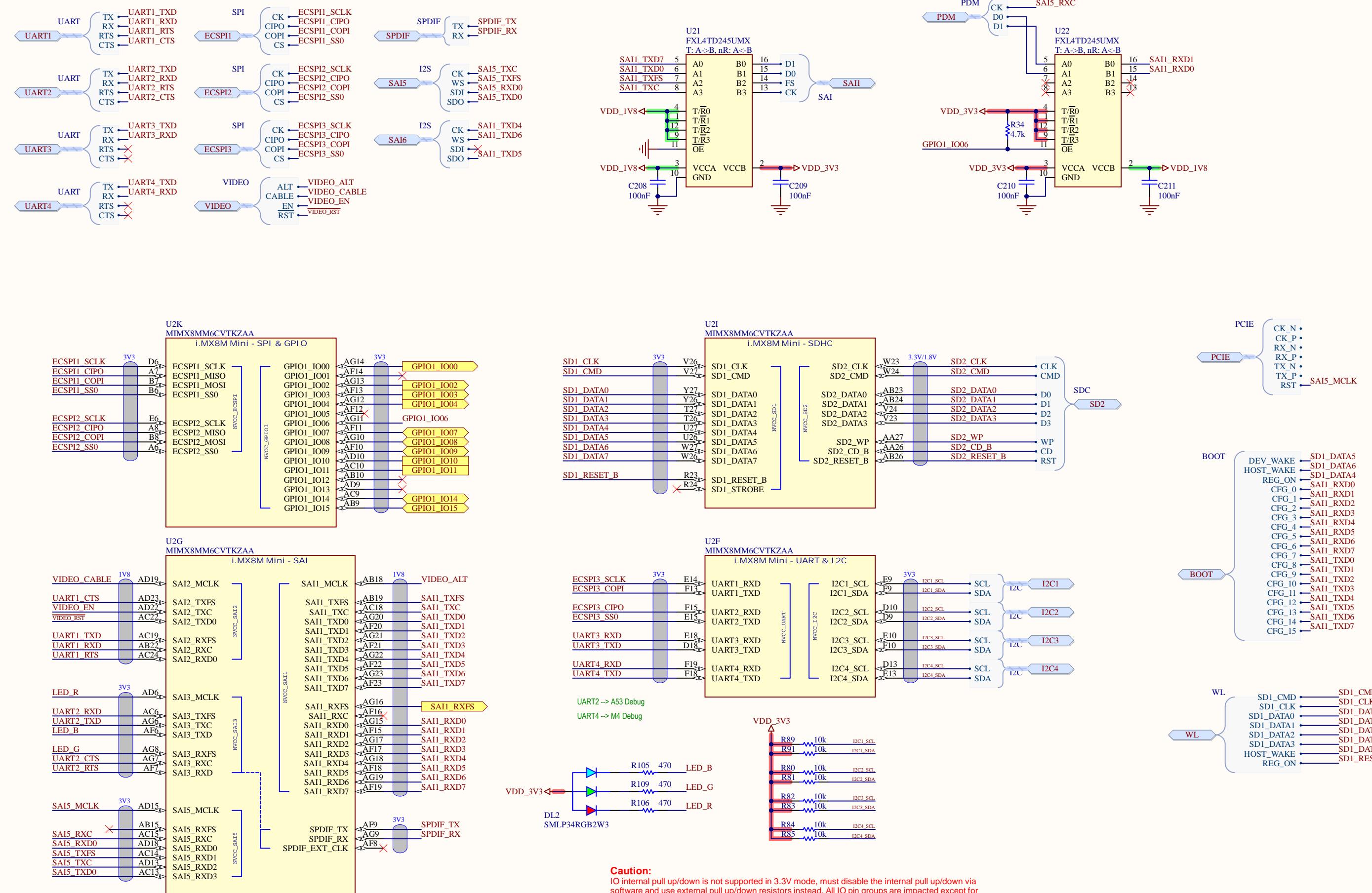
File: **10-WLBT.SchDoc**

Author: **Dario Pennisi**

RevAuthor: **Silvio Navaretti**



IMX8Mmini IO



**Caution:**  
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead. All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY I/O's. See Errata e50080 for detailed information.

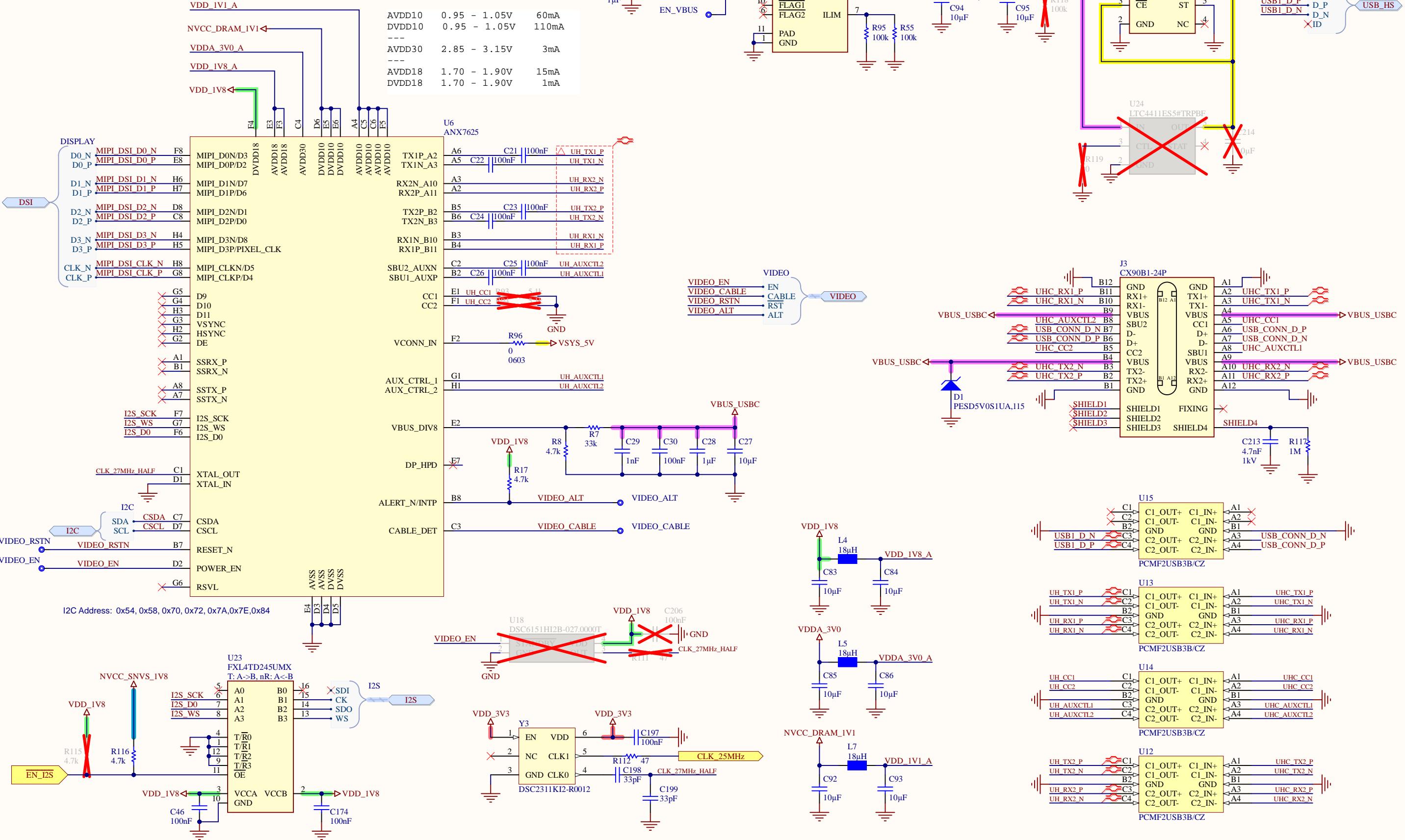
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Title: <b>IO</b>			
ID: <b>10</b>	Revision: <b>V4.5</b>		
Date: <b>6/3/2025</b>	Time: <b>3:40:24 PM</b>	Sheet <b>11</b> of <b>16</b>	
File: <b>09-IO.SchDoc</b>		Author: <b>Dario Pennisi</b>	RevAuthor: <b>Silvio Navaretti</b>

## *IMX8Mmini USB-C*



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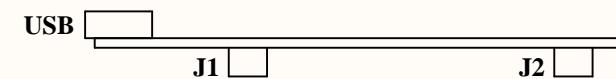
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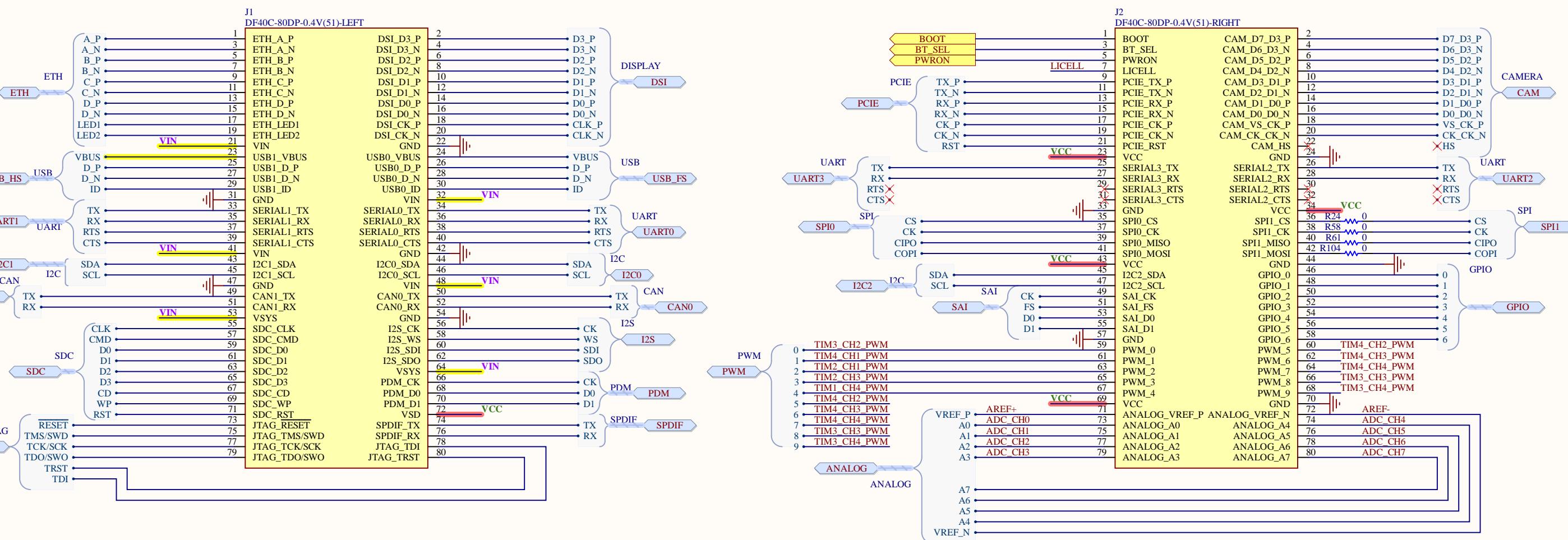
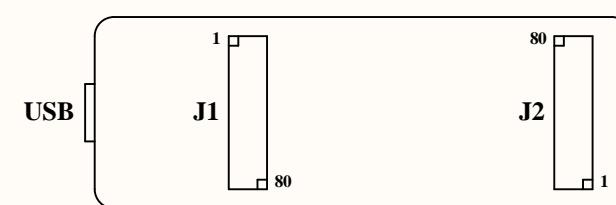
Title: <b>VIDEO</b>			
ID: <b>12</b>	Revision: <b>V4.5</b>		
Date: <b>6/3/2025</b>	Time: <b>3:40:26 PM</b>	Sheet <b>12</b> of <b>16</b>	
File: <b>11-Video.SchDoc</b>		Author: <b>Dario Pennisi</b>	RevAuthor: <b>Silvio Navaretti</b>

## IMX8Mmini Connectors

Board side view:



Board BOTTOM view:



### POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U1) programmable output.
VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U1) programmable output.
LICELL	PORTENTA INPUT		Max 4uA with PMIC (U1) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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Title: CONNECTORS

ID: 13

Revision: V4.5

Date: 6/3/2025 Time: 3:40:27 PM

Sheet 13 of 16

File: 12-Connectors.SchDoc

Author: Dario Pennisi



# IMX8Mmini LevelShifter

A

A

B

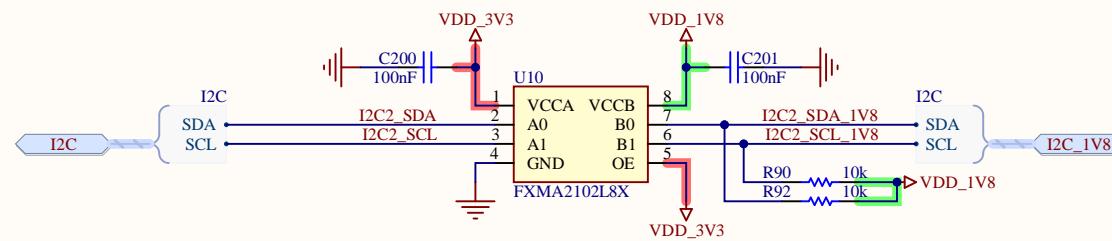
B

C

C

D

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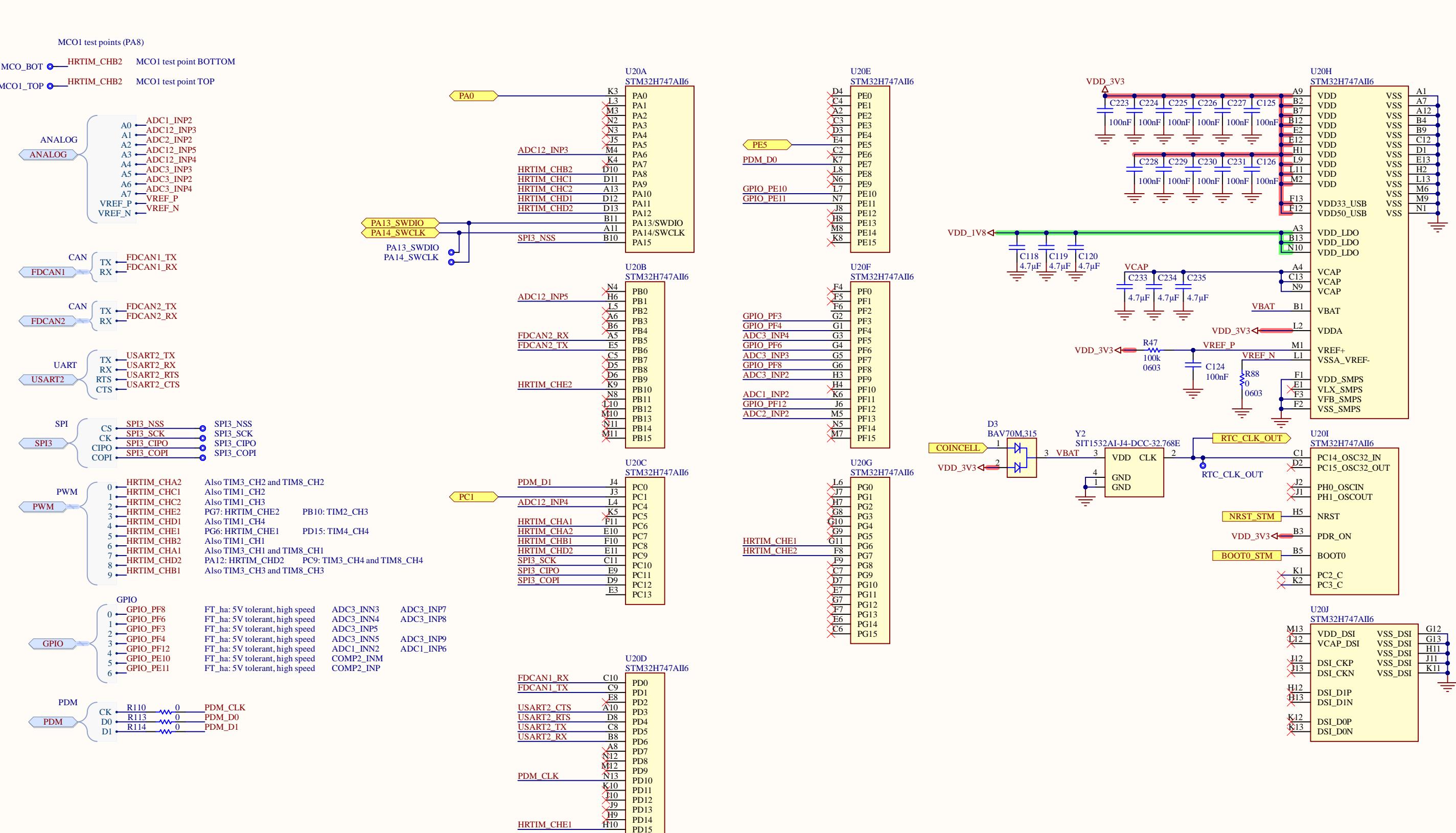
## Title: LEVEL SHIFTER

ID: 14	Revision: v4.5
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Date: 6/3/2025	Time: 3:40:29 PM	Sheet 14 of 16
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File: 13-LevelShifter.SchDoc	Author: Dario Pennisi	RevAuthor: Silvio Navaretti
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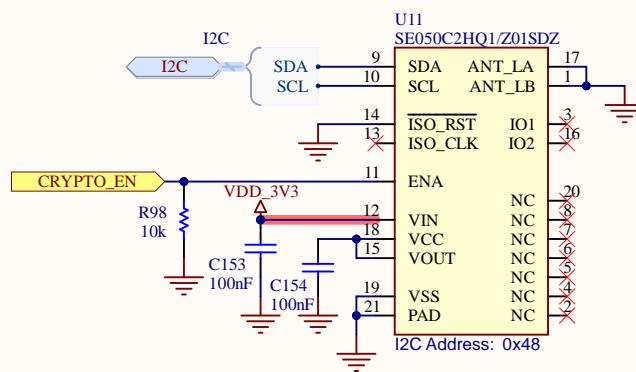
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### Title: CRYPTO

ID: 16 Revision: v4.5

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File: 15-CRYPTO.SchDoc Author: Dario Pennisi



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