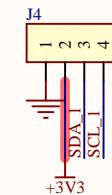
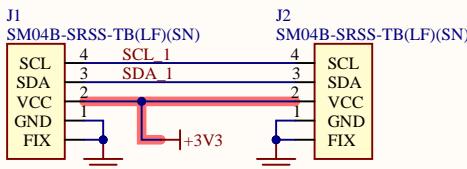
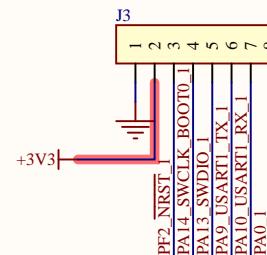
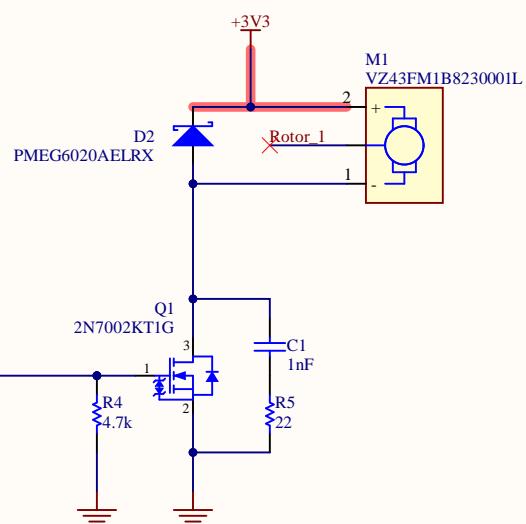
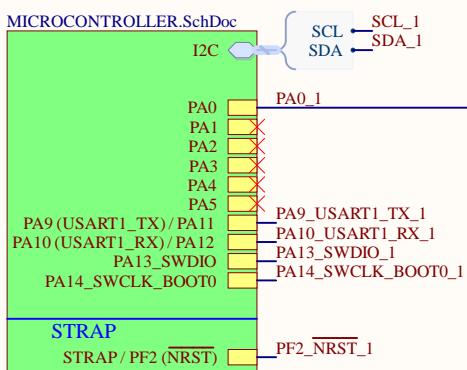


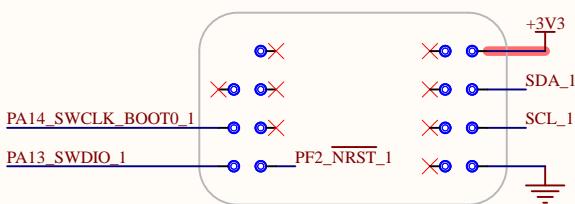
I2C CONNECTORS



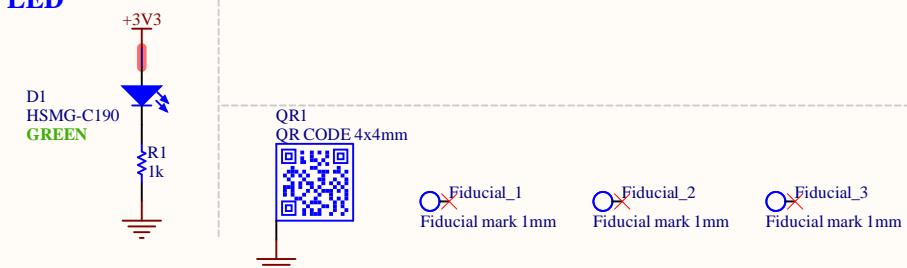
MICROCONTROLLER



TEST POINTS BOTTOM VIEW



POWER LED



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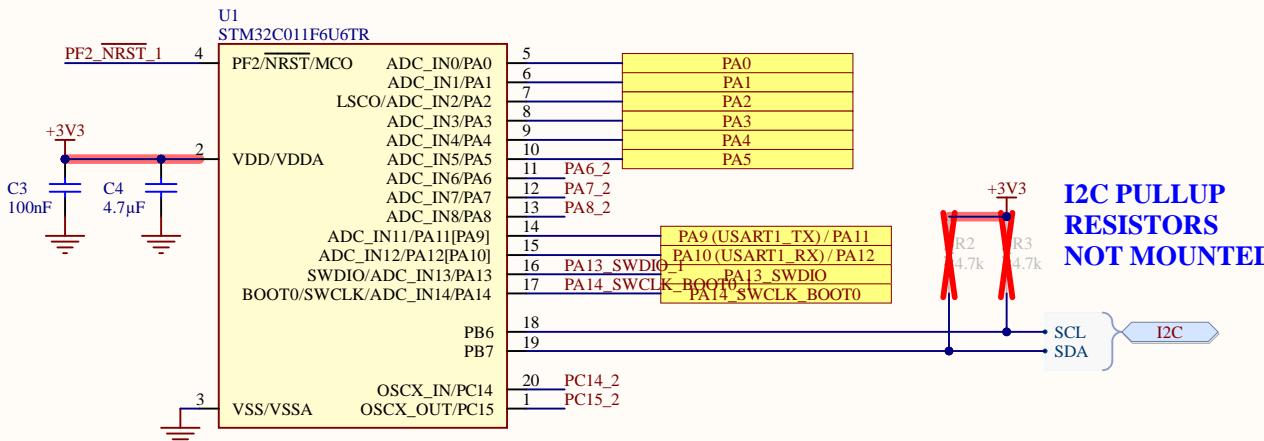
Author: Silvio Navaretti

RevAuthor: Silvio Navaretti



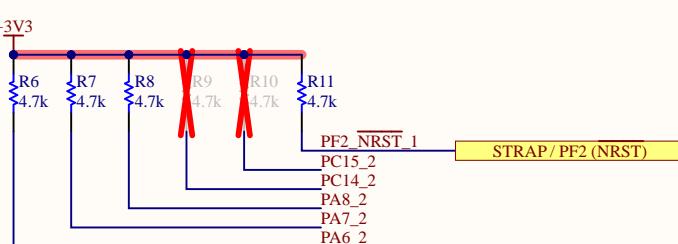
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A



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Table 11. Terms and symbols used in Table 12

Column	Symbol	Definition
Pin name		Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	FT	5 V tolerant I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
I/O structure	Options for FT I/Os	
	_f	I/O, Fm+ capable
	_a	I/O, with analog switch function

Table 12. Pin assignment and description

Pin	Pin name (function upon reset)	Pin type	IO structure	Note	Alternate functions	Additional functions
20	PC14-OSCX_IN (PC14)	I/O	FT	-	USART1_TX, TIM1_ETR, TIM1_BKIN2, IR_OUT, USART2 RTS, DE, CK, TIM17_CH1, TIM3_CH2, I2C1_SDA, EVENTOUT	OSCX_IN
1	PC15-OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM16_ETR, TIM3_CH3	OSCX_OUT
2	VDD/VDDA	S	-	-	-	-
3	VSS/VSSA	S	-	-	-	-
4	PF2-NRST	I/O	-	-	MCO, TIM1_CH4	NRST
5	PA0	I/O	FT	-	USART2_CTS, TIM16_CH1, USART1_RX, TIM1_CH1	ADC_IN0, WKUP1
6	PA1	I/O	FT	-	SP1_SCK/IS1_CS, USART2_RTS, DE, CK, TIM17_CH1, USART1_RX, TIM1_CH2, I2C1_SMB, EVENTOUT	ADC_IN1
7	PA2	I/O	FT	-	SP1_MOSI/IS1_SD, USART2_RX, TIM16_CH1N, TIM3_ETR, TIM1_CH3	ADC_IN2, WKUP4, LSCO
8	PA3	I/O	FT	-	USART2_RX, TIM1_CH1N, TIM1_CH4, EVENTOUT	ADC_IN3
9	PA4	I/O	FT	-	SP1 NSS/IS1_WS, USART2_RX, TIM1_CH2N, TIM1_CH1, EVENTOUT	ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
10	PA5	I/O	FT	-	SP1_MOSI/IS1_CS, USART2_RX, TIM1_CH3N, TIM1_CH1, EVENTOUT	ADC_IN5
11	PA6	I/O	FT	-	SP1_MISO/IS1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1	ADC_IN6
12	PA7	I/O	FT	-	SP1 MOSI/IS1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
13	PA8	I/O	FT	-	MCO, USART2_RX, TIM1_CH1, EVENTOUT, SP1 NSS/IS1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MCO2	ADC_IN8
-	PA9	I/O	FT	(1)	MCO, USART1_RX, TIM1_CH2, TIM3_ETR, I2C1_SCL, EVENTOUT	-
-	PA10	I/O	FT	(1)	USART1_RX, TIM1_CH3, MCO2, TIM7_BKIN, I2C1_SDA, EVENTOUT	-
14	PA11 [PA9]	I/O	FT	(1)	SP1_MISO/IS1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN2	ADC_IN11
15	PA12 [PA10]	I/O	FT	(1)	SP1_MOSI/IS1_SD, USART1_RTS_DE, CK, TIM1_ETR, I2S_CHIN	ADC_IN12
16	PA13	I/O	FT	(2)	SWDIO, IR_OUT, TIM3_ETR, USART2_RX, EVENTOUT	ADC_IN13
17	PA14-BOOT0	I/O	FT	(2)	SWCLK, USART2_RX, EVENTOUT, SP1 NSS/IS1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS_DE, CK	ADC_IN14, BOOT0
18	PB6	I/O	FT	-	USART1_TX, TIM1_CH1, TIM16_CH1N, TIM3_CH3, USART1_RTS_DE, CK, USART1_CTS, I2C1_SCL, SP1_SCK/IS1_CS, USART1_RX, TIM1_CH2, TIM3_CH1, TIM17_CH2, TIM16_BKIN, TIM17_BKIN	WKUP3
19	PB7	I/O	FT	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, I2C1_SDA, EVENTOUT, USART2_CTS, TIM16_CH1, TIM3_CH1, I2C1_SCL	RTC_REFIN

1. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFRG1 register.

2. Upon reset, these pins are configured as SWD alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.

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