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Title: TOP		
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File: TOP.SchDoc	Author: Silvio Navaretti	RevAuthor: Silvio Navaretti

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I2C PULLUP RESISTORS NOT MOUNTED

PF2_NRST_1

PF2_NRST/MCO

VDD/VDDA

ADC_IN0/PA0
ADC_IN1/PA1
LSCO/ADC_IN2/PA2
ADC_IN3/PA3
ADC_IN4/PA4
ADC_IN5/PA5
ADC_IN6/PA6
ADC_IN7/PA7
ADC_IN8/PA8
ADC_IN11/PA11[PA9]
ADC_IN12/PA12[PA10]
SWDIO/ADC_IN13/PA13
BOOT0/SWCLK/ADC_IN14/PA14

PA0
PA1
PA2
PA3
PA4
PA5
PA6_2
PA7_2
PA8_2
PA9 (USART1_TX) / PA11
PA10 (USART1_RX) / PA12
PA13_SWDIO
PA14_SWCLK_BOOT0
PA14_SWCLK_BOOT0

PB6
PB7

OSCX_IN/PC14
OSCX_OUT/PC15

PA14_2
PA15_2

SCL
SDA

I2C

R7 4.7k
R8 4.7k
R9 4.7k
R10 4.7k
R11 4.7k

PF2_NRST_1

STRAP / PF2 (NRST)

PC15_2
PC14_2
PA8_2
PA7_2
PA6_2

Table 11. Terms and symbols used in Table 12

Column	Symbol	Definition
Pin name	Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Options for FT I/Os	
	_f	I/O, Fm+ capable
	_a	I/O, with analog switch function

Table 12. Pin assignment and description

Pin							
	UFOFPN20	Pin name (function upon reset)	Pin type	IO structure	Note	Alternate functions	Additional functions
20	PC14-OSCX_IN (PC14)	I/O	FT	-	USART1_TX, TIM1_ETR, TIM1_BKIN, IR_DUT, USART2_RTS_DE_CK, TIM17_CH1, TIM3_CH2, I2C1_SDA, EVENTOUT		OSCX_IN
1	PC15-OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM1_ETR, TIM3_CH3		OSCX_OUT
2	VDD/VDDA	S	-	-	-	-	-
3	VSS/VSSA	S	-	-	-	-	-
4	PF2-NRST	I/O	-	-	MCO, TIM1_CH4		NRST
5	PA0	I/O	FT	-	USART2_CTS, TIM16_CH1, USART1_TX, TIM1_CH1		ADC_IN0, WKUP1
6	PA1	I/O	FT	-	SP11_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM17_CH1, USART1_RX, TIM1_CH2, I2C1_SMB, EVENTOUT		ADC_IN1
7	PA2	I/O	FT	-	SP11_MOSI/I2S1_SD, USART2_RX, TIM16_CHN, TIM3_ETR, TIM1_CH3		ADC_IN2, WKUP4, LSCO
8	PA3	I/O	FT	-	USART2_RX, TIM1_CH1N, TIM1_CH4, EVENTOUT		ADC_IN3
9	PA4	I/O	FT	-	SP11_NSS/I2S1_WS, USART2_RX, TIM1_CH2N, TIM14_CH1, TIM17_CH1N, EVENTOUT		ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
10	PA5	I/O	FT	-	SP11_SCK/I2S1_CK, USART2_RX, TIM1_CH3N, TIM1_CH1, EVENTOUT		ADC_IN5
11	PA6	I/O	FT	-	SP11_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1		ADC_IN6
12	PA7	I/O	FT	-	SP11_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1		ADC_IN7
13	PA8	I/O	FT	-	MCO, USART2_TX, TIM1_CH1, EVENTOUT, SP11_NSS/I2S1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MC02		ADC_IN8
-	PA9	I/O	FT	(1)	MCO, USART1_TX, TIM1_CH2, TIM3_ETR, I2C1_SCL, EVENTOUT		-
-	PA10	I/O	FT	(1)	USART1_RX, TIM1_CH3, MC02, TIM17_BKIN, I2C1_SDA, EVENTOUT		-
14	PA11 [PA9]	I/O	FT	(1)	SP11_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN		ADC_IN11
15	PA12 [PA10]	I/O	FT	(1)	SP11_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN		ADC_IN12
16	PA13	I/O	FT	(2)	SWDIO, IR_OUT, TIM3_ETR, USART2_RX		ADC_IN13
17	PA14-BOOT0	I/O	FT	(2)	SWCLK, USART2_RX, EVENTOUT, SP11_NSS/I2S1_WS, USART1_RX, TIM1_CH1, MC02, USART1_RTS_DE_CK		ADC_IN14, BOOT0
	PB6	I/O	FT	-	USART1_TX, TIM1_CH3, TIM16_CHN, TIM3_CH3, USART1_RTS_DE_CK, USART1_CTS, I2C1_SCL, USART1_SMB, SP11_MOSI/I2S1_SD, USART1_RX, TIM1_CH1, MC02, SP11_SCK/I2S1_CK, TIM1_CH2, TIM3_CH1, TIM3_CH2, TIM16_BKIN, TIM17_BKIN		WKUP3
19	PB7	I/O	FT	-	USART1_RX, TIM1_CH4, TIM17_CHN, TIM3_CH4, I2C1_SDA, EVENTOUT, USART2_CTS, TIM16_CH1, TIM3_CH1, I2C1_SCL		RTC_REFIN

1. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFGR1 register.

1. Pins PA0 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_C1_CRL register.
2. Upon reset, these pins are configured as SWD alternate functions, and the internal pull-up on PA13 pin and the internal pull-downs on PA14 pin are activated.

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Title: MICROCONTROLLER

ID: ABX001

Version: V0.3



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