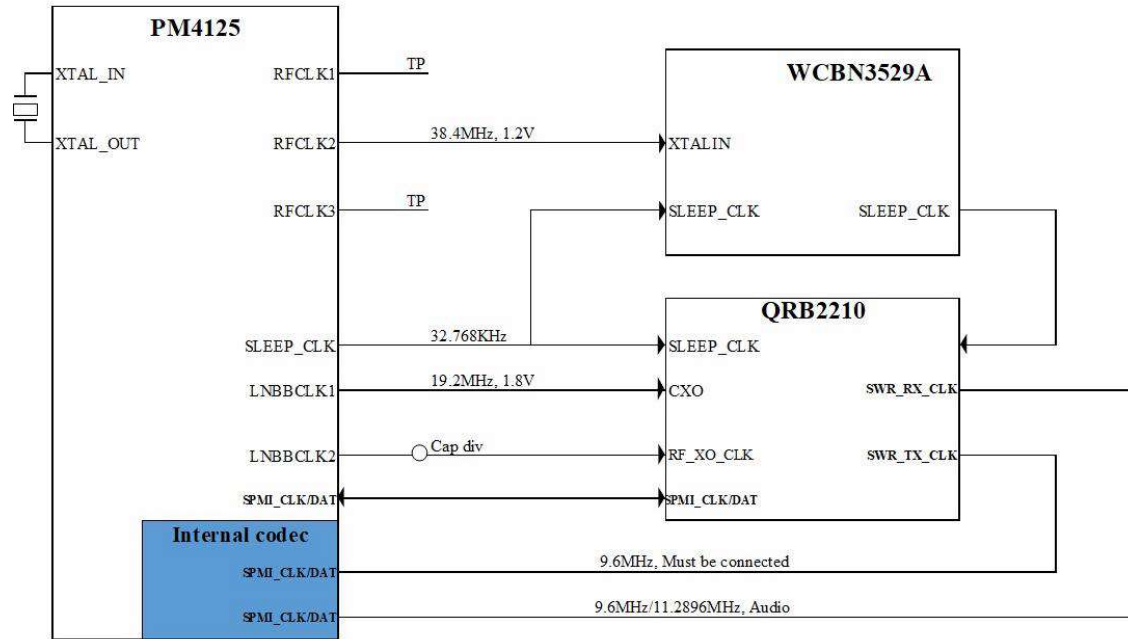


VERSION HISTORY

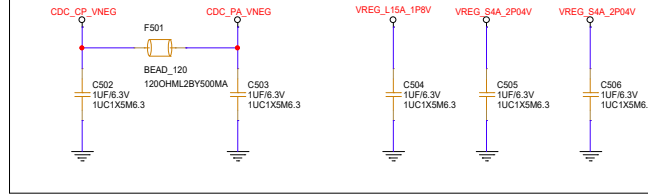
IMOLA REFERENCE DESIGN FOR ARDUINO

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR
	02/Apr./2025	RFQ version	Wistron NeWeb Corporation (WNC)
	18/Apr./2025	RFQ version V2	
	9/Jun./2025	ENG version	
	30/Jun./2025	ENG version V2	

SoC Clock Block Diagram

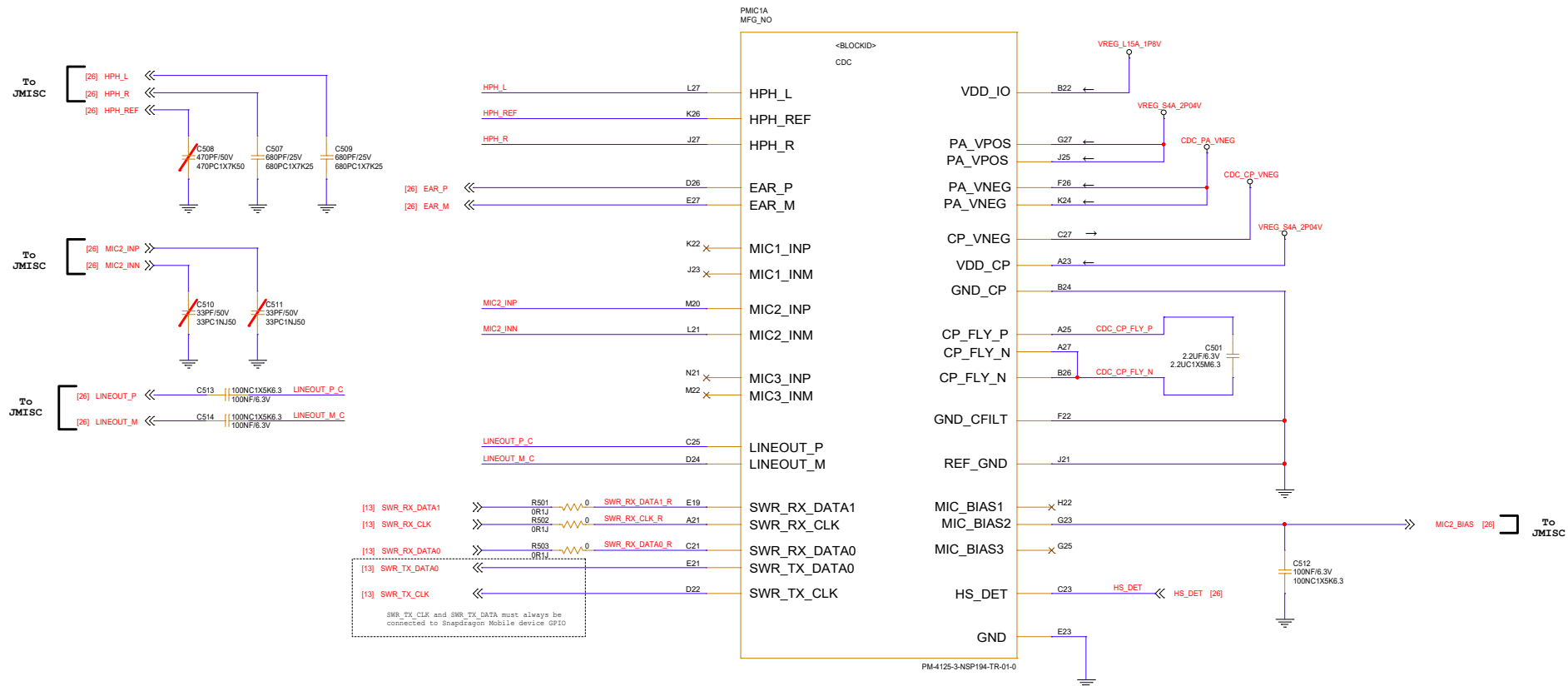


Close to PMIC1



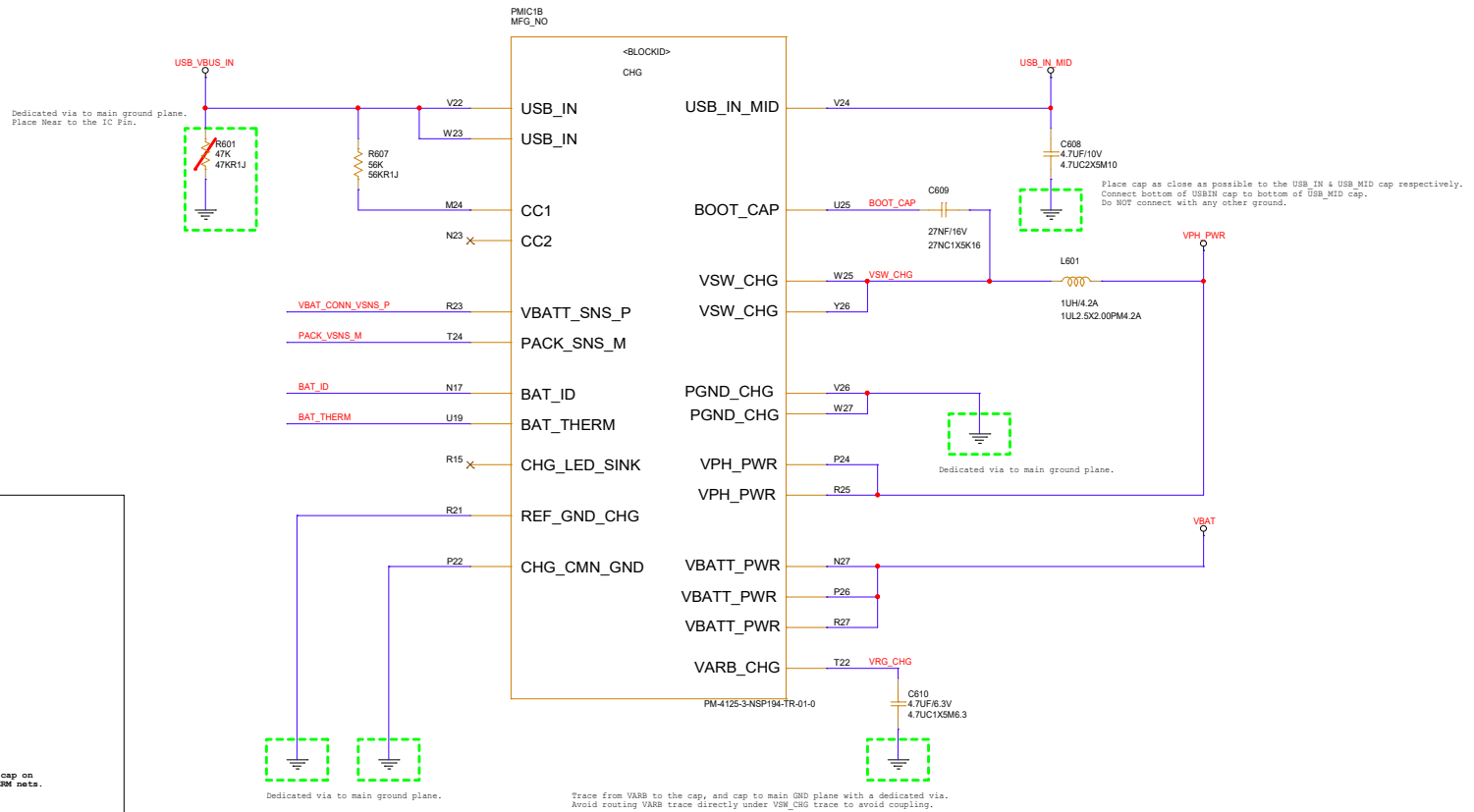
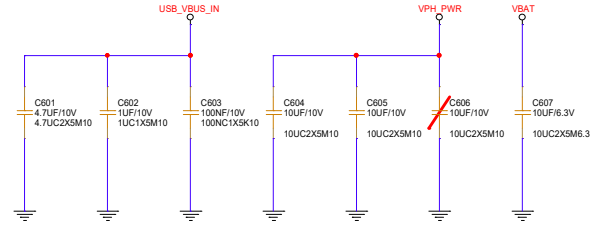
Block	Pins	Recommended unused pin termination	Notes
SoundWire	SWR_CLK ¹	GND	Applicable only for SWR_RX_CLK
	SWR_DATA ¹	GND	Applicable only for SWR_RX_DATA
Analog I/P and O/P	MICx_INP	Floating (NC)	
	MICx_INM	Floating (NC)	
	MIC_BIASx	Floating (NC)	
	EAR_P	Floating (NC)	
	EAR_M	Floating (NC)	
	LINEOUT_P	Floating (NC)	
	LINEOUT_M	Floating (NC)	
	HPH_L	Floating (NC)	
	HPH_R	Floating (NC)	
	HPH_REF	GND	
Supply	HS_DET	Floating (NC)	
	VDD_IO	Connect to the recommended supply.	Decoupling capacitors are not required.
	PA_VPOS		
	VDD_CP		
	PA_VNEG	Floating (NC)	
	CP_VNEG		
Ground	GND_x	GND	There are no strict CAD routing requirements.
	DNC	DNC	Floating (NC)

1. SWR_TX_CLK and SWR_TX_DATA must always be connected to Snapdragon Mobile device GPIO

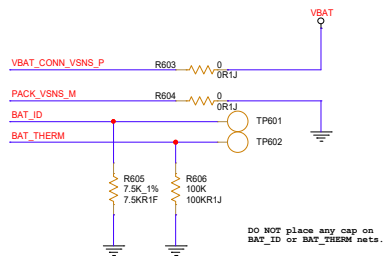


Note:
 Codec not used, reserved audio function as test point
 If layout not enough spacing to routing can delete:
 1.test points on page 5
 2.DNP parts

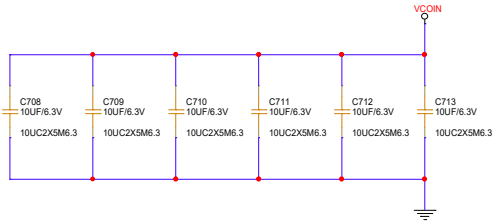
Close to PMIC1



Power from DCDC

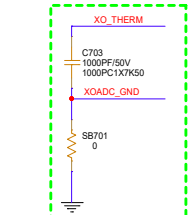
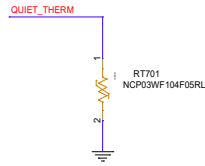
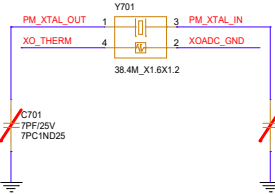


Close to PMIC1

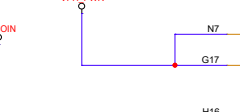
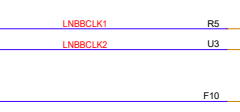
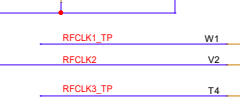
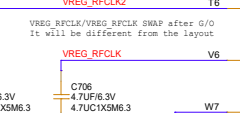
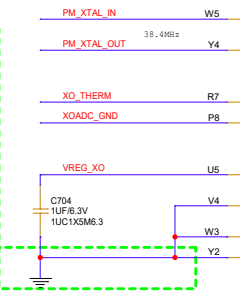
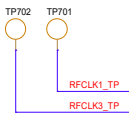


Close to PMIC1

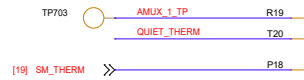
Route XTAL IN/OUT trace with length between 3-10mm



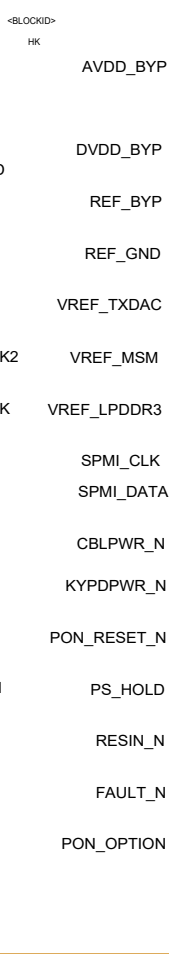
Dedicated via to main ground plane
Place Near to the IC Pin.



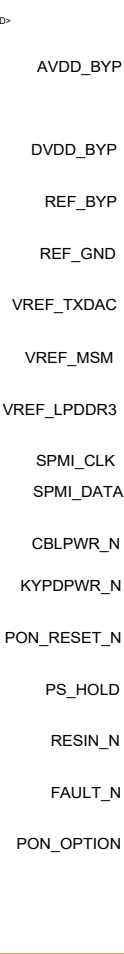
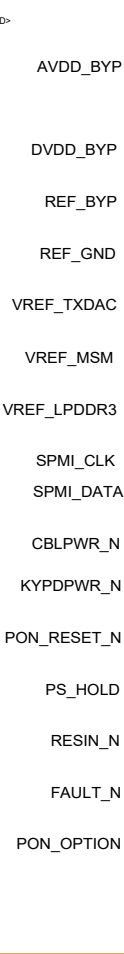
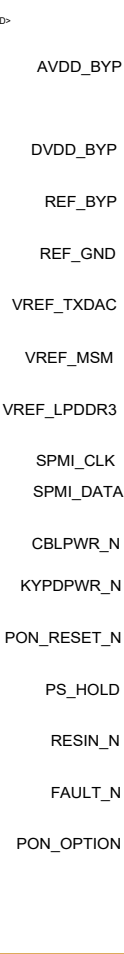
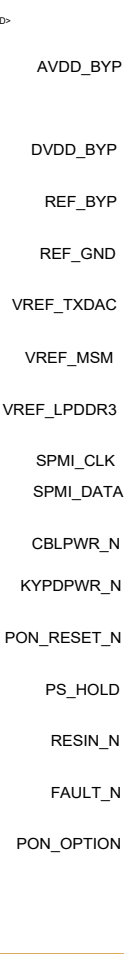
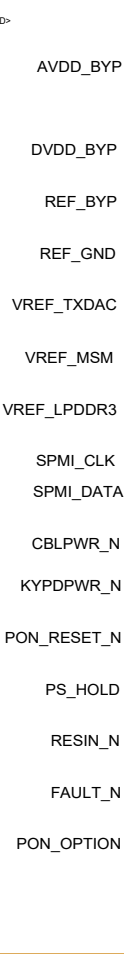
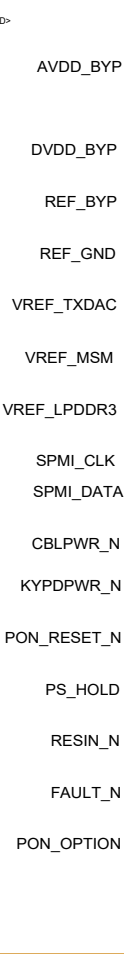
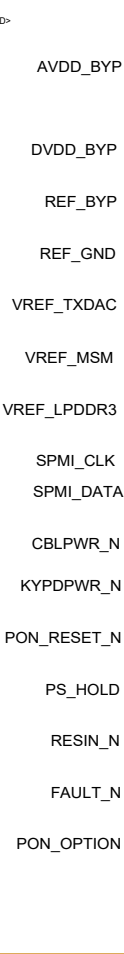
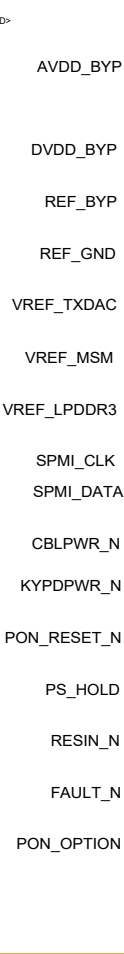
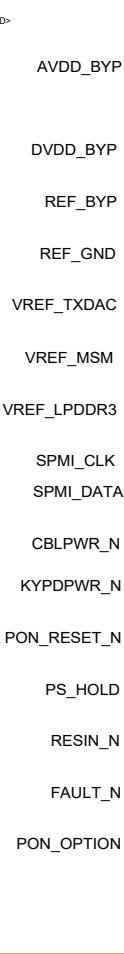
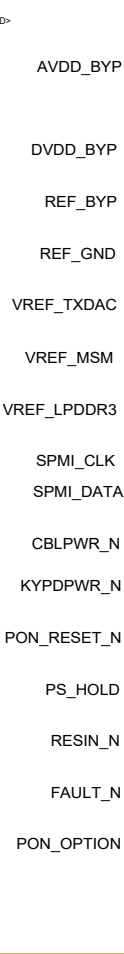
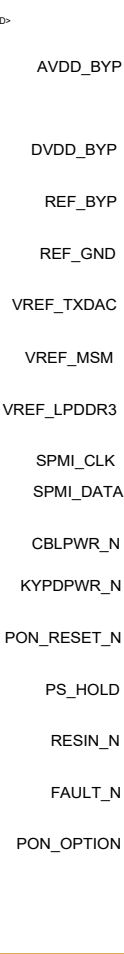
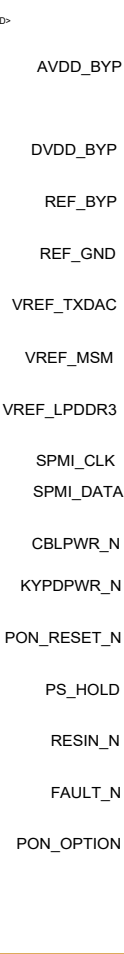
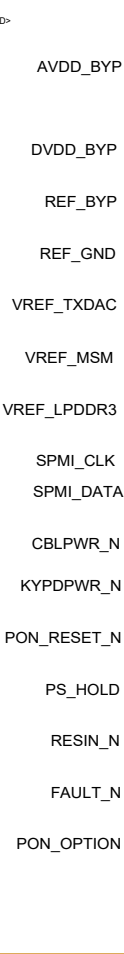
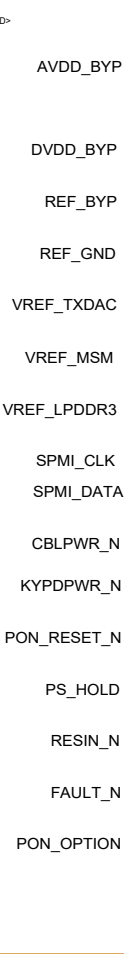
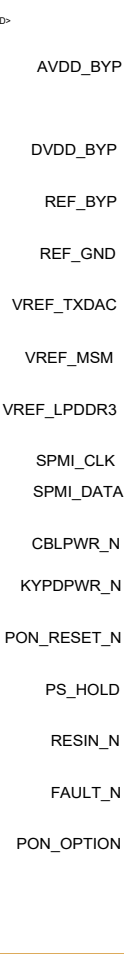
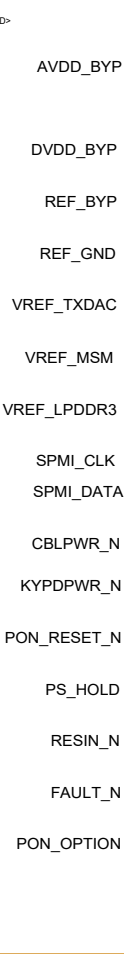
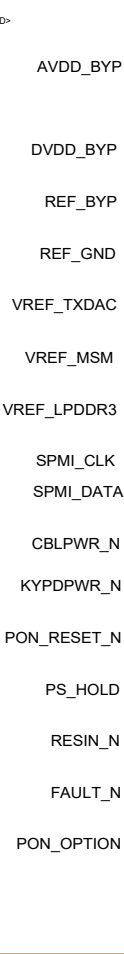
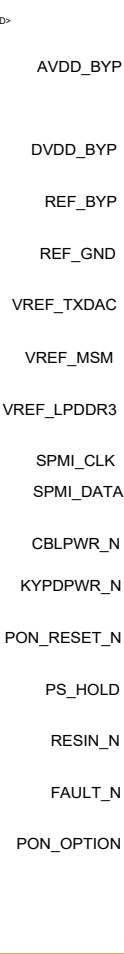
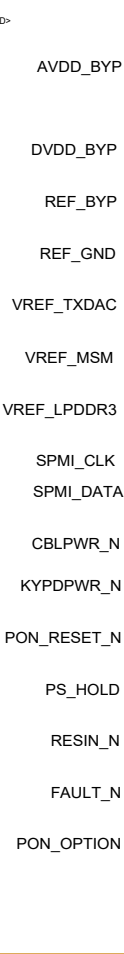
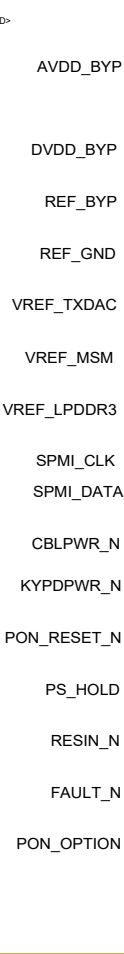
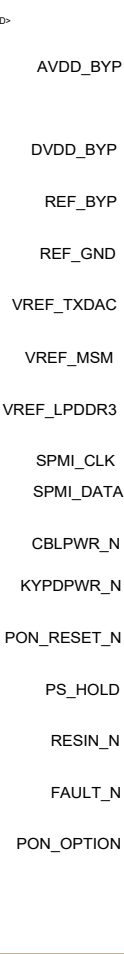
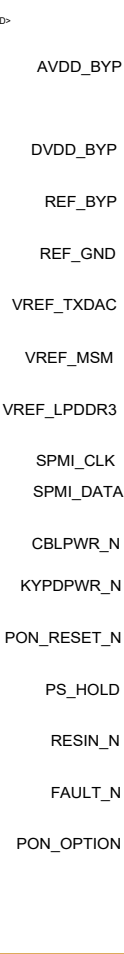
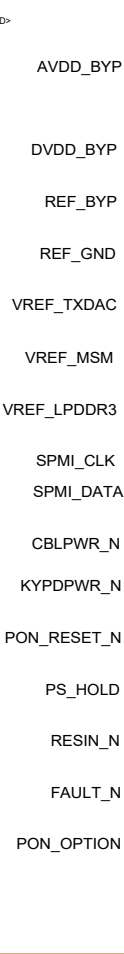
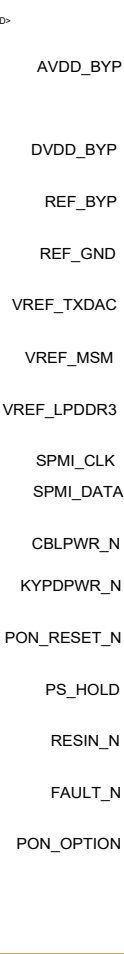
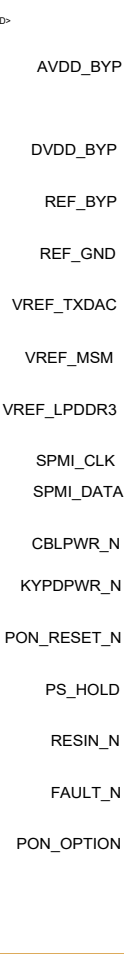
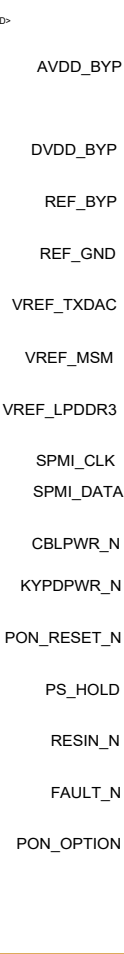
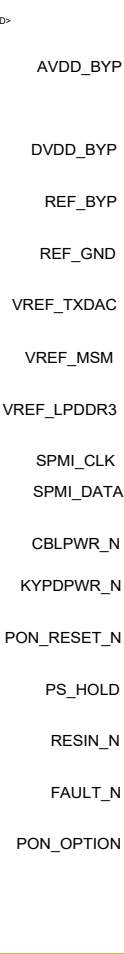
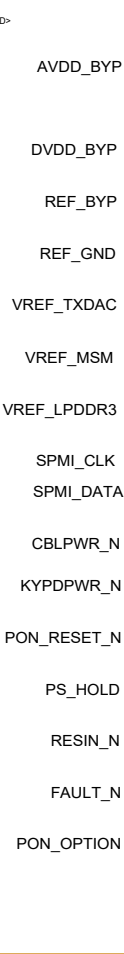
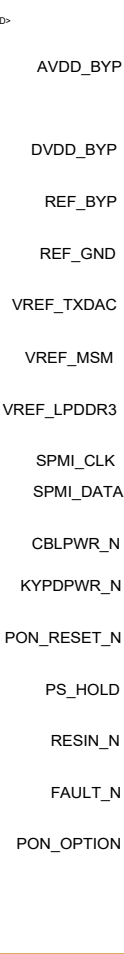
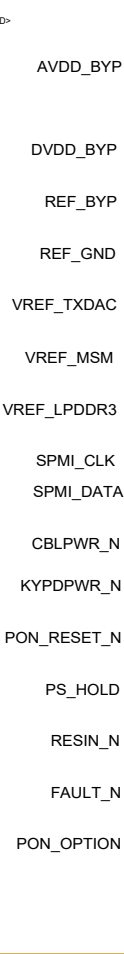
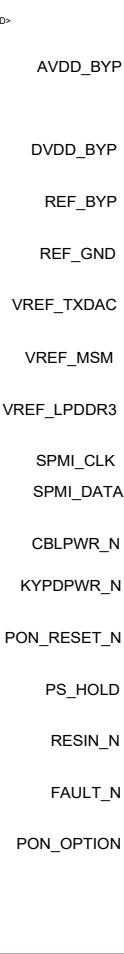
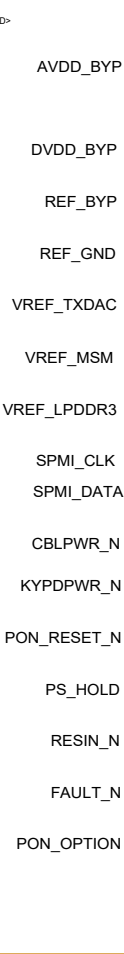
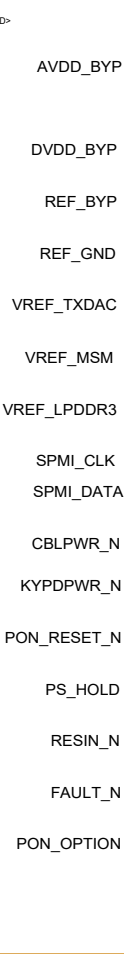
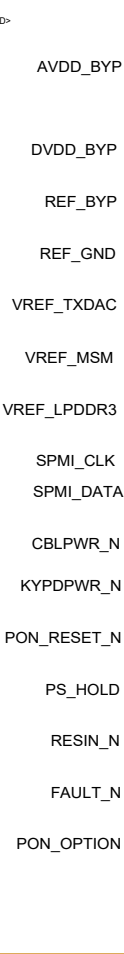
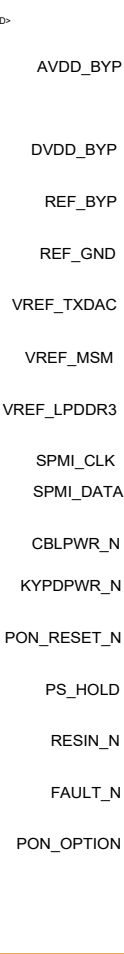
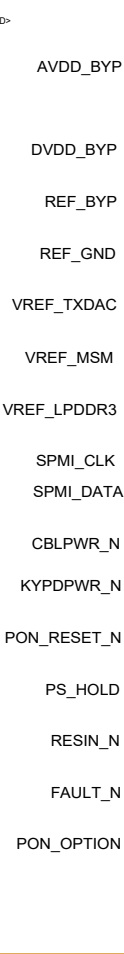
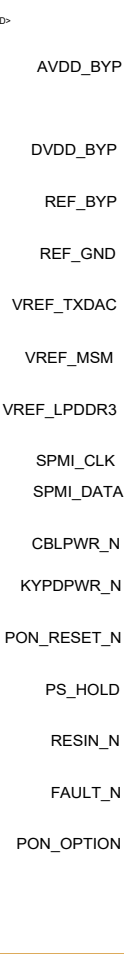
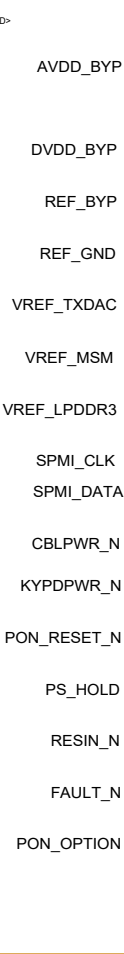
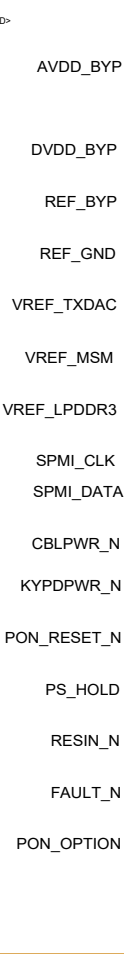
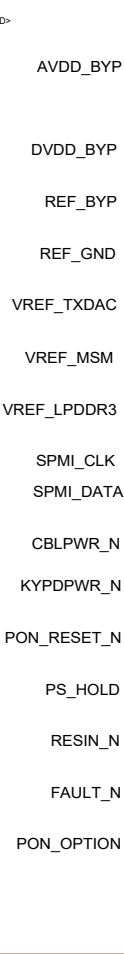
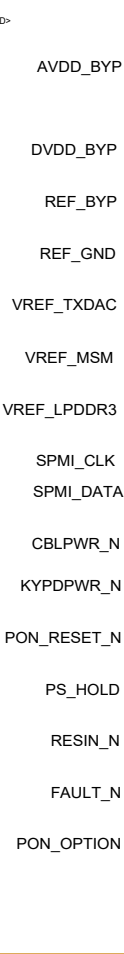
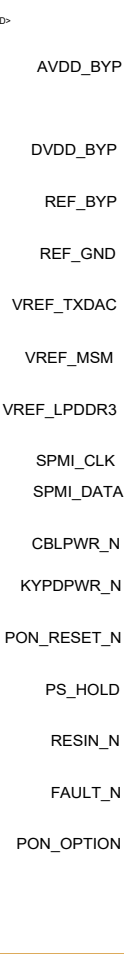
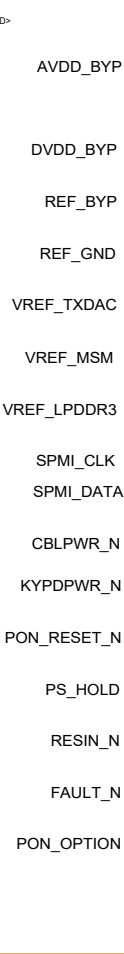
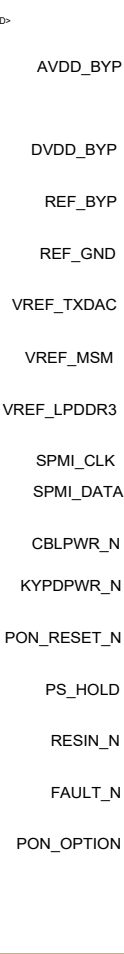
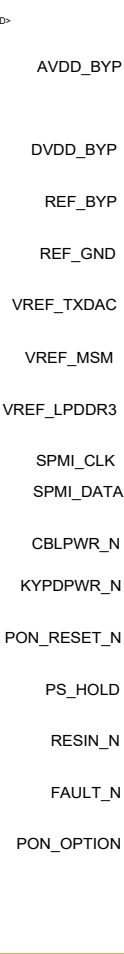
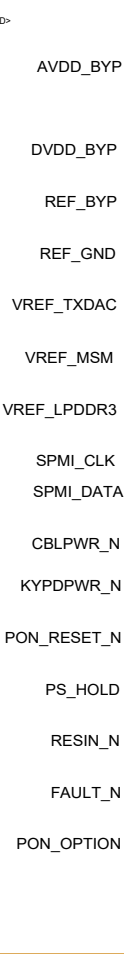
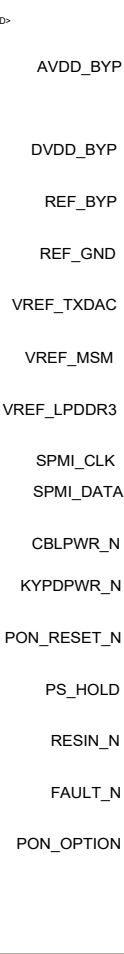
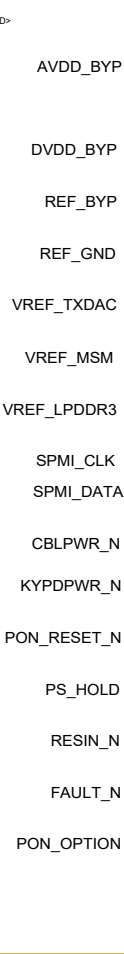
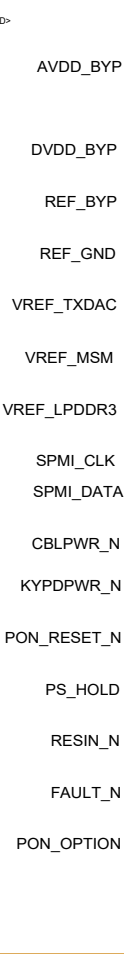
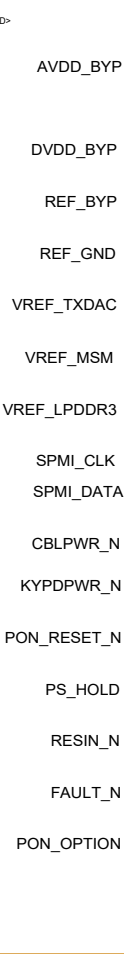
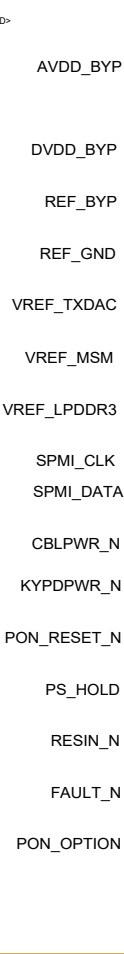
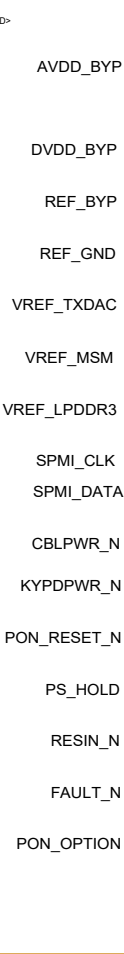
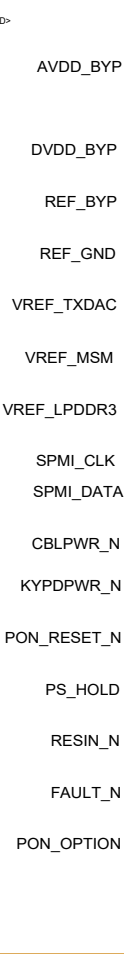
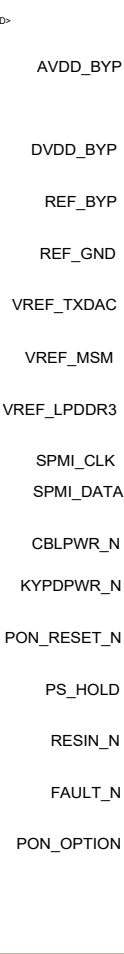
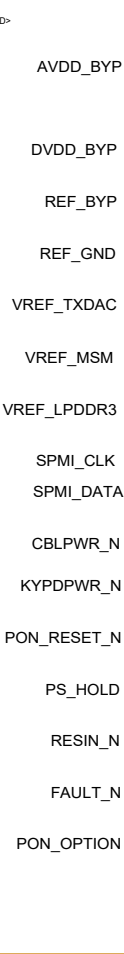
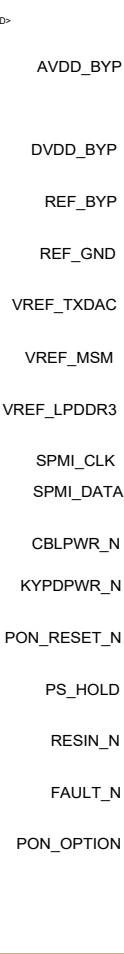
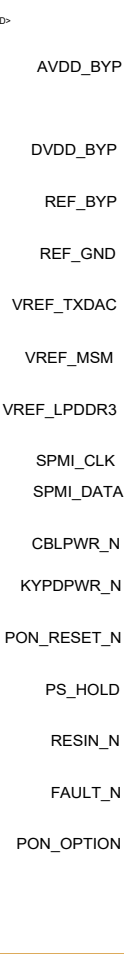
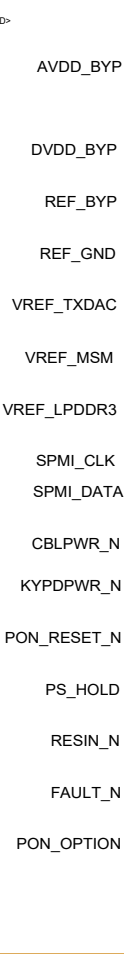
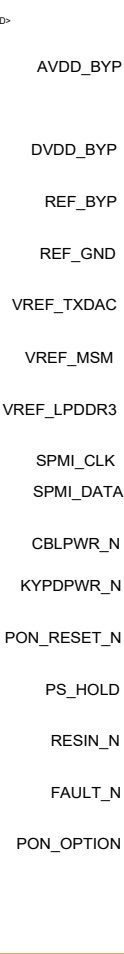
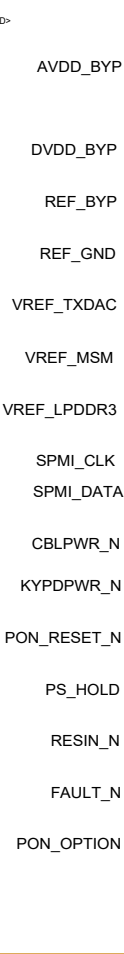
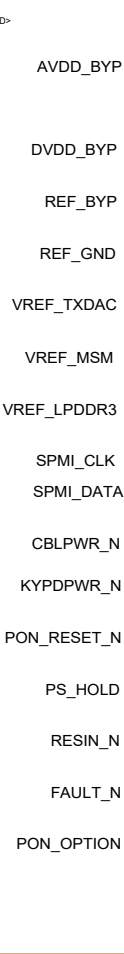
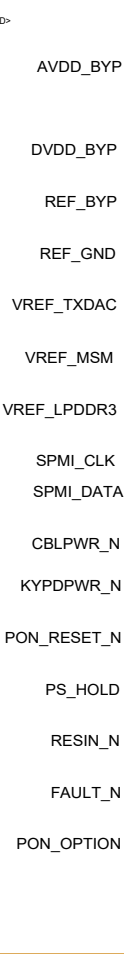
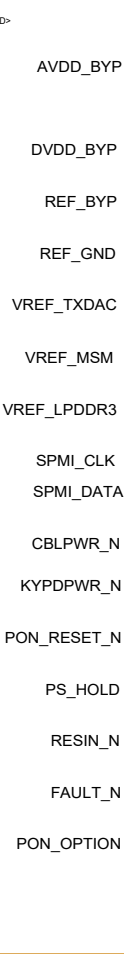
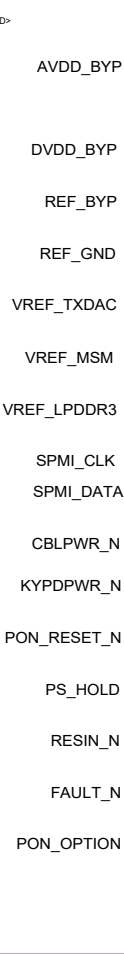
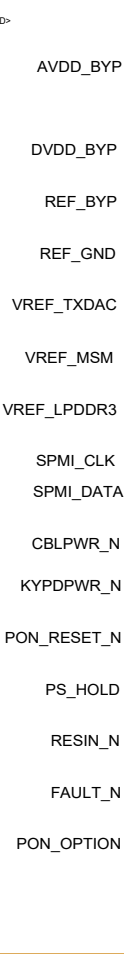
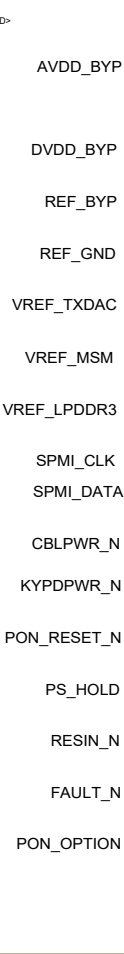
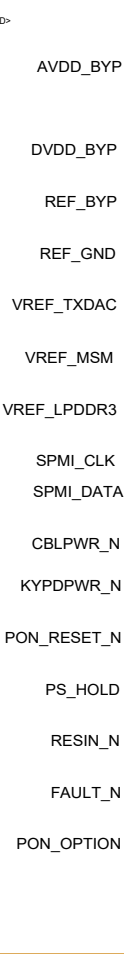
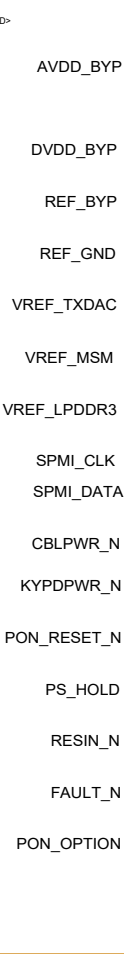
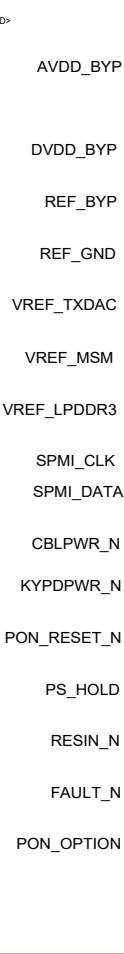
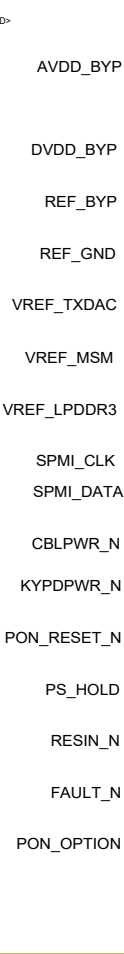
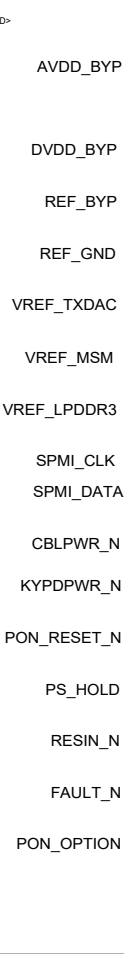
Analog Mux Reserved



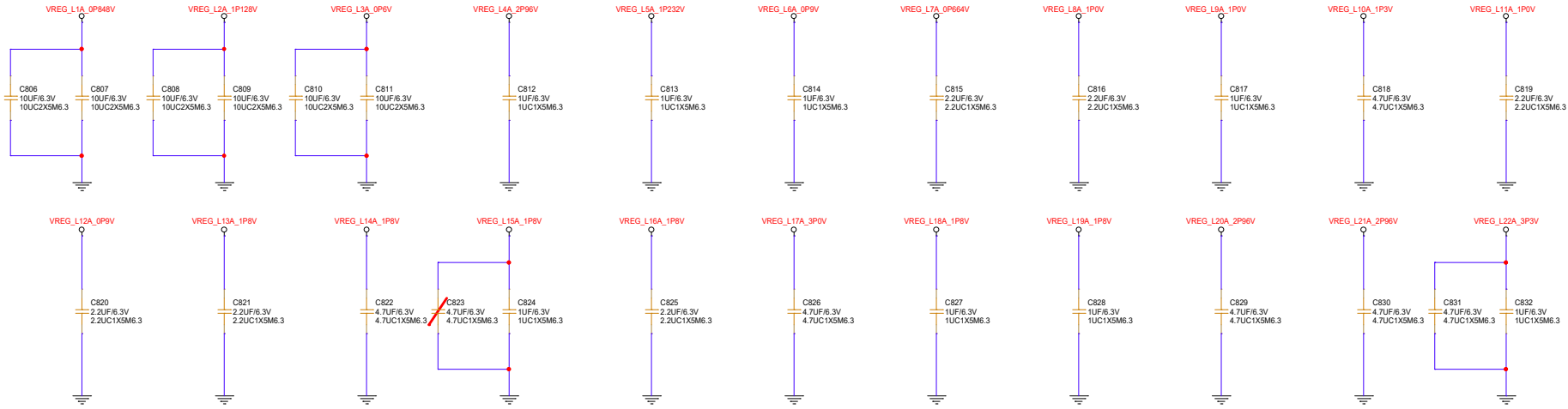
PMIC1E
MFG_NO



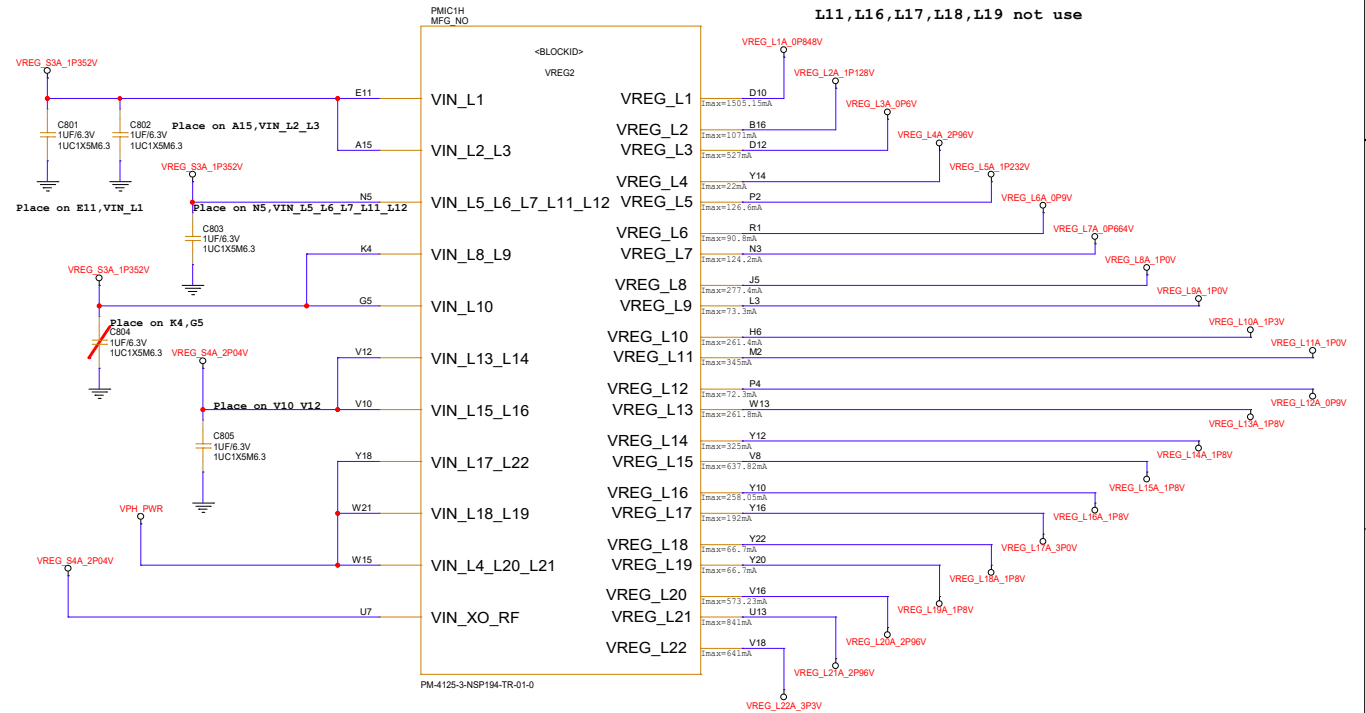
PM-4125-3-NSP194-TR-01-0

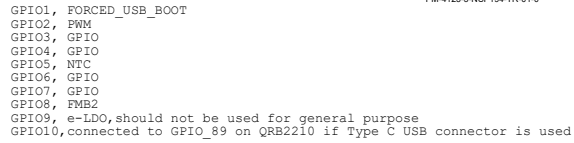


Close to PMIC1

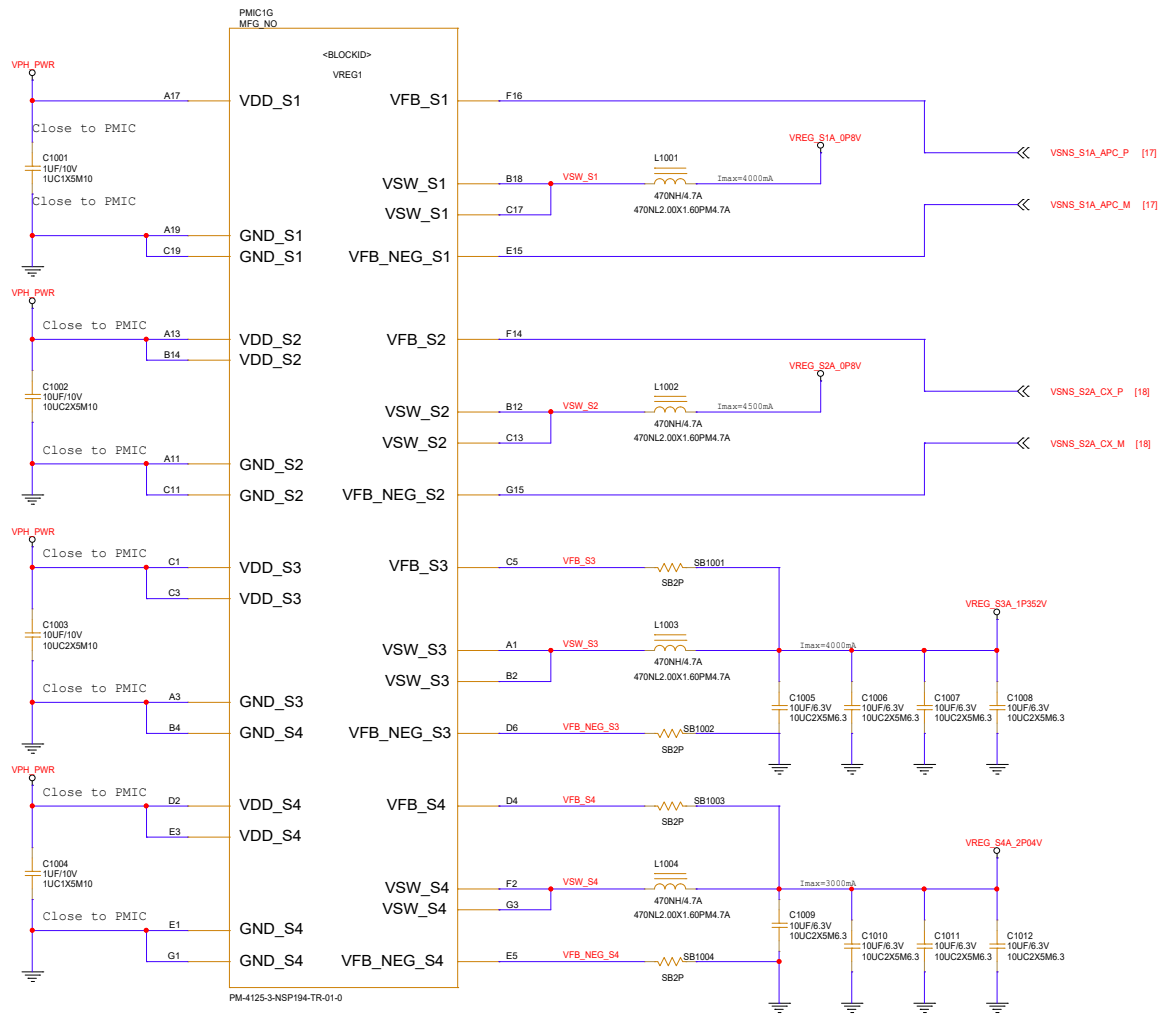


Regulator	Circuit type	I _{RATED} (mA)	Default on booting voltage (V) ¹	Nominal voltage (V)	Programmable range (V)	Default on	Slope state	Expected use(SM4125/QCS2 290/QCM2290)
L1	N1800_FT	1800	0.96	0.88	0.4-1.076	Y	ON	VDD_MX, VDDA_EBI_ABC, LPDDR3_VDD2
L2	N1200_FT	1200	1.136	1.136	0.136-1.30	Y	ON	For LPDDR3 voltage = 1.224V
L3	N1200_FT	1200	0.616	0.616	0.57-0.65	Y	OFF	LPDDR3_VDDQ
L4	MVP50	50	3.056	3.056	1.65-3.056	Y	OFF	VDDPX_2
L5	N300	300	1.232	1.232	1.10-1.312	Y	OFF	VDDA_CSI_VDD_DSI, VDD_BBRX
L6	N300	300	0.928	0.928	0.488-1.00	Y	OFF	VDD_EBI_PLL
L7	N300	300	0.728	0.664	0.40-0.728	Y	OFF	VDD_WCSS_CX
L8	N300	300	0.872	0.8	0.40-1.076	Y	ON	VDD_LPI_CX
L9	N300	300	0.928	0.8/8	0.488-0.992	Y	ON	VDD_LPI_MX
L10	N1200_FT	1200	OFF	1.304	1.15-1.38	N	OFF	WCN3950_IP3_REA
L11	N300	300	1	1	0.95-1.15	Y	OFF	WTR3925_VDD_RF1
L12	N300	300	0.928	0.928	0.488-1.00	Y	OFF	VDDA_USB_SS_DP_CORE, VDD_USB_HS_CORE
L13	LVP300	300	1.8	1.8	1.80-1.95	Y	OFF	VDDA_TXDAC, WCN3950_IP8_XO
L14	LVP600	600	1.8	1.8	1.70-1.95	Y	OFF	EMMC1_VCCQ
L15 ¹	LVP600	600	1.8	1.8	1.20-2.00	Y	ON	VDD_IO, MEM_LPDDR3_VDD1, MEM_LPDDR3_VDD1, SN100U-VDDIO
L16	LVP300	300	1.8	1.8	1.50-1.95	Y	OFF	WTR3925 (VDD_RF2)
L17	MVP300	300	OFF	3	3.00-3.544	N	OFF	TMD2725_VLED
L18	MVP150	150	OFF	1.8	1.62-3.30	N	OFF	VDD_IUM1
L19	MVP150	150	OFF	1.8	1.62-3.30	N	OFF	VDD_IUM2
L20 ¹	CP-N900	900	2.864	2.856	2.40-3.544	Y	OFF	EMMC1_VCC
L21 ¹	CP-N900	900	3.056	3.056	2.90-3.30	Y	OFF	MEM_SD_MMC_VDD and VDD_HS_USB3P1
L22	MVP600	600	OFF	3.304	2.85-3.4	N	ON	WCN3950_IP3_CHAIN0



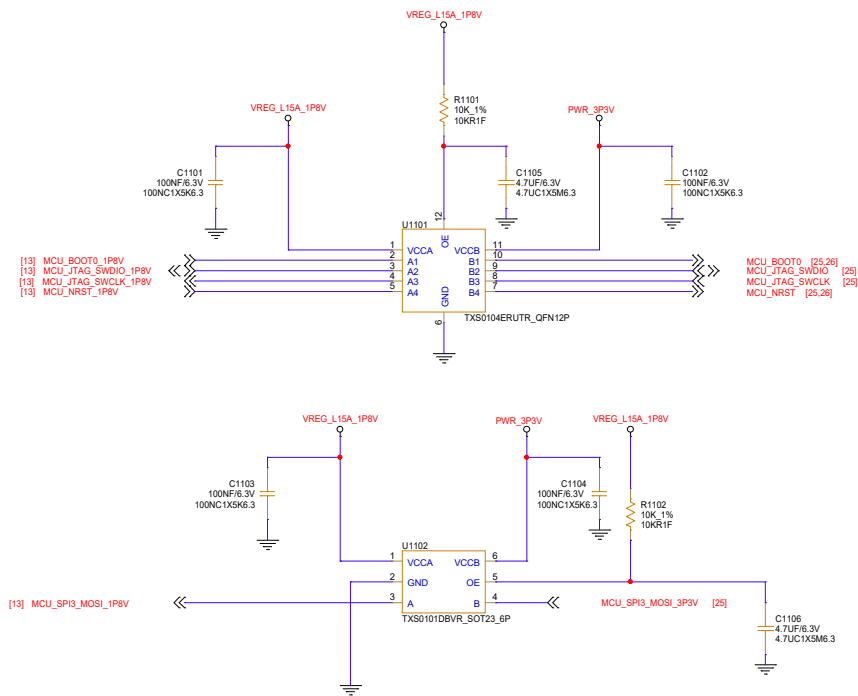


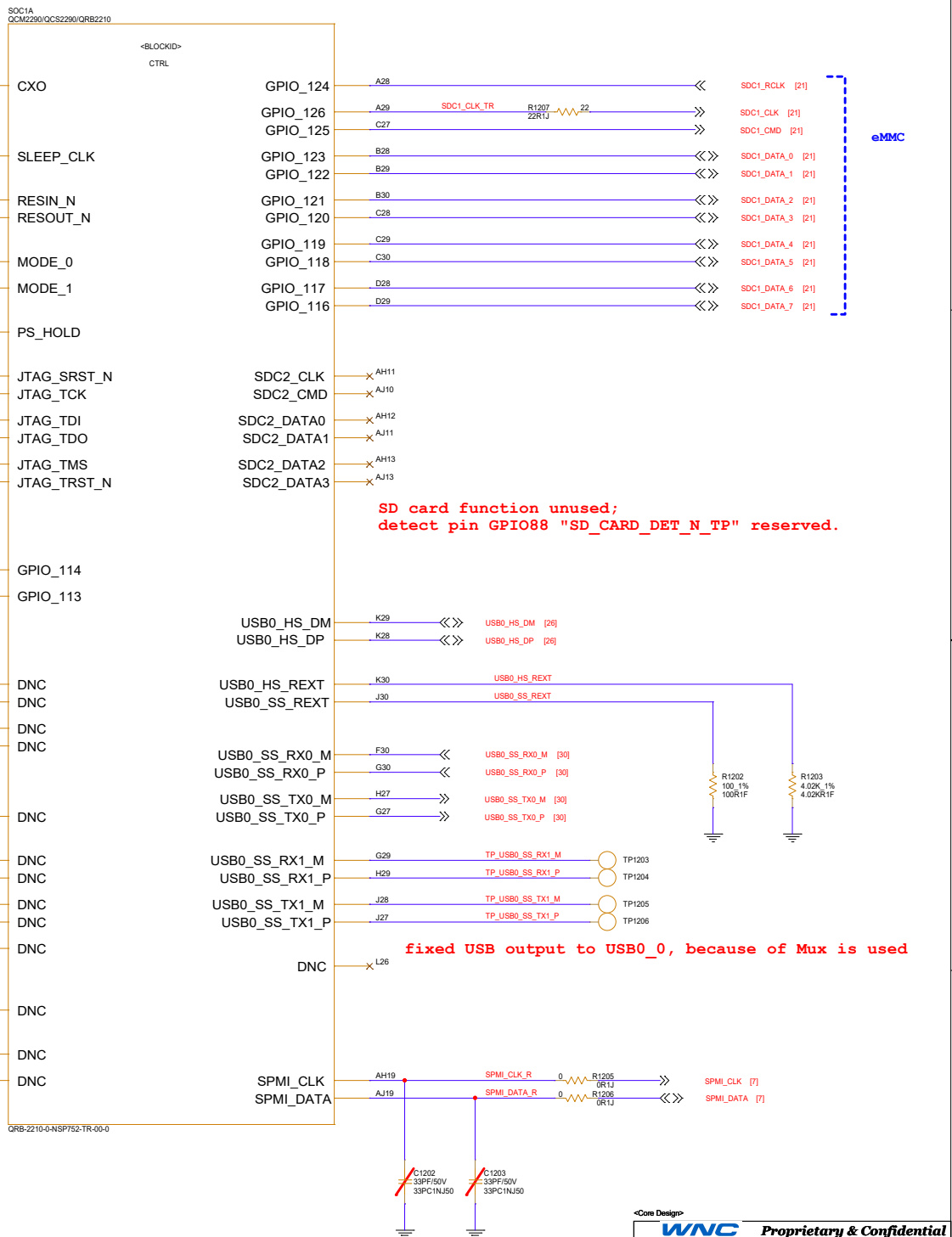
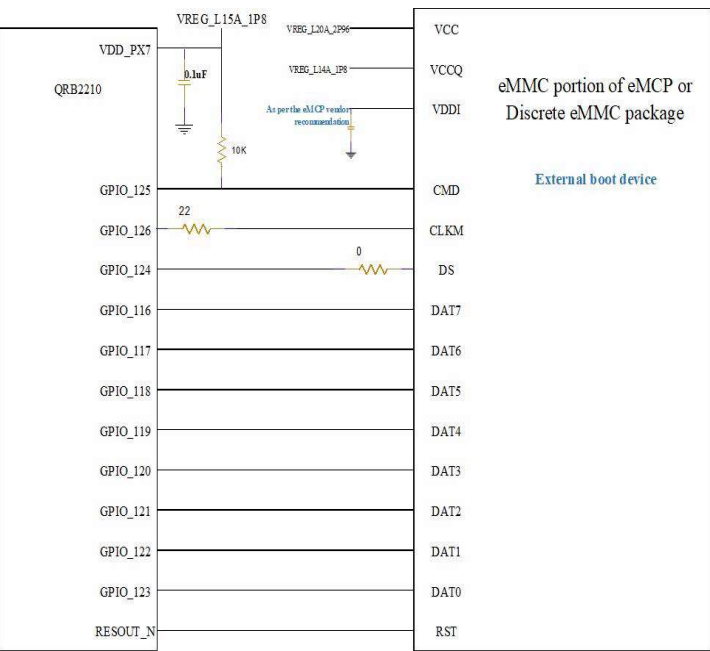
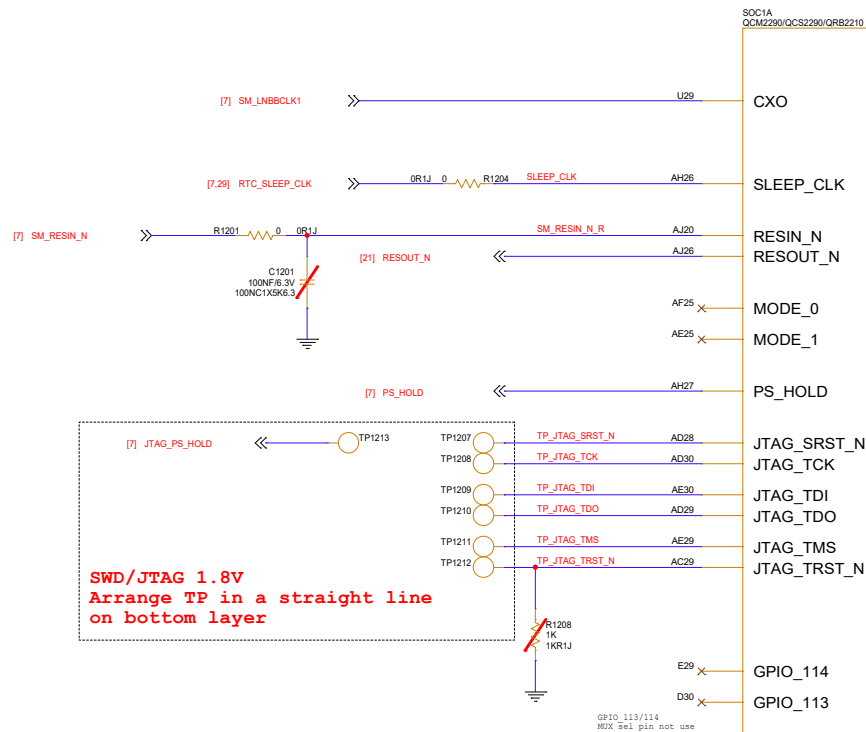
Regulator	Circuit type	I _{RATED} (mA)	Default on booting voltage (V)	Nominal voltage (V)	Programmable range (V)	Default on	Slppe state	Expected use(SM4125/QCS2 290/QCM2290)
S1	FTS512 SMPS	4000	0.728	0.8	0.72-0.99	Y	OFF	APC0
S2	FTS512 SMPS	4500	1.076	0.8	0.4-1.09	Y	Lowered	VDD_Cx
S3	FTS512 SMPS	4000	1.408	1.408	0.4-1.662	Y	Lowered	LV sub regulation
S4	FTS512 SMPS	3000	2.072	2.072	1.10-2.35	Y	Lowered	MV sub regulation



Note:
Place Cap as close to PMIC as possible,
requirement:
-Loop inductance from (VIN_Sx to Cin + Cin to GND_Sx) must be < 3nH

3.3V to 1.8V level shift

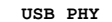
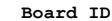
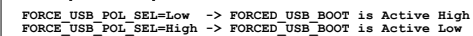


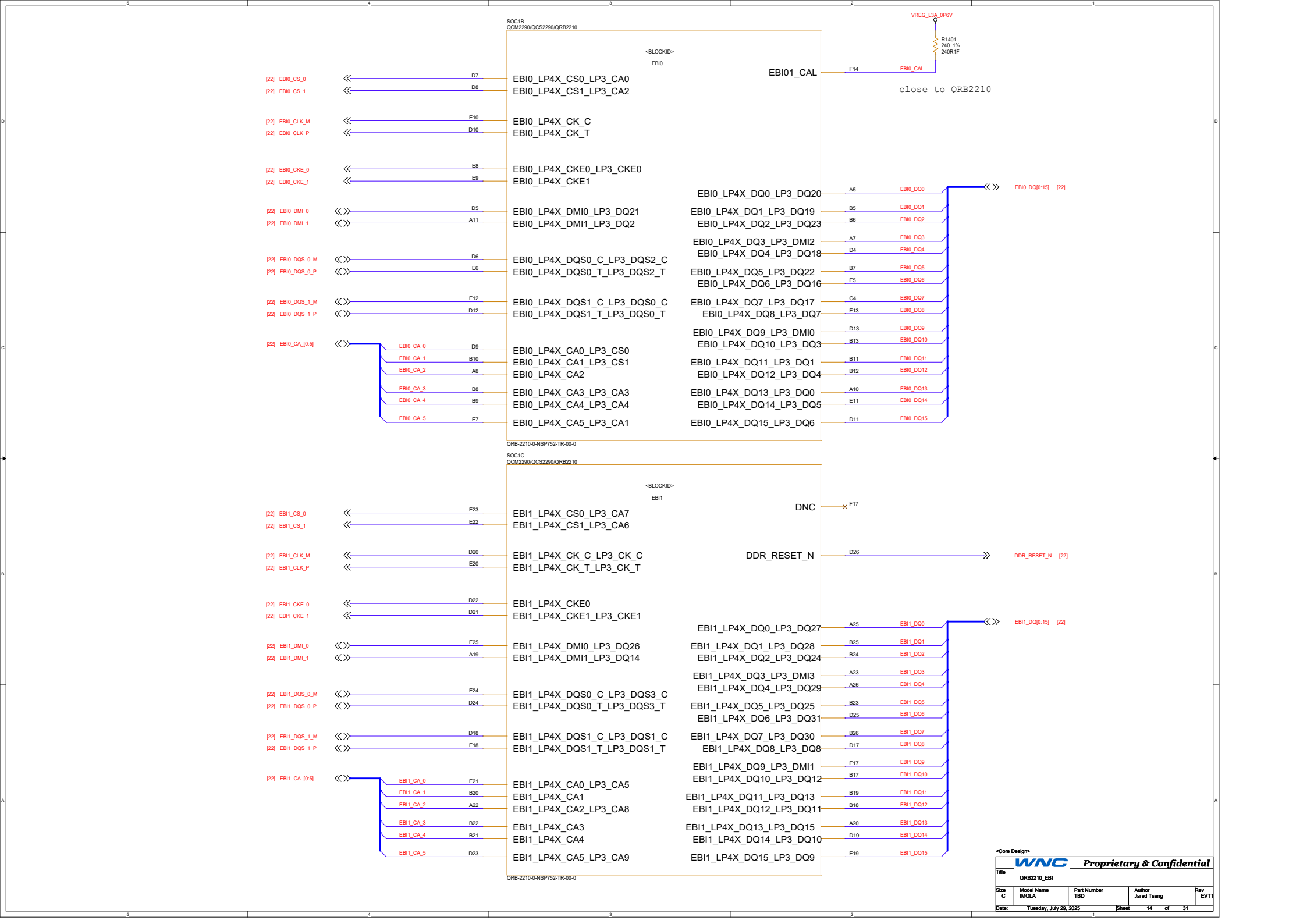


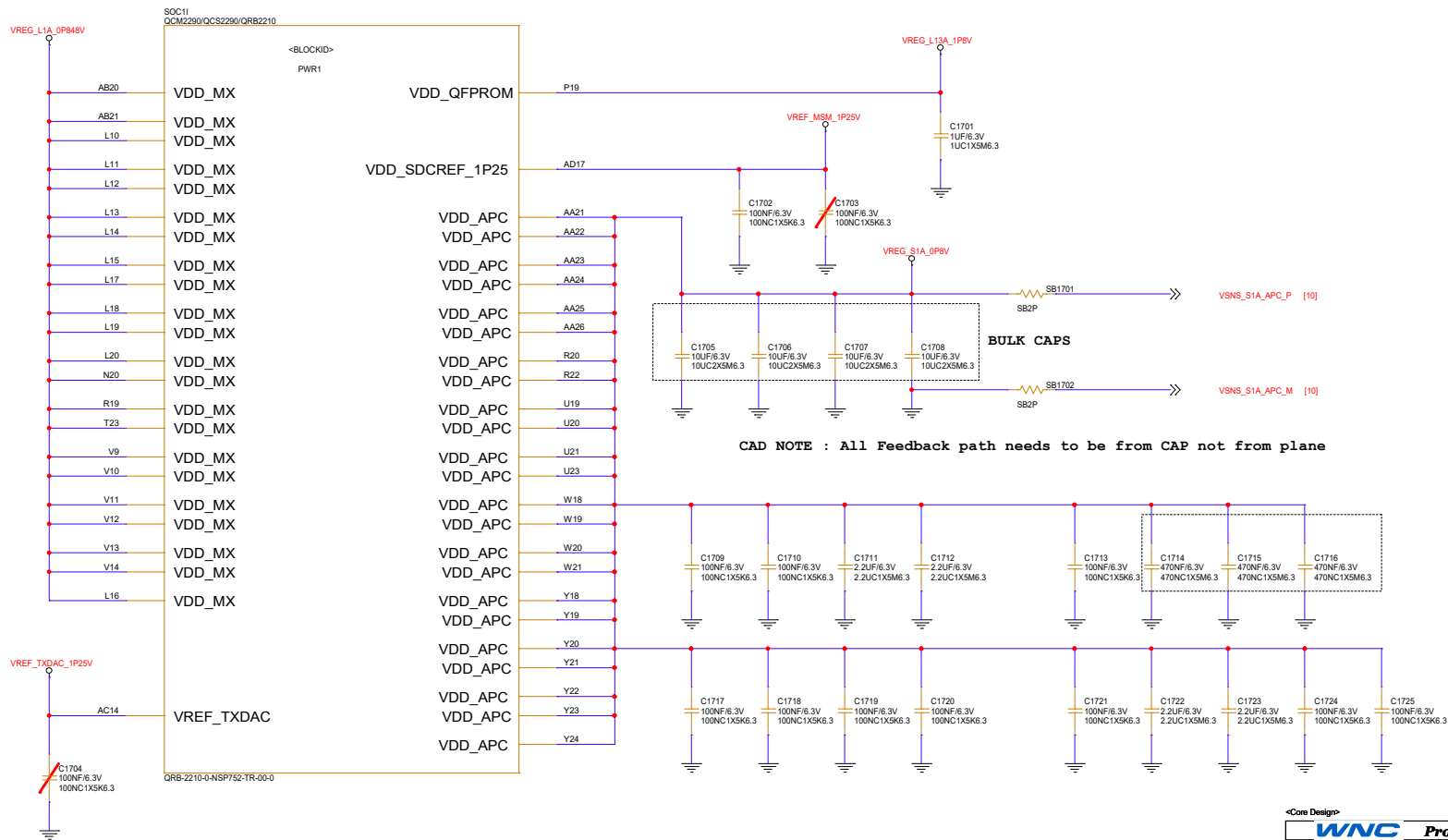
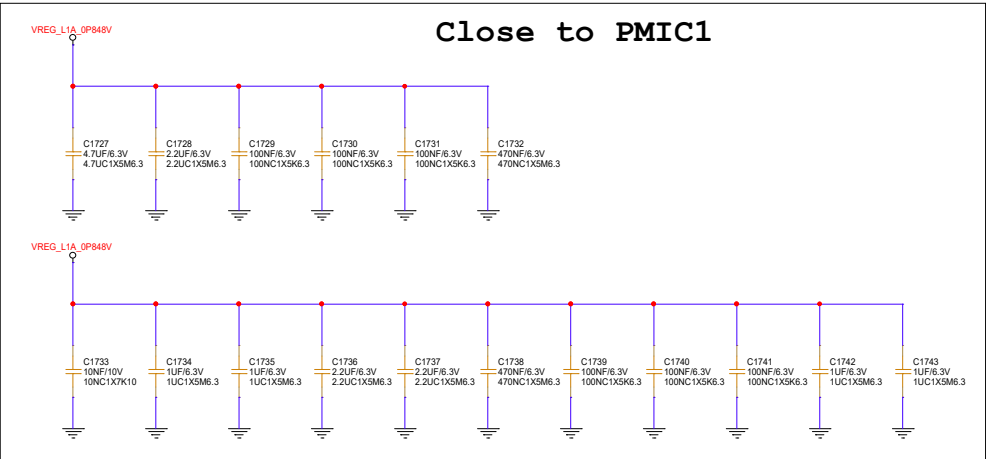
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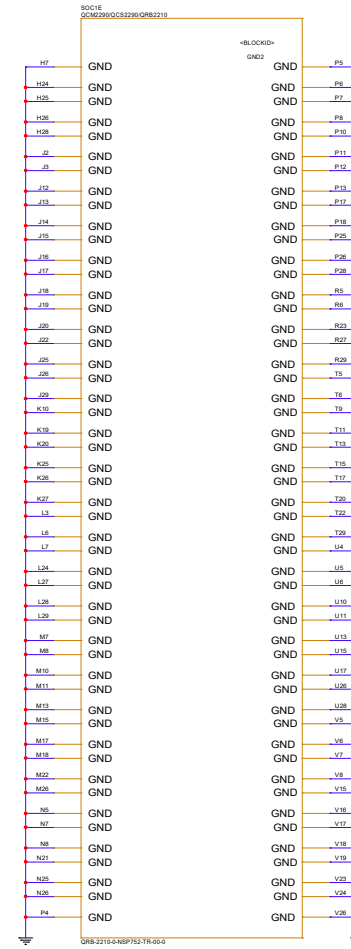
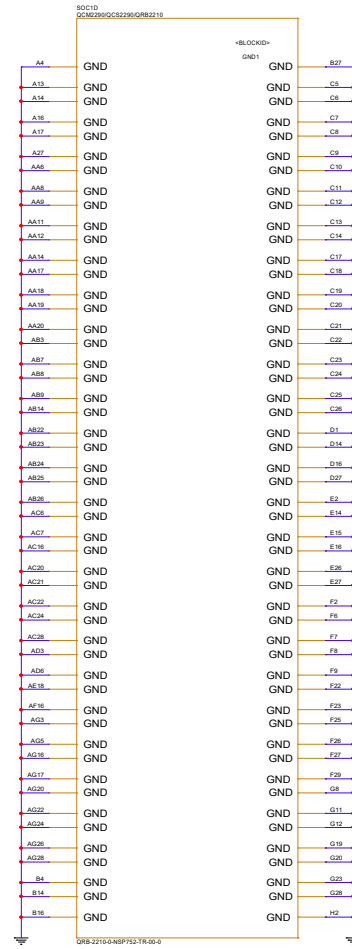
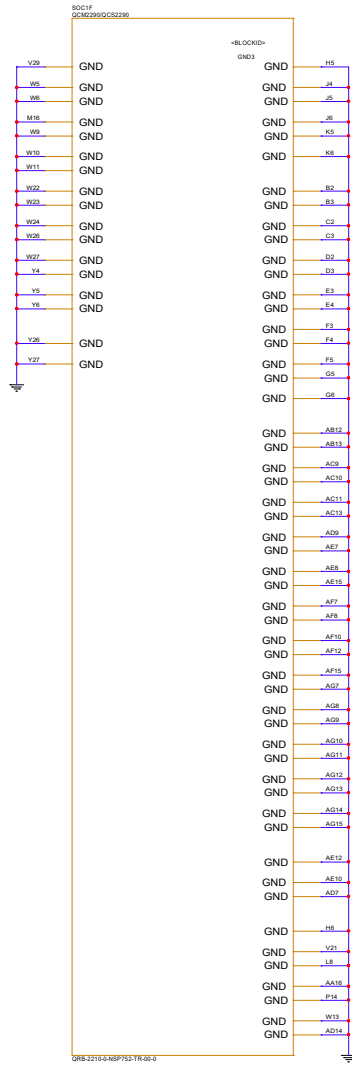
graph LR
    PGIO_48[WDOG] --> Inverter[Inverter]
    Inverter --> OR[OR]
    Qfuse[Watchdog enable Qfuse] --> OR
    OR --> WDOG_EN[WDOG_EN]
  
```

```
Boot config
Set default 0b000
```

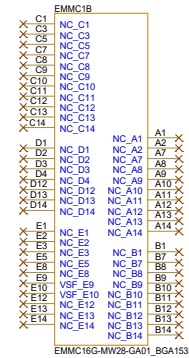
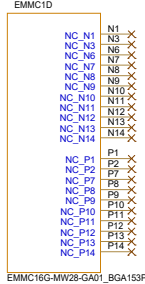
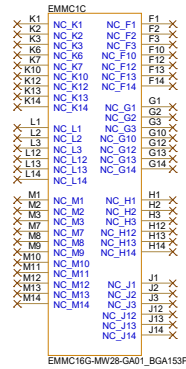
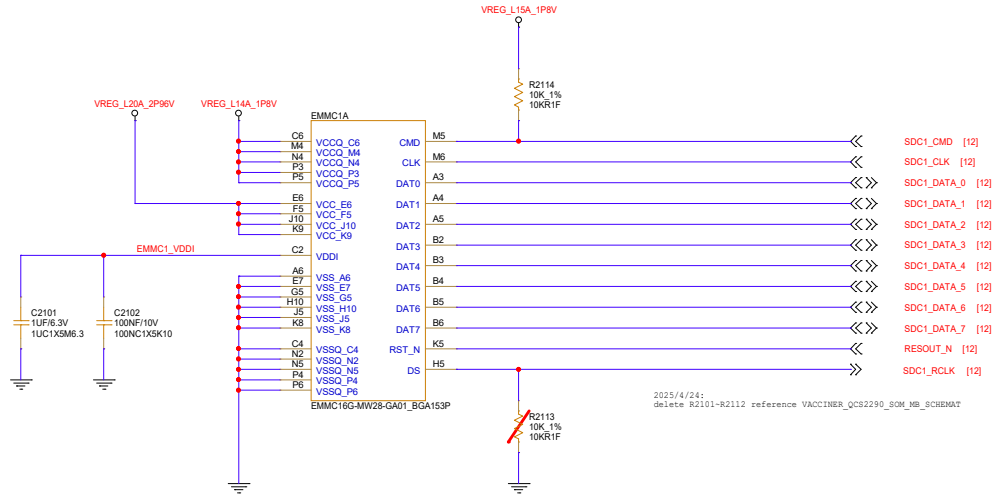
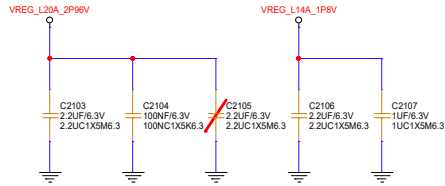




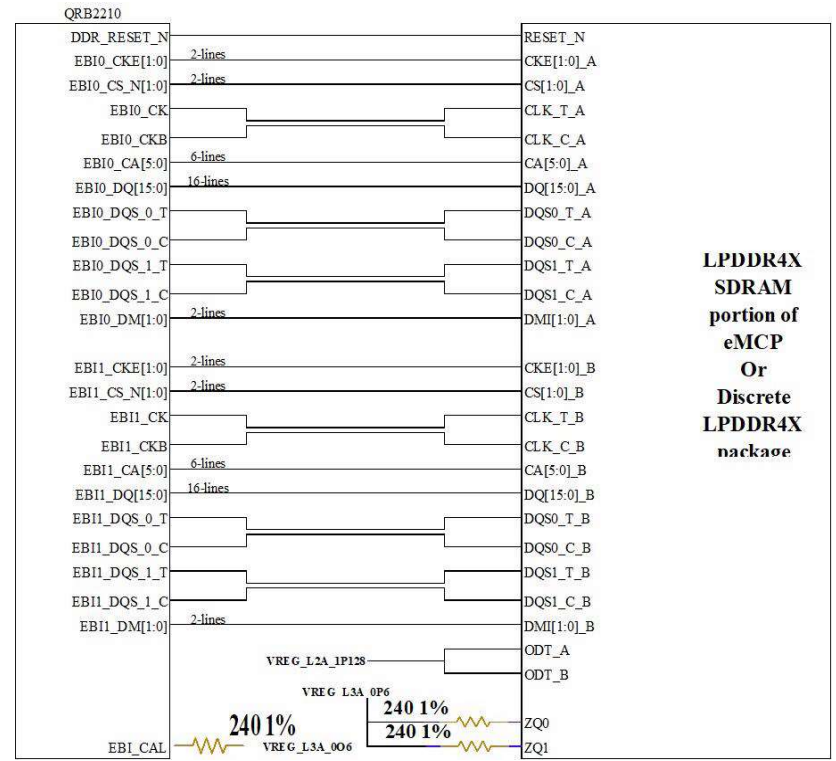
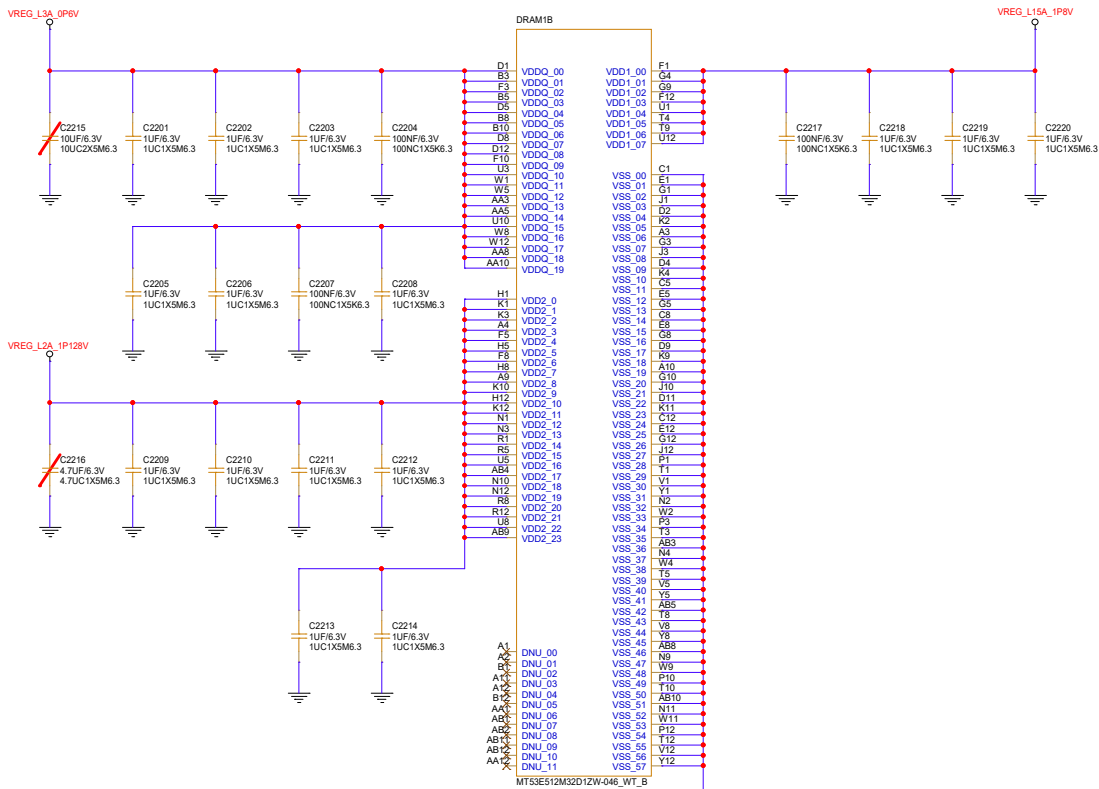




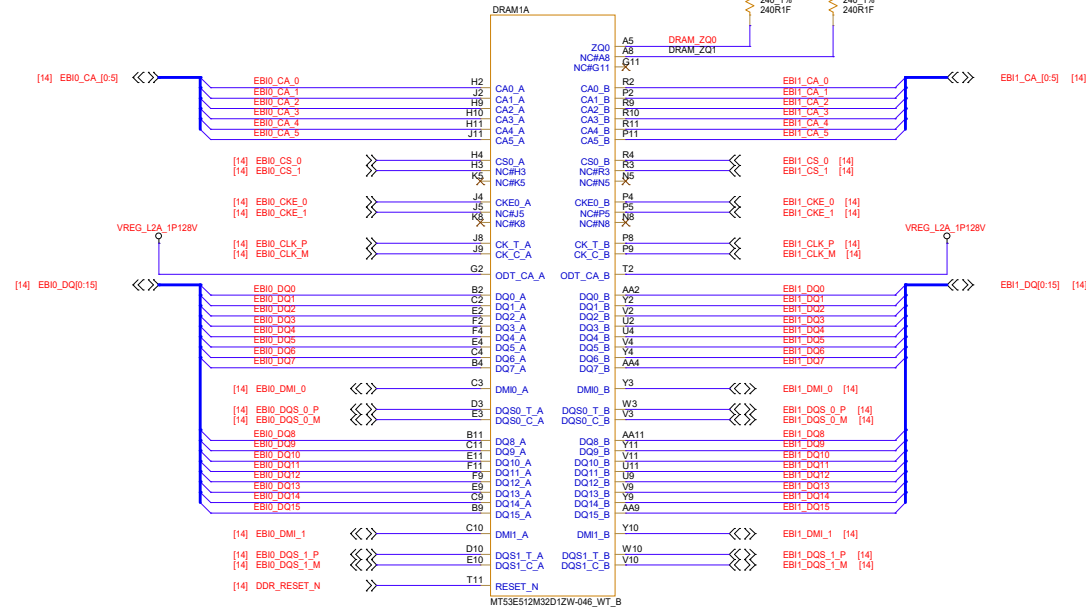
Close to eMMC1

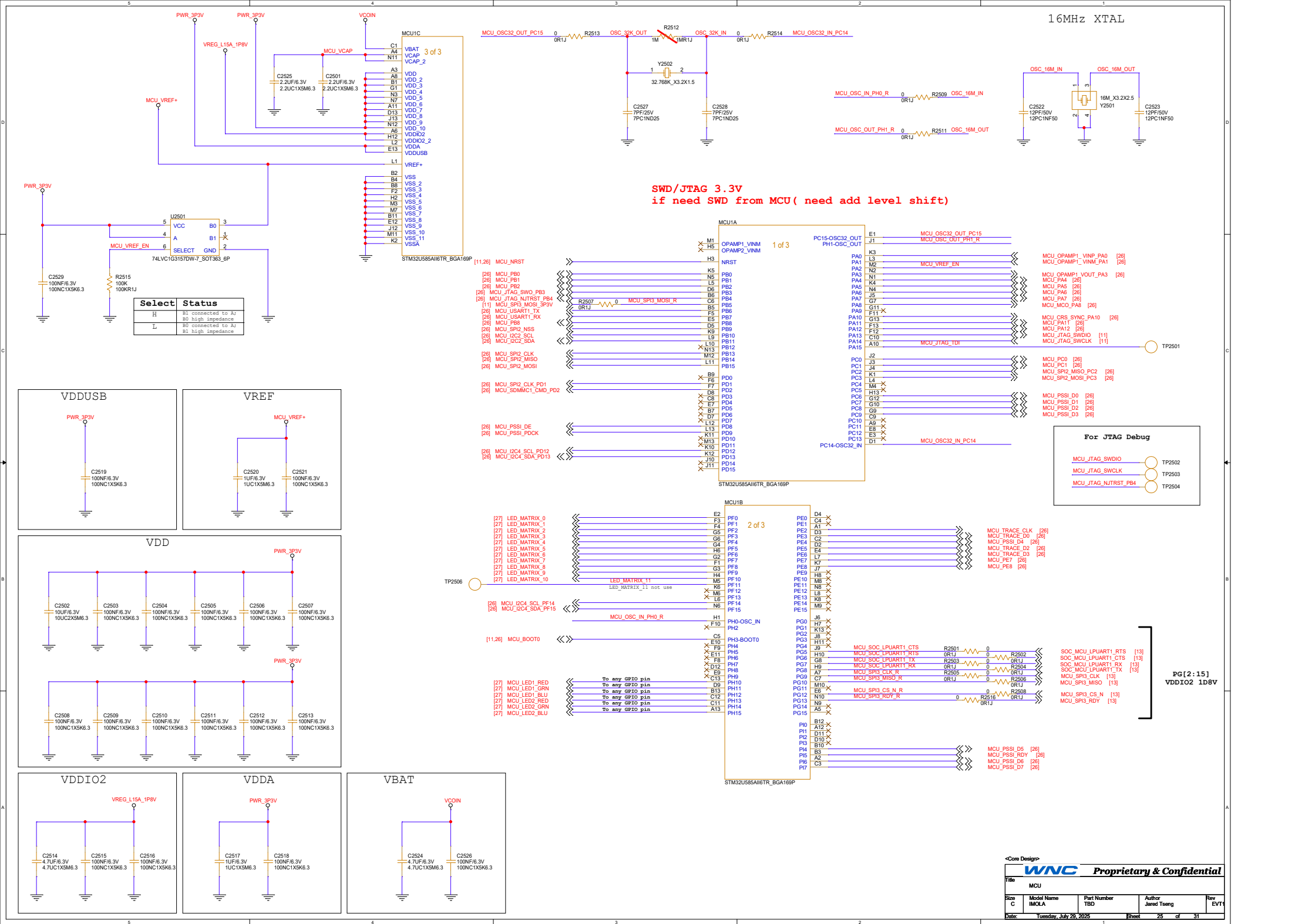


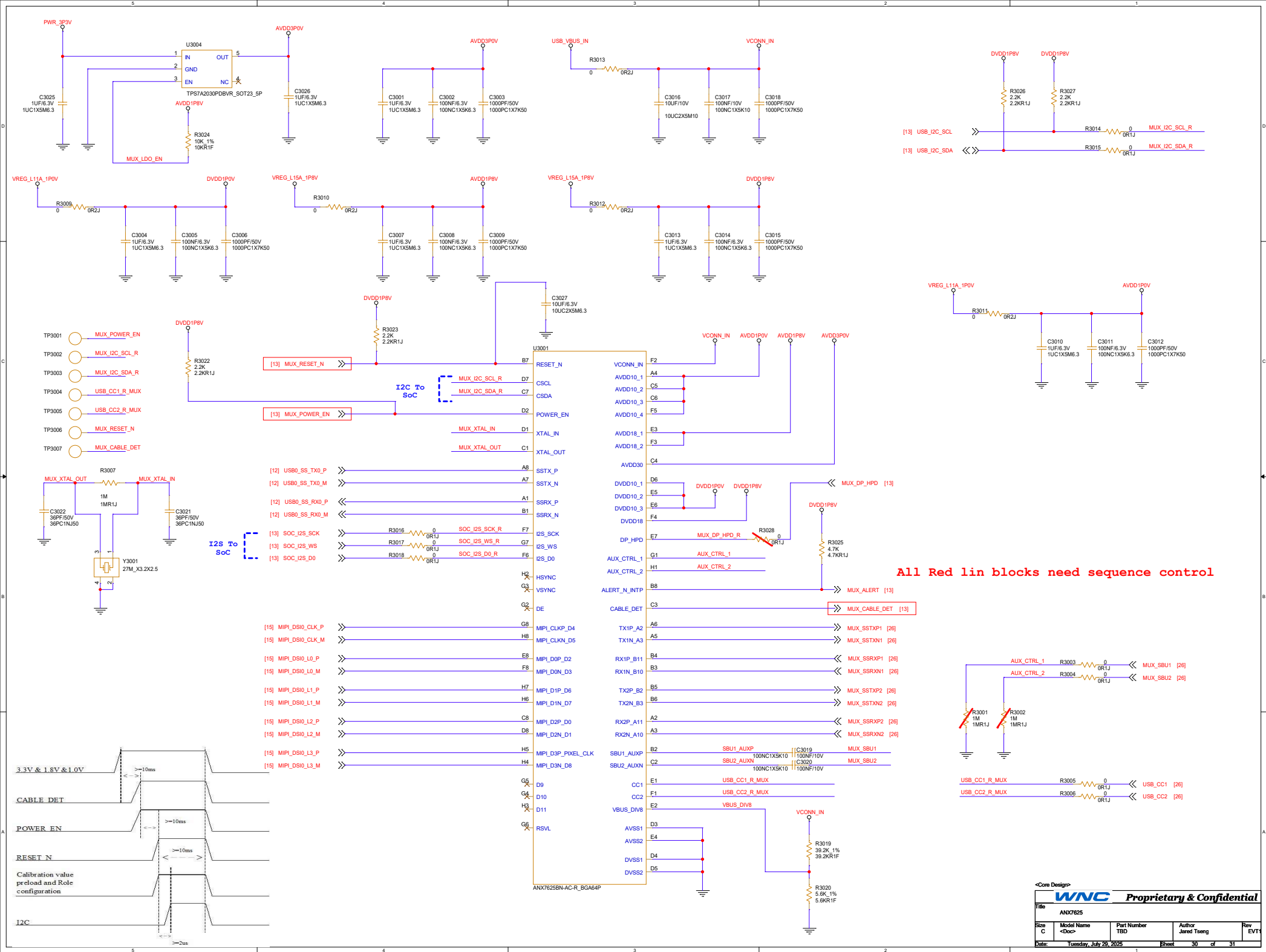
2025/6/16 change to KINGSTON EMMC16G-MW28-GA01



LPDDR4X
SDRAM
portion of
eMCP
Or
Discrete
LPDDR4X
package







Date	Version	Modified by	Change notice
2025/6/30	EVT2	Jared	Imola schematic change list 20250630.xlsx