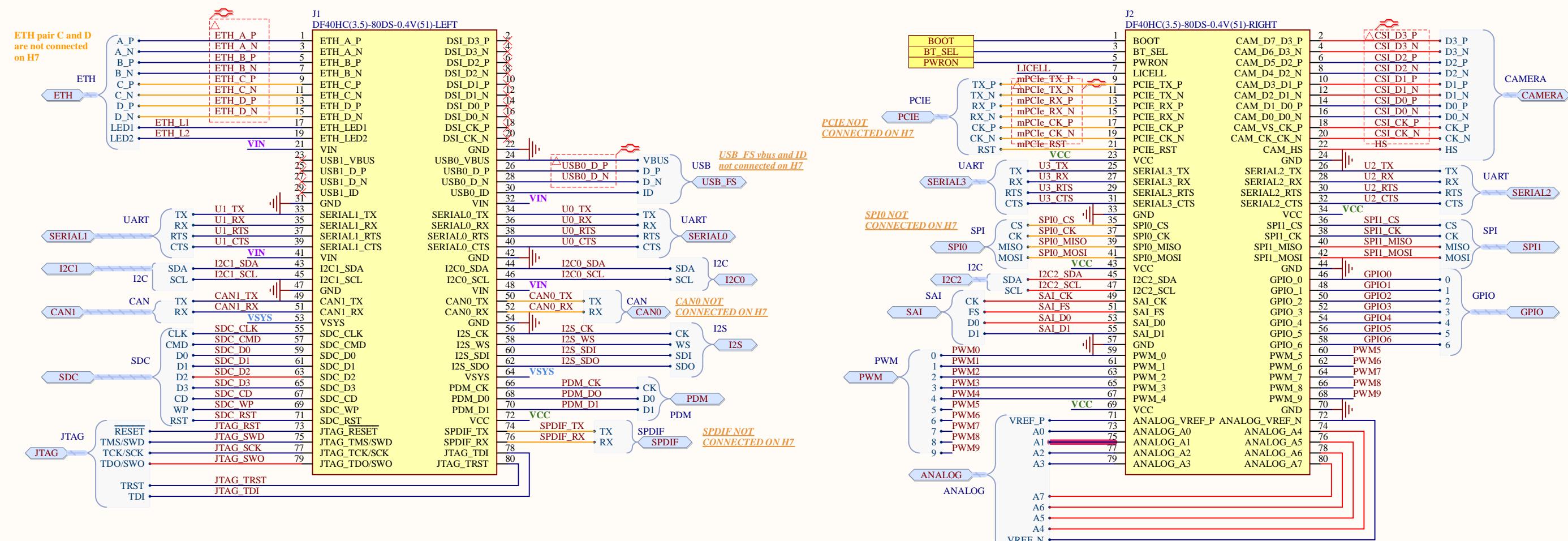
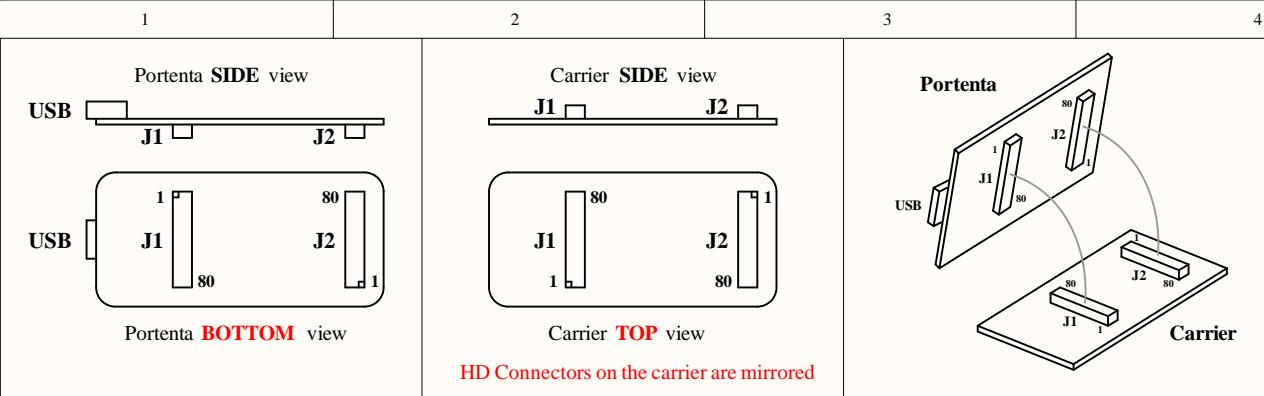


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Title: TOP			
ID: ABX00043	Revision: V3.12		
Date: 05/06/2024	Time: 12:38:09	Sheet 1 of 14	
File: TOP.SchDoc		Author: Arturo Guadalupe	RevAuthor: S. Navaretti





SHARED PINS on H7

POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	VIN	PORTENTA INPUT	4.1V to 6V. Default 3.3V, PMIC (U10) programmable output.
VCC	VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A. Default 3.3V, PMIC (U10) programmable output.
VSYS	VSYS	PORTENTA RESERVED OUTPUT	RESERVED, DO NOT USE 3.5V to 4.2V, max 600mA. Default 4.2V, PMIC (U10) programmable output which is also the input voltage of the bucks inside the PMIC itself.
LICELL	LICELL	PORTENTA INPUT	Coin cell max 3.6V, max 46uA. Max 4uA with PMIC (U10) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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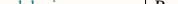
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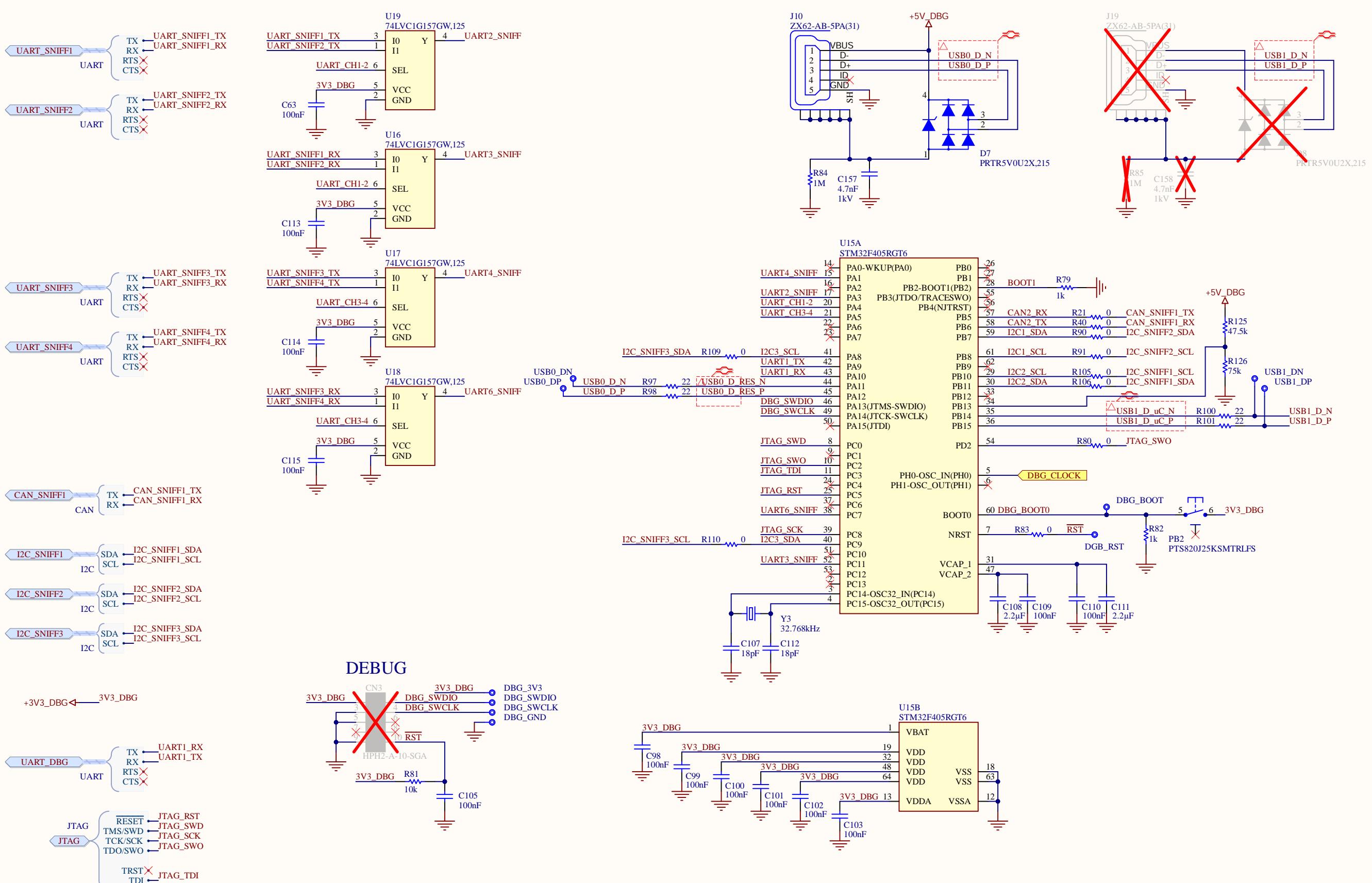
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DEBUG

Title: HD Connectors female
 ID: ABX00043 Revision: V3.12
 Date: 05/06/2024 Time: 12:38:10 Sheet 2 of 14
 File: HDConn_FEMALE_SchDoc Author: ActuaG Cucadellusi
 Rev Author: S. Nevarotti



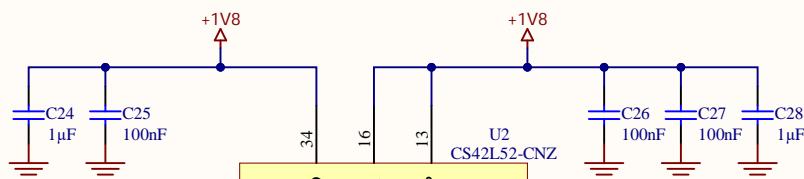



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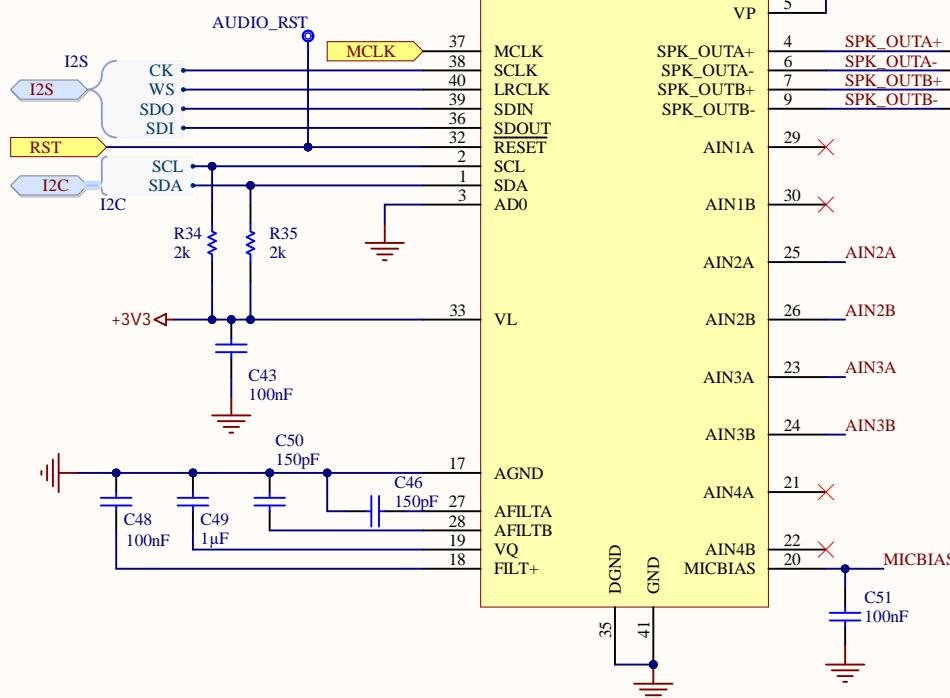
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ID: ABX00043	Revision: V3.12		
Date: 05/06/2024	Time: 12:38:11	Sheet: 3 of 14	
File: DEBUGGER.SchDoc		Author: Arturo Guadalupe	RevAuthor: S. Navaretti



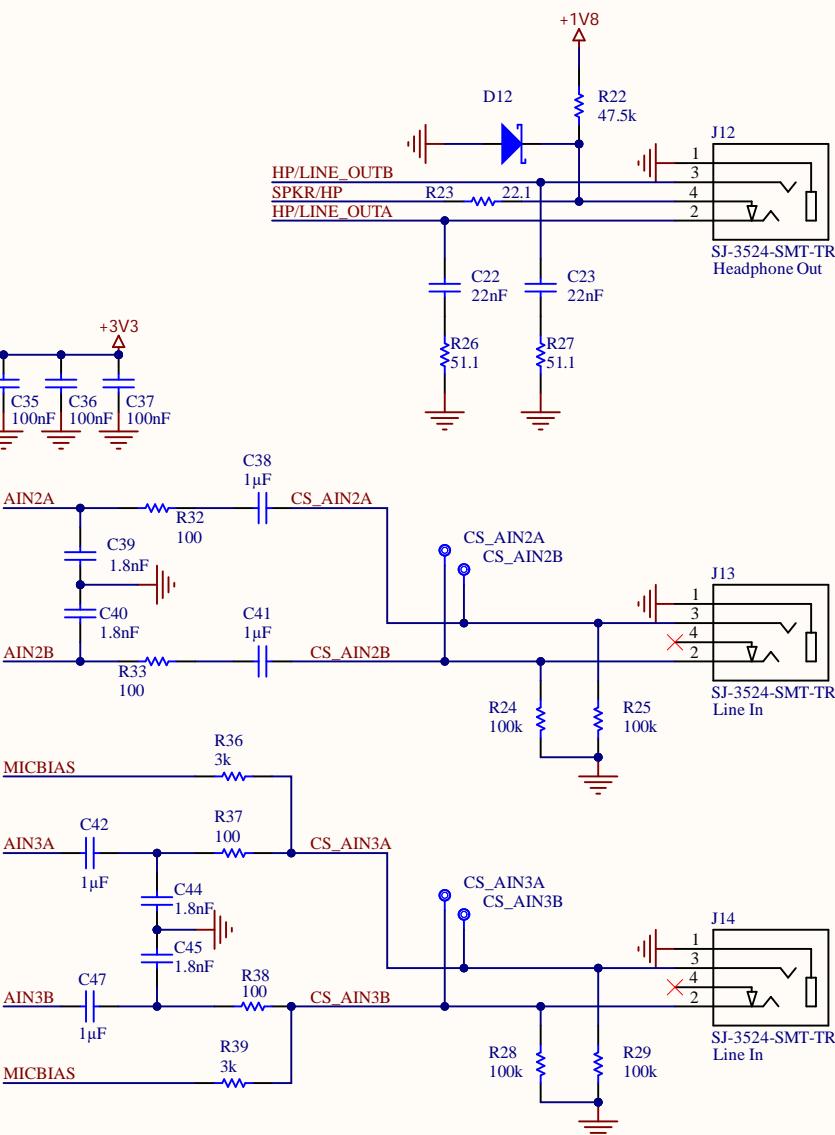
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Title: AUDIO

ID: ABX00043

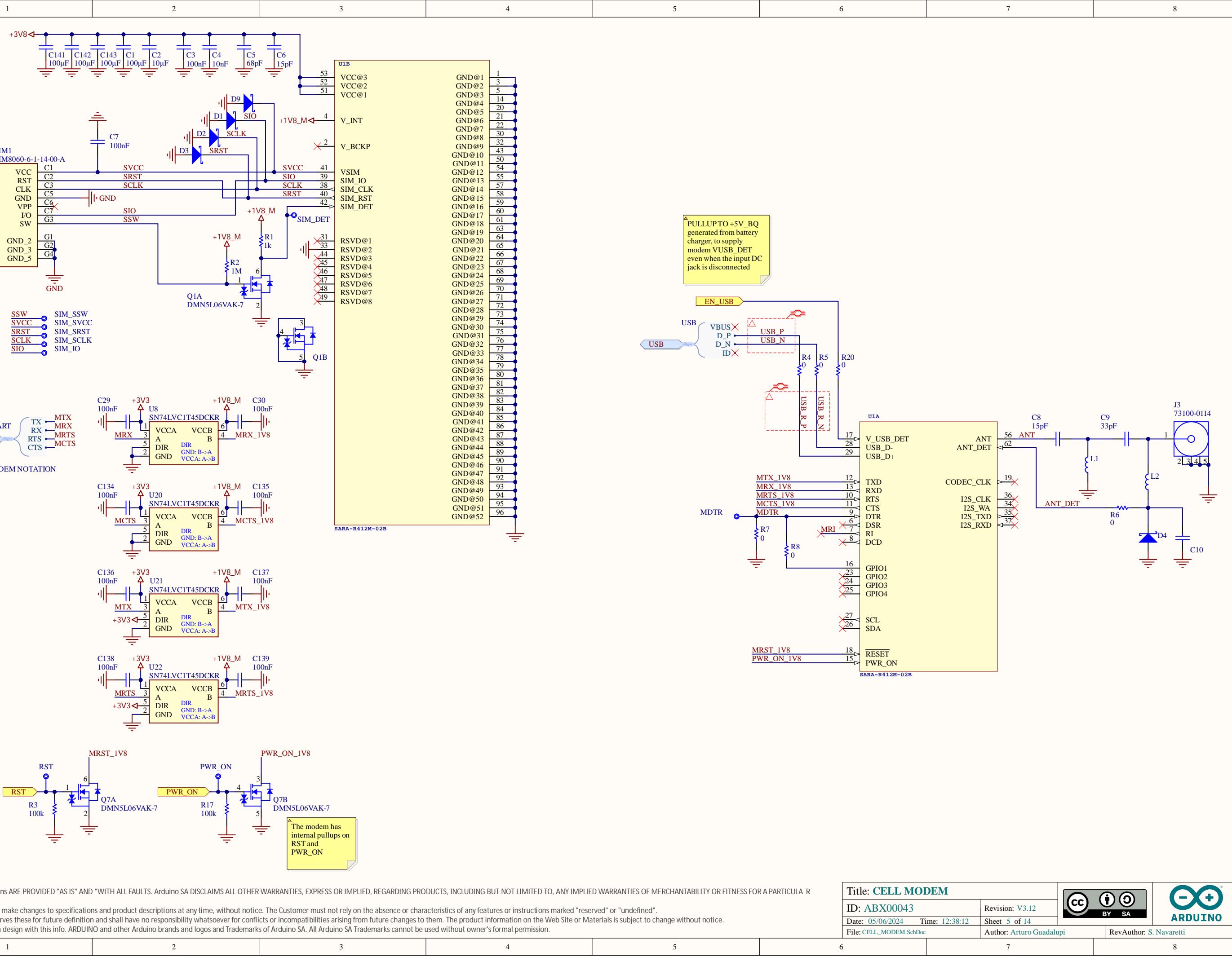
Revision: V3.12

Date: 05/06/2024 Time: 12:38:12

Sheet 4 of 14

File: AUDIO.SchDoc Author: Arturo Guadalupe

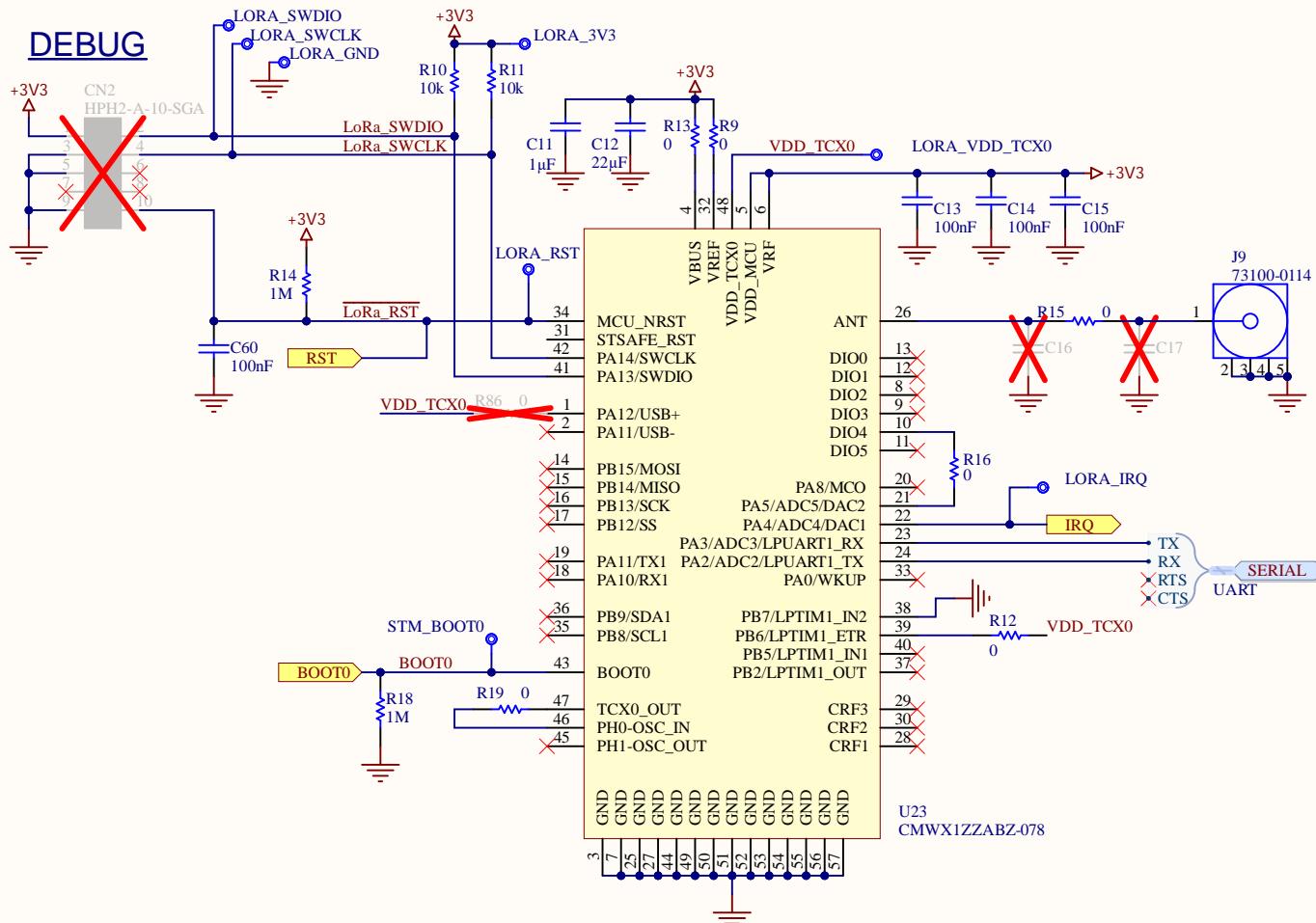




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Title: CELL MODEM	
ID: ABX00043	Revision: V3.12
Date: 05/06/2024	Time: 12:38:12
Sheet: 5 of 14	
File: CELL_MODEM.SchDoc	Author: Arturo Guadalupe
	RevAuthor: S. Navaretti





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Title: LORA

ID: ABX00043

Revision: V3.12

Date: 05/06/2024 Time: 12:38:13

Sheet 6 of 14

File: LORA.SchDoc

Author: Arturo Guadalupi



Top side		Bottom side	
1		2	3.3V
3	Reserved****	4	GND
5	Reserved****	6	1.5V
7	CLKREQ#	8	VCC**
9	GND	10	I/O**
11	REFCLK-	12	CLK**
13	REFCLK+	14	RST**
15	N/C or GND	16	VPP**
Mechanical key			
17	Reserved	18	GND
19	Reserved	20	Reserved***
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	Reserved*	38	USB_D+
39	Reserved*	40	GND
41	Reserved*	42	LED_WWAN#
43	Reserved*	44	LED_WLAN#
45	Reserved*	46	LED_WPAN#
47	Reserved*	48	+1.5V
49	Reserved*	50	GND
51	Reserved*	52	+3.3V

*Reserved for future second PCI Express Lane (if needed). Pin 51 has changed to be W_DISABLE2#

**Reserved for future Subscriber Identity Module (SIM) interface (if needed)

***Reserved for future wireless disable signal (if needed)

****Reserved for future wireless coexistence control interface (if needed)

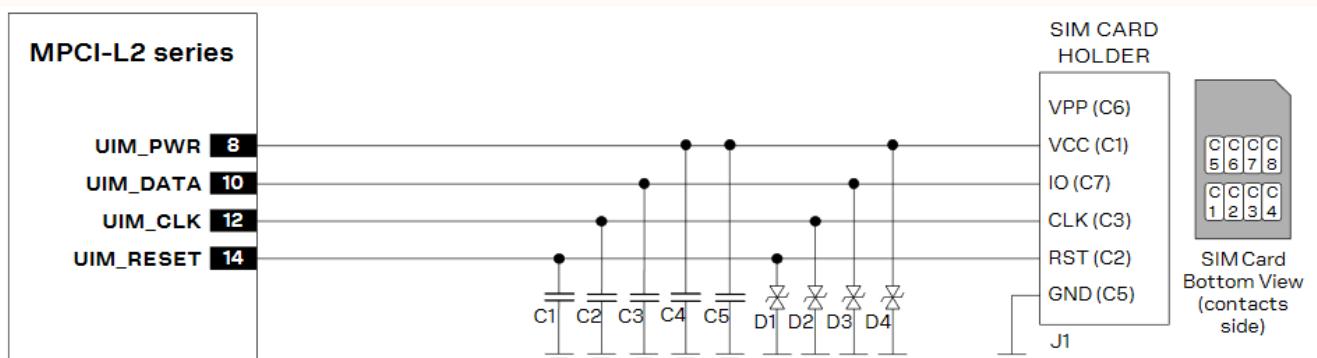
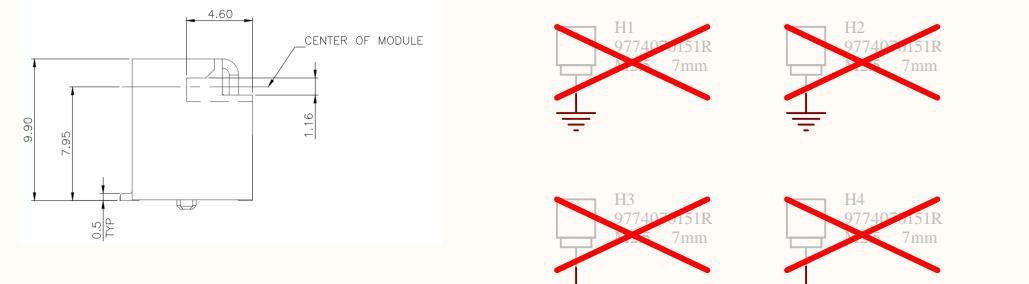
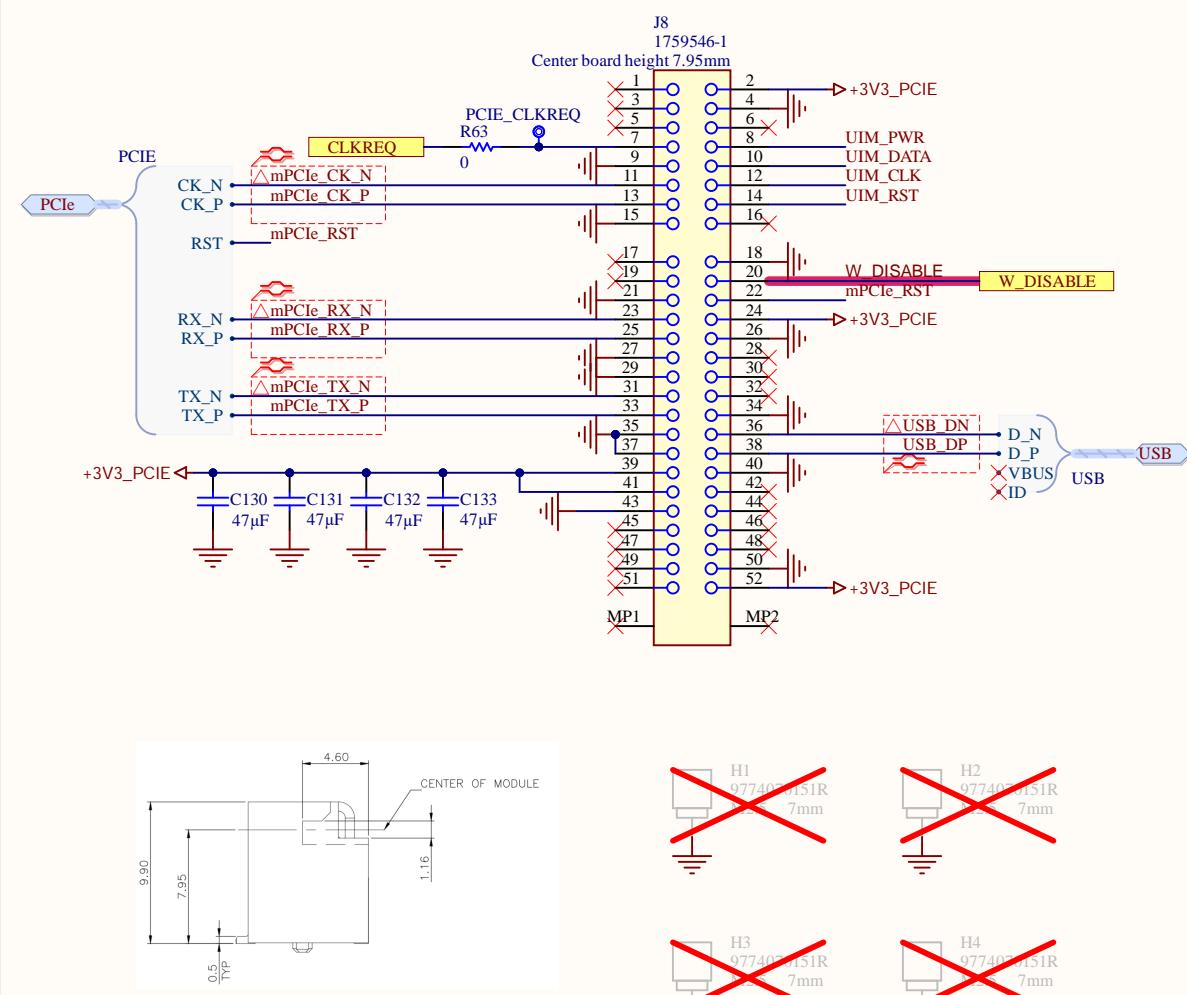
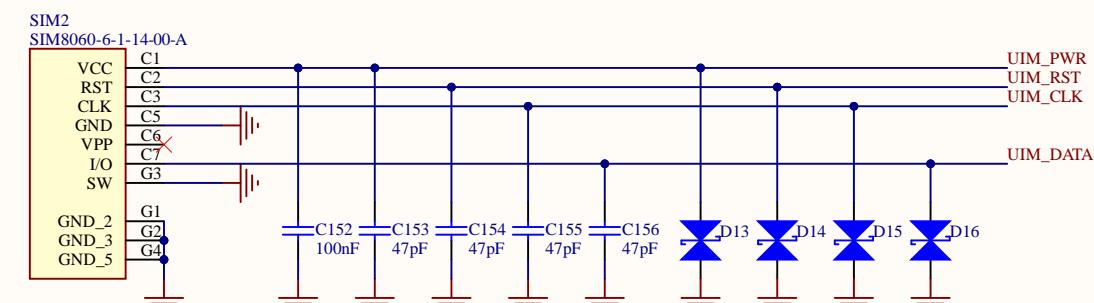
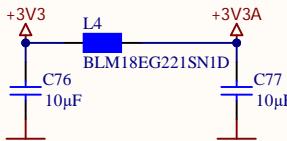
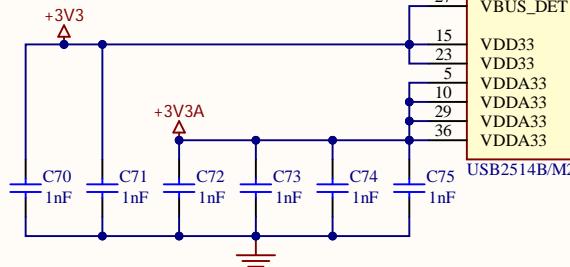
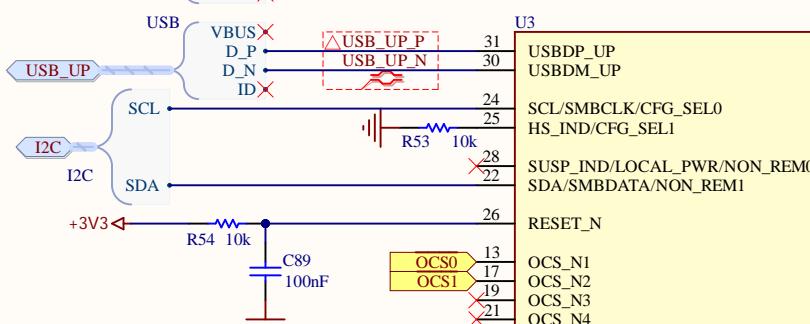
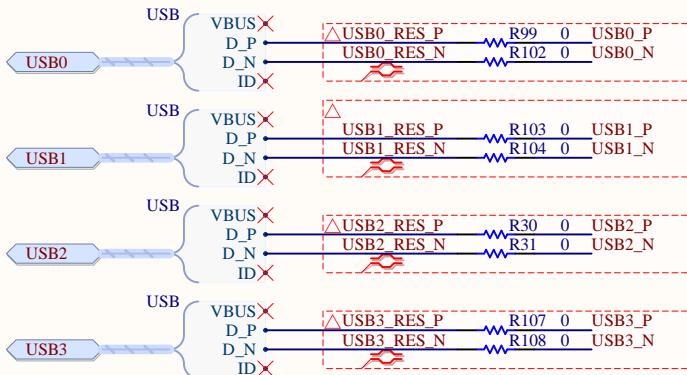


Figure 50: Application circuits for the connection to a single removable SIM card, with SIM detection not implemented



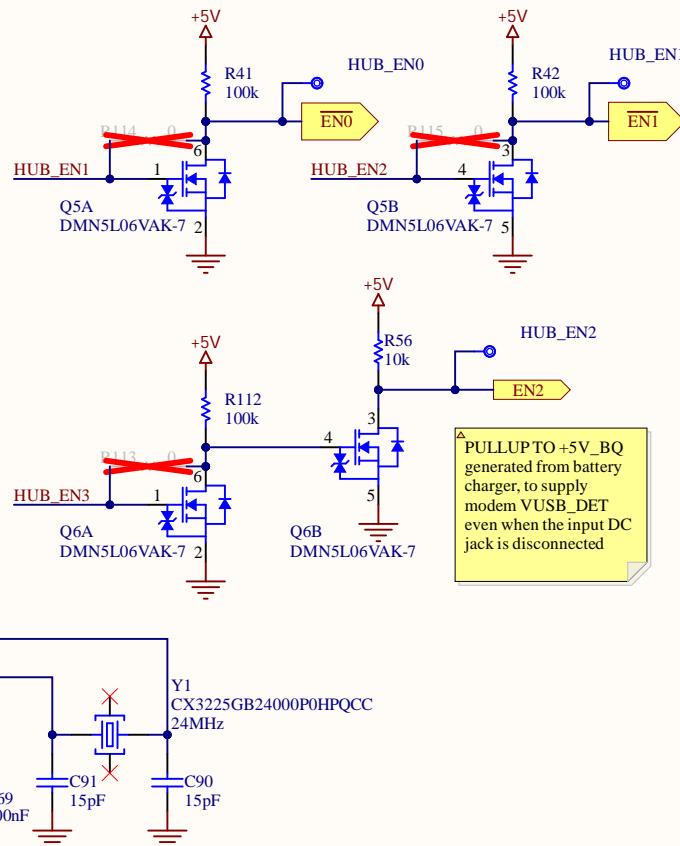


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EN0 and EN1 pullup to 5V due to NCP383 which wants EN pullup to VIN



Title: USB HUB

ID: ABX00043

Revision: V3.12

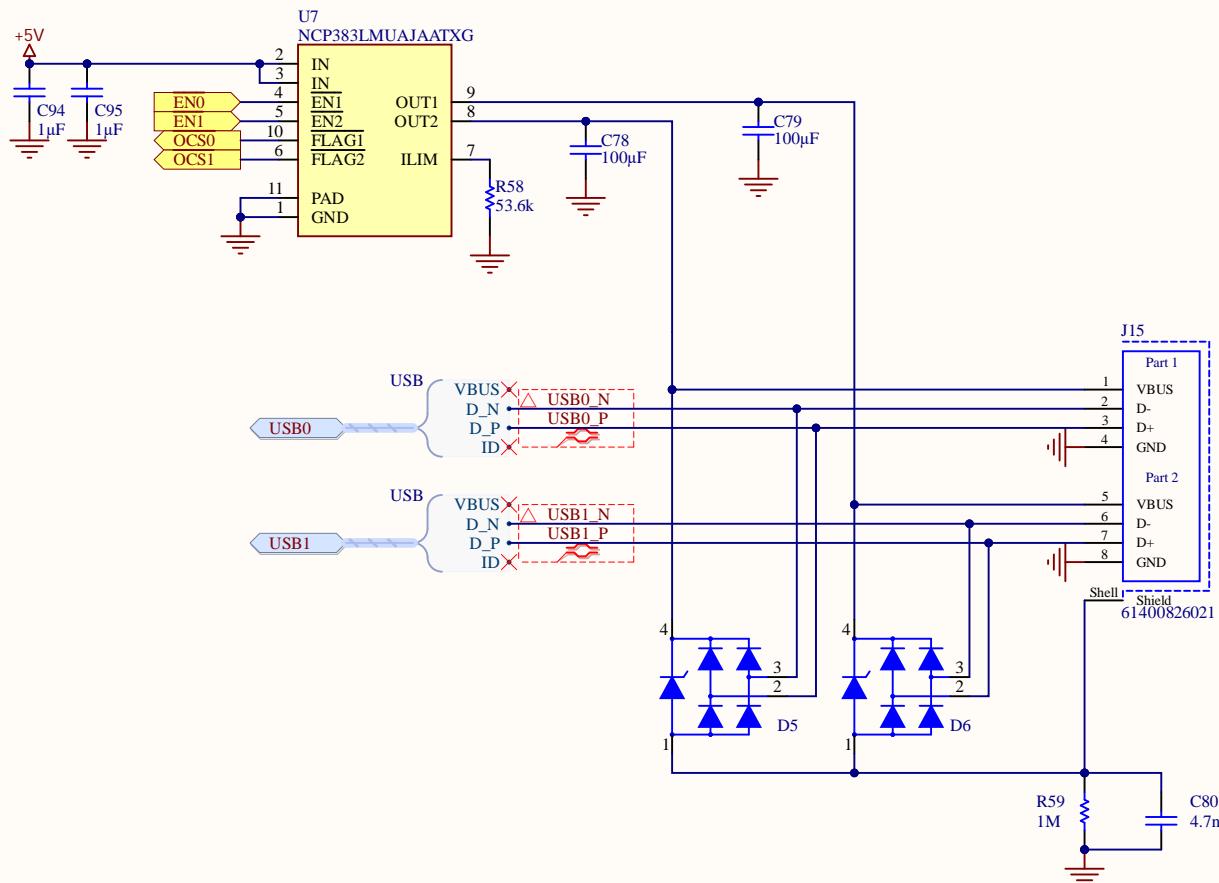
Date: 05/06/2024 Time: 12:38:14

Sheet 8 of 14

File: USB_HUB.SchDoc



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Title: USB CONNECTORS

ID: ABX00043

Revision: V3.12

Date: 05/06/2024 Time: 12:38:15

Sheet 9 of 14

File: USBA_CONNECTORS.SchDoc

Author: Arturo Guadalupi



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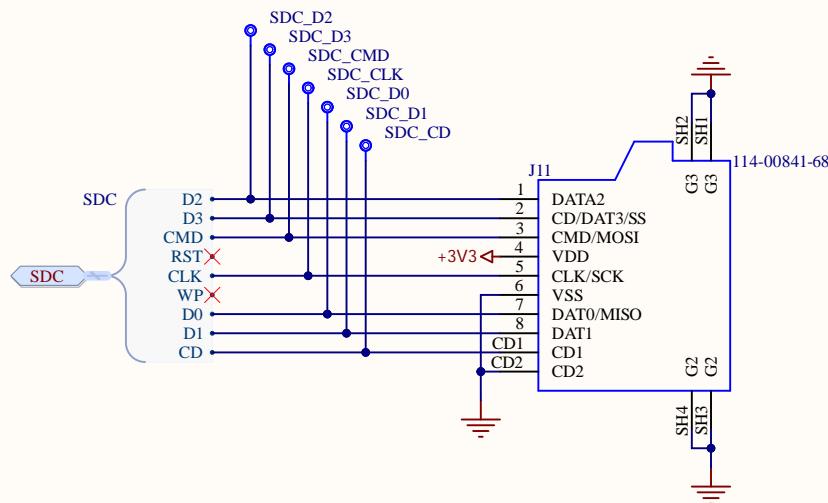
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Title: SD CARD

ID: ABX00043

Revision: V3.12

Date: 05/06/2024 Time: 12:38:16

Sheet 10 of 14

File: SD_CONNECTOR.SchDoc

Author: Arturo Guadalupi



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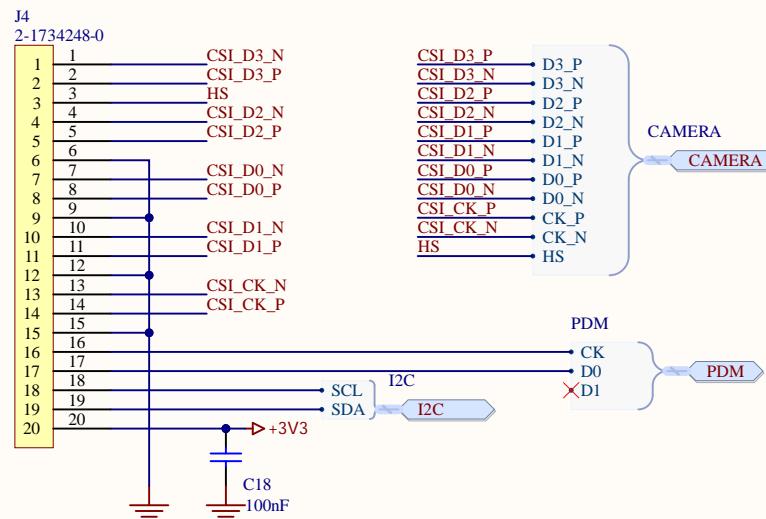
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Title: CAMERA CONNECTOR

ID: ABX00043

Revision: V3.12

Date: 05/06/2024 Time: 12:38:16

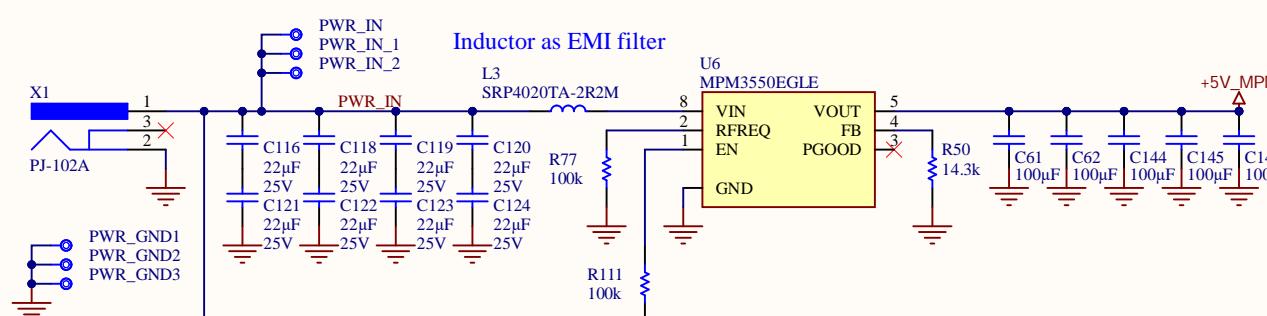
Sheet 11 of 14

File: CAMERA_CONNECTOR.SchDoc

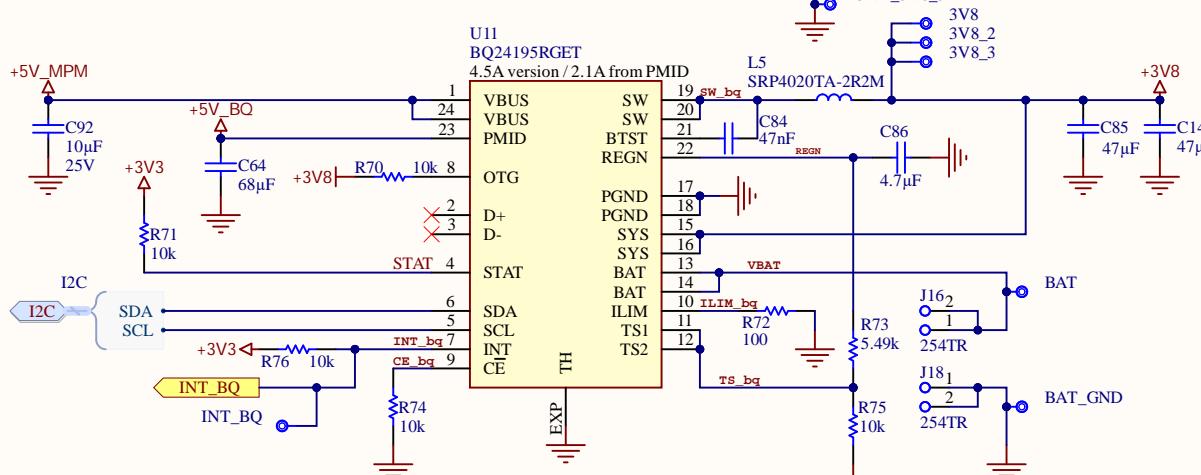
Author: Arturo Guadalupi



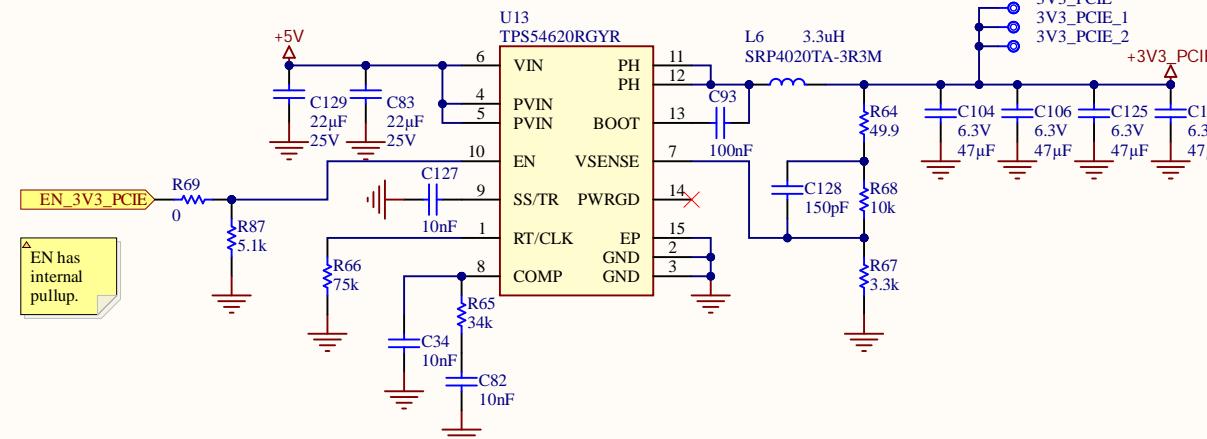
Power in from jack, +5V step down



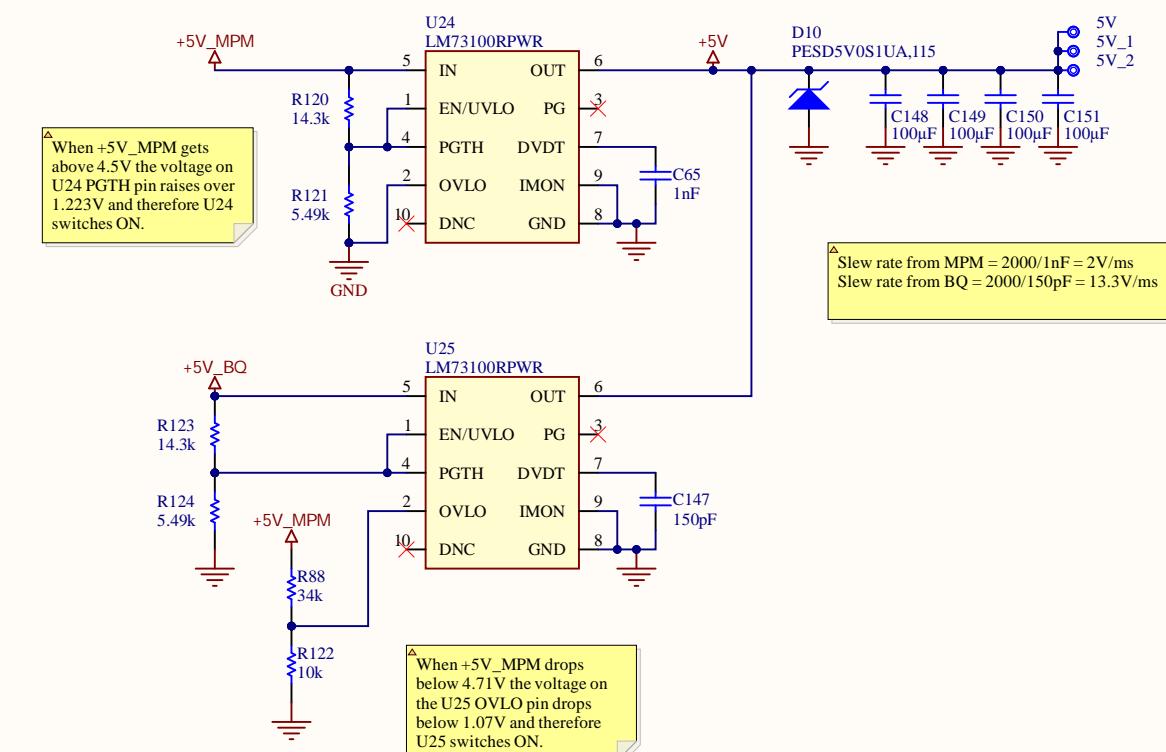
Battery charger and +5V boost from battery



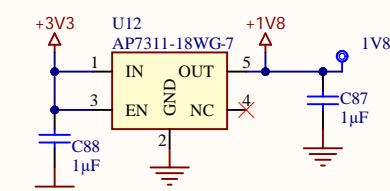
PCIE dedicated high current 3V3



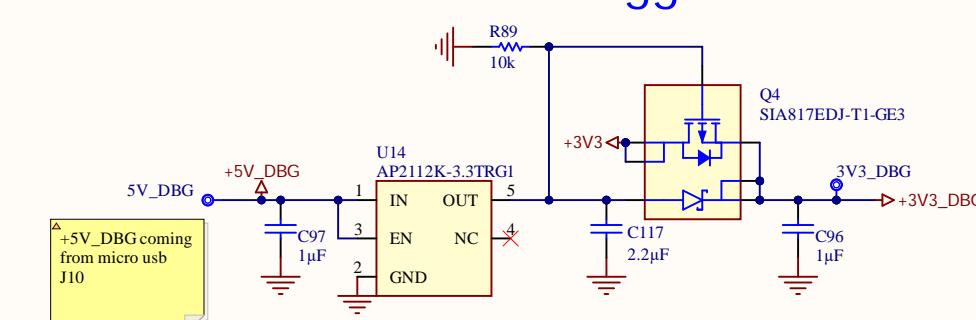
Power OR between +5V from jack or battery boost



Audio 1V8 linear regulator



Dedicated Debugger PWR



PIN DESCRIPTIONS

Pin	Name	RS-232	RS-485 Full Duplex	RS-485 Half Duplex
1				
2	GND		Ground	
3	T1OUT, B/Z	Transmitter 1 Output	Z Driver Neg Output	B/Z Neg Input/Output
4	T2OUT, A/Y	Transmitter 2 Output	Y Driver Pos Output	A/Y Pos Input/Output
5				
6	R1OUT	Receiver 1 Output	X	X
7	R2OUT, RO	Receiver 2 Output	Receiver TTL Output	Receiver TTL Output
8				
9				
10	SHDN		Low power shutdown mode when low	
11	SLEW		Data rate limited to 250kops when low	
12	FD_TX_TERM	X	120Ω X-2 termination enabled when both TERM and FD_TX_TERM are high	X
13	TERM	X	120Ω A-B termination enabled when high	
14	RS-485_RS-232	0	1	1
15	HALF/FULL	X	0	1
16				
17	GND		Ground	
18	R2IN, A	Receiver 2 Input	A Pos Receiver Input	X
19	R1IN, B	Receiver 1 Input	B Neg Receiver Input	X
20	RE	X	Receiver enabled when low	
21	T2IN, DE	Transmitter 2 Input	Driver enabled when high	
22	T1IN, DI	Transmitter 1 Input	Driver TTL Input	
23				
24	V-		Charge pump negative supply, 0.1μF from ground	
25	C2-		Charge pump cap 2 negative lead	
26	C2+		Charge pump cap 2 positive lead, 0.1μF	
27	V+		Charge pump cap 1 positive lead, 0.1μF	
28	C1+		Charge pump cap 1 positive lead, 0.1μF	
29	VL		Logic Supply for TTL Inputs and Outputs, $V_L = +1.65V$ to $+5.5V$, bypass to ground with 1.0μF	
30	VCC		Main Supply, $V_{CC} = +3.0V$ to $+5.5V$, bypass to ground with 1.0μF	
31	C1-			
32	C1-		Charge pump cap 1 negative lead	

TABLE 3: RS-485/422 TX TRUTH TABLE

INPUTS			OUTPUTS		
SHDN	RS-485_RS-232	DE/T2IN	D/I/T1IN	Z/B/T1OUT	Y/A/T2OUT
0	X	X	X	1/8th unit load	1/8th unit load
1	1	0	X	1/8th unit load	1/8th unit load
1	1	1	1	0	1
1	1	1	1	0	1
X	0	X	X	X	RS-232 Mode

TABLE 4: RS-485/422 RX TRUTH TABLE

INPUTS			OUTPUT	
RS-485_RS-232	SHDN	HALF/FULL	RE	(A-B)
1	0	X	X	X
1	1	0	0	$\geq -50mV$
1	1	0	0	$\leq -200mV$
1	1	0	0	Floating
1	1	1	0	X
1	1	1	0	$\geq -50mV$
1	1	1	0	$\leq -200mV$
1	1	1	0	Floating
0	X	X	X	X

TABLE 5: RS-485/422 TERMINATION TRUTH TABLE

FD_TX_TERM	TERM	RS-485_RS-232	HALF/FULL	TX TERM	RX TERM
Pin 12	Pin 13	Pin 14	Pin 15	Pins 3-4	Pins 18-19
X	0	1	0	-	-
0	1	1	0	-	ON
1	1	1	0	ON	ON
X	0	1	1	-	-
X	1	1	1	ON	-
X	X	0	X	-	-

The DE and RE pins have no effect on the termination setting in any mode.



RJ45 CAN Bus PinOut

RJ45 Pin #	RJ10 Pin #	Signal name	Signal Description
1	2	CAN_H	Dominant High
2	3	CAN_L	Dominant Low
3	4	CAN_GND	Ground
4	-	Reserved	Upgrade Path
5	-	Reserved	Upgrade Path
6	-	CAN_SHLD	CAN Shield, Optional
7	-	CAN_GND	Ground
8	1	CAN_V+	Power, Optional

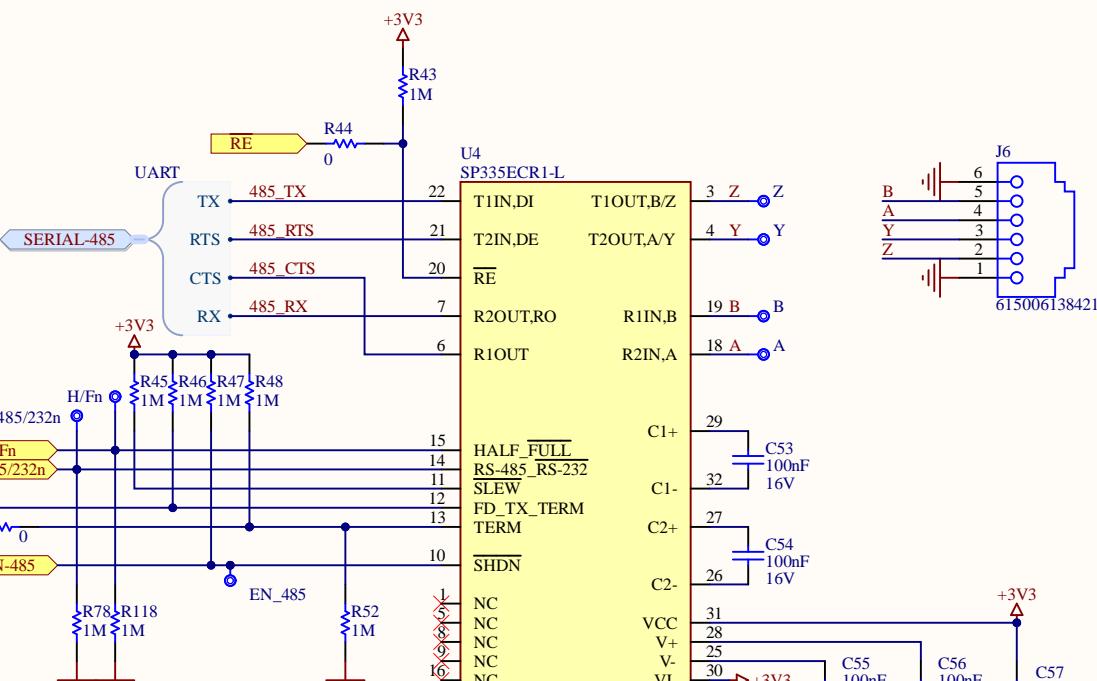
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TABLE 1: RS-232 TX TRUTH TABLE			
INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	D/I/T1IN, DE/T2IN	Z/B/T1OUT, Y/A/T2OUT
0	X	X	X
1	0	0	0
1	1	0	1
1	1	1	X

TABLE 2: RS-232 RX TRUTH TABLE			
INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	B/I/R1IN, A/R2IN	R1OUT, R2/R2OUT
X	0	0	0
X	1	0	1
X	1	0	Inputs open
X	1	1	X



The full duplex driver termination is enabled only when both TERM and FD_TX_TERM are high.

Title: FIELDBUS

ID: ABX00043

Revision: V3.12

Date: 05/06/2024 Time: 12:38:18

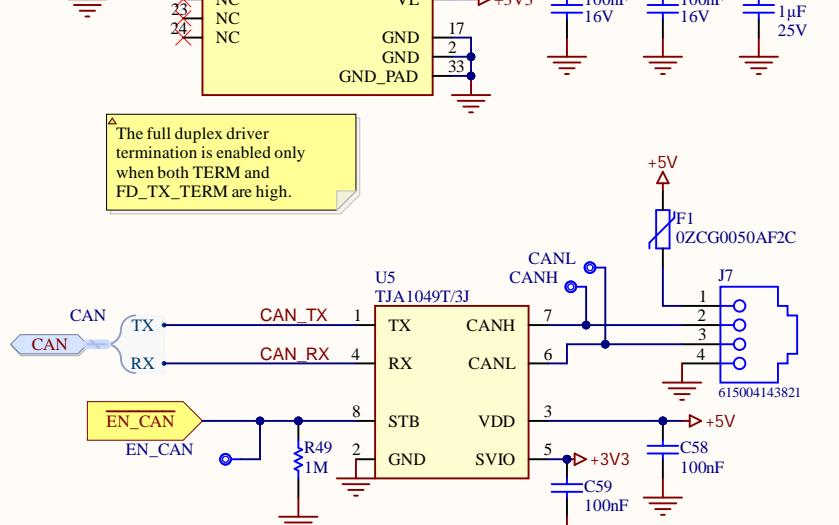
Sheet 13 of 14

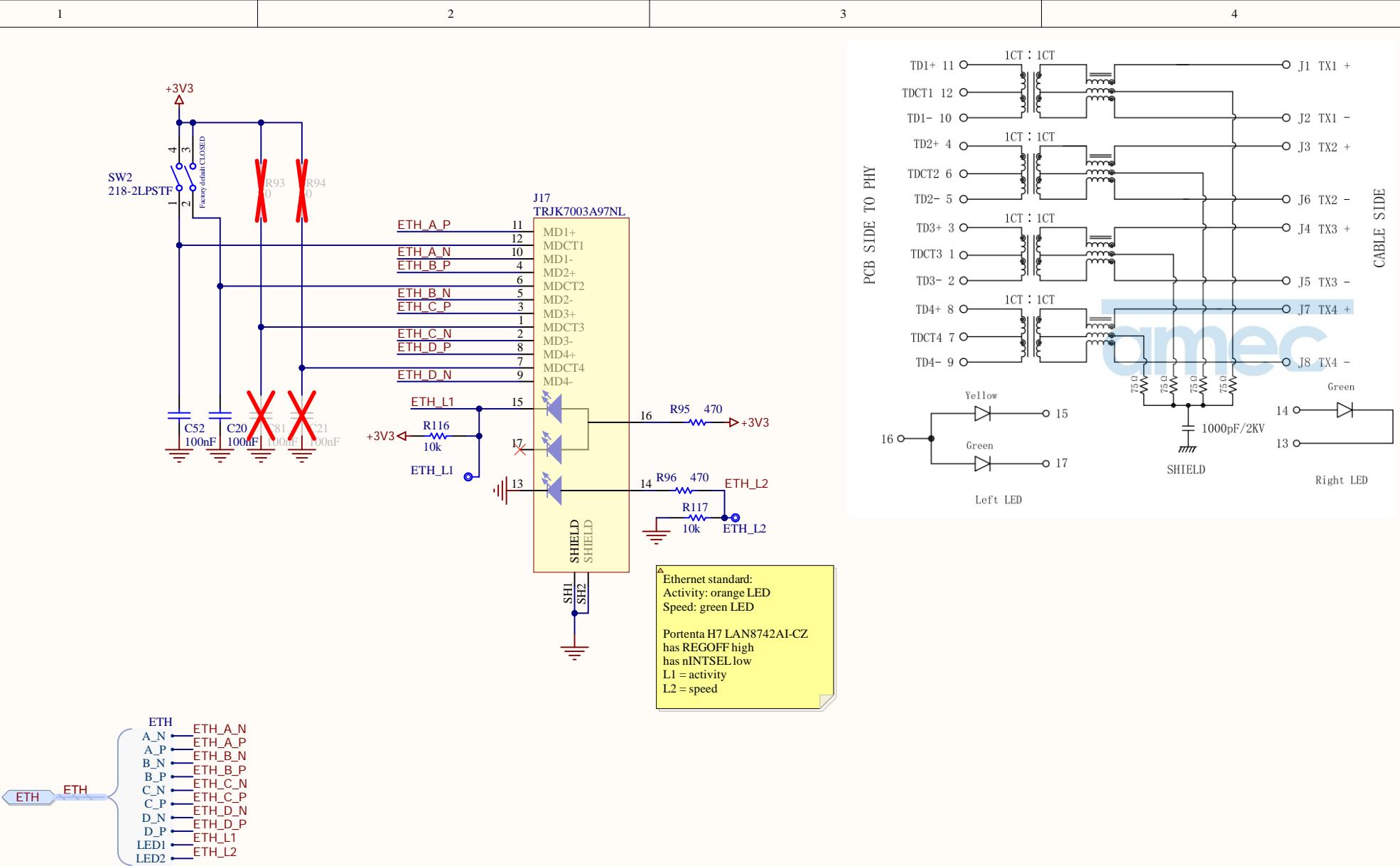
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Author: Arturo Guadalupe

RevAuthor: S. Navaretti





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Title: ETHERNET

ID: ABX00043

Revision: V3.12

Date: 05/06/2024 Time: 12:38:19

Sheet 14 of 14

File: ETH_CONNECTOR.SchDoc

Author: Arturo Guadalupi



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