Design Report

Design

https://app.lucidchart.com/invitations/accept/3aaaeda-cd08-49e1-9268-3f851624c7a3

2 op -> 5 op , 3 Rsrc1 , 3 Rsrc2 , 3 Rdst , 16 immediate
Mem -> 5 op , 3 Rdst , 20 EA or imm , 1 EA or imm
BR -> 5 op , 3 Rdst

IR Format (32 Bits)

2 bits Differentiation code	

One Operand instructions
IR Format (one op) → 16 bits

NOP	00000
NOT Rdst	00001
INC Rdst	00010
DEC Rdst	00011
OUT Rdst	00100
IN Rdst	00101

For the following instructions

1- NOP,NOT , INC and DEC

5 OP Code 31 30 29 28 27	3 Rsrc1 26 25 24	3 X 23 22 21	3 Rdst 20 19 18	2X Doses not to be fetched

2- IN

5 OP Code 31 30 29 28 27	3 X 26 25 24	3 X 23 22 21	3 Rdst 20 19 18	2X Doses not to be fetched

3- OUT

5 OP Code 31 30 29 28 27	3 Rdst 26 25 24	3 X 23 22 21	3 X 20 19 18	2X Doses not to be fetched

Two Operand instructions

IR Format (2 OP) → 32 bits

SWAP	01000
ADD	01001
IADD	01010
SUB	01011
AND	01100
OR	01101
SHL	01110
SHR	01111

AND,OR,SUB,ADD (16 bits)

5 OP Code 31 30 29 28 27	3 Rsrc1 26 25 24	3 Rsrc2 23 22 21	3 Rdst 20 19 18	2 x

SWAP INSTRUCTION(16 bits)

5 OP Code 31 30 29 28 27	3 Rsrc1 26 25 24	3X	3 Rdst 20 19 18	2 X 1 0

LADD(32 bits)

5 OP Code 31 30 29 28 27	3 Rsrc1 26 25 24	3X	3 Rdst 20 19 18	16 immediate value 17 16 15 14 .. 2	2 X 1 0

SHL,SHR INSTRUCTIONS (Rsrc1 and Rdst are the same)(32 bits)

5 OP Code 31 30 29 28 27	3 Rsrc1 26 25 24	3X	3 Rdst 20 19 18	16 immediate value 17 16 15 14 .. 2	2 X 1 0

Memory instructions

IR Format (Mem) →32 bits

PUSH	10000
POP	10001
LDM Rdst, Imm	10010
LDD Rdst, EA	10011
STD Rsrc, EAt	10100

Push(16 bits)

5 OP Code	3 X	3 Rdst	5x

POP(16 bits)

5 OP Code	6 X	3 Rdst	2x

LDM(32 bits)

5 OP Code 31 30 29 28 27	3 X 26 25 24	3 Rdst 23 22 21	3 x 20 19 18	16 imm 17 .. 2	2 X 1 0

LDD(32)

5 OP Code 31 30 29 28 27	3 X 26 25 24	3 Rdst 23 22 21	20 EA 20 .. 1	1 x 0

STD(32)

5 OP Code 31 30 29 28 27	3 X 26 25 24	3 Rsrc2 23 22 21	20 EA 20 .. 1	1 x 0

Branch

IR Format (BR) → 16 bits

5 OP Code	3 Rdst	8 X

JZ	11000
JMP	11001
CALL	11010
RET	11011
RTI	11100

PIPELINE BUFFERS

IF/ID 32	ID/EX	EX/M	M/WB
IR (32)			
PC (32)	PC/Rdst data (32)	PC/Rdst data (32)	PC/Rdst data (32)
	Control signals (32)	Control signals(32)	Control signals(32)
	Rdst,Rsrc address(6)	Rdst,Rsrc address(6)	Rdst,Rsrc address(6)
		ALU Result(32)	
	Read Data1(32)		
	Read Data2(32)	Read Data2(32)	
	Sign Extended data (32)		

MUX	INPUTS	SELECTORS	OUTPUT
1	1-Correct branch address 2-ADDRESS 2 3-MUX 8 OUTPUT 4-READ DATA 1 5-Predicted branch addr 6-PC 7-PC+2	1-MISS PREDICTED 2-INT FSM 3-FUNCTION 4-BRANCH 5-BRANCH PREDICTION 6-STALLING 7- if all are 0`s	Same as input
2	1- IR : 22->20 2- Ir : 20->18	Reg dst	Write address 1
3	1-Sign extend o/p 2-Zero extend o/p	EA/IMM SIG	Immediate Value at ALU I/P
4	1- Rsrc Data 2 2- immediate value 3- forwarding date from alu buffer 4- forwarding date from mem buffer 5- Inport	1- ALU src 2- IN 3- forwarding unit output	ALU input 2
5	1-Rsrc Data 1 2-forwarding date from alu buffer 3- forwarding date from memory buffer	Forwarding Unit Signal (2 bits)	ALUinput 1
6	1-sp 2-sp+2	1-not(INT) or (increment or decrement sp signal)	1-sp 2-sp+2
7	1- Mux 6 2- ALU result	1- SP signal Oring int	Memory address
8	1-PC+1 2-Read Data 2 3-PC	1-INT 2-CALL	00->Read Data2 01->PC+1 10,11->PC
9	1- decrementor 2-SP	1- (increment or decrement sp) Oring (not int)	Input to tri state 1
10	1-ALU RESULT 2-MEM RESULT	1- MEM to register	0->ALU 1->MEM

Block Name	Description	Inputs	Outputs
Hazard Detections Unit	**Detects when Load use case happens And stalls pc , IF/ID and resets ID/EX if it detects hazard and if it was memory operation**	**1-Rsrc1 2-Rsrc2 3-Rdst(Prev instruction) (Ex MEM) 4-Memory operation**	**1- PC STALLING 2-IF/ID Stalling 3-reset ID/EX**
INT FSM	**INT signal as input To interrupt the system**	**INT SIGNAL**	**1-ADDRESS 2 load to PC 2-Fetch _ Finished SIG Load M[2],M[3] to PC**
RESET FSM	**Reset signal as input To reset the system**	**RESET SIGNAL**	**1-Reset PC (load=0) 2-Fetch _ Finished SIG Load M[0],M[1] to PC**
Control Branching	**Responsible for predicting branching address (taken or not)**	**1-BRANCH REGISTER FORWARDING 2-BRANCH REGISTER NO FORWARDING 3-OP CODE 4-**	**1-selector for branching 2-predicted branch address 3-predict bit**

Forwarding Unit	**-If the signal of memToReg is enable in alu buffer And Rdis in alu buffer is the same Rsrc1 or Rsrc2 The output will be 10** **-if the signal or memToReg is enable in mem buffer And Rdis in mem buffer is the same Rsrc1 or Rsrc2 The output will be 01**	**1-memToReg signal for buffer alu and mem** **2-Rdis from buffer alu and mem** **3-ALU RESULT**	**2-bits Selector for mux4 and mux5**
Miss Prediction Unit	**-Checks if I did the branch prediction right or wrong** **-If prediction was wrong I should send correct PC (Rdst or PC) to MUX1 and flush ID/EX and IF/ID** **-It should Update the state of branch predictor each time there was Jump zero instruction**	**1- Zero flag** **2- Branch prediction** **3-Rdst , PC , OPCODE**	**1-Wrong prediction** **2-Update DYNAMIC BRANCH FSM** **3-Correct PC** **4-FLUSH**

Fetching Unit	**Detecting the instructions contains 32 bits or 16 bits** **If contains 32 bits it fetching twice or RST/INT signals.** **Else it fetches once.**	**IR of instruction memory and Oring(fetch_again,O/P FSM_RST , O/P FSM_INT)**	**To IF/ID**

- Dynamic Branch Prediction Unit FSM