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Dayananda Sagar College of Engineering
Department of Electronics & Communication Engg.
Continuous Internal Evaluation – III

Cou	rse N	ame: EMBEDDED SYSTEM DESIGN and IOT APPLICATIONS	Date:		07 /202: day Webet		
Course Code: 19EC6DCEAI Day:							
		: 6 th A, B, C and D	Timings:	1-2.30 PM 1½ Hrs.			
	Max Marks: 50 M Duration:						
No.		Question Description		Mks	CO & Levels		
QI	(a)	The term 'Internet of Things' was coined by i) Bill gates ii) Kevin Ashton iii)McDonald iv) Steve jobs		1			
	(b)	ing other	1				
	(c)	i) IoT-A ii) IoT-RM iii) IoT-CM iv) IoT-RA The model(s) involved in the IoT Reference model is/are. i) communication ii) domain iii) information iv)all		1			
	(d)	(d) The RA of IoT-A mainly consists of					
	(e)	i) perspectives ii) views iii) both(i) and(ii) iv) none ISO/IEC/IEEE 42010:2011: "Systems and Software Engineering Ard Description." is the basis of i) IEEE P2413 ii) IEEE P2143 iii) IEEE P2341 iv) IEEE P2213	chitecture	ı			
	(f) In the CISCO Reference Model, the levels are considered operational technology (OT).						
	(g)	The most common and widely implemented RFID naming standards the NAC ID WSN		1			
	(h)	An IoT development platform is a small single electron board with limited memory and processing power that can be used interactive electronic objects. i) software ii) hardware iii) firmware iv) middleware	ic circuit to create	ı			
	(i)	Hardware platforms for IoT can be programmed via i) webIDE iii) both iv) none.		1			
	(j)	are usually used for IoT prototyping, for educational purposes use as embedded computer controllers.	s, and for	1			
		i) SBCs ii) SoCs iii) USB iv) HDMl Describe briefly the RM proposed by IoT-A and its perspectives and views.		10	CO4,L2		
3		List and explain IOT hardware development platforms and its application	ons.	10	CO5,L2		
14		Briefly discuss the six layers of RILA.		10	CO4,L2		
-		OR					
5		Discuss in brief any three issues in organizational integration of IoT systems.		10	CO4,L2		
6		Elaborate briefly on the Connectivity and I/O interfaces of IOT hardware platf the past, present and future.	orms in	10	CO5,L2		
-		OR					
)7		Summarize any five specifications of the Current Microcontroller Boards.		10	CO5,L2		



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(Accredited by National Assessment & Accreditation Council (NAAC) with 'A' grade)



-		Embedded Systems and IoT Applications	Max Marks: 50 M.				
	test: 06-07-2022	Embedded Systems and for Approximation	Sub Mentor: SP				
	Vednesday		Sub Mentor Sign:				
	n: ECE	19EC6DCEAI	Staff i/c of sec:				
Semest	ter:6	192002	SP,SMR,MRK,NYM				
	1,0,0	Internal Test	Staffs i/c sign:				
	n : A,B,C,D	III	HOD Name: Dr. TCM				
	gs: 2:00 PM TO 3:30 PM	Test Solutions	HOD's sign :	ath			
Test D	Ouration: 1½ Hrs.			Marks			
Q.	Te	est question paper solutions with steps	2010	Allocatio			
No			7.00	11			
·			Dr. J. & T.	1x10=10			
1	ii) Kevin Ashton		OK. B.				
	i) IoT-A	200	OFF				
	*	College	Gia				
-	iv)all iii) both i) and ii)		1831				
d.	i) IEEE P2413	146.45.45.45.45.45.45.45.45.45.45.45.45.45.	[]				
e.	iii) lower three		GC				
f.	iii) EPC	VOZ O	- July				
g.	ii) hardware	137					
h.	iii) both	VAVO X	BANGA				
1.	i) SBCs						
j.	,			2.2.5			
2	The RM, presented in Figure	1.1, provides a common understanding of the lo	f domain by mod-	3+2+5 = 10M			
2		onships. Similar to the Open Systems Interconnectify the technical particularities of an IoT systems.		101/1			
	the for Rivery index	•					
		IoT reference model					
	Communication	Domain model	ormation model				
	model (behavior)	(top-level) (kn	owledge)				
	High-level	Main concepts, entitles, Specify d	ata semantics				
	communication paradigms pertinent to		omain model				
	the IoT domain						
		Discourse/general concerns (abstract quality concepts)					
		Heterogeneity Interoperability					
		Scalability Manageability					
		Security and privacy Reliability					
	named at 1934 and and builted	-A. (Adapted from Bassi, A., et al., Enabling Things to	Talk: Designing IoT				
	FIGURE 1.1 RM proposed by Iol Solutions with the IoT Architecture	al Reference Model, Springer, Berlin, 2013, 163–211.)	20				
			E' 214				
			Fig – 3M				
	Perspection	ves Views					
	Evolution and interoperability Functional						
	Performance and scalability Information						
	Trust, security, as	nd privacy Deploymen	nt and				
	Availability and	operation					
	EICLIBE 12 Parametrison and	views of IoT-A. (Adapted from Bassi, A., et al., En	abling Things to Talk:				
	Designing IoT Solutions with the	IoT Architectural Reference Model, Springer, Berlin	, 2013, 163–211.)				
			Fig - 2M				

The domain model considers a top-level description of the concepts and entities (physical entities. devices, resources, and services) that represent particular aspects of the IoT domain, and defines their relations. Therefore, the domain model can also be used as a taxonomy of the IoT. The information model specifies the data semantics of the domain model; that is, it refers to the knowledge and behavior of the entities considered in the domain model, since they are responsible for either keeping track of certain information or performing specific tasks (it describes which type of information the entities are responsible for). The communication model, in turn, addresses the main communication paradigms necessary for connecting entities, ensuring interoperability between heterogeneous networks. The proposed communication model is structured in a seven-layer stack and describes how communication has to be managed, by each layer, in order to achieve the interoperability features required in the IoT. It also describes the actors (communicating elements) and the channel model for communication in IoT. The RA of IoT-A mainly consists of "views" and "perspectives," which vary depending on the requirements of each specific application. Figure 1.2 illustrates that the perspectives "evolution and interoperability," "performance and scalability," "trust, security, and privacy," and "availability and resilience" are applied to all the views: the "functional" view, the "information" view, and the "deployment and operation" view, respectively. While applying perspectives to views, not every view is impacted by the perspectives in the same manner or grade. For example, the perspectives have a high impact when applied to the operation Explanation – 5M IOT hardware development platforms and its applications....10M 3 6+4 = 10M -Microcontroller based -System on chip -Single board Computers Eg:Arduino Beagle boards Rasberry Pi ----with detailed Explanation......6M Applications: Zigbee WIFIExplanation-----4M RILA consists of six layers, as depicted in Figure 1.6. Besides these layers, there are two cross 4 section layers, "security" and "management," that affect all other layers. 6+4 = The device integration layer includes all the different types of devices, receives their measure-10M ments, and communicates actions. This layer can be seen as a translator that speaks many languages (Karzel et al., 2016). The output of the sensors and tags, as well as the input of the actuators, depends on the protocol they implement. The device management layer is responsible for receiving device registrations and sensor measurements from the device integration layer, and for communicating status changes for actuators to the device integration layer. Then, the device integration layer checks if the status change (i.e., the action) conforms with the respective actuator and translates the status change to the actuator. The device management layer controls the devices that are connected to the system; every change to a device's registration, as well as new measurement data, should be communicated from the device integration layer to the device management layer, so the information can be updated and stored. Normally, the data management layer is a central database (but it can also be a data warehouse or even a complete data farm, in the case of larger IoT systems) that stores all data of a thing. Thus, the implementation of the data management layer strongly depends on the use case (Karzel et al., The context management layer defines the central business logic and is responsible for tasks like defining the goals of the thing, consuming and producing the context situations of the things, evaluating the context situation toward the goals, triggering actions that will help to fulfill the goal according to the evaluated rules, and finally, publishing context situations for other things. The thing integration layer is responsible for finding other things to communicate, verifies if communication with the new thing is possible, and is responsible for a registration mechanism. The application integration layer connects the user to the thing, being considered the service layer, or even a simple user interface. The concrete implementation of the layer depends on the use Explanation – 6M

	/ Y Level	RILA architecture					
	6	Application integration (services and user interface)					
/	5	Thing integration (finds other things to communicate)					
	Wanagement 3	Context management (central business logic)] ,				
	Mana 3	Data management (central database)	Security				
	2	Device management (controls the devices)					
	1	Device integration (includes different devices, measurements, and actions)					
	FIGURE 1.6 Reference loT layered the Internet of things, January 29, 201	d architecture. (Adapted from Karzel, D. 16, https://www.infoq.com/articles/intern	et al., A reference architecture for et-of-things-reference-architecture.) Figure – 4M				
+		OR					
+	Issues in organizational integration			3+3+4			
		•		=10M			
	Interoperability						
	Standards						
	Privacy						
	Security Trust	Any 3 Wi	th detail explanation 3+3+4M				
	Trust	•		101/			
	Connectivity and I/O interfaces	of IOT hardware platforms		10 M			
	 Yun:built-in Ethernet and Wi-Fi support. Arduino: digital I/O pins and analog pins with USB ports and feature other hardware I/O and communication interfaces. Diecimila, Uno, Duemilanove: USB port, 14 GPIO digital pins, and 6 analog input pins, SPI, 12C/TWI, and UART hardware I/O and communication interfaces. Due: 2 USB ports, 54 GPIO digital pins, 12 analog input pins, and 2 DAC analog output pins, 4 UART ports, 1 SPI header, 1 I2C, and 2 TWI headers. Yun: 2 USB ports, 20 GPIO digital pins, and 12 analog input pins, 1 UART port,1 ICSP header, SPI and I2C/TWI I/O communications. BeagleBoard has no onboard Ethernet port, communication interfaces including I2C, I2S, and SPI for serial communication, Digital Visual Interface (DVI)-D and S-Video for video display. But BeagleBoard-xM has an onboard Ethernet jack. PandaBoard is not Internet enabled, ES version has Ethernet and Wi-Fi and Bluetooth connectivity. Both boards include some communication interfaces, such as DVI, HDMI, camera expansion header, audio I/O, USB, serial/RS-232, and two USB host ports, as well as a 14-pin Joint Test Action Group (JTAG) GPIO, UART, I2C. A13-OlinuXino has a Video Graphics Array (VGA), Universal EXTension (UEXT) connector, asynchronous, I2C, and SPI, Internet connectivity is optional, OLinuXino-MINI-Wi-Fi version has built-in Wi-Fi connectivity. RaspberryPi 1 model A has one USB port, no Ethernet port, The SBC features HDMI, 						
	 Model B has an I 	n MIPI, camera interface, 26 GPIO p Ethernet port and two USB ports, a					
	that are on mode Intel Galileo has an Ethe the RS-232 serial port.	el A. ernet port, a USB port, and USB ho	st ports, in addition UART and				
		net port, two USB hubs, a mini-US	в, номі, 10м				
		OP					
		OR					

RILA architecture

Specification Highlights	Arduino 101	Arduino MKR1000	Adafruit Feather M0 Wi-Fi	Tessel 2 Almel SAMD2 IG14A-MU Cortex MOLMCU	Particle Photon 92-bit STM 92 ARM Cortex-M3 MCU	Particle Electro V-6 (STMV APM Corec M3 MCU
Processor architecture	2 cores: x 86 (intel Quark) core and 32-bit ARC core	SAMD2 : Cortex-M0+22-bit low-power ARM MCU	ATS AMD21G18 ARM Certex-M0 MCU		12C MHz	120 MHz
Processar speed	Eigh cores clocked at 32 MHz.	48 MLk	48 MHz	15 KB of SRAM	125 KB cfRAM	128 KB of RAM
Memory (RAM) Onboard storage	24 KB of SRAM 196 KB of flash	32 KB of SRAM 256 KB of flash	32 KB of SRAM 256 KB of Eash	2 KB of flash, 64 MB of DDR2 system memory 32 MB flash for firmware	I MB of flash memory	1 MB of flash memory
Onboard correctivity	FLE	HEEE 802.115/g/n W. Fi	TEEE \$62.11g or a Wi-Pi	197:00 M bit/s Ethernet and IEFE 802 TH/g/n Wi-Ff	IEFE 802. 16/g/n W - Fi	2 medek; U blox SARA U260 for 2G and U-blo SARA G350/U290 for
Peripheral intertaces	Micro-USB	Micro-USB	Micro-USB	2 USB ports, 1 micro-USB	Micro-USB	M-cro-USB
GPIO low-kwel pe upherals	14 digital I/O pins (of which 4 are PWM), 6 analog input pins	8 d.g tal 90 pins. 12 PWM pins. Paratog input pins. 1 UART, 1 SPL 112C	S PWM p.ns, 10 analog input pirs, and 1 unalog output pin, 12C, SPI	15 GPIO pins on 2 primary ports, A and B	8 Jigital PO pins 8 analog (ADC) inputs, 2 analog (DAC) outputs, 9 PWM output pins, 2 SM, 1 [28, 1 DC	28 GPIOs and TXRX
Os support	Open-source RTOS		311	1090	FreeRTOS	
Pauce concumption	Name	436 mW	481 and XI mW when unneeded parts shut down	Not specified	400 mW and 40 µW caring deep sleep	900mW to 9W
Size L×W or L×W×H(mia)	686×53.4	65×25×6	53.65×23×8 (without headers soldered)	Not specified	36.58×29.32×6.86 (with Inaders), 36.58×20.32×4.32	50.8×20.32× 12.7 cw th Leaders), 50.8×20.32
Des. (\$)	30	34.99	34.99	35	(vithou) 19	(without) 49 fer 2G, 69 for 3G
incryption chips Release date	January 2016	ECC508, WINC1500 April 2016	ATWINC1500 March 2016	— April 2016	On the MCU March 2015	29107.30, 69157.30 — February 2016