Chapter 4

Differential Amplifiers

The differential amplifier is among the most important circuit inventions, dating back to the vacuum tube era. Offering many useful properties, differential operation has become the dominant choice in today's high-performance analog and mixed-signal circuits.

This chapter deals with the analysis and design of CMOS differential amplifiers. Following a review of single-ended and differential operation, we describe the basic differential pair, and analyze both the large-signal and the small-signal behavior. Next, we introduce the concept of common-mode rejection and formulate it for differential amplifiers. We then study differential pairs with diode-connected and current-source loads as well as differential cascode stages. Finally, we describe the Gibert cell.

4.1 Single-Ended and Differential Operation

A single-ended signal is defined as one that is measured with respect to a fixed potential, usually the ground. A differential signal is defined as one that is measured between two nodes that have *equal* and *opposite* signal excursions around a fixed potential. In the strict sense, the two nodes must also exhibit equal impedances to that potential. Fig. 4.1 illustrates the two types of signals conceptually. The "center" potential in differential signaling is called the "common-mode" (CM) level.

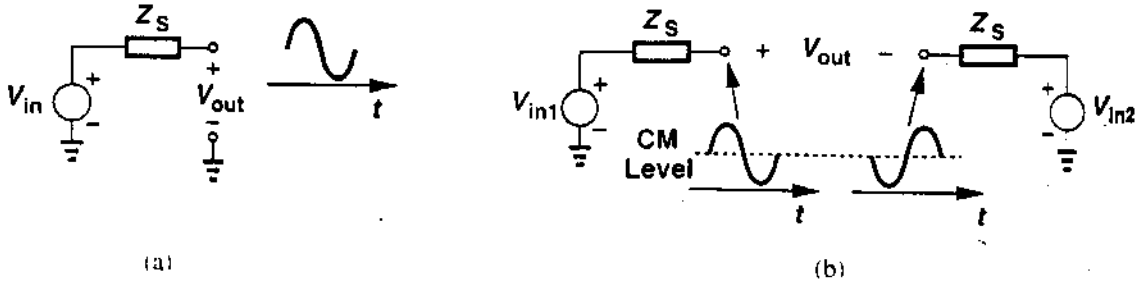


Figure 4.1 (a) Single-ended and (b) differential signals.

An important advantage of differential operation over single-ended signaling is higher immunity to "environmental" noise. Consider the example depicted in Fig. 4.2, where two adjacent lines in a circuit carry a small, sensitive signal and a large clock waveform. Due to capacitive coupling between the lines, transitions on line L_2 corrupt the signal on line L_1. Now suppose, as shown in Fig. 4.2(b), the sensitive signal is distributed as two equal and opposite phases. If the clock line is placed midway between the two, the transitions disturb the differential phases by equal amounts, leaving the *difference* intact. Since the common-mode level of the two phases is disturbed but the differential output is not corrupted, we say this arrangement "rejects" common-mode noise.

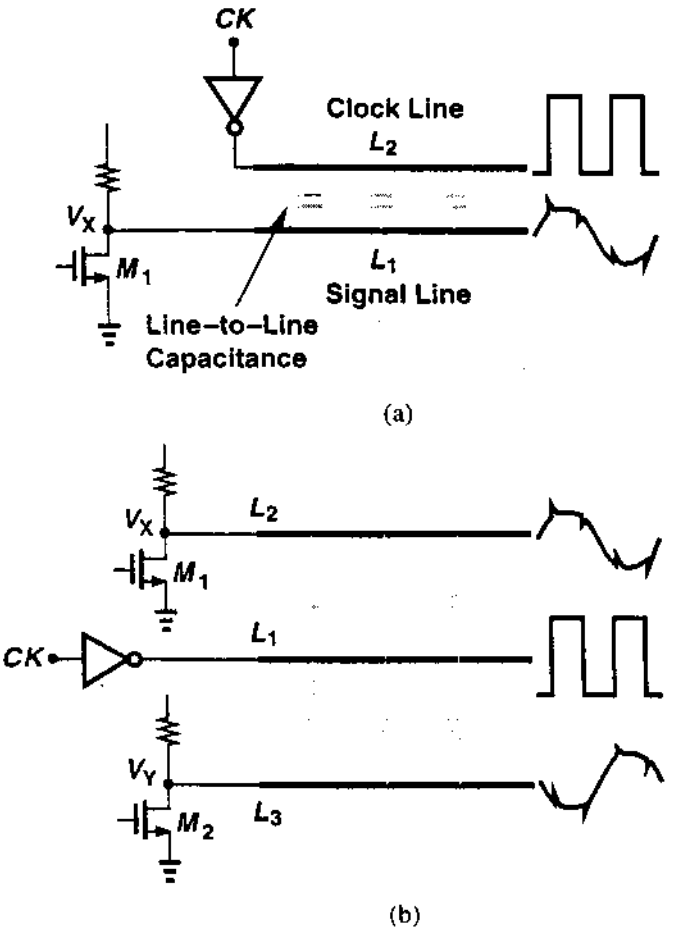


Figure 4.2 (a) Corruption of a signal due to coupling, (b) reduction of coupling by differential operation.

Another example of common-mode rejection occurs with noisy supply voltages. In Fig. 4.3(a), if V_{DD} varies by ΔV, then V_{out} changes by approximately the same amount, i.e., the output is quite susceptible to noise on V_{DD}. Now consider the circuit in Fig. 4.3(b). Here, if the circuit is symmetric, noise on V_{DD} affects V_X and V_Y but not $V_X - V_Y = V_{out}$. Thus, the circuit of Fig. 4.3(b) is much more robust to supply noise.

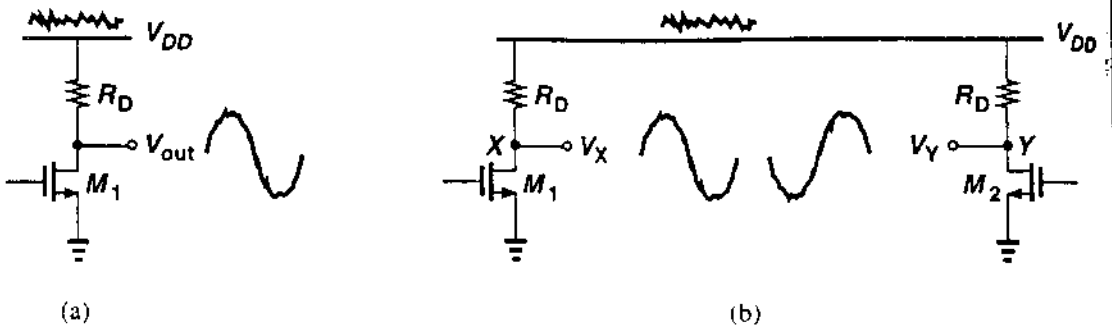


Figure 4.3 Effect of supply noise on (a) a single-ended circuit, (b) a differential circuit.

Thus far, we have seen the importance of employing differential paths for sensitive signals. It is also beneficial to employ differential distribution for *noisy lines*. For example, suppose the clock signal of Fig. 4.2 is distributed in differential form on two lines (Fig. 4.4). Then, with perfect symmetry, the components coupled from CK and $\overline{CK}$ to the signal line cancel each other.

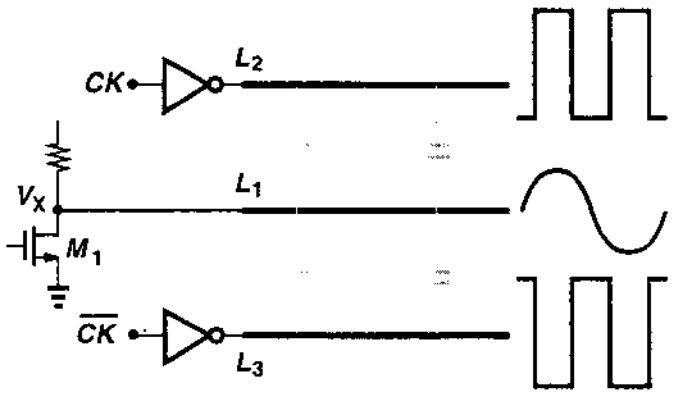


Figure 4.4 Reduction of coupled noise by differential operation.

Another useful property of differential signaling is the increase in maximum achievable voltage swings. In the circuit of Fig. 4.3, for example, the maximum output swing at X or Y is equal to $V_{DD} - (V_{GS} - V_{TH})$, whereas for $V_X - V_Y$, the peak-to-peak swing is equal to $2[V_{DD} - (V_{GS} - V_{TH})]$.

Other advantages of differential circuits over single-ended counterparts include simpler biasing and higher linearity (Chapter 13).

While it may seem that differential circuits occupy twice as much area as single-ended alternatives, in practice this is a minor drawback. Also, the suppression of nonideal effects by differential operation often results in a *smaller* area than that of a brute-force single-ended design. Furthermore, the numerous advantages of differential operation by far outweigh the possible increase in the area.

4.2 Basic Differential Pair

How do we amplify a differential signal? As suggested by the observations in the previous section, we may incorporate two identical single-ended signal paths to process the two phases [Fig. 4.5(a)]. Such a circuit indeed offers some of the advantages of differential

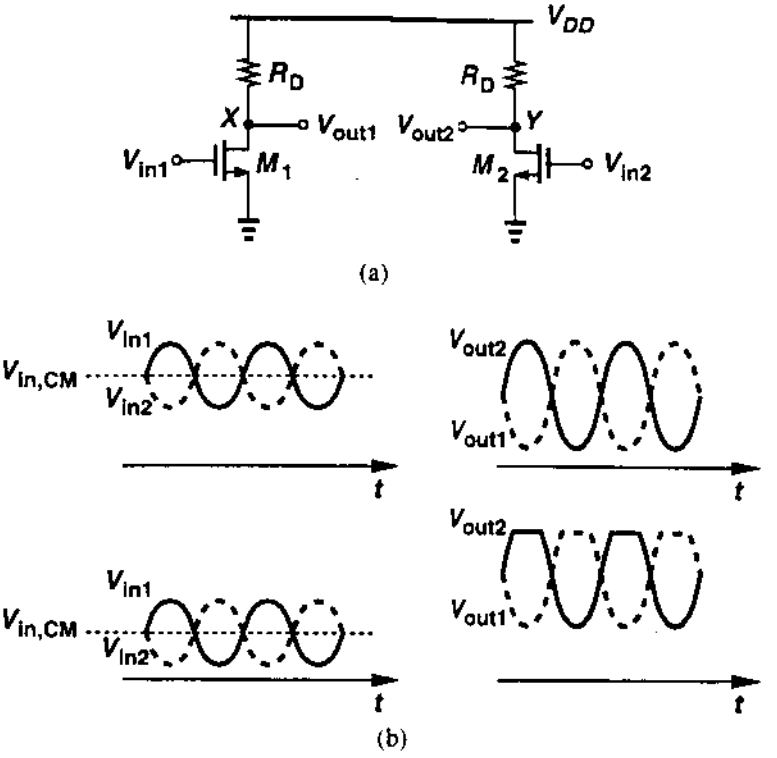


Figure 4.5 (a) Simple differential circuit, (b) illustration of sensitivity to the input common-mode level.

signaling: high rejection of supply noise, higher output swings, etc. But what happens if V_{in1} and V_{in2} experience a large common-mode disturbance or simply do not have a well-defined common-mode dc level? As the input CM level, $V_{in,CM}$, changes, so do the bias currents of M_1 and M_2, thus varying both the transconductance of the devices and the output CM level. The variation of the transconductance in turn leads to a change in the small-signal gain while the departure of the output CM level from its ideal value lowers the maximum allowable output swings. For example, as shown in Fig. 4.5(b), if the input CM level is excessively low, the minimum values of V_{in1} and V_{in2} may in fact turn off M_1 and M_2, leading to severe clipping at the output. Thus, it is important that the bias currents of the devices have minimal dependence on the input CM level.

A simple modification can resolve the above issue. Shown in Fig. 4.6, the "differential pair"[1] employs a current source I_{SS} to make $I_{D1} - I_{D2}$ independent of $V_{in,CM}$. Thus, if $V_{in1} = V_{in2}$, the bias current of each transistor equals $I_{SS}/2$ and the output common-mode

[1] Also called a source-coupled pair or (in the British literature) a long-tailed pair.

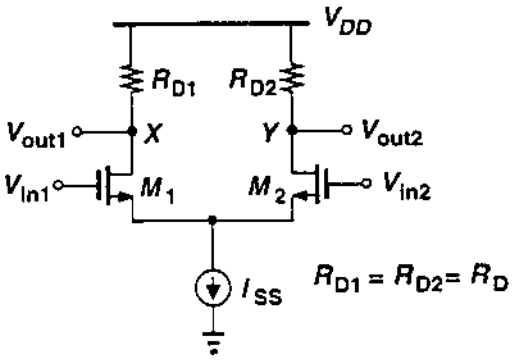


Figure 4.6 Basic differential pair.

level is $V_{DD} - R_D I_{SS}/2$. It is instructive to study the large-signal behavior of the circuit for both differential and common-mode input variations.

4.2.1 Qualitative Analysis

Let us assume that in Fig. 4.6, $V_{in1} - V_{in2}$ varies from $-\infty$ to $+\infty$. If V_{in1} is much more negative than V_{in2}, M_1 is off, M_2 is on, and $I_{D2} = I_{SS}$. Thus, $V_{out1} = V_{DD}$ and $V_{out2} = V_{DD} - R_D I_{SS}$. As V_{in1} is brought closer to V_{in2}, M_1 gradually turns on, drawing a fraction of I_{SS} from R_{D1} and hence lowering V_{out1}. Since $I_{D1} + I_{D2} = I_{SS}$, the drain current of M_2 decreases and V_{out2} rises. As shown in Fig. 4.7(a), for $V_{in1} = V_{in2}$, we have $V_{out1} = V_{out2} = V_{DD} - R_D I_{SS}/2$. As V_{in1} becomes more positive than V_{in2}, M_1 carries a greater current than does M_2 and V_{out1} drops below V_{out2}. For sufficiently large $V_{in1} - V_{in2}$, M_1 "hogs" all of I_{SS}, turning M_2 off. As a result, $V_{out1} = V_{DD} - R_D I_{SS}$ and $V_{out2} = V_{DD}$. Fig. 4.7 also plots $V_{out1} - V_{out2}$ versus $V_{in1} - V_{in2}$.

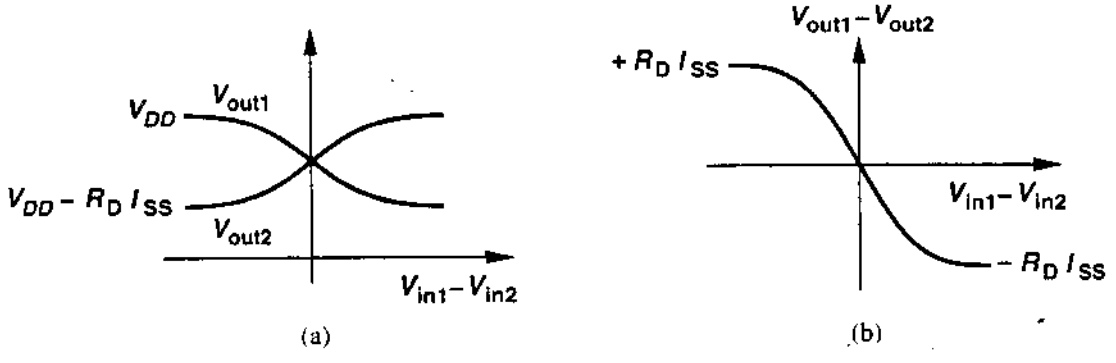


Figure 4.7 Input-output characteristics of a differential pair.

The foregoing analysis reveals two important attributes of the differential pair. First, the maximum and minimum levels at the output are well-defined (V_{DD} and $V_{DD} - R_D I_{SS}$, respectively) and independent of the input CM level. Second, the small-signal gain (the slope of $V_{out1} - V_{out2}$ versus $V_{in1} - V_{in2}$) is maximum for $V_{in1} = V_{in2}$, gradually falling to zero as $|V_{in1} - V_{in2}|$ increases. In other words, the circuit becomes more nonlinear as the input voltage swing increases. For $V_{in1} = V_{in2}$, we say the circuit is in equilibrium.

Now let us consider the common-mode behavior of the circuit. As mentioned earlier, the role of the tail current source is to suppress the effect of input CM level variations on the operation of M_1 and M_2 and the output level. Does this mean that $V_{in,CM}$ can assume arbitrarily low or high values? To answer this question, we set $V_{in1} = V_{in2} = V_{in,CM}$ and vary $V_{in,CM}$ from 0 to V_{DD}. Fig. 4.8(a) shows the circuit with I_{SS} implemented by an NFET. Note that the symmetry of the pair requires that $V_{out1} = V_{out2}$.

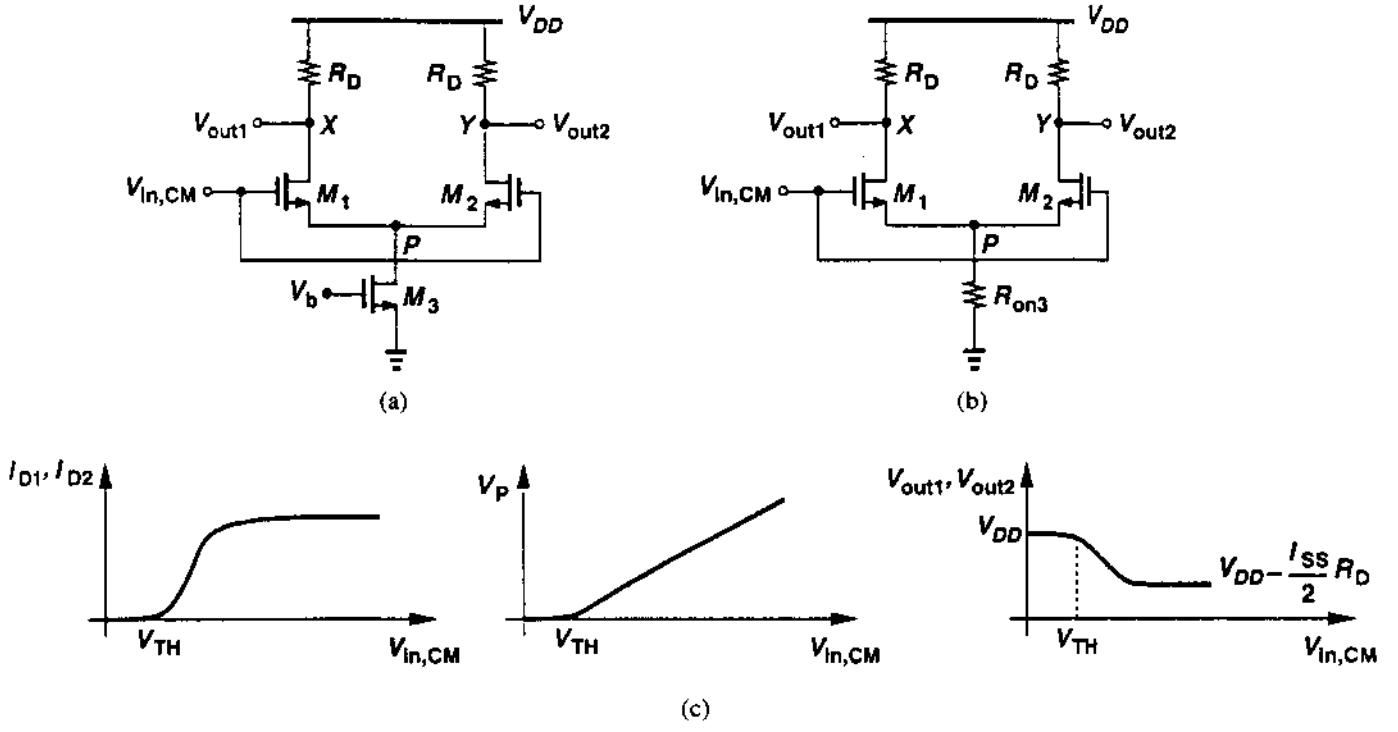


Figure 4.8 (a) Differential pair sensing an input common-mode change. (b) equivalent circuit if M_3 operates in deep triode region, (c) common-mode input-output characteristics.

What happens if $V_{in,CM} = 0$? Since the gate potential of M_1 and M_2 is not more positive than their source potential, both devices are off, yielding $I_{D3} = 0$. This indicates that M_3 is in deep triode region because V_b is high enough to create an inversion layer in the transistor. With $I_{D1} = I_{D2} = 0$, the circuit is incapable of signal amplification, and $V_{out1} = V_{out2} = V_{DD}$.

Now suppose $V_{in,CM}$ becomes more positive. Modeling M_3 by a resistor as in Fig. 4.8(b), we note that M_1 and M_2 turn on if $V_{in,CM} \geq V_{TH}$. Beyond this point, I_{D1} and I_{D2} continue to increase and V_P also rises [Fig. 4.8(c)]. In a sense, M_1 and M_2 constitute a source follower, forcing V_P to track $V_{in,CM}$. For a sufficiently high $V_{in,CM}$, the drain-source voltage of M_3 exceeds $V_{GS3} - V_{TH3}$, allowing the device to operate in saturation. The total current through M_1 and M_2 then remains constant. We conclude that for proper operation, $V_{in,CM} \geq V_{GS1} + (V_{GS3} - V_{TH3})$.

What happens if $V_{in,CM}$ rises further? Since V_{out1} and V_{out2} are relatively constant, we expect that M_1 and M_2 enter the triode region if $V_{in,CM} > V_{out1} + V_{TH} = V_{DD} - R_D I_{SS}/2 + V_{TH}$. This sets an upper limit on the input CM level. In summary, the allowable value of

$V_{in,CM}$ is bounded as follows:

$$V_{GS1} + (V_{GS3} - V_{TH3}) \leq V_{in,CM} \leq \min\left[V_{DD} - R_D\frac{I_{SS}}{2} + V_{TH},\ V_{DD}\right]. \quad (4.1)$$

Example 4.1

Sketch the small-signal differential gain of a differential pair as a function of the input CM level.

Solution

As shown in Fig. 4.9, the gain begins to increase as $V_{in,CM}$ exceeds V_{TH}. After the tail current source

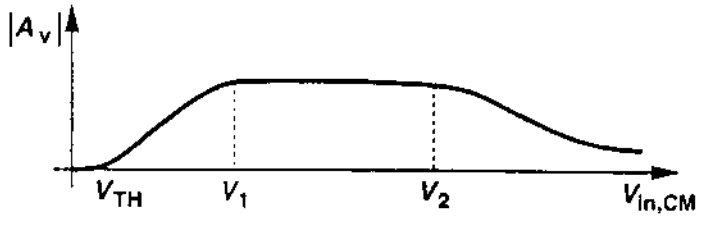


Figure 4.9

enters saturation ($V_{in,CM} = V_1$), the gain remains relatively constant. Finally, if $V_{in,CM}$ is so high that the input transistors enter the triode region ($V_{in,CM} = V_2$), the gain begins to fall.

With our understanding of differential and common-mode behavior of the differential pair, we can now answer another important question: How large can the output voltage swings of a differential pair be? As illustrated in Fig. 4.10, for M_1 and M_2 to be saturated, each output can go as high as V_{DD} but as low as approximately $V_{in,CM} - V_{TH}$. In other

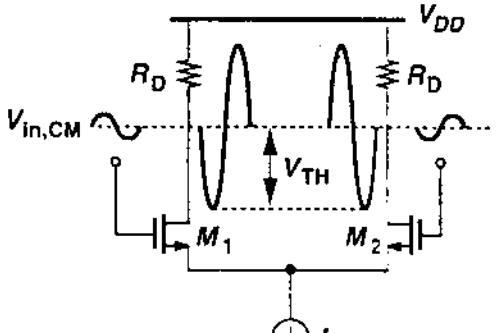


Figure 4.10 Maximum allowable output swings in a differential pair.

words, the higher the input CM level, the smaller the allowable output swings. For this reason, it is desirable to choose a relatively low $V_{in,CM}$, but the preceding stage may not provide such a level easily.

An interesting trade-off exists in the circuit of Fig. 4.10 between the maximum value of $V_{in,CM}$ and the differential *gain*. Similar to a simple common-source stage (Chapter 3),

the gain of a differential pair is a function of the dc drop across the load resistors. Thus, if $R_D I_{SS}/2$ is large, $V_{in,CM}$ must remain close to ground potential.

4.2.2 Quantitative Analysis

We now quantify the behavior of a MOS differential pair as a function of the input differential voltage. We begin with large-signal analysis to arrive at an expression for the plots shown in Fig. 4.7.

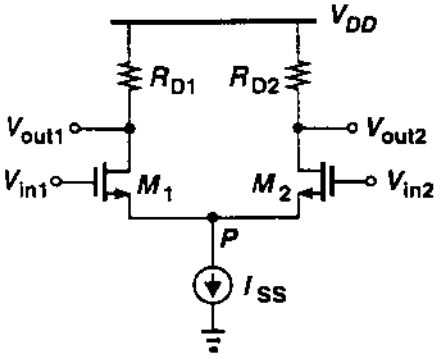


Figure 4.11 Differential pair.

For the differential pair in Fig. 4.11, we have $V_{out1} = V_{DD} - R_{D1} I_{D1}$ and $V_{out2} = V_{DD} - R_{D2} I_{D2}$, i.e., $V_{out1} - V_{out2} = R_{D2} I_{D2} - R_{D1} I_{D1} = R_D(I_{D2} - I_{D1})$ if $R_{D1} = R_{D2} = R_D$. Thus, we simply calculate I_{D1} and I_{D2} in terms of V_{in1} and V_{in2}, assuming the circuit is symmetric, M_1 and M_2 are saturated, and $\lambda = 0$. Since the voltage at node P is equal to $V_{in1} - V_{GS1}$ and $V_{in2} - V_{GS2}$,

$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}. \tag{4.2}$$

For a square-law device, we have:

$$(V_{GS} - V_{TH})^2 = \frac{I_D}{\frac{1}{2}\mu_n C_{ox} \frac{W}{L}}, \tag{4.3}$$

and, therefore,

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} + V_{TH}. \tag{4.4}$$

It follows from (4.2) and (4.4) that

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}}. \tag{4.5}$$

Our objective is to calculate the differential output current, $I_{D1} - I_{D2}$. Squaring the two sides of (4.5) and recognizing that $I_{D1} + I_{D2} = I_{SS}$, we obtain

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox} \dfrac{W}{L}} (I_{SS} - 2\sqrt{I_{D1} I_{D2}}). \tag{4.6}$$

That is,

$$\frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{D1} I_{D2}}. \tag{4.7}$$

Squaring the two sides again and noting that $4I_{D1}I_{D2} = (I_{D1} + I_{D2})^2 - (I_{D1} - I_{D2})^2 = I_{SS}^2 - (I_{D1} - I_{D2})^2$, we arrive at

$$(I_{D1} - I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox} \frac{W}{L}\right)^2 (V_{in1} - V_{in2})^4 + I_{SS}\mu_n C_{ox} \frac{W}{L}(V_{in1} - V_{in2})^2. \tag{4.8}$$

Thus,

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \dfrac{W}{L}} - (V_{in1} - V_{in2})^2}. \tag{4.9}$$

As expected, $I_{D1} - I_{D2}$ is an odd function of $V_{in1} - V_{in2}$, falling to zero for $V_{in1} = V_{in2}$. As $|V_{in1} - V_{in2}|$ increases from zero, $|I_{D1} - I_{D2}|$ also increases because the factor preceding the square root rises more rapidly than the argument in the square root drops.[2]

Before examining (4.9) further, it is instructive to calculate the slope of the characteristic, i.e., the equivalent G_m of M_1 and M_2. Denoting $I_{D1} - I_{D2}$ and $V_{in1} - V_{in2}$ by ΔI_D and ΔV_{in}, respectively, the reader can show that

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \frac{\dfrac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\dfrac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}. \tag{4.10}$$

For $\Delta V_{in} = 0$, $G_m = \sqrt{\mu_n C_{ox}(W/L) I_{SS}}$. Moreover, since $V_{out1} - V_{out2} = R_D \Delta I = R_D G_m \Delta V_{in}$, we can write the small-signal differential voltage gain of the circuit in the equilibrium condition as

$$|A_v| = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}\, R_D. \tag{4.11}$$

[2]It is interesting to note that, even though I_{D1} and I_{D2} are *even* functions of their respective gate-source voltages, $I_{D1} - I_{D2}$ is an odd function of $V_{in1} - V_{in2}$. This effect is studied in Chapter 13.

Equation (4.10) also suggests that G_m falls to zero for $\Delta V_{in} = \sqrt{2I_{SS}/(\mu_n C_{ox} W/L)}$. As we will see below, this value of ΔV_{in} plays an important role in the operation of the circuit.

Let us now examine Eq. (4.9) more closely. It appears that the argument in the square root drops to zero for $\Delta V_{in} = \sqrt{4I_{SS}/(\mu_n C_{ox} W/L)}$, implying that ΔI_D crosses zero at *two* different values of ΔV_{in}. This was not predicted in our qualitative analysis in Fig. 4.7. This conclusion, however, is incorrect. To understand why, recall that (4.9) was derived with the assumption that both M_1 and M_2 are on. In reality, as ΔV_{in} exceeds a limit, one transistor carries the entire I_{SS}, turning off the other.[3] Denoting this value by ΔV_{in1}, we have $I_{D1} = I_{SS}$ and $\Delta V_{in1} = V_{GS1} - V_{TH}$ because M_2 is nearly off. It follows that

$$\Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \dfrac{W}{L}}}. \tag{4.12}$$

For $\Delta V_{in} > \Delta V_{in1}$, M_2 is off and (4.9) does not hold. As mentioned above, G_m falls to zero for $\Delta V_{in} = \Delta V_{in1}$. Figure 4.12 plots the behavior.

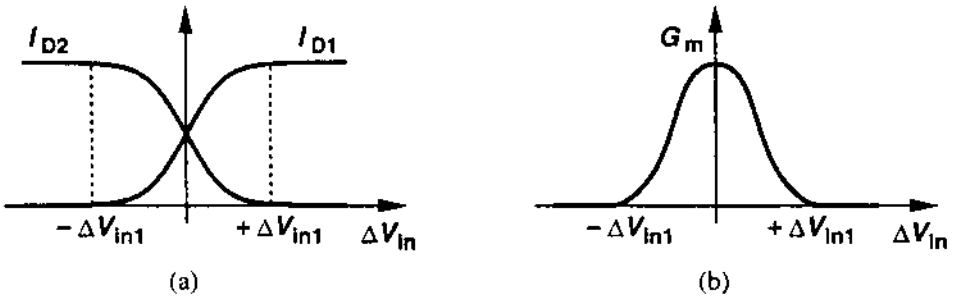


Figure 4.12 Variation of drain currents and overall transconductance of a differential pair versus input voltage.

Example 4.2

Plot the input-output characteristic of a differential pair as the device width and the tail current vary.

Solution

Consider the characteristic shown in Fig. 4.13(a). As W/L increases, ΔV_{in1} decreases, narrowing the input range across which both devices are on [Fig. 4.13(b)]. As I_{SS} increases, both the input range and the output current swing increase [Fig. 4.13(c)]. Intuitively, we expect the circuit to become more linear as I_{SS} increases or W/L decreases.

The value of ΔV_{in1} given by (4.12) in essence represents the maximum differential input that the circuit can "handle." It is possible to relate ΔV_{in1} to the overdrive voltage

[3] We neglect subthreshold conduction here.

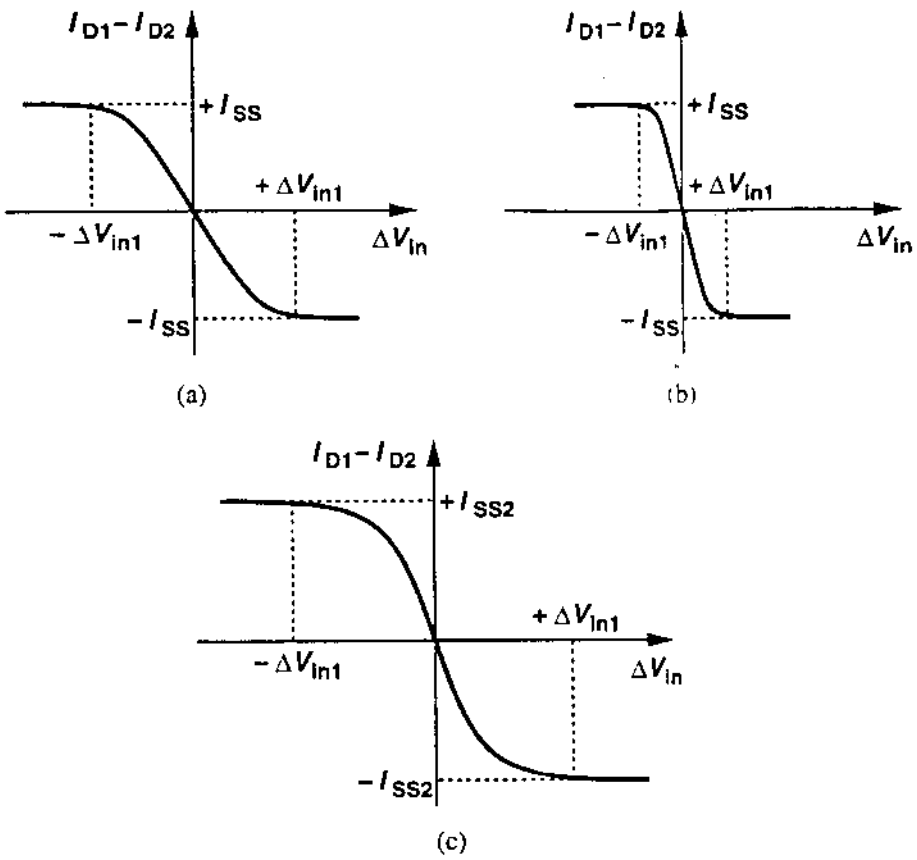


Figure 4.13

of M_1 and M_2 in equilibrium. For a zero differential input, $I_{D1} = I_{D2} = I_{SS}/2$, and hence

$$(V_{GS} - V_{TH})_{1,2} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \dfrac{W}{L}}}. \tag{4.13}$$

Thus, the equilibrium overdrive is equal to $\Delta V_{in1}/\sqrt{2}$. The point is that increasing ΔV_{in1} to make the circuit more linear inevitably increases the overdrive voltage of M_1 and M_2. For a given I_{SS}, this is accomplished only by reducing W/L and hence the transconductance of the transistors.

We now study the small-signal behavior of differential pairs. As depicted in Fig. 4.14, we apply small signals V_{in1} and V_{in2} and assume M_1 and M_2 are saturated. What is the differential voltage gain, $V_{out}/(V_{in1} - V_{in2})$? Recall from Eq. (4.11) that this quantity equals $\sqrt{\mu_n C_{ox} I_{SS} W/L} R_D$. Since in the vicinity of equilibrium, each transistor carries approximately $I_{SS}/2$, this expression reduces to $g_m R_D$, where g_m denotes the transconductance of M_1 and M_2. To arrive at the same result by small-signal analysis, we employ two different methods, each providing insight into the circuit's operation. We assume $R_{D1} = R_{D2} = R_D$.

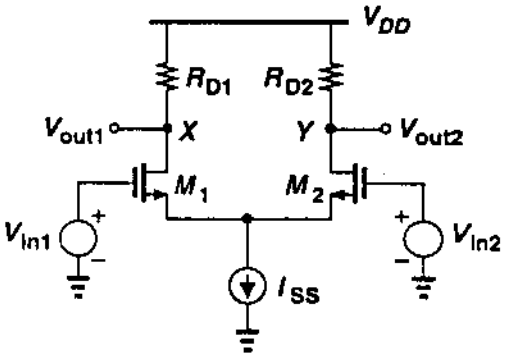
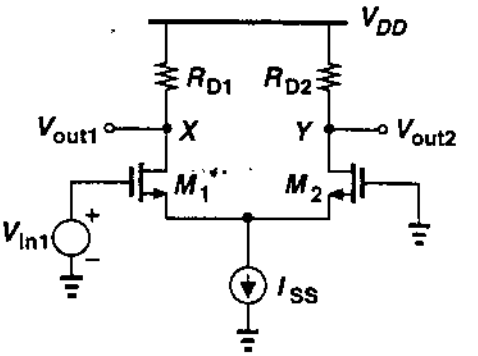
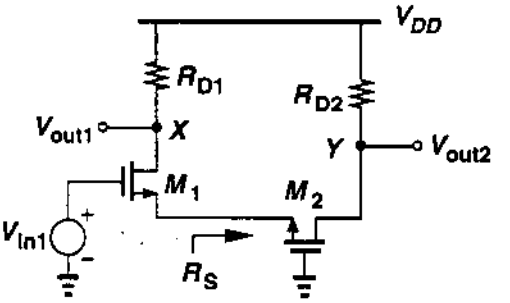


Figure 4.14 Differential pair with small-signal inputs.



(a)



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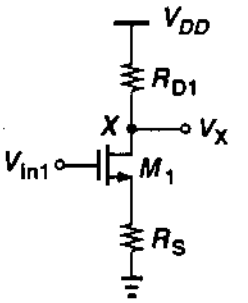


(c)

Figure 4.15 (a) Differential pair sensing one input signal, (b) circuit of (a) viewed as a CS stage degenerated by M_2, (c) equivalent circuit of (b).

Method I The circuit of Fig. 4.14 is driven by two independent signals. Thus, the output can be computed by superposition.

Let us set V_{in2} to zero and find the effect of V_{in1} at X and Y [Fig. 4.15(a)]. To obtain V_X, we note that M_1 forms a common-source stage with a degeneration resistance equal to the impedance seen looking into the source of M_2 [Fig. 4.15(b)]. Neglecting channel-length

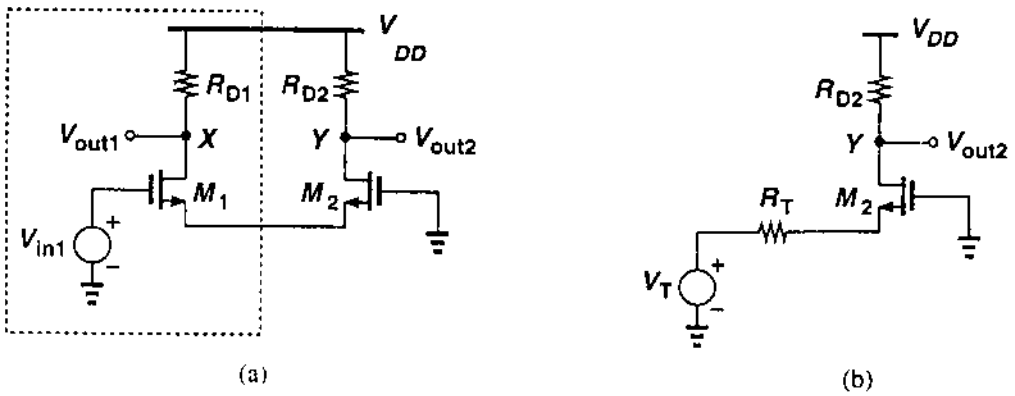


Figure 4.16 Replacing M_1 by a Thevenin equivalent.

modulation and body effect, we have $R_S = 1/g_{m2}$ [Fig. 4.15(c)] and

$$\frac{V_X}{V_{in1}} = \frac{-R_D}{\dfrac{1}{g_{m1}} + \dfrac{1}{g_{m2}}}. \tag{4.14}$$

To calculate V_Y, we note that M_1 drives M_2 as a source follower and replace V_{in1} and M_1 by a Thevenin equivalent (Fig. 4.16): the Thevenin voltage $V_T = V_{in1}$ and the resistance $R_T = 1/g_{m1}$. Here, M_2 operates as a common-gate stage, exhibiting a gain equal to

$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\dfrac{1}{g_{m2}} + \dfrac{1}{g_{m1}}}. \tag{4.15}$$

It follows from (4.14) and (4.15) that the overall voltage gain for V_{in1} is

$$(V_X - V_Y)|_{\text{Due to } V_{in1}} = \frac{-2R_D}{\dfrac{1}{g_{m1}} + \dfrac{1}{g_{m2}}} V_{in1}, \tag{4.16}$$

which, for $g_{m1} = g_{m2} = g_m$, reduces to

$$(V_X - V_Y)|_{\text{Due to } V_{in1}} = -g_m R_D V_{in1}. \tag{4.17}$$

By virtue of symmetry, the effect of V_{in2} at X and Y is identical to that of V_{in1} except for a change in the polarities:

$$(V_X - V_Y)|_{\text{Due to } V_{in2}} = g_m R_D V_{in2}. \tag{4.18}$$

Adding the two sides of (4.17) and (4.18) to perform superposition, we have

$$\frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D. \tag{4.19}$$

Comparison of (4.17), (4.18), and (4.19) indicates that the magnitude of the differential gain is equal to $g_m R_D$ regardless of how the inputs are applied: in Figs. 4.15 and 4.16, the input is applied to only one side whereas in Fig. 4.14 the input is the *difference* between two sources. It is also important to recognize that if the output is single-ended, i.e., it is sensed between X or Y and ground, the gain is halved.

Example 4.3

In the circuit of Fig. 4.17, M_2 is twice as wide as M_1. Calculate the small-signal gain if the bias values of V_{in1} and V_{in2} are equal.

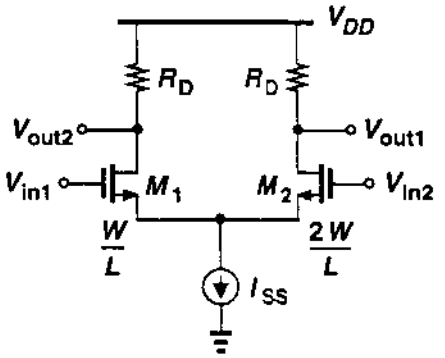


Figure 4.17

Solution

If the gates of M_1 and M_2 are at the same dc potential, then $V_{GS1} = V_{GS2}$ and $I_{D2} = 2I_{D1} = 2I_{SS}/3$. Thus, $g_{m1} = \sqrt{2\mu_n C_{ox}(W/L)I_{SS}/3}$ and $g_{m2} = \sqrt{2\mu_n C_{ox}(2W/L)2I_{SS}/3} = 2g_{m1}$. Following the same procedure as above, the reader can show that

$$|A_v| = \frac{2R_D}{\frac{1}{g_{m1}} + \frac{1}{2g_{m1}}} \tag{4.20}$$

$$= \frac{4}{3} g_{m1} R_D. \tag{4.21}$$

Note that, for a given I_{SS}, this value is lower than the gain of a symmetric differential pair (with $2W/L$ for each device) [Eq. (4.19)] because g_{m1} is smaller.

How does the gain of a differential pair compare with that of a common-source stage? For a given *total* bias current, the value of g_m in (4.19) is $1/\sqrt{2}$ times that of a single transistor biased at I_{SS} with the same dimensions. Thus, the total gain is proportionally less. Equivalently, for given device dimensions and load impedance, a differential pair achieves the same gain as a CS stage at the cost of twice the bias current.

Method II If a fully-symmetric differential pair senses differential inputs (i.e., the two inputs change by equal and opposite amounts from the equilibrium condition), then the concept of "half circuit" can be applied. We first prove a lemma.

Lemma. Consider the symmetric circuit shown in Fig. 4.18(a), where D_1 and D_2 represent

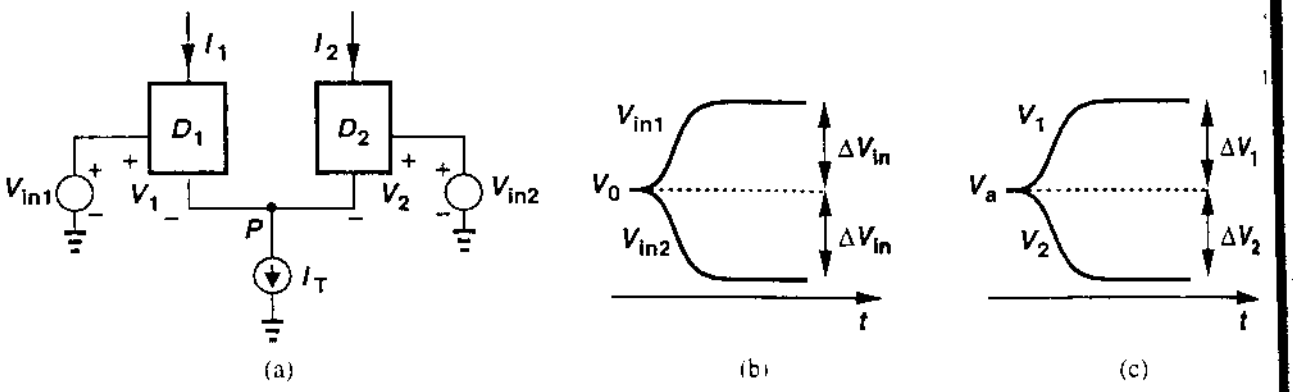


Figure 4.18 Illustration of why node P is a virtual ground.

any three-terminal active device. Suppose V_{in1} changes from V_0 to $V_0 + \Delta V_{in}$ and V_{in2} from V_0 to $V_0 - \Delta V_{in}$ [Fig. 4.18(b)]. Then, if the circuit remains linear, V_P does not change. Assume $\lambda = 0$.

Proof. Let us assume that V_1 and V_2 have an equilibrium value of V_a and change by ΔV_1 and ΔV_2, respectively [Fig. 4.18(c)]. The output currents therefore change by $g_m \Delta V_1$ and $g_m \Delta V_2$. Since $I_1 + I_2 = I_T$, we have $g_m \Delta V_1 + g_m \Delta V_2 = 0$, i.e., $\Delta V_1 = -\Delta V_2$. We also know $V_{in1} - V_1 = V_{in2} - V_2$, and hence $V_0 + \Delta V_{in} - (V_a + \Delta V_1) = V_0 - \Delta V_{in} - (V_a + \Delta V_2)$. Consequently, $2\Delta V_{in} = \Delta V_1 - \Delta V_2 = 2\Delta V_1$. In other words, if V_{in1} and V_{in2} change by $+\Delta V_{in}$ and $-\Delta V_{in}$, respectively, then V_1 and V_2 change by the same values. i.e., a differential change in the inputs is simply "absorbed" by V_1 and V_2. In fact, since $V_P = V_{in1} - V_1$, and since V_1 exhibits the same change as V_{in1}, V_P does not change. ❑

The proof of the foregoing lemma can also be invoked from symmetry. As long as the operation remains linear so that the difference between the bias currents of D_1 and D_2 is negligible, the circuit is symmetric. Thus, V_P cannot "favor" the change at one input and "ignore" the other.

From yet another point of view, the effect of D_1 and D_2 at node P can be represented by Thevenin equivalents (Fig. 4.19). If V_{T1} and V_{T2} change by equal and opposite amounts and R_{T1} and R_{T2} are equal, then V_P remains constant. We emphasize that this is valid if the changes are small such that we can assume $R_{T1} = R_{T2}$.[4]

The above lemma greatly simplifies the small-signal analysis of differential amplifiers. As shown in Fig. 4.20, since V_P experiences no change, node P can be considered "ac ground" and the circuit can be decomposed into two separate halves, hence the term "half-circuit concept" [1]. We can write $V_X / V_{in1} = -g_m R_D$ and $V_Y/(-V_{in1}) = -g_m R_D$, where V_{in1} and $-V_{in1}$ denote the voltage *change* on each side. Thus, $(V_X - V_Y)/(2V_{in1}) = -g_m R_D$.

[4] It is also possible to derive an expression for the large-signal behavior of V_P and prove that for small $V_{in1} - V_{in2}$, V_P remains constant. We defer this calculation to Chapter 14.

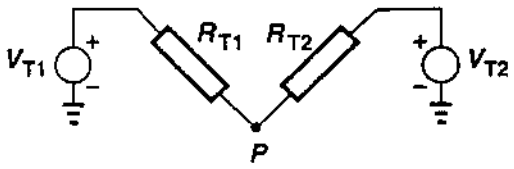


Figure 4.19 Replacing each half of a differential pair by a Thevenin equivalent.

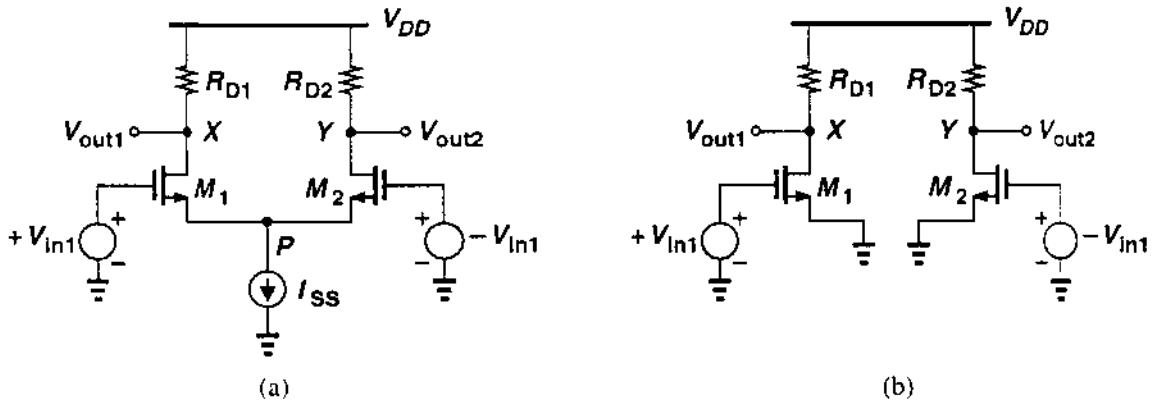


Figure 4.20 Application of the half-circuit concept.

Example 4.4

Calculate the differential gain of the circuit of Fig. 4.20(a) if $\lambda \neq 0$.

Solution

Applying the half-circuit concept as illustrated in Fig. 4.21, we have $V_X/V_{in1} = -g_m(R_D \| r_{O1})$ and $V_Y/(-V_{in1}) = -g_m(R_D \| r_{O2})$, thus arriving at $(V_X - V_Y)/(2V_{in1}) = -g_m(R_D \| r_O)$, where $r_O = r_{O1} = r_{O2}$. Note that Method I would require lengthy calculations here.

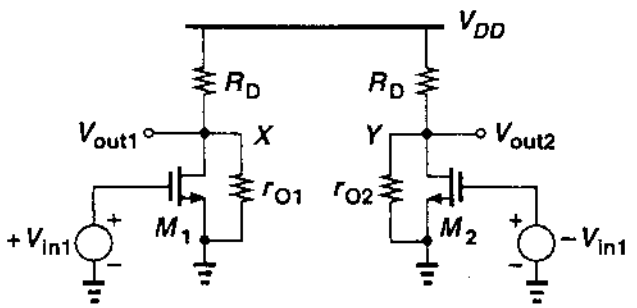


Figure 4.21

The half-circuit concept provides a powerful technique for analyzing symmetric differential pairs with fully differential inputs. But what happens if the two inputs are not fully

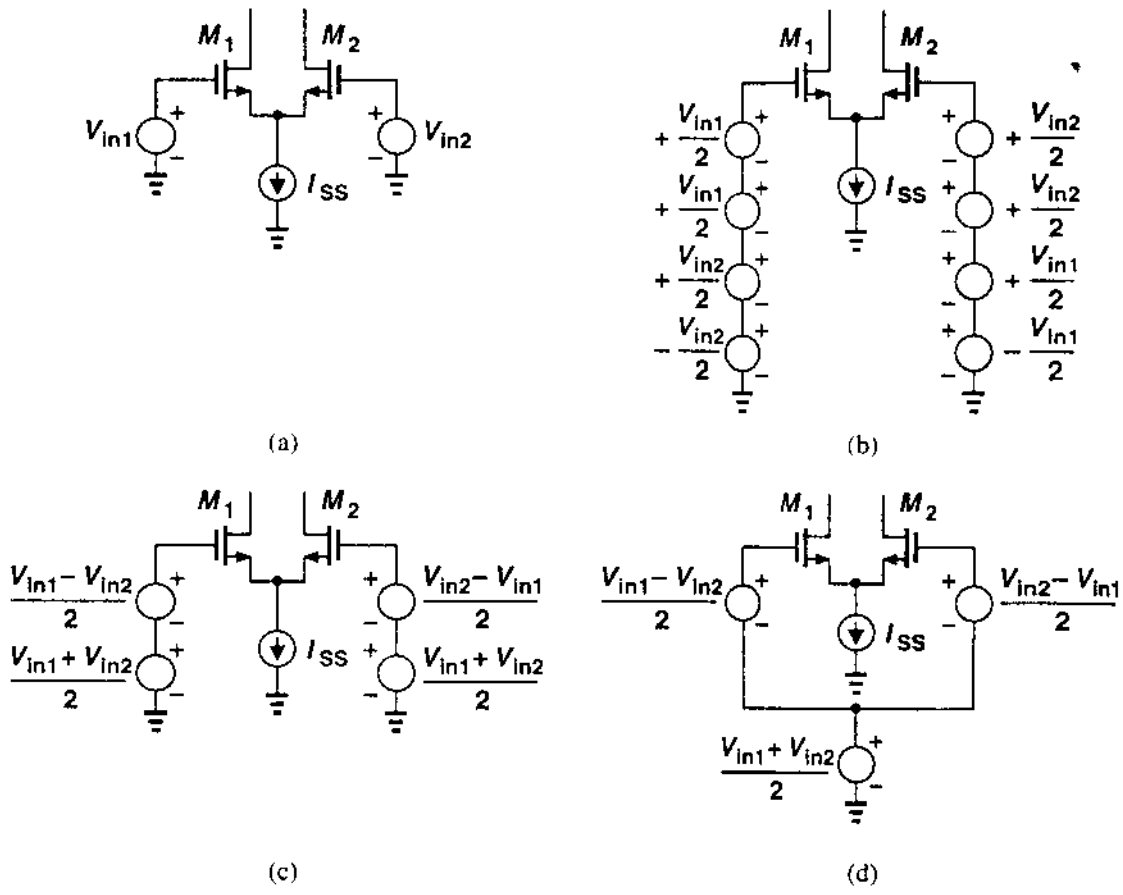


Figure 4.22 Conversion of arbitrary inputs to differential and common-mode components.

differential [Fig. 4.22(a)]? As depicted in Figs. 4.22(b) and (c), the two inputs V_{in1} and V_{in2} can be viewed as

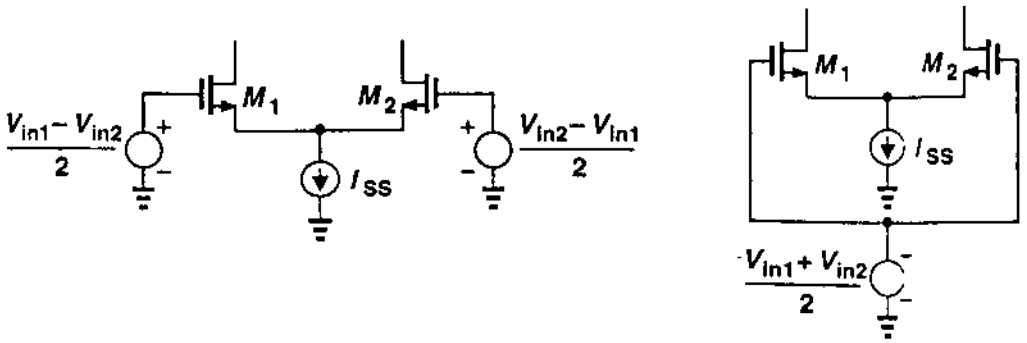
$$V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2} \tag{4.22}$$

$$V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2} \tag{4.23}$$

Since the second term is common to both inputs, we obtain the equivalent circuit in Fig. 4.22(d), recognizing that the circuit senses a combination of a differential input and a common-mode variation. Therefore, as illustrated in Fig. 4.23, the effect of each type of input can be computed by superposition, with the half-circuit concept applied to the differential-mode operation.

Example 4.5

In the circuit of Fig. 4.20(a), calculate V_X and V_Y if $V_{in1} \neq -V_{in2}$ and $\lambda \neq 0$.



(a) (b)

Figure 4.23 Superposition for differential and common-mode signals.

Solution

For differential-mode operation, we have from Fig. 4.24(a)

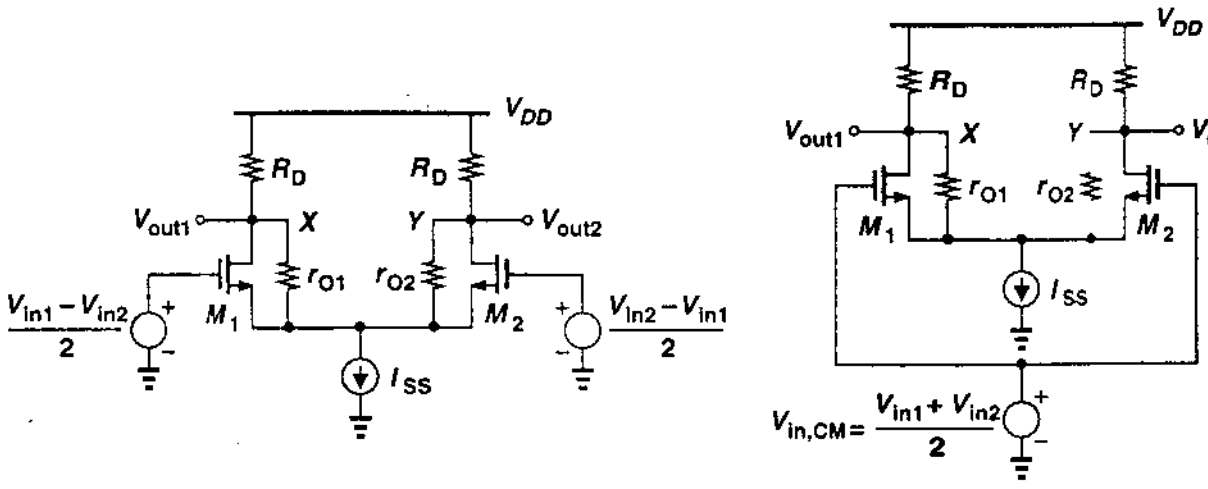
$$V_X = -g_m(R_D \| r_{O1})\frac{V_{in1} - V_{in2}}{2} \tag{4.}$$

$$V_Y = -g_m(R_D \| r_{O2})\frac{V_{in2} - V_{in1}}{2}. \tag{4.}$$

That is,

$$V_X - V_Y = -g_m(R_D \| r_O)(V_{in1} - V_{in2}), \tag{4.}$$

which is to be expected.



(a) (b)

Figure 4.24

For common-mode operation, the circuit reduces to that in Fig. 4.24(b). How much do V_X and V_Y change as $V_{in,CM}$ changes? If the circuit is fully symmetric and I_{SS} an ideal current source,

current drawn by M_1 and M_2 from R_{D1} and R_{D2} is exactly equal to $I_{SS}/2$ and independent of $V_{in,CM}$. Thus, V_X and V_Y experience no change as $V_{in,CM}$ varies. Interestingly, the circuit simply amplifies the difference between V_{in1} and V_{in2} while eliminating the effect of $V_{in,CM}$.

4.3 Common-Mode Response

An important attribute of differential amplifiers is their ability to suppress the effect of common-mode perturbations. Example 4.5 portrays an idealized case of common-mode response. In reality, neither is the circuit fully symmetric nor does the current source exhibit an infinite output impedance. As a result, a fraction of the input CM variation appears at the output.

We first assume the circuit is symmetric but the current source has a finite output impedance, R_{SS} [Fig. 4.25(a)]. As $V_{in,CM}$ changes, so does V_P, thereby increasing the drain currents of M_1 and M_2 and lowering both V_X and V_Y. Owing to symmetry, V_X remains equal to V_Y and, as depicted in Fig. 4.25(b), the two nodes can be shorted together. Since M_1 and M_2 are now "in parallel," i.e., they share all of their respective terminals, the

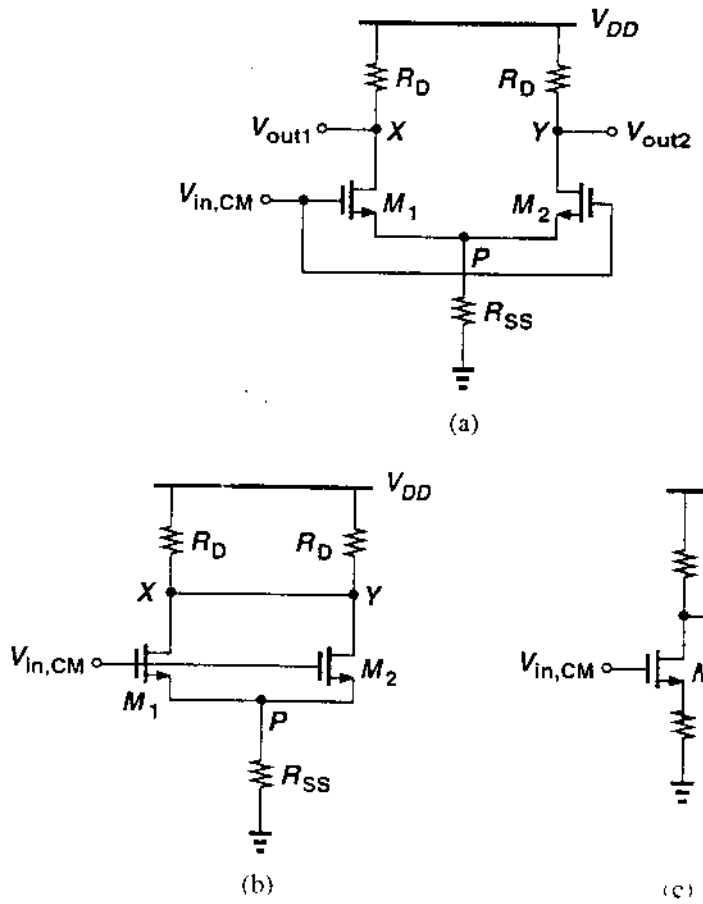


Figure 4.25 (a) Differential pair sensing CM input, (b) simplified version of (a), (c) equivalent circuit of (b).

circuit can be reduced to that in Fig. 4.25(c). Note that the compound device, $M_1 + M_2$, has twice the width and the bias current of each of M_1 and M_2 and, therefore, twice their transconductance. The CM gain of the circuit is thus equal to

$$A_{v,CM} = \frac{V_{out}}{V_{in,CM}} \tag{4.27}$$

$$= -\frac{R_D/2}{1/(2g_m) + R_{SS}}, \tag{4.28}$$

where g_m denotes the transconductance of each of M_1 and M_2 and $\lambda = \gamma = 0$.

What is the significance of this calculation? In a symmetric circuit, input CM variations disturb the bias points, altering the small-signal gain and possibly limiting the output voltage swings. This can be illustrated by an example.

Example 4.6

The circuit of Fig. 4.26 uses a resistor rather than a current source to define a tail current of 1 mA.

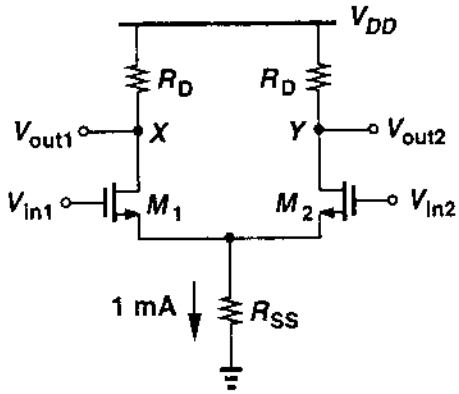


Figure 4.26

Assume $(W/L)_{1,2} = 25/0.5$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{TH} = 0.6$ V, $\lambda = \gamma = 0$, and $V_{DD} = 3$ V.

(a) What is the required input CM for which R_{SS} sustains 0.5 V?

(b) Calculate R_D for a differential gain of 5.

(c) What happens at the output if the input CM level is 50 mV higher than the value calculated in (a)?

Solution

(a) Since $I_{D1} = I_{D2} = 0.5$ mA, we have

$$V_{GS1} = V_{GS2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - V_{TH} \tag{4.29}$$

$$= 1.23\ \text{V}. \tag{4.30}$$

Thus, $V_{in,CM} = V_{GS1} + 0.5$ V$= 1.73$ V. Note that $R_{SS} = 500\ \Omega$.

(b) The transconductance of each device is $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_{D1}} = 1/(632\ \Omega$, requiring $R_D = 3.16\ \text{k}\Omega$ for a gain of 5.

Note that the output bias level is equal to $V_{DD} - I_{D1}R_D = 1.42$ V. Since $V_{in,CM} = 1.73$ V and $V_{TH} = 0.6$ V, the transistors are 290 mV away from the triode region.

(c) If $V_{in,CM}$ increases by 50 mV, the equivalent circuit of Fig. 4.25(c) suggests that V_X and V_Y drop by

$$|\Delta V_{X,Y}| = \Delta V_{in,CM} \frac{R_D/2}{R_{SS} + 1/(2g_m)} \tag{4.31}$$

$$= 50 \text{ mV} \times 1.94 \tag{4.32}$$

$$= 96.8 \text{ mV}. \tag{4.33}$$

Now, M_1 and M_2 are only 143 mV away from the triode region because the input CM level has increased by 50 mV and the output CM level has decreased by 96.8 mV.

The foregoing discussion indicates that the finite output impedance of the tail current source results in some common-mode gain in a symmetric differential pair. Nonetheless, this is usually a minor concern. More troublesome is the variation of the *differential* output as a result of a change in $V_{in,CM}$, an effect that occurs because in reality the circuit is not fully symmetric, i.e., the two sides suffer from slight mismatches during manufacturing. For example, in Fig. 4.25(a), R_{D1} may not be exactly equal to R_{D2}.

We now study the effect of input common-mode variation if the circuit is asymmetric and the tail current source suffers from a finite output impedance. Suppose, as shown in Fig. 4.27, $R_{D1} = R_D$ and $R_{D2} = R_D + \Delta R_D$, where ΔR_D denotes a small mismatch and

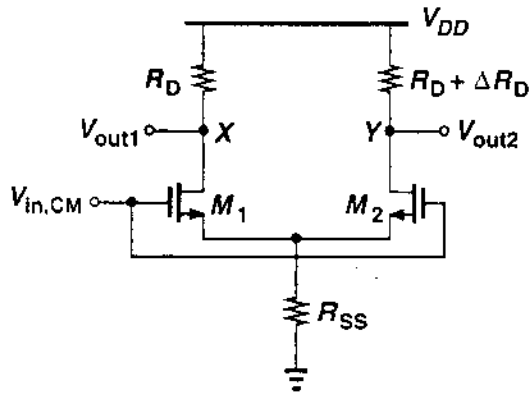


Figure 4.27 Common-mode response in the presence of resistor mismatch.

the circuit is otherwise symmetric. What happens to V_X and V_Y as $V_{in,CM}$ increases? Since M_1 and M_2 are identical, I_{D1} and I_{D2} increase by $[g_m/(1 + 2g_m R_{SS})]\Delta V_{in,CM}$, but V_X and V_Y change by different amounts:

$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D \tag{4.34}$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D). \tag{4.35}$$

Thus, a common-mode change at the input introduces a *differential* component at the output. We say the circuit exhibits common-mode to differential conversion. This is a critical problem because if the input of a differential pair includes both a differential signal and

current drawn by M_1 and M_2 from R_{D1} and R_{D2} is exactly equal to $I_{SS}/2$ and independent of $V_{in,CM}$. Thus, V_X and V_Y experience no change as $V_{in,CM}$ varies. Interestingly, the circuit simply amplifies the difference between V_{in1} and V_{in2} while eliminating the effect of $V_{in,CM}$.

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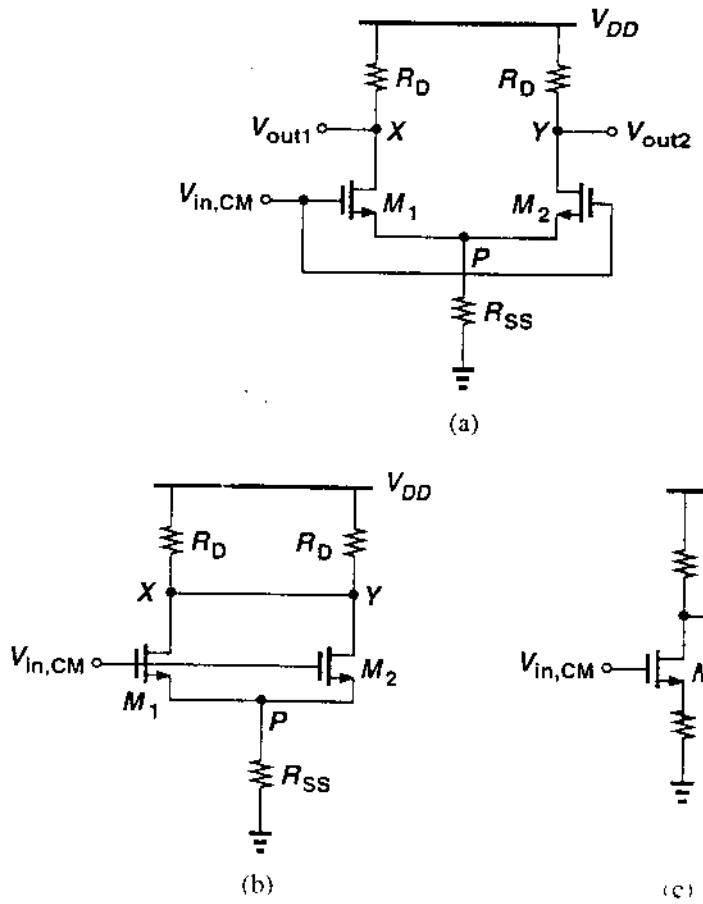

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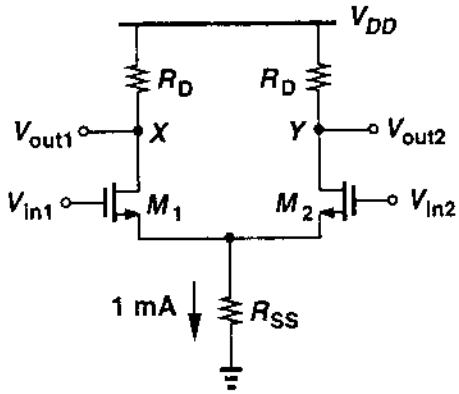

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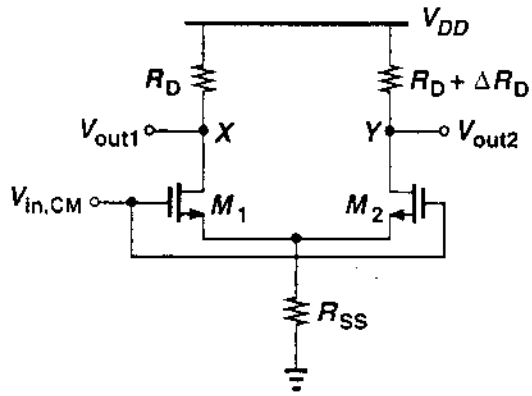

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$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D \tag{4.34}$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D). \tag{4.35}$$

Thus, a common-mode change at the input introduces a *differential* component at the output. We say the circuit exhibits common-mode to differential conversion. This is a critical problem because if the input of a differential pair includes both a differential signal and

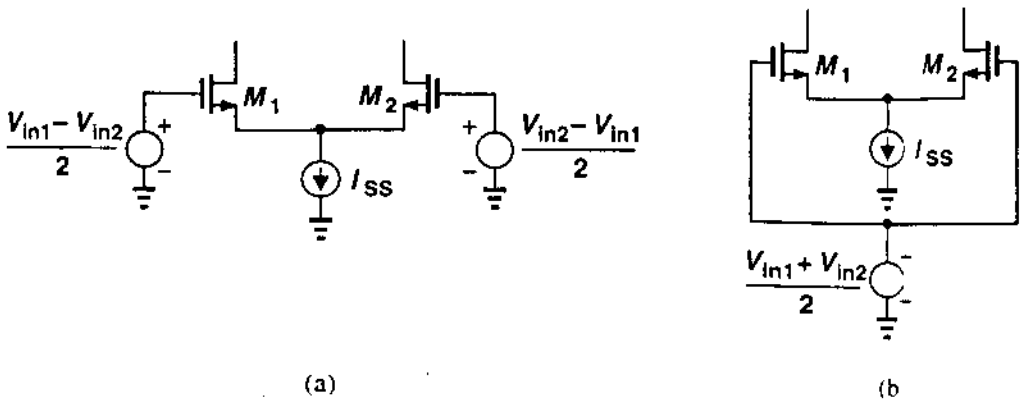


Figure 4.23 Superposition for differential and common-mode signals.

Solution

For differential-mode operation, we have from Fig. 4.24(a)

$$V_X = -g_m(R_D \| r_{O1}) \frac{V_{in1} - V_{in2}}{2} \tag{4.24}$$

$$V_Y = -g_m(R_D \| r_{O2}) \frac{V_{in2} - V_{in1}}{2}. \tag{4.25}$$

That is,

$$V_X - V_Y = -g_m(R_D \| r_O)(V_{in1} - V_{in2}), \tag{4.26}$$

which is to be expected.

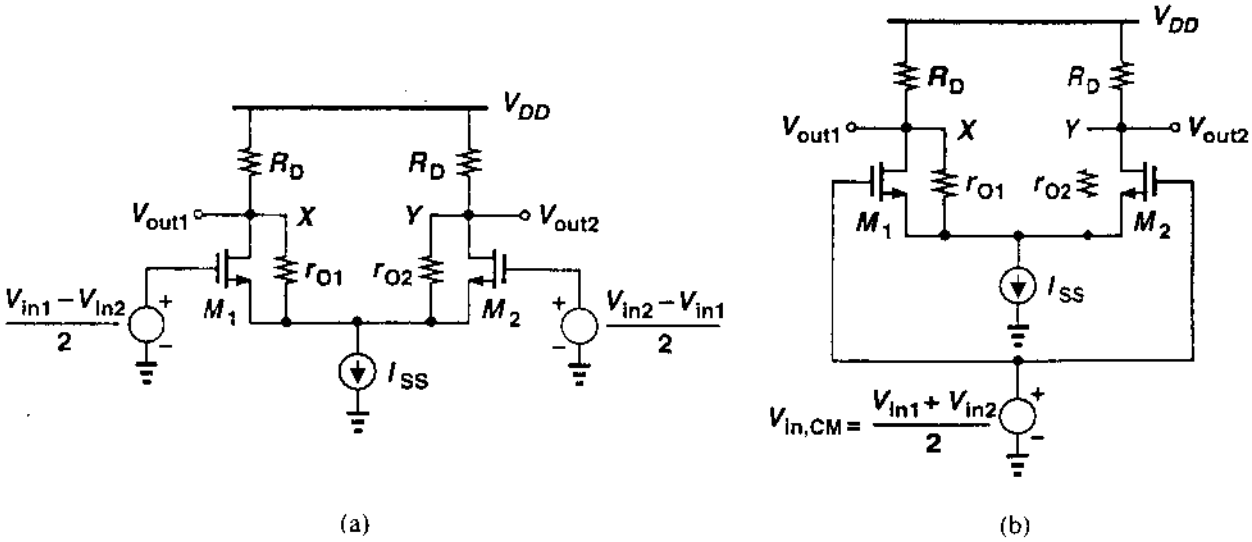


Figure 4.24

For common-mode operation, the circuit reduces to that in Fig. 4.24(b). How much do V_X and V_Y change as $V_{in,CM}$ changes? If the circuit is fully symmetric and I_{SS} an ideal current source, the

common-mode noise, the circuit corrupts the amplified differential signal by the input CM change. The effect is illustrated in Fig. 4.28.

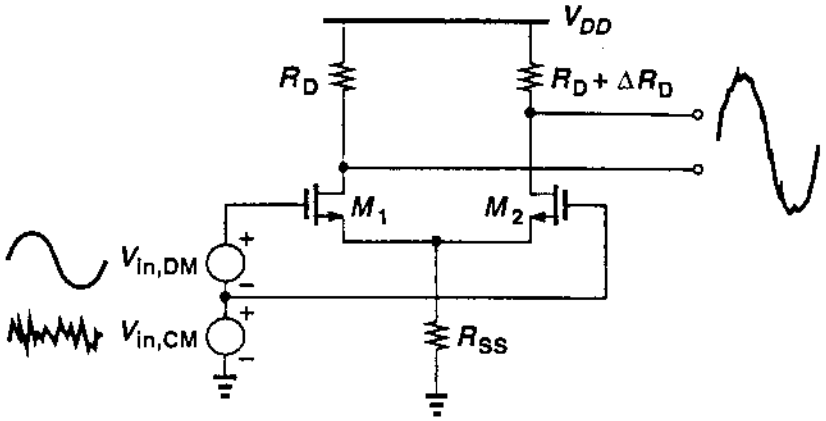


Figure 4.28 Effect of CM noise in the presence of resistor mismatch.

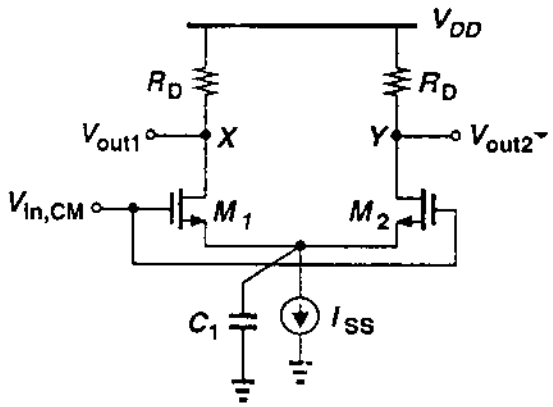


Figure 4.29 CM response with finite tail capacitance.

In summary, the common-mode response of differential pairs depends on the output impedance of the tail current source and asymmetries in the circuit, manifesting itself through two effects: variation of the output CM level (in the absence of mismatches) and conversion of input common-mode variations to differential components at the output. In analog circuits, the latter effect is much more severe than the former. For this reason, the common-mode response should usually be studied with mismatches taken into account.

How significant is common-mode to differential conversion? We make two observations. First, as the *frequency* of the CM disturbance increases, the total capacitance shunting the tail current source introduces larger tail current variations. Thus, even if the output *resistance* of the current source is high, common-mode to differential conversion becomes significant at high frequencies. Shown in Fig. 4.29, this capacitance arises from the parasitics of the current source itself as well as the source-bulk junctions of M_1 and M_2. Second, the asymmetry in the circuit stems from both the load resistors and the input transistors, the latter contributing a typically much greater mismatch.

Let us now study the asymmetry resulting from mismatches between M_1 and M_2 in Fig. 4.30(a). Owing to dimension and threshold voltage mismatches, the two transistors

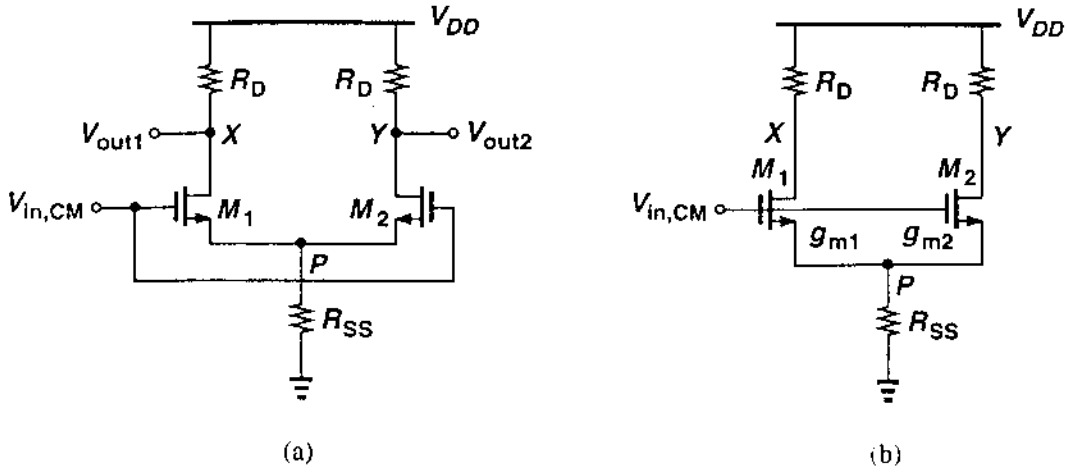


Figure 4.30 (a) Differential pair sensing CM input, (b) equivalent circuit of (a).

carry slightly different currents and exhibit unequal transconductances. To calculate the gain from $V_{in,CM}$ to X and Y, we use the equivalent circuit in Fig. 4.30(b), writing $I_{D1} = g_{m1}(V_{in,CM} - V_P)$ and $I_{D2} = g_{m2}(V_{in,CM} - V_P)$. That is,

$$(g_{m1} + g_{m2})(V_{in,CM} - V_P)R_{SS} = V_P, \tag{4.36}$$

and

$$V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM}. \tag{4.37}$$

We now obtain the output voltages as

$$V_X = -g_{m1}(V_{in,CM} - V_P)R_D \tag{4.38}$$

$$= \frac{-g_{m1}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} \tag{4.39}$$

and

$$V_Y = -g_{m2}(V_{in,CM} - V_P)R_D \tag{4.40}$$

$$= \frac{-g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM}. \tag{4.41}$$

The differential component at the output is therefore given by

$$V_X - V_Y = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM}. \tag{4.42}$$

In other words, the circuit converts input CM variations to a differential error by a factor

equal to

$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1} + g_{m2})R_{SS} + 1}, \tag{4.43}$$

where A_{CM-DM} denotes common-mode to differential-mode conversion and $\Delta g_m = g_{m1} - g_{m2}$.

Example 4.7

Two differential pairs are cascaded as shown in Fig. 4.31. Transistors M_3 and M_4 suffer from a g_m

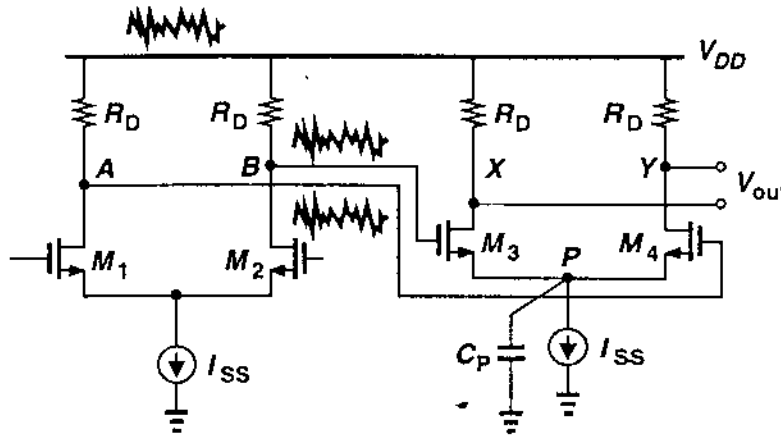


Figure 4.31

mismatch of Δg_m, the total parasitic capacitance at node P is represented by C_P, and the circuit is otherwise symmetric. What fraction of the supply noise appears as a differential component at the output? Assume $\lambda = \gamma = 0$.

Solution

Neglecting the capacitance at nodes A and B, we note that the supply noise appears at these nodes with no attenuation. Substituting $1/(C_P s)$ for R_{SS} in (4.43) and taking the magnitude, we have

$$|A_{CM-DM}| = \frac{\Delta g_m R_D}{\sqrt{1 + (g_{m3} + g_{m4})^2 \left|\frac{1}{C_P \omega}\right|^2}}. \tag{4.44}$$

The key point is that the effect becomes more noticeable as the supply noise frequency, ω, increases.

For meaningful comparison of differential circuits, the undesirable differential component produced by CM variations must be normalized to the wanted differential output resulting from amplification. We define the "common-mode rejection ratio" (CMRR) as

$$CMRR = \left|\frac{A_{DM}}{A_{CM-DM}}\right|. \tag{4.45}$$

If only g_m mismatch is considered, the reader can show from the analysis of Fig. 4.15 that

$$|A_{DM}| = \frac{R_D}{2}\frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}}. \tag{4.46}$$

where it is assumed $V_{in1} = -V_{in2}$, and hence

$$CMRR = \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m} \tag{4.47}$$

$$\approx \frac{g_m}{\Delta g_m}(1 + 2g_m R_{SS}), \tag{4.48}$$

where g_m denotes the mean value, i.e., $g_m = (g_{m1} + g_{m2})/2$. In practice, all mismatches must be taken into account.

4.4 Differential Pair with MOS Loads

The load of a differential pair need not be implemented by linear resistors. As with the common-source stages studied in Chapter 3, differential pairs can employ diode-connected or current-source loads (Fig. 4.32). The small-signal differential gain can be derived using

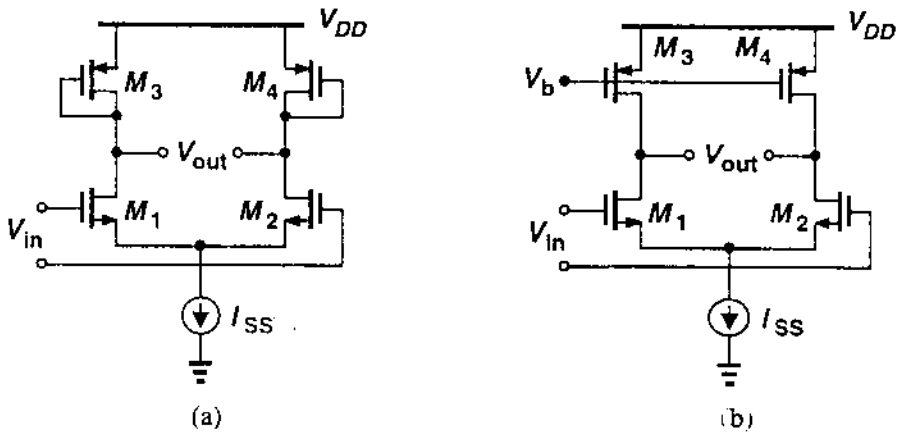


Figure 4.32 Differential pair with (a) diode-connected and (b) current-source loads.

the half-circuit concept. For Fig. 4.32(a),

$$A_v = -g_{mN}\left(g_{mP}^{-1} \| r_{ON} \| r_{OP}\right) \tag{4.49}$$

$$\approx -\frac{g_{mN}}{g_{mP}}. \tag{4.50}$$

where subscripts N and P denote NMOS and PMOS, respectively. Expressing g_{mN} and g_{mP} in terms of device dimensions, we have

$$A_v \approx -\sqrt{\frac{\mu_n(W/L)_N}{\mu_p(W/L)_P}}. \tag{4.51}$$

For Fig. 4.32(b), we have

$$A_v = -g_{mN}(r_{ON} \| r_{OP}). \tag{4.52}$$

In the circuit of Fig. 4.32(a), the diode-connected loads consume voltage headroom, thus creating a trade-off between the output voltage swings, the voltage gain, and the input CM range. Recall from Eq. (3.35) that, for given bias current and input device dimensions, the circuit's gain and the PMOS overdrive voltage scale together. To achieve a higher gain, $(W/L)_P$ must decrease, thereby increasing $|V_{GSP} - V_{THP}|$ and lowering the CM level at nodes X and Y.

In order to alleviate the above difficulty, part of the bias currents of the input transistors can be provided by PMOS current sources. Illustrated in Fig. 4.33, the idea is to lower the g_m of the load devices by reducing their current rather than their aspect ratio. For example,

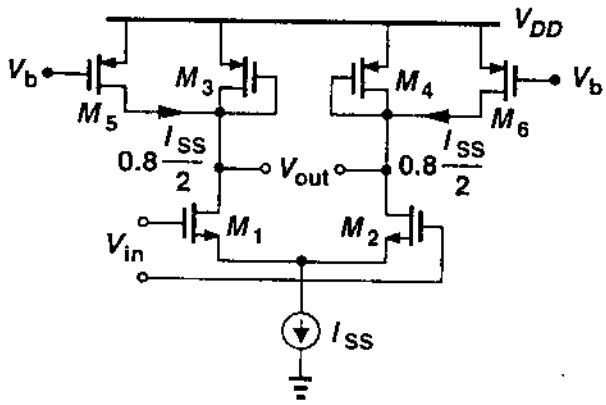


Figure 4.33 Addition of current sources to increase the voltage gain.

if M_5 and M_6 carry 80% of the drain current of M_1 and M_2, the current through M_3 and M_4 is reduced by a factor of five. For a given $|V_{GSP} - V_{THP}|$, this translates to a factor of five reduction in the transconductance of M_3 and M_4 because the aspect ratio of the devices can be lowered by the same factor. Thus, the differential gain is now approximately five times that of the case with no PMOS current sources.

The small-signal gain of the differential pair with current-source loads is relatively low—in the range of 10 to 20 in submicron technologies. How do we increase the voltage gain? Borrowing ideas from the amplifiers in Chapter 3, we increase the output impedance of both PMOS and NMOS devices by cascoding, in essence creating a differential version of the cascode stage introduced in Chapter 3. The result is depicted in Fig. 4.34(a). To calculate the gain, we construct the half circuit of Fig. 4.34(b), which is similar to the cascode stage of Fig. 3.60. Thus,

$$|A_v| \approx g_{m1}[(g_{m3}r_{O3}r_{O1}) \| (g_{m5}r_{O5}r_{O7})]. \tag{4.53}$$

Cascoding therefore increases the differential gain substantially but at the cost of consuming more voltage headroom.

As a final note, we should mention that high-gain fully differential amplifiers require a means of defining the output common-mode level. For example, in Fig. 4.32(b), the output

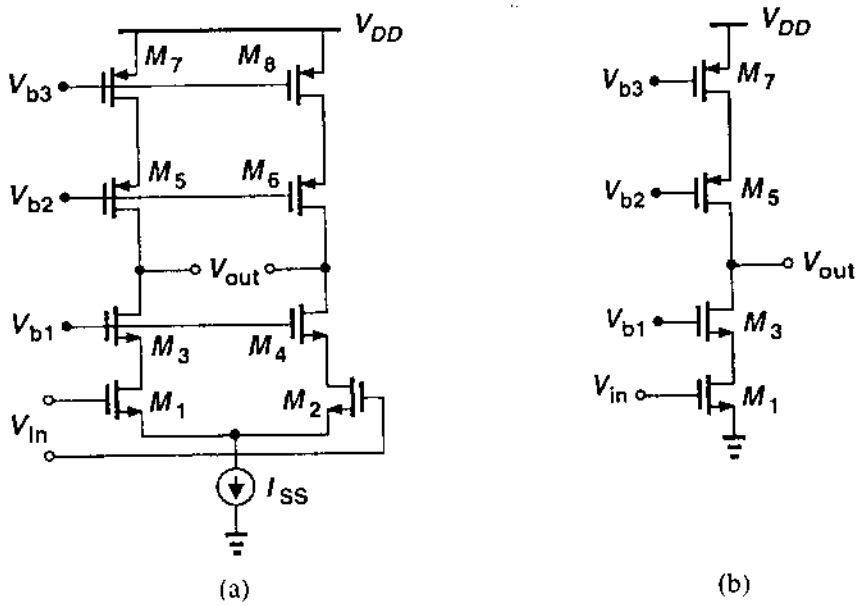


Figure 4.34 (a) Cascode differential pair, (b) half circuit of (a).

common-mode level is not well-defined whereas in Fig. 4.32(a), diode-connected transistors define the output CM level as $V_{DD} - V_{GSP}$. We return to this issue in Chapter 9.

4.5 Gilbert Cell

Our study of differential pairs reveals two important aspects of their operation: (1) the small-signal gain of the circuit is a function of the tail current and (2) the two transistors in a differential pair provide a simple means of steering the tail current to one of two destinations. By combining these two properties, we can develop a versatile building block.

Suppose we wish to construct a differential pair whose gain is varied by a control voltage. This can be accomplished as depicted in Fig. 4.35(a), where the control voltage defines the

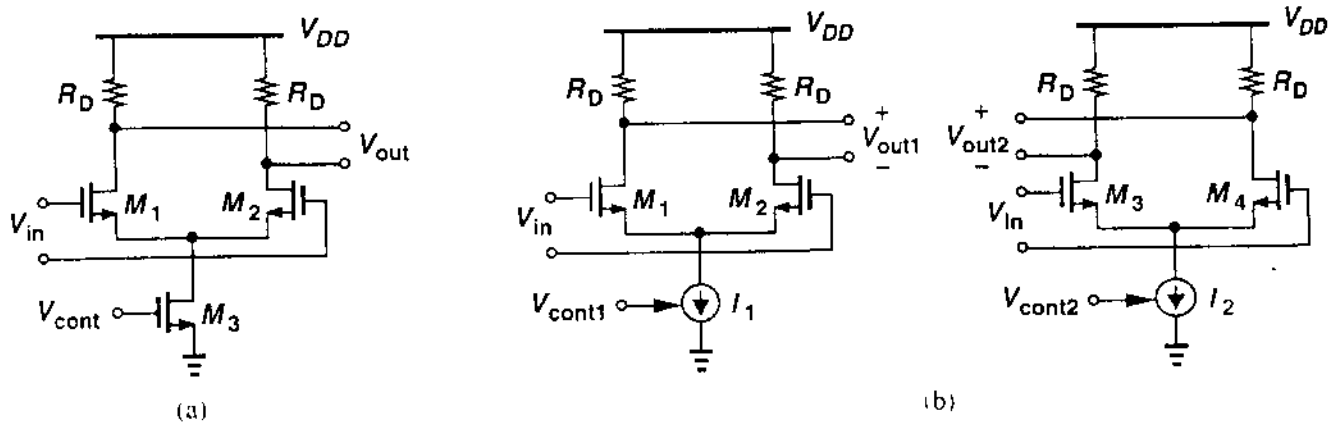


Figure 4.35 (a) Simple VGA, (b) two stages providing variable gain.

Chapter 5

Passive and Active Current Mirrors

Our study of single-stage and differential amplifiers in Chapters 3 and 4 points to the wide usage of current sources. In these circuits current sources act as a large resistor without consuming excessive voltage headroom. We also noted that MOS devices operating in saturation can act as a current source.

Current sources find other applications in analog design as well. For example, some digital-to-analog (D/A) converters employ an array of current sources to produce an analog output proportional to the digital input. Also, current sources, in conjunction with "current mirrors," can perform useful functions on analog signals.

This chapter deals with the design of current mirrors as both bias elements and signal processing components. Following a review of basic current mirrors, we study cascode mirror operation. Next, we analyze active current mirrors and describe the properties of differential pairs using such circuits as loads.

5.1 Basic Current Mirrors

Fig. 5.1 illustrates two examples where a current source proves useful. From our study in Chapter 2, recall that the output resistance and capacitance and the voltage headroom of a current source trade with the magnitude of the output current. In addition to these issues, several other aspects of current sources are important: supply, process, and temperature dependence, output noise current, and matching with other current sources. We postpone noise and matching considerations to Chapters 7 and 13, respectively.

How should a MOSFET be biased so as to operate as a stable current source? To gain a better view of the issues, let us consider the simple resistive biasing shown in Fig. 5.2. Assuming M_1 is in saturation, we can write

$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD}-V_{TH}\right)^2. \tag{5.1}$$

This expression reveals various dependencies of I_{out} upon the supply, process, and temperature. The overdrive voltage is a function of V_{DD} and V_{TH}: the threshold voltage may

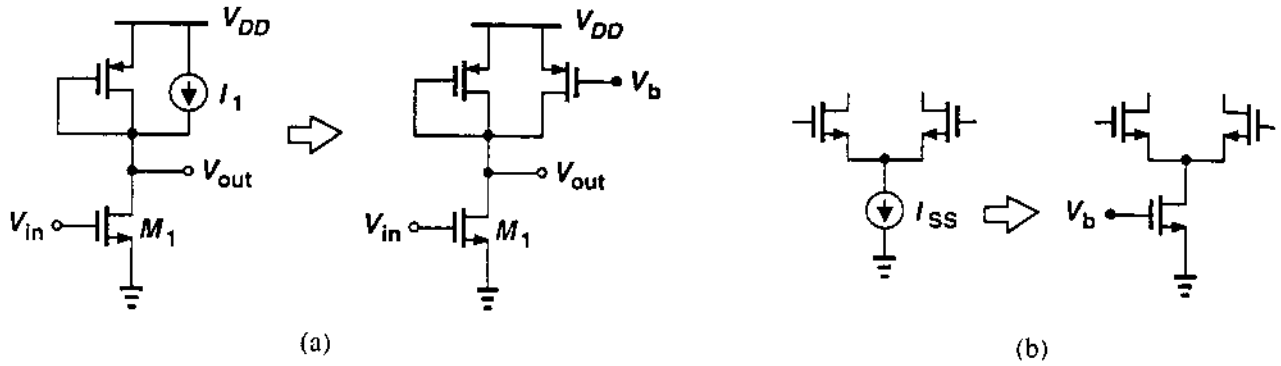


Figure 5.1 Applications of current sources.

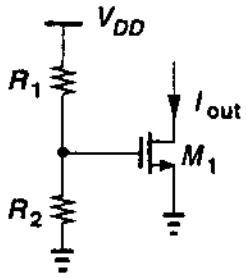


Figure 5.2 Definition of current by resistive divider.

vary by 100 mV from wafer to wafer. Furthermore, both μ_n and V_{TH} exhibit temperature dependence. Thus, I_{out} is poorly defined. The issue becomes more severe as the device is biased with a smaller overdrive voltage, e.g., to consume less headroom. With a nominal overdrive of, say, 200 mV, a 50-mV error in V_{TH} results in a 44% error in the output current.

It is important to note that the above process and temperature dependencies exist even if the gate voltage is not a function of the supply voltage. In other words, if the gate-source *voltage* of a MOSFET is precisely defined, then its drain *current* is not! For this reason, we must seek other methods of biasing MOS current sources.

The design of current sources in analog circuits is based on "copying" currents from a reference, with the assumption that *one* precisely-defined current source is already available. While this method may appear to entail an endless cycle, it is carried out as illustrated in Fig. 5.3. A relatively complex circuit—sometimes requiring external adjustments—is used

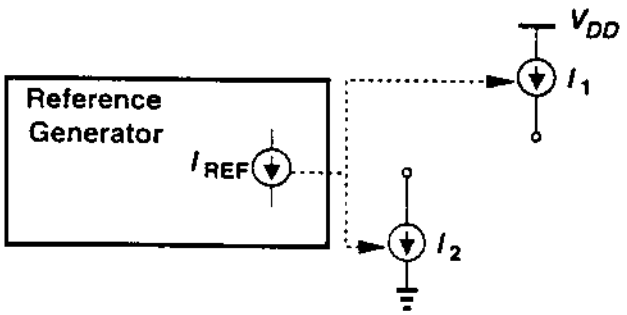


Figure 5.3 Use of a reference to generate various currents.

to generate a stable reference current, I_{REF}, which is then copied to many current sources in the system. We study the copying operation here and the reference generator circuit in Chapter 11.

How do we generate copies of a reference current? For example, in Fig. 5.4, how do we guarantee $I_{out} = I_{REF}$? For a MOSFET, if $I_D = f(V_{GS})$, where $f(\cdot)$ denotes the

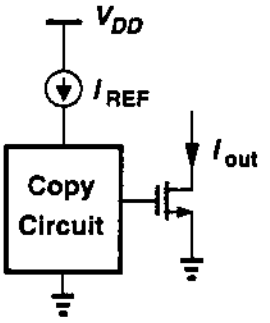


Figure 5.4 Conceptual means of copying currents.

functionality of I_D versus V_{GS}, then $V_{GS} = f^{-1}(I_D)$. That is, if a transistor is biased at I_{REF}, then it produces $V_{GS} = f^{-1}(I_{REF})$ [Fig. 5.5(a)]. Thus, if this voltage is applied to the gate and source terminals of a second MOSFET, the resulting current is $I_{out} = ff^{-1}(I_{REF}) = I_{REF}$ [Fig. 5.5(b)]. From another point of view, two identical MOS devices that have equal gate-source voltages and operate in saturation carry equal currents (if $\lambda = 0$).

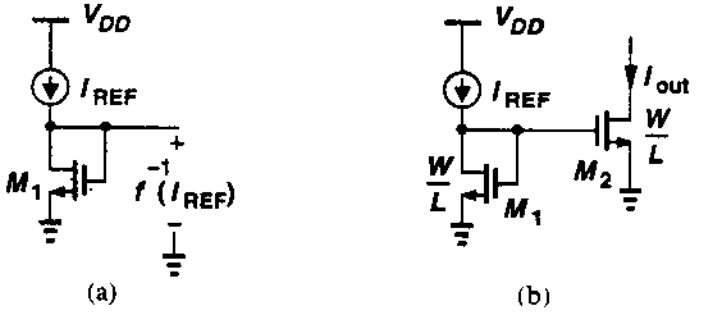


Figure 5.5 (a) Diode-connected device providing inverse function, (b) basic current mirror.

The structure consisting of M_1 and M_2 in Fig. 5.5(b) is called a "current mirror." In the general case, the devices need not be identical. Neglecting channel-length modulation, we can write

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 \tag{5.2}$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2, \tag{5.3}$$

obtaining

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}. \tag{5.4}$$

The key property of this topology is that it allows precise copying of the current with no dependence on process and temperature. The ratio of I_{out} and I_{REF} is given by the *ratio* of device dimensions, a quantity that can be controlled with reasonable accuracy.

Example 5.1

In Fig. 5.6, find the drain current of M_4 if all of the transistors are in saturation.

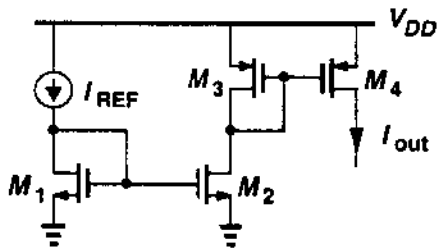


Figure 5.6

Solution

We have $I_{D2} = I_{REF}[(W/L)_2/(W/L)_1]$. Also, $|I_{D3}| = |I_{D2}|$ and $I_{D4} = I_{D3}[(W/L)_4/(W/L)_3]$. Thus, $|I_{D4}| = \alpha\beta I_{REF}$, where $\alpha = (W/L)_2/(W/L)_1$ and $\beta = (W/L)_4/(W/L)_3$. Proper choice of α and β can establish large or small ratios between I_{D4} and I_{REF}. For example, $\alpha = \beta = 5$ yields a magnification factor of 25. Similarly, $\alpha = \beta = 0.2$ can be utilized to generate a small, well-defined current.

Current mirrors find wide application in analog circuits. Fig. 5.7 illustrates a typical case, where a differential pair is biased by means of an NMOS mirror for the tail current source and a PMOS mirror for the load current sources. The device dimensions shown establish a

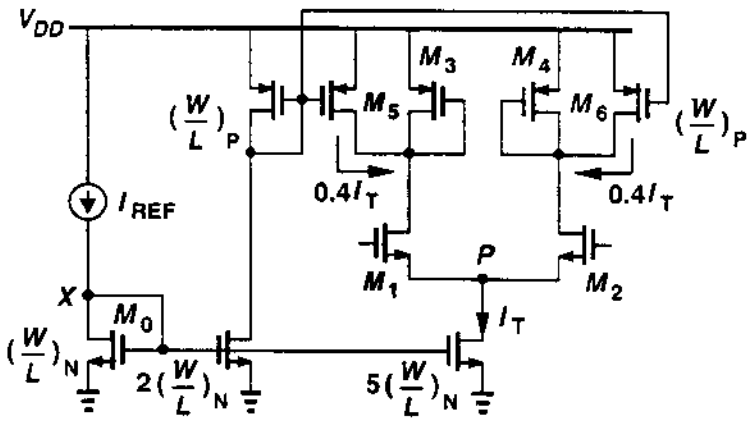


Figure 5.7 Current mirrors used to bias a differential amplifier.

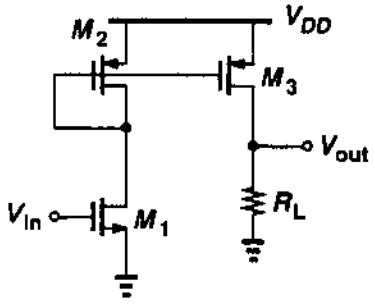
drain current of $0.4I_T$ in M_5 and M_6, reducing the drain current of M_3 and M_4 and hence increasing the gain.

Current mirrors usually employ the same *length* for all of the transistors so as to minimize errors due to the side-diffusion of the source and drain areas (L_D). For example, in Fig. 5.7, the NMOS current sources must have the same channel length as M_0. This is because if L_{drawn} is, say, doubled, then $L_{eff} = L_{drawn} - 2L_D$ is not. Furthermore, the threshold voltage of short-channel devices exhibits some dependence on the channel length (Chapter 16). Thus, current ratioing is achieved by only scaling the width of transistors.[1]

We should also mention that current mirrors can process *signals* as well. In Fig. 5.5(b), for example, if I_{REF} increases by ΔI, then I_{out} increases by $\Delta I(W/L)_2/(W/L)_1$. That is, the circuit *amplifies* the small-signal current if $(W/L)_2/(W/L)_1 > 1$ (but at the cost of proportional multiplication of the bias current).

Example 5.2

Calculate the small-signal voltage gain of the circuit shown in Fig. 5.8.



Figur

Solution

The small-signal drain current of M_1 is equal to $g_{m1}V_{in}$. Si
$(W/L)_2$, the small-signal drain current of M_3 is equal to
gain of $g_{m1}R_L(W/L)_3/(W/L)_2$.

5.2 Cascode Current Mirrors

In our discussion of current mirrors th
In practice, this effect results in signi
length transistors are used so as to
the current source. For the simp

$$I_{D1} =$$

[1] As explained in Ch
rather than making a

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(5.9)

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V_{GS} = headroom. For simplicity,
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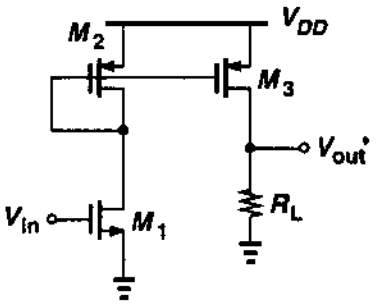

Figure 5.8

Solution

The small-signal drain current of M_1 is equal to $g_{m1}V_{in}$. Since $I_{D2} = I_{D1}$ and $I_{D3} = I_{D2}(W/L)_3/(W/L)_2$, the small-signal drain current of M_3 is equal to $g_{m1}V_{in}(W/L)_3/(W/L)_2$, yielding a voltage gain of $g_{m1}R_L(W/L)_3/(W/L)_2$.

5.2 Cascode Current Mirrors

In our discussion of current mirrors thus far, we have neglected channel length modulation. In practice, this effect results in significant error in copying currents, especially if minimum-length transistors are used so as to minimize the width and hence the output capacitance of the current source. For the simple mirror of Fig. 5.5(b), we can write

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1}) \tag{5.5}$$

[1] As explained in Chapter 18, the widths are actually scaled by placing multiple unit transistors in parallel rather than making a device wider.