Single Ended and differential operation.

⇒ Single ended signal → defined ~~as one~~ that " signal is measured with respect to a fixed potential usually the ground.

⇒ differential signal → defined that the signal measured b/w two nodes that have equal and opposite signal excursion around a fixed potential.

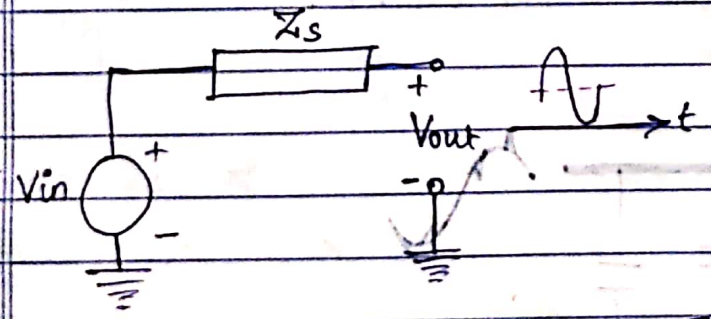
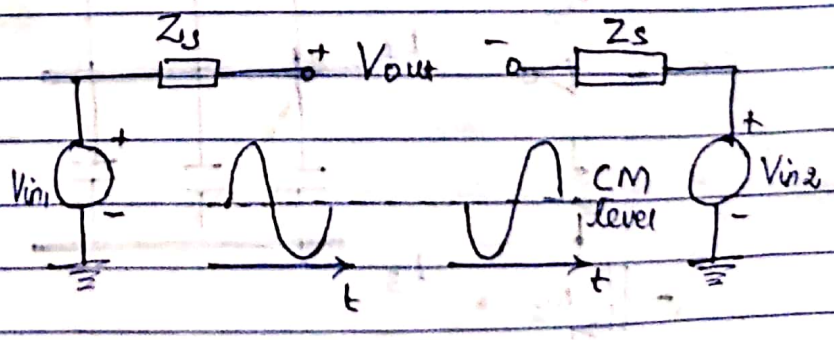


fig: single-ended



⇒ The 'center' potential in differential signaling is called the common-mode (CM) level.

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Advantages of differential operation: over single ended

(1) higher immunity to environmental noise:-

* First example:

(How to employing differential Path for sensitive signals)

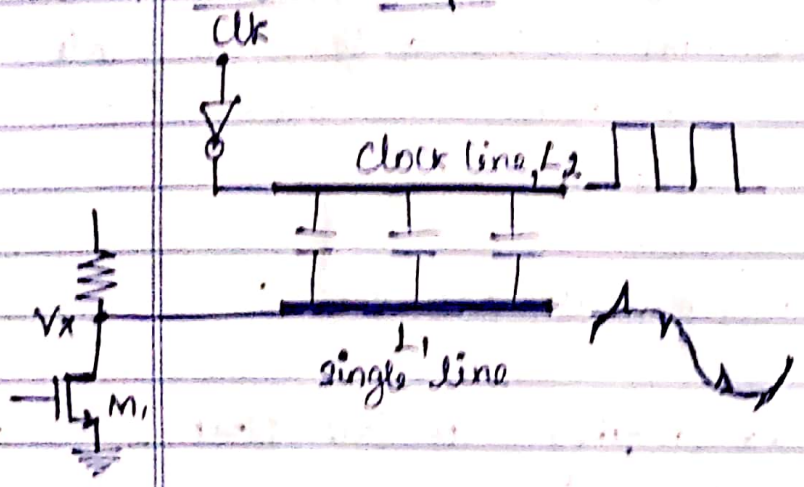

Fig: Corruption of a signal due to Coupling.

→ In digital, two adjacent lines in a circuit, carry a small, sensitive signal and clock waveform (large)
⇒ due to capacitive coupling b/w the lines, transition on line L2, corrupt the signal on L1.

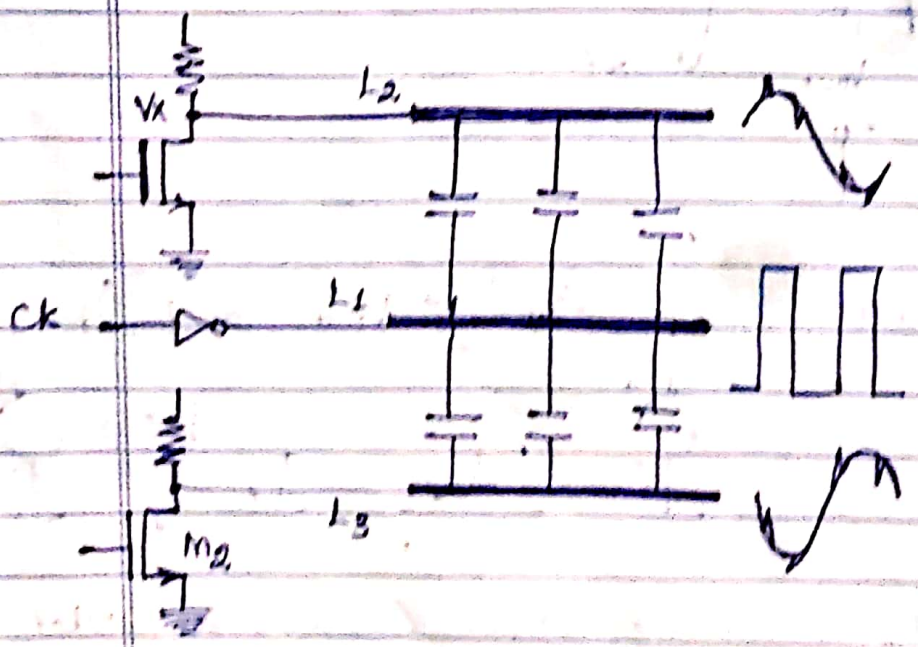

Fig: reduction of coupling by differential operation.

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⇒ Now consider the sensitive signal is distributed as two equal and opposite phases.

⇒ If the clk signal line is placed midway b/w the two, the transitions disturb the differential phases by equal amounts, leaving the difference intact.

⇒ Since, the common mode level of two ~~signal~~ phases is disturbed but the differential output is not corrupted. This arrangement rejects noise (common-mode noise)

* Second example: (differential path for sensitive signal)

⇒ Common mode rejection occurs with noisy supply voltages.

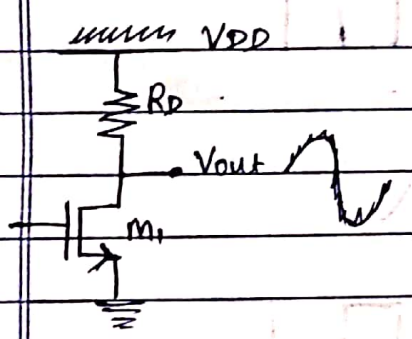

Fig: Effect of noise in single ended circuit

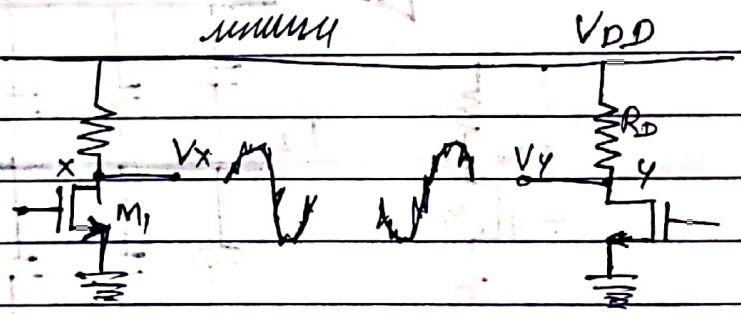

Fig: Effect of noise in differential circuit.

⇒ If VDD varies with ΔV_D, the Vout changes almost the same amount (i.e) output voltage affects with the same amount of noise available in VDD

⇒ If circuit is symmetric, noise on VDD affects Vx and Vy.

⇒ but not $V_{out} = V_x - V_y$.

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* Third example: (to employ differential distribution for noisy lines).

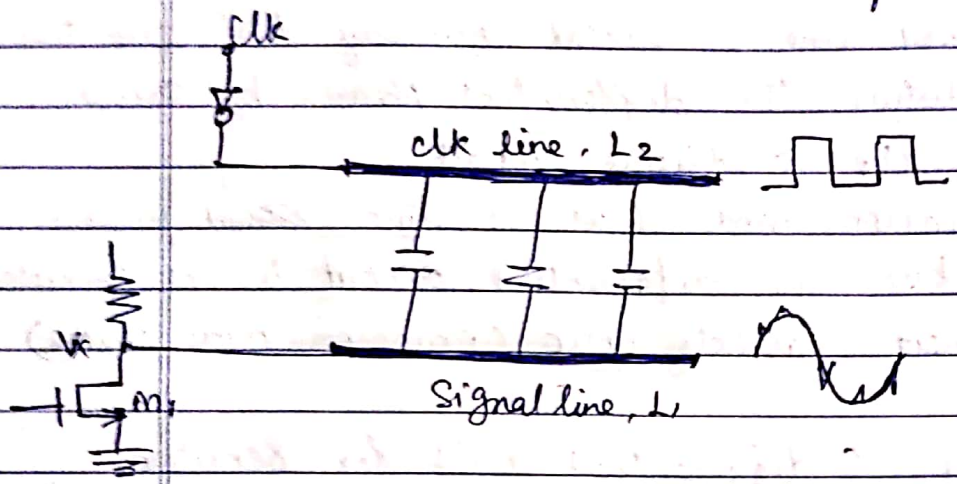

Fig: Corruption of a signal due to coupling.

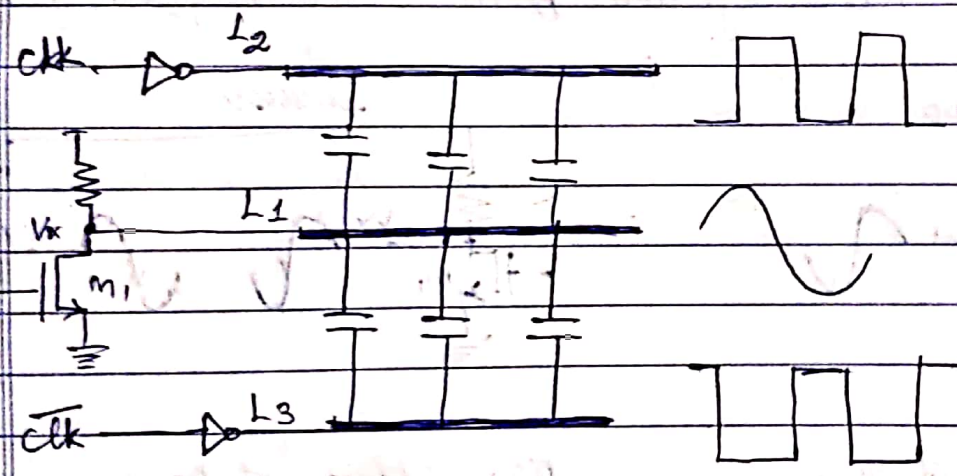

Fig: Reduction of coupling noise by differential operation.

=> If the clock signal is distributed by differential form on two lines (L_2 & L_3), then with perfect symmetry, the components coupled from clk and $\overline{clk}$ to the signal line (L_1) cancel each other.

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(2) increase in maximum achievable voltage swings.

⇒ In the second example of employing differential distribution in supply voltages,

* The maximum output swing at X or Y is equal to $V_{DD} - (V_{GS} - V_t)$.

* where as for $V_X - V_Y$ the peak to peak swing is equal to $2[V_{DD} - (V_{GS} - V_t)]$.

(3) include simpler biasing and higher linearity.

Disadvantages of differential operation

① ⇒ circuit occupy twice as much area as single ended.

The suppression of non ideal effects by differential operation makes this as minor disadvantage/drawback.

Basic Differential Pair:

How do we amplify a differential signal?

⇒ To process two phases, we may include two identical single-ended signal paths.

* It has advantages as: high rejection of supply noise, higher output swings.

* But, if the common-mode disturbance is large for V_{in1} & V_{in2} (or) i/p cm level is not well defined then,

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⇒ The bias ct of M_1 & M_2 also changes.
⇒ g_m of the devices varies
⇒ finally the o/p cm level also varies.

* The g_m value variation leads to a change in the small-signal gain.

Example:

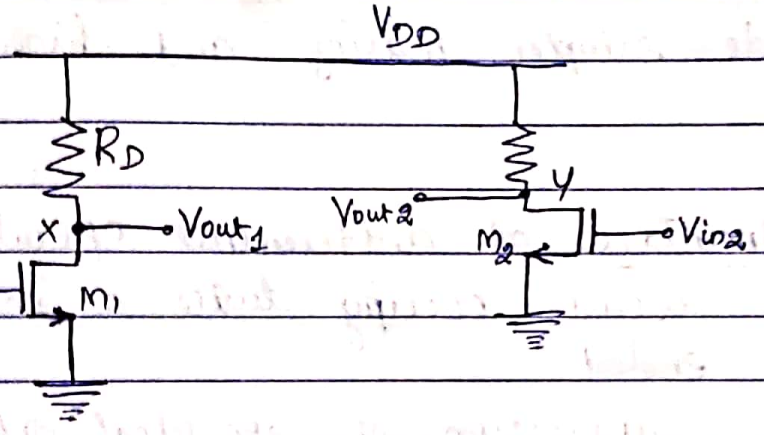

Fig (a) simple differential circuit

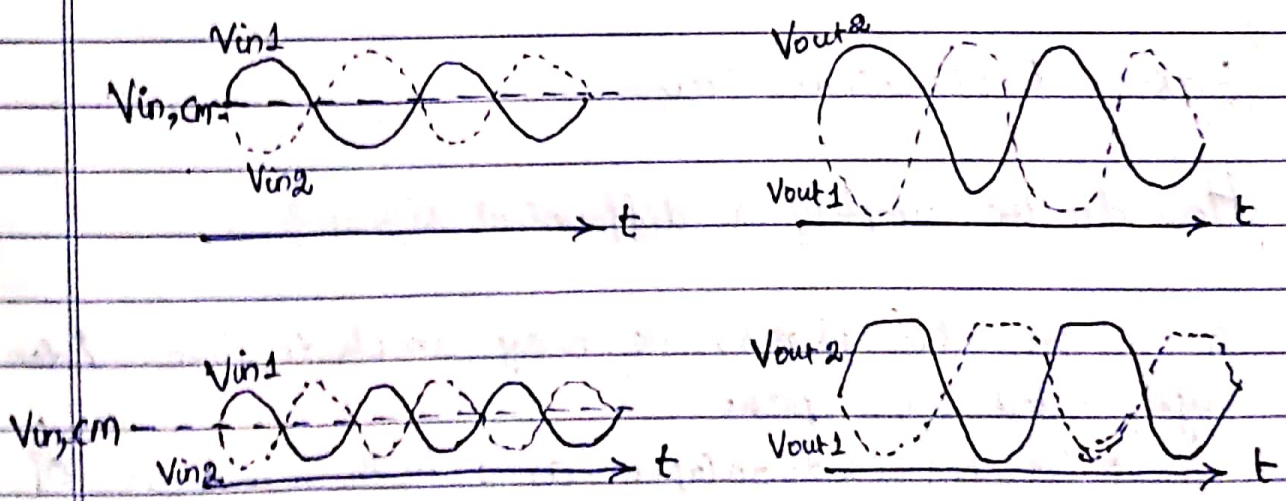

fig (b) illustration of sensitivity to the input common-mode level

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Fig b: if the i/p cm level is excessively low, the minmum value of ~~M1 & M2~~ Vin1 & Vin2 may turn off M1 & M2 → leading to cliping in the o/p signal.

⇒ Thus, it is important that the bias current of the device should have minimal dependence on the i/p cm level.

⇒ A simple modification can resolve the above issue.
* The differential pair employs a current source Iss to make $I_{D1}+I_{D2}$ independent of Vin,cm. Thus, if Vin1 = Vin2, the bias current of each transistor equals Iss/2 and the o/p cm level is $V_{DD} - R_D I_{SS}/2$.

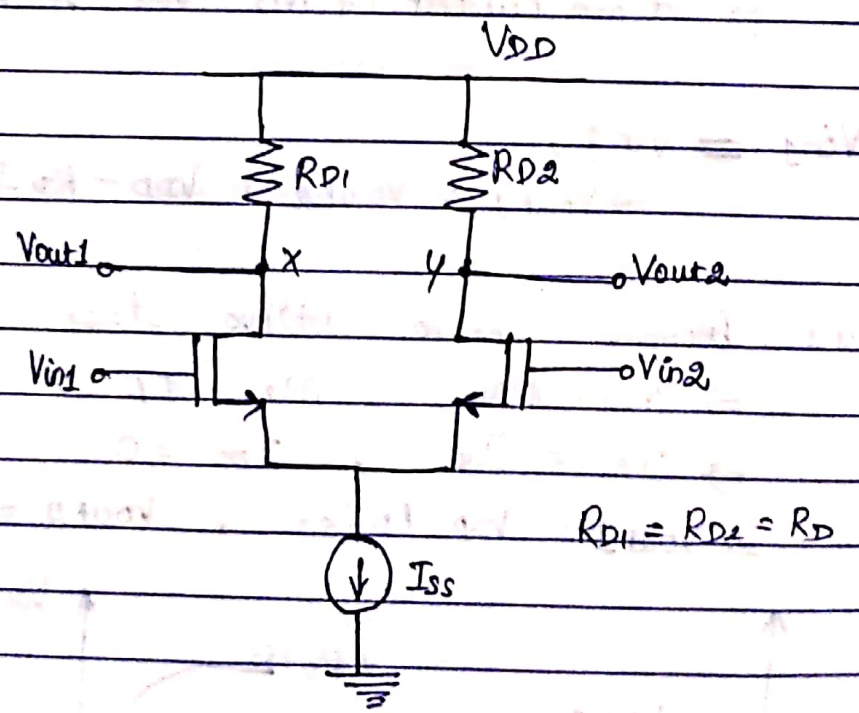

fig: Basic differential Pair.

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(1) Qualitative Analysis:

Differential behaviour:-

→ Assume $V_{in1} - V_{in2}$ varies from $-\infty$ to $+\infty$.

* if V_{in1} is much more (−)ive than V_{in2},
  - ⇒ M_1 – OFF & M_2 – ON
  - ⇒ $I_{D1} = 0$, $I_{D2} = I_{SS}$
  - ⇒ $V_{out1} = V_{DD}$, $V_{out2} = V_{DD} - R_D I_{SS}$.

* V_{in1} is brought closer to V_{in2}.
  - ⇒ M_1 – ON (gradually turn ON)
  - ⇒ drawing a fraction of I_{SS} from R_{D1}
  - ⇒ lowering V_{out1}.
  - ⇒ $I_{D1} + I_{D2} = I_{SS}$.
  - ⇒ drain current of M_2 ↓es & V_{out2} ↑es.

* $V_{in1} = V_{in2}$,
  - ⇒ $V_{out1} = V_{out2} = V_{DD} - R_D I_{SS}/2$

* V_{in1} become more (+)ive than V_{in2}.
  - ⇒ M_1 – ON, M_2 – OFF
  - ⇒ $I_{D1} = I_{SS}$, $I_{D2} = 0$
  - ⇒ $V_{out1} = V_{DD} - R_D I_{SS}$, $V_{out2} = V_{DD}$

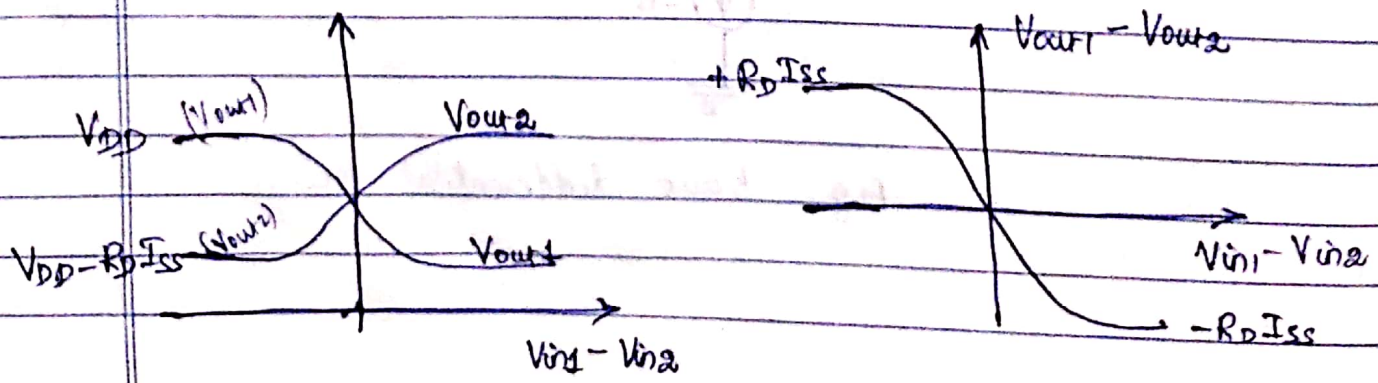

Fig: input – output characteristics of a differential Pair

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⇒ Based on analysis, (two important attributes of the differential pair)

(i) The maximum and minimum levels at the o/p are well defined (V_{DD} and $V_{DD} - R_D I_{SS}$ respectively), and independent of $V_{in,cm}$ level.

(ii) Small signal gain (the slope of $V_{out1} - V_{out2}$ vs $V_{in1} - V_{in2}$) is maximum for $V_{in1} = V_{in2}$, and gradually falling to zero as $|V_{in1} - V_{in2}| \uparrow$es. for $V_{in1} = V_{in2}$ → circuit is in equilibrium.

⇒ Common-mode behavior of the circuit :

* The role of tail current source is to suppress the effect of input cm level variations on the operation of M_1 and M_2 and the output level.

* The $V_{in,cm}$ can set as, $V_{in1} = V_{in2} = V_{in,cm}$ and vary $V_{in,cm}$ from 0 to V_{DD}. Fig. shows the circuit with I_{SS} implemented by an NFET. where $V_{out1} = V_{out2}$

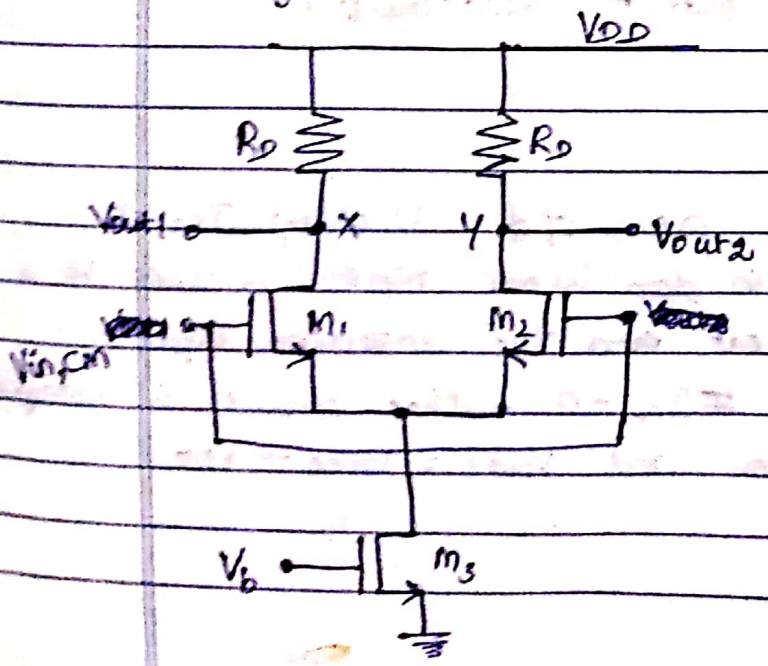

fig:1 differential pair sensing an input common-mode change.

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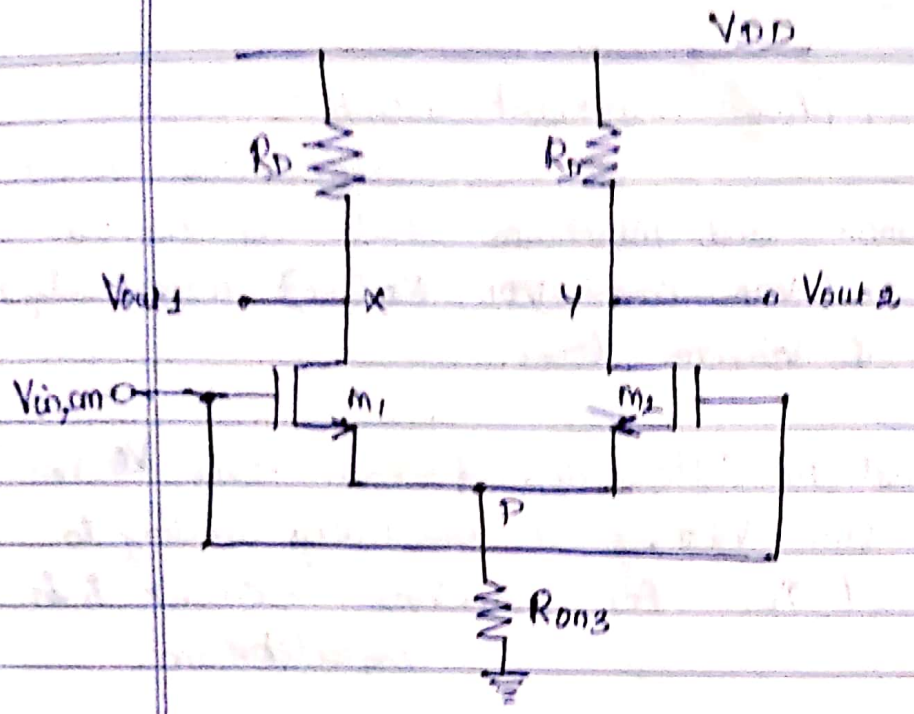

Fig: 2 equivalent circuit if M3 operates in deep triode region

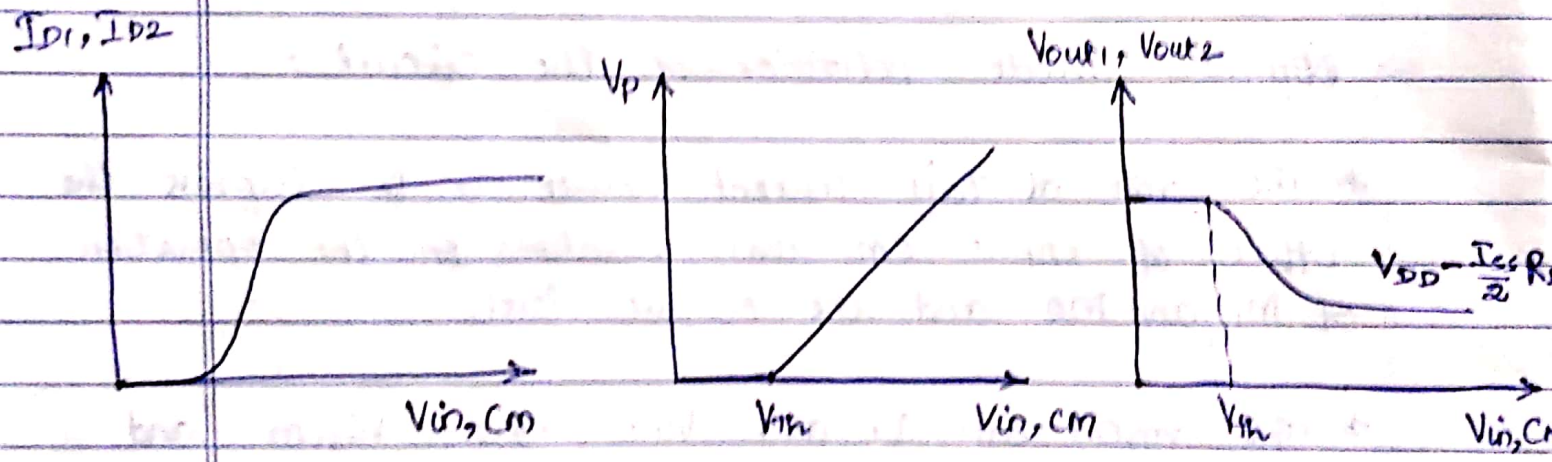

Fig: 3 input output characteristics.

* if $V_{in,cm} = 0$,
  - ⇒ M_1 & M_2 are off, yielding $I_{D3} = 0$
  - ⇒ M_3 is in deep triode region because V_b is high enough to create the inversion layer.
  - ⇒ with $I_{D1} = I_{D2} = 0$, the circuit is not capable of signal amplification and $V_{out1} = V_{out2} = V_{DD}$.

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* if $V_{in,cm}$ becomes more (+)ive.

⇒ modeling M_3 by a resistor shown in fig. 2 ~~and its operate in~~

⇒ M_1 & M_2 turns on if $V_{in,cm} \geq V_{th}$.

⇒ I_{D1} & I_{D2} continous to increase and V_P also rises shown in fig. 3.

⇒ (i.e) M_1 & M_2 constitute a source follower forcing V_P to track $V_{in,cm}$.

⇒ For sufficient high $V_{in,cm}$ the drain source voltage of M_3 (V_P) exceeds $V_{G3} - V_{th3}$, allowing the device to operate in saturation.

⇒ The total current through M_1 & M_2 then remains constant.

⇒ For proper operation, ~~$V_{in,cm} \geq V_{GS1}$~~

$$V_{in,cm} \geq V_{GS1} + (V_{GS3} - V_{th3})$$

* if $V_{in,cm}$ rises further,

⇒ M_1 & M_2 is in deep triode region if $V_{in,cm} > V_{out1} + V_{th} = V_{DD} - R_D I_{SS}/2 + V_{th}$

⇒ This sets the upper limit on the input cm level

⇒ The allowable value of $V_{in,cm}$ is bounded as,

$$V_{GS1} + (V_{GS3} - V_{th3}) \leq V_{in,cm} \leq \min\left[V_{DD} - R_D \frac{I_{SS}}{2} + V_{th}, V_{DD}\right]$$

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(1) How ~~large~~ large can the output voltage swings of a differential pair be?

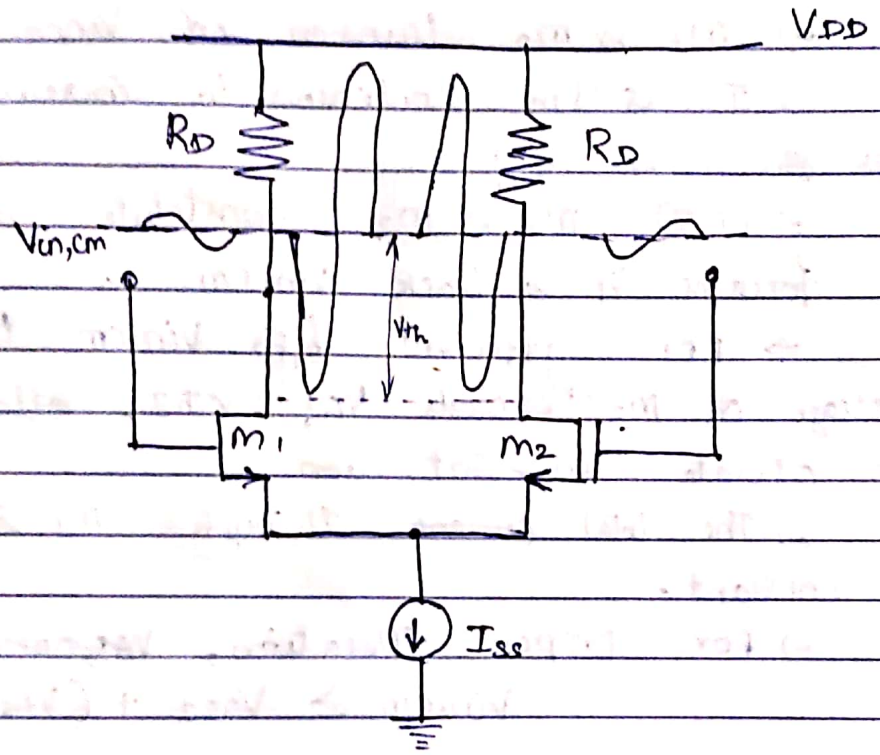


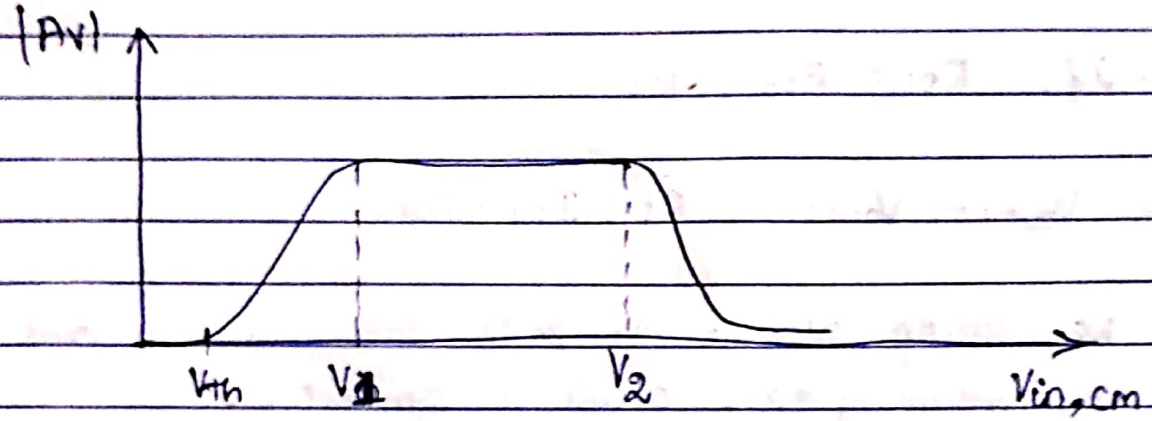
Fig: max. allowable output swings in a differential pair.

⇒ M_1 & M_2 to be saturated,
each o/p can go as high as V_{DD} but as low as approximately $V_{in,cm} - V_{Th}$.

Similar to common source stage,
⇒ The gain of the differential ~~amp~~ pair is a function of the dc drop across the load resistors.

* if $R_D I_{SS}/2$ is large, $V_{in,cm}$ must remain close to ground potential

(2) Sketch the small-signal differential gain of a differential pair as a function of the input cm level.



⇒ The gain begins to rise as Vin,cm exceeds Vth.
→ After the tail of source enters saturation, (Vin,cm = V1) the Av is constant.
→ if Vin,cm is so high, then i/p transistors enter the triode region (Vin,cm = V2), the gain begins to fall.

Quantitative Analysis:

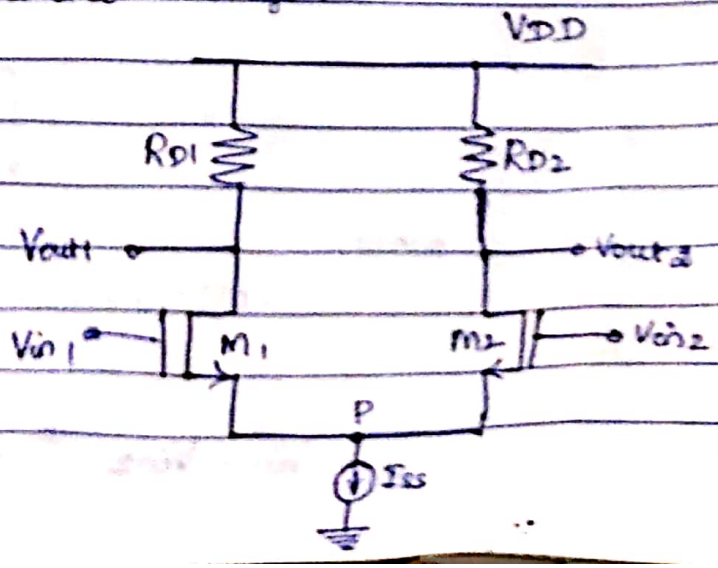
⇒ quantify the behavior of a MOS differential pair as a function of i/p differential voltage.

Large signal Analysis:

$V_{out1} = V_{DD} - R_{D1} I_{D1}$

$V_{out2} = V_{DD} - R_{D2} I_{D2}$

$V_{out} = V_{out1} - V_{out2}$



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$$= V_{DD} - R_{D1} I_{D1} - V_{DD} + R_{D2} I_{D2}$$

$$= R_{D2} I_{D2} - R_{D1} I_{D1}$$

If, $R_{D1} = R_{D2} = R_D$

$$V_{out1} - V_{out2} = R_D (I_{D2} - I_{D1})$$

⇒ We simply calculate I_{D1} & I_{D2} in terms of V_{in1} and V_{in2}, by assuming * the circuit is symmetric.

* M_1 & M_2 are saturated
* $\lambda = 0$

The voltage at P is equal to $V_{in1} - V_{GS1}$ & $V_{in2} - V_{GS2}$

$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}.$$

WKT,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$(V_{GS} - V_{th})^2 = \frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}$$

$$(V_{GS} - V_{th}) = \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}}$$

$$V_{GS} = \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}} + V_{th}$$

Now,

$$V_{in1} - V_{in2} = \sqrt{\frac{2 I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} + \cancel{V_{th}} - \sqrt{\frac{2 I_{D2}}{\mu_n C_{ox} \frac{W}{L}}} - \cancel{V_{th}}$$

$$\therefore V_{in1} - V_{in2} = \sqrt{\frac{2 I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2 I_{D2}}{\mu_n C_{ox} \frac{W}{L}}}$$

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Our objective is to calculate the output current, $I_{D1} - I_{D2}$.

squaring the above eqn,

$$(V_{in1} - V_{in2})^2 = \left[\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}\right]^2 \quad \left[\because (a-b)^2\right]$$

$$= \frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}} + \frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}} - 2\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}}\sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$= \frac{2}{\mu_n C_{ox}\frac{W}{L}}\left[\underbrace{I_{D1} + I_{D2}}_{I_{SS}} - 2\sqrt{I_{D1}I_{D2}}\right]$$

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}\left[I_{SS} - 2\sqrt{I_{D1}I_{D2}}\right]$$

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 = I_{SS} - 2\sqrt{I_{D1}I_{D2}}$$

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{D1}I_{D2}}$$

square both side again,

$$4I_{D1}I_{D2} = \frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2\right)^2 + I_{SS}^2 - 2 \cdot I_{SS} \cdot \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2$$

where,

$$4I_{D1}I_{D2} = (I_{D1} + I_{D2})^2 - (I_{D1} - I_{D2})^2$$

$$= I_{SS}^2 - (I_{D1} - I_{D2})^2$$

$I_{D1}^2 + I_{D2}^2 + 2I_{D1}I_{D2} - (I_{D1}^2 + I_{D2}^2 - 2I_{D1}I_{D2})$

$\downarrow$

$4I_{D1}I_{D2}$

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$$I_{SS}^2 - (I_{D1} - I_{D2})^2 = \frac{1}{4}\left(\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2\right)^2 + \cancel{I_{DS}^2} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 I_{SS}$$

$$(I_{D1} - I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2\right)^2 + \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 I_{SS}$$

$$(I_{D1} - I_{D2})^2 = \frac{1}{4}\left(\mu_n C_{ox} \frac{W}{L}\right)^2 (V_{in1} - V_{in2})^2 \left[(V_{in1} - V_{in2})^2 + \frac{4 I_{SS}}{\mu_n C_{ox} \frac{W}{L}}\right]$$

$$I_{D1} - I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2}) \sqrt{\frac{4 I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2} \quad \text{—— (1)}$$

* for $I_{D1} - I_{D2}$ is odd function
  $f(-x) = -f(x)$
  which leads $V_{in1} - V_{in2} = 0$
  $\therefore V_{in1} = V_{in2}$

* when $|V_{in1} - V_{in2}|$ ↑es from zero $\Rightarrow |I_{D1} - I_{D2}|$ ↑es

$\Rightarrow$ To calculate the slope of the characteristic (i.e) g_m of M_1 & M_2.

$$I_{D1} - I_{D2} = \Delta I_D \quad \& \quad V_{in1} - V_{in2} = \Delta V_{in}$$

$$\Delta I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \Delta V_{in} \sqrt{\frac{4 I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (\Delta V_{in})^2}$$

Partially differentiate wrt ΔV_{in}, $\quad (UV = UV' + U'V)$

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \Delta V_{in} \left(\frac{0 - \cancel{2} \Delta V_{in}}{\cancel{2}\sqrt{\frac{4 I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}\right) + \sqrt{\frac{4 I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - \Delta V_{in}^2} \left(\frac{1}{2} \mu_n C_{ox} \frac{W}{L}\right)$$

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$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[\frac{-\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}} + \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}\right]$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[\frac{-\Delta V_{in}^2 + \frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}\right]$$

$$g_m = \frac{\Delta I_D}{\Delta V_{in}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[\frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}\right]$$

for $\Delta V_{in} = 0$,

$$g_m = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L}} = \sqrt{\frac{\frac{1}{4}\mu_n^2 C_{ox}^2 \left(\frac{W}{L}\right)^2 4 I_{SS}}{\mu_n C_{ox} W/L}}$$

$$g_m = \sqrt{I_{SS}\mu_n C_{ox}\frac{W}{L}}$$

$$V_{out1} - V_{out2} = \Delta V_{out} = R_D \Delta I_D \Rightarrow \Delta I_D = \frac{\Delta V_{out}}{R_D}$$

$$\because g_m = \frac{\Delta I_D}{\Delta V_{in}} \rightarrow \Delta I_D = g_m \Delta V_{in}$$

$$\Delta V_{out} = g_m \Delta V_{in} R_D.$$

$$\frac{\Delta V_{out}}{\Delta V_{in}} = g_m R_D$$

$$\boxed{\therefore |A_v| = R_D\sqrt{I_{SS}\mu_n C_{ox} W/L}}$$

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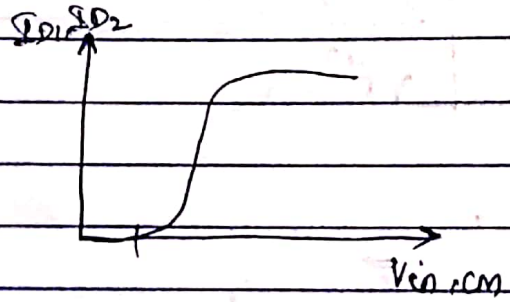
⇒ G_m falls to zero, for $\Delta V_{in} = \sqrt{\frac{2 I_{ss}}{\mu_n C_{ox} W/L}}$ (1)

⇒ ΔV_{in} plays an important role in the operation of the ckt.

⇒ $\sqrt{\frac{4 I_s}{\mu_n C_{ox} W/L}} (V_{in1} - V_{in2})^2 = 0$ for $\Delta V_{in} = \sqrt{\frac{4 I_{ss}}{\mu_n C_{ox} W/L}}$ (2)

⇒ (i.e) ΔI_D crosses zero at 2 different values of ΔV_{in}

How ever this ~~assumption~~ conclusion is not correct.
based on,



* To understand why, we calculated $(I_{D1} - I_{D2})$ (expr 1) with the assumption that both M_1 & M_2 are on.

⇒ But in reality, as ΔV_{in} exceeds a limit, one transistor carries the entire I_{ss} & turning off the other transistor.

⇒ ΔV_{in} ⇒ we have, $I_{D1} = I_{ss}$ & $\Delta V_{in1} = V_{gs1} - V_{th}$ } $M_1 \rightarrow$ ON
$M_2 \rightarrow$ off

$$\boxed{\Delta V_{in1} = \sqrt{\frac{2 I_{ss}}{\mu_n C_{ox} \frac{W}{L}}}}$$

* For $\Delta V_{in} > \Delta V_{in1}$, M_2 – off and we can't hold good $(I_{D1} - I_{D2})$ expression (expr. 1), $G_m \rightarrow 0$ for $\Delta V_{in} = \Delta V_{in1}$

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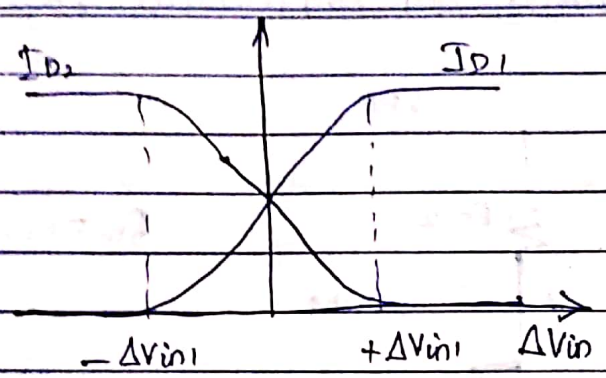

Fig: variation of drain current

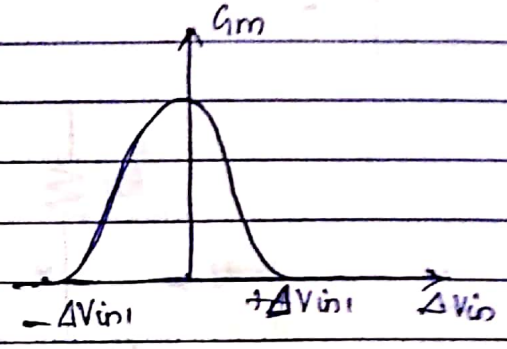

Fig: overall transconductance of differential pair vs i/p voltage.

* The ΔV_{in1} value (in the above expression) is the maximum differential i/p that the circuit can handle.

* It's possible to relate the ΔV_{in1} to overdrive voltage of M_1 & M_2 in equilibrium.

For zero differential i/p, $I_{D1} = I_{D2} = I_{SS}/2$

from page no: 4

$$(V_{GS} - V_{th})_{1,2} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

∴ Equilibrium overdrive V_t is equal to $\Delta V_{in1}/\sqrt{2}$

⇒ increasing ΔV_{in1} to make the circuit more linear

* inevitably ↑es the overdrive voltage of M_1 & M_2.
* For given I_{SS}, the above will be accomplished by reducing W/L.

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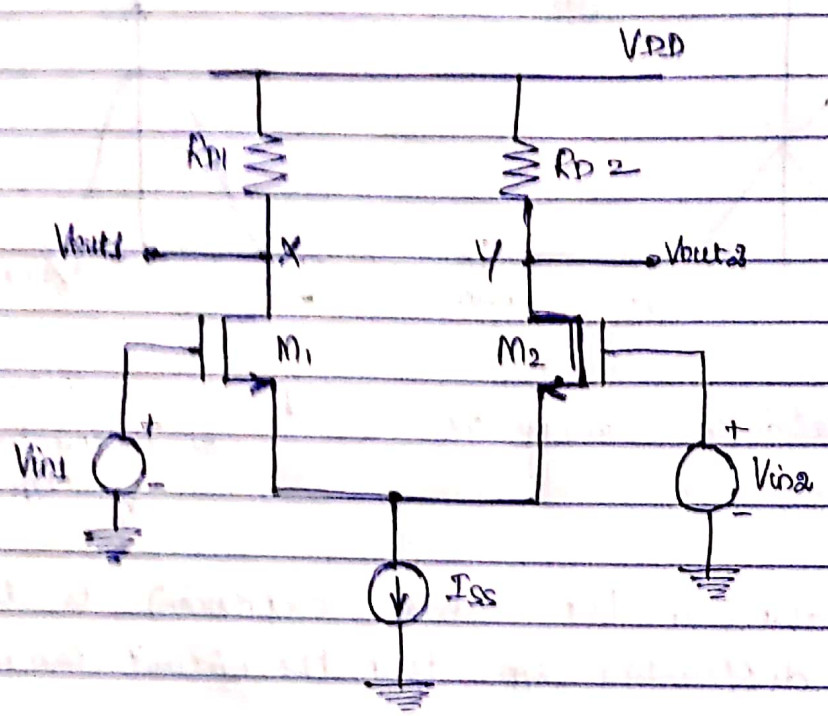
Small - signal behavior of differential pair:



$R_{D1} = R_{D2} = R_D$

Fig: Differential pair with small-signal inputs

⇒ V_{in1} & V_{in2} → small signals

⇒ M_1 & M_2 are saturated (Assumption)

⇒ differential gain, $A_v = \frac{V_{out}}{V_{in1} - V_{in2}}$

⇒ for large signal analysis, $|A_v| = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS} R_D}$

$$\frac{V_{out}}{V_{in1} - V_{in2}} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS} R_D}$$

⇒ at equilibrium, $g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$

$$A_v = g_m R_D.$$

⇒ To get same result in small signal analysis, two methods can employ.

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Method - I :

⇒ The circuit is driven by 2 independent signals.
* O/p can be computed by superposition.

⇒ $V_{in2} = 0$, and find the effect of V_{in1} at X and Y.

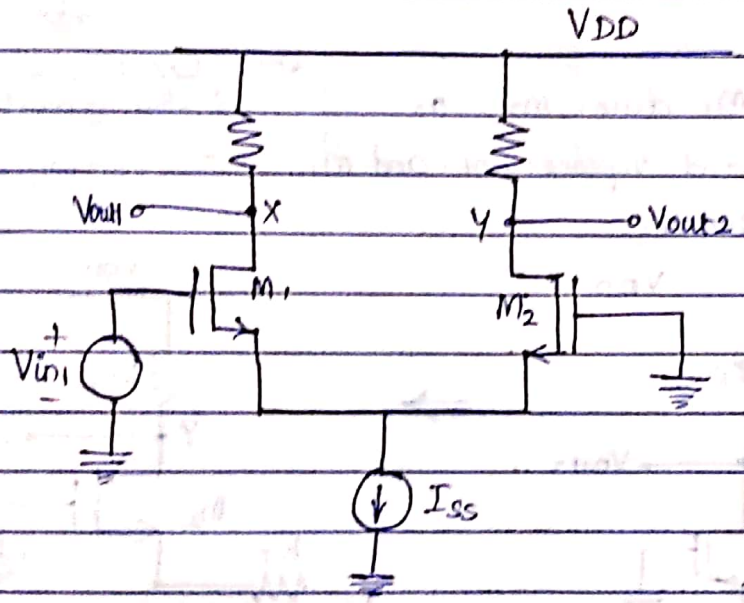

Fig: Differential Pair sensing one input signal

⇒ M_1 forms a common source stage with a degeneration resistance
* Resistance equal to the impedance of source of M_2.

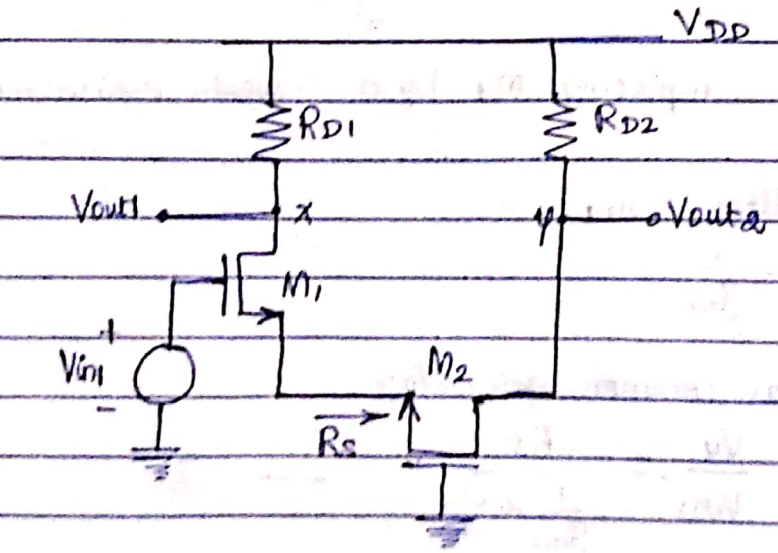

Fig: circuit viewed as a CS stage degenerated by M_2.

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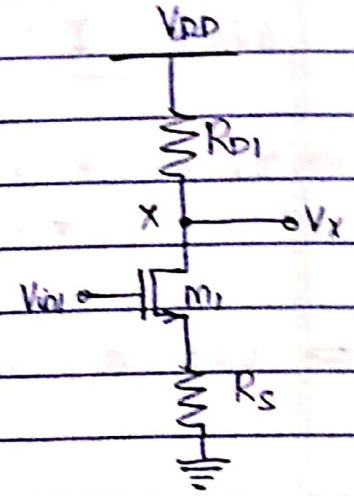
⇒ neglecting the λ and body effect,

$$R_S = \frac{1}{g_{m2}}$$

$$\text{gain} = \frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \quad \text{—— (1)}$$



equivalent circuit of CS stage generated by M2.

⇒ To calculate V_Y, M_1 drives M_2 as a source follower and replace V_{in1} and M_1 by a Thevenin equivalent.

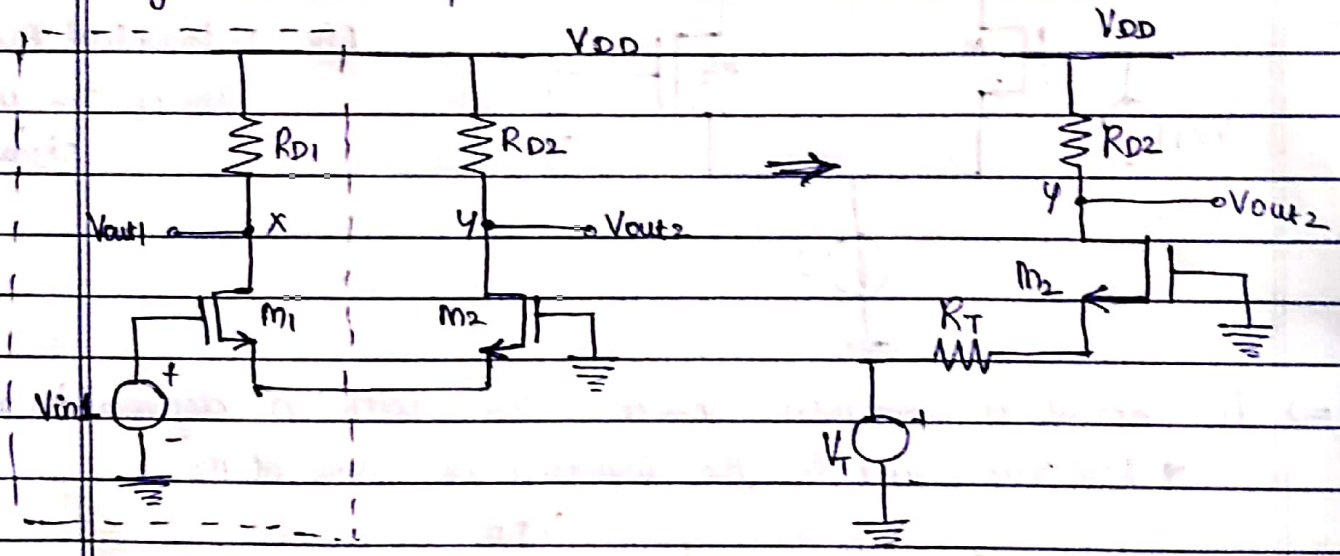


Fig: replacing M_1 by a Thevenin equivalent

⇒ V_T → Thevenin voltage $= V_{in1}$.

Resistance, $R_T = \frac{1}{g_{m1}}$

M_2 → operates as common-gate stage.

$$\text{gain} = \frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}} \quad \text{—— (2)}$$

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By ① & ② the overall voltage gain for V_{in1} is,

$$\frac{(V_x - V_y)}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} - \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

$$(V_x - V_y)\Big|_{\text{Due to } V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1}$$

for $g_{m1} = g_{m2} = g_m$ reduces to,

$$(V_x - V_y)\Big|_{\text{Due to } V_{in1}} = \frac{-2R_D}{\frac{1}{g_m} + \frac{1}{g_m}} V_{in1}$$

$$= \frac{-\cancel{2}R_D}{\frac{\cancel{2}}{g_m}} V_{in1}$$

$$\boxed{(V_x - V_y)\Big|_{\text{Due to } V_{in1}} = -g_m R_D V_{in1}} \quad \text{— ③}$$

⇒ By symmetry, V_{in2} effect at X & Y is identical to that of V_{in1} except the polarities.

$$\boxed{\therefore (V_x - V_y)\Big|_{\text{Due to } V_{in2}} = g_m R_D V_{in2}} \quad \text{— ④}$$

⇒ To perform superposition add both inputs influence.

$$(V_x - V_y)_{total} = -g_m R_D V_{in1} + g_m R_D V_{in2}$$

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$$(V_x - V_y)_{tot} = -g_m R_D (V_{in1} - V_{in2})$$

$$\boxed{\frac{(V_x - V_y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D} \quad \text{--- (5)}$$

* Comparing the mag of (3), (4) & (5) the gain value is $g_m R_D$, regardless of how the inputs are applied.

* If the o/p is single ended, the gain is halved (i.e) o/p is sensed b/w x or y & ground.

⇒ How does the gain of differential pair compare with that of common-source stage?

* For given total bias current

$$g_m = \frac{-(V_x - V_y)_{total}}{(V_{in1} - V_{in2}) R_D} \text{ for differential pair}$$

* $\frac{1}{\sqrt{2}}$ times of single transistor biased at I_{SS} with same dimensions. (i.e) total gain is less.

* For given device dimensions & load impedance, a differential pair achieves the same gain as a CS stage at the cost of twice the bias current.

<u>Method - II</u>

⇒ If a fully-symmetric differential pair senses differential i/p's. (i.e) 2 - i/p's change by equal and opposite amount from equilibrium cond. tion)

* Concept of half-circuit can be applied. (lemma)

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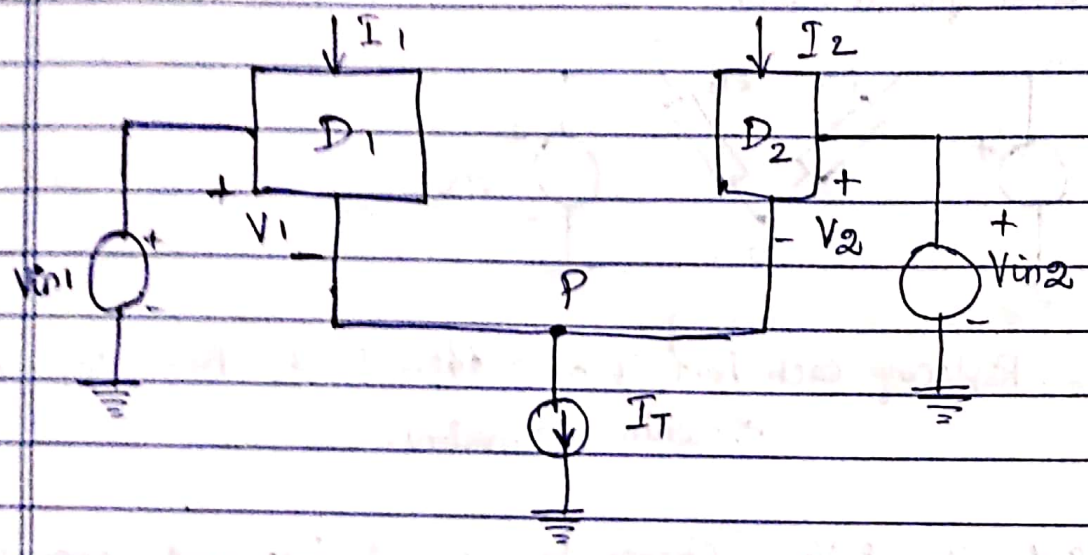
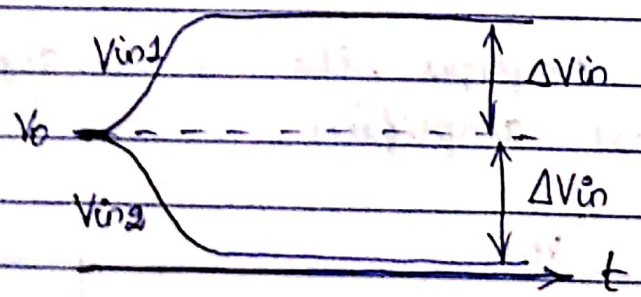
Lemma:

⇒ Consider the symmetric circuit, where D_1 & D_2 represent any three-terminal active device.



⇒ Suppose V_{in1} changes from V_0 to $V_0 + \Delta V_{in}$ and V_{in2} from V_0 to $V_0 + \Delta V_{in}$, then the circuit remain linear, V_P does not change and $\Delta = 0$ (assume).



⇒ Lemma can also be invoked from symmetry.

⇒ If the operation remains linear for long → the difference b/w the bias currents of D_1 and D_2 is negligible, the circuit is symmetry.

∴ The V_P can't favour the change at one if & ignore the other.

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⇒ Another point of view,

* the effect of D_1 & D_2 at node P can be represented by thevenin parameters.

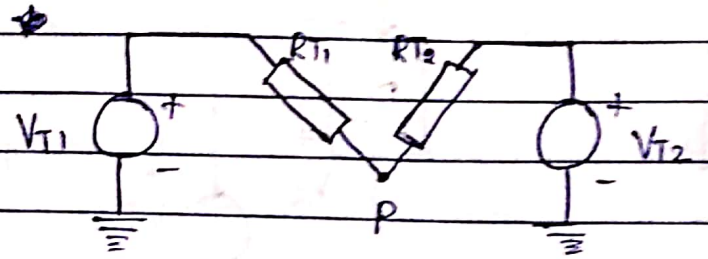

Fig: Replacing each half of a differential pair by a thevenin equivalent.

* If V_{T1} & V_{T2} change by equal ~~&~~ and opposite amounts, and $R_{T1} = R_{T2}$ then,

⇒ V_P remains const.

till this lemma (only the changes are small, we can assume $R_{T1} = R_{T2}$).

⇒ The lemma simplifies the small signal analysis of differential amplifiers.

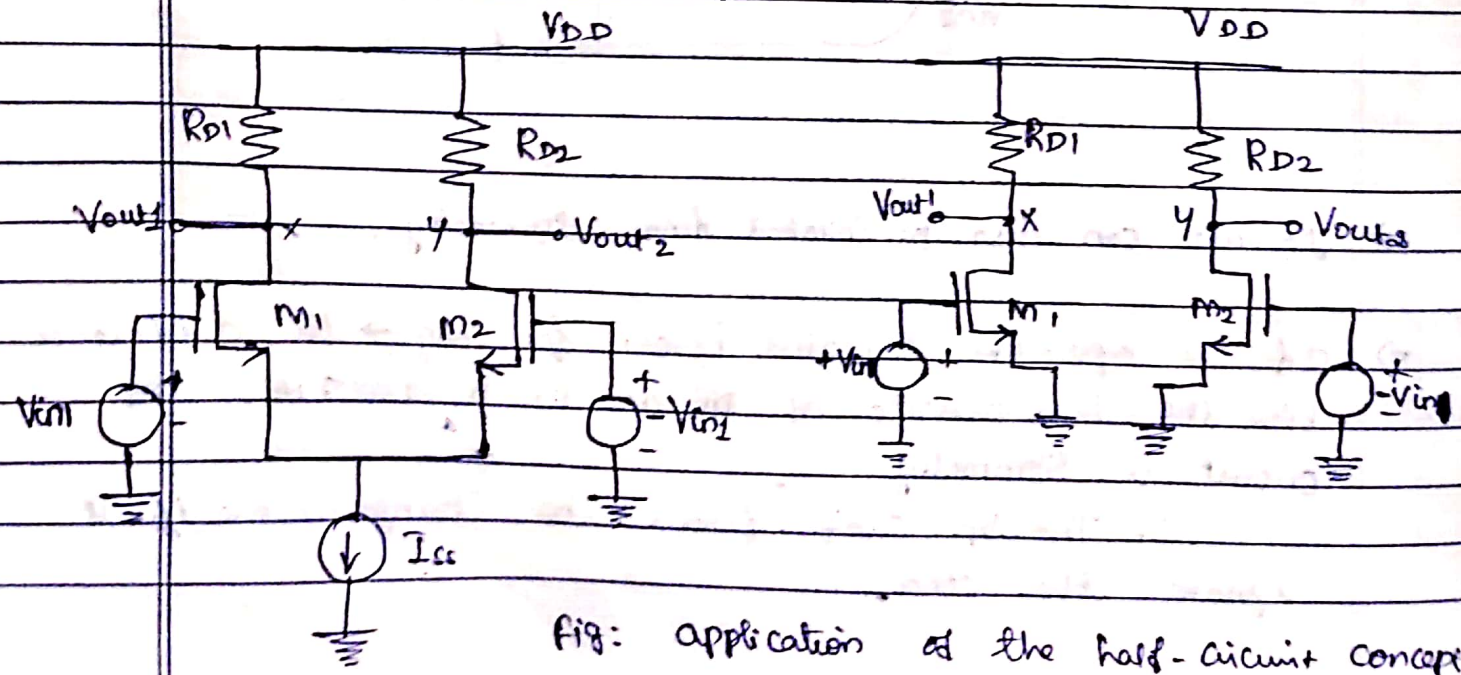

Fig: application of the half-circuit concept.

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⇒ by lemma, V_P experiences no changes.

⇒ Node P can be considered as "ac ground" and the circuit can be decomposed into two seperate halves.
(concept of half-circuit)

⇒ $\frac{V_X}{V_{in1}} = -g_m R_D$

$\frac{V_Y}{-V_{in1}} = -g_m R_D$

where V_{in1} & $-V_{in1}$ are the voltage change in each side

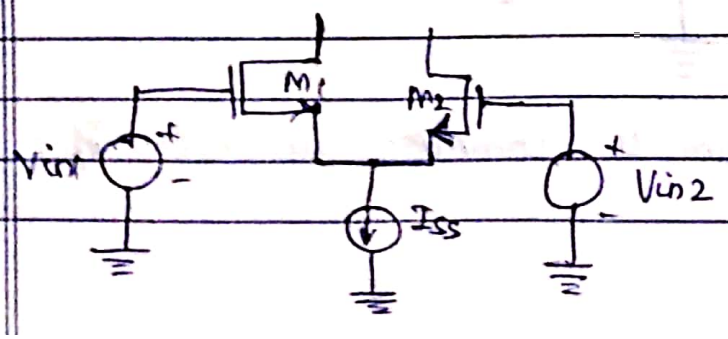
⇒ $\frac{V_X - V_Y}{V_{in1}} = -g_m R_D - (g_m R_D)$

$\frac{V_X - V_Y}{V_{in1}} = -2 g_m R_D$

$$\boxed{\frac{V_X - V_Y}{2V_{in1}} = -g_m R_D}$$

⇒ The half circuit concept provides a powerful technique for analyzing symmetric differential pairs with fully differential i/p's.

⇒ If the i/p's are not fully differential,



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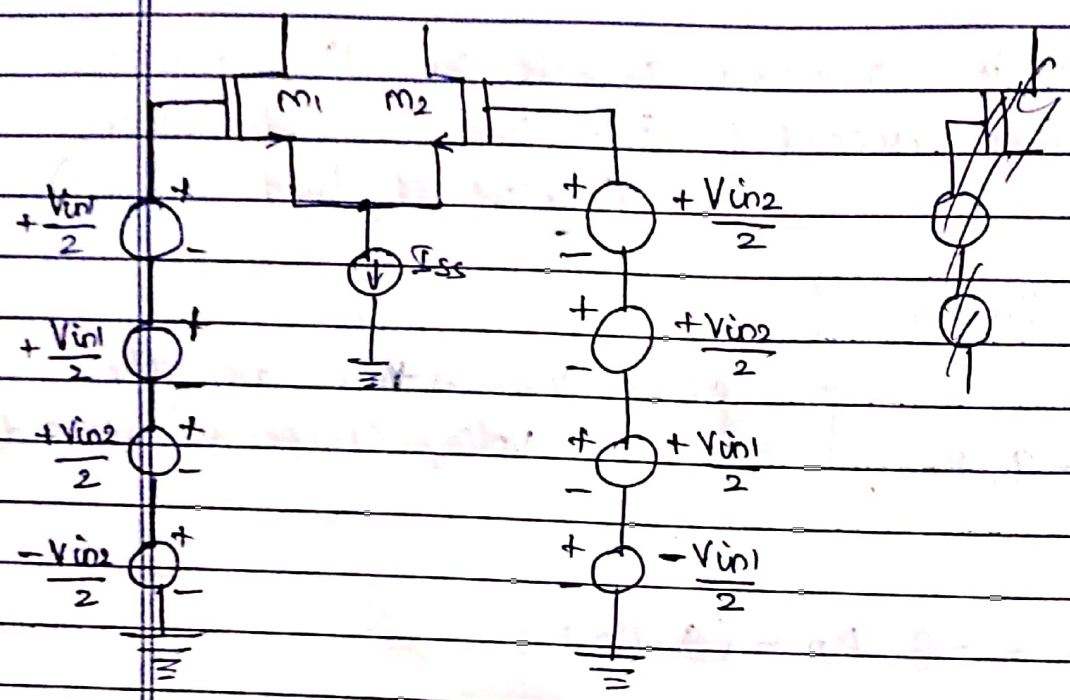
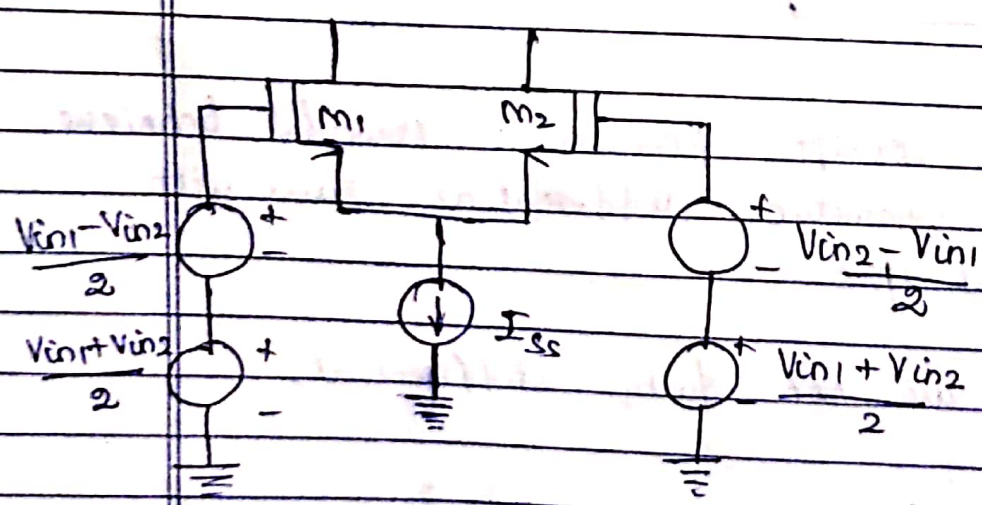
As depicated,



$$\Rightarrow V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2}$$

$$V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2}$$



⇒ The second term is common in both i/p's

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⇒ The equivalent circuit as,

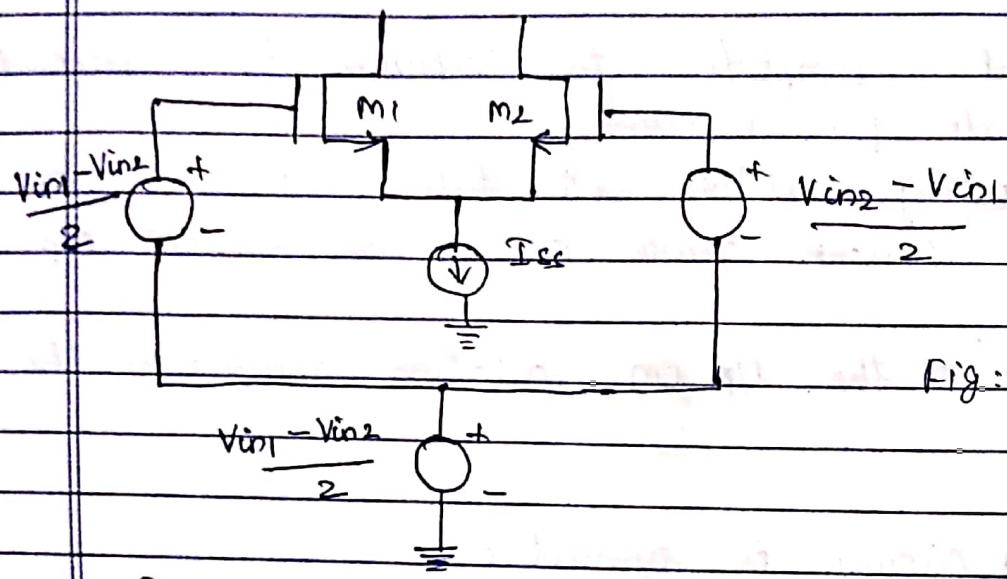

Fig: equivalent circuit

(i.e) the circuit senses a combination of a differential i/p and a common mode variation.

⇒ The effect of each type of i/p can be computed by superposition, with the half-circuit concept applied to the differential-mode operation.

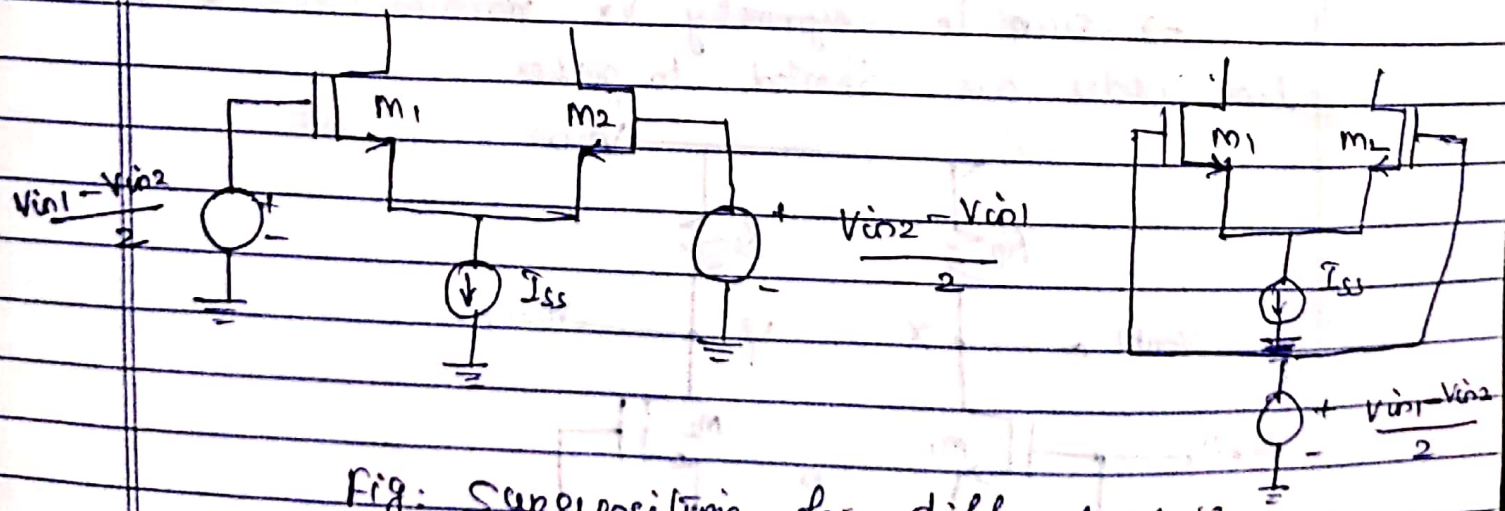

Fig: Superposition for differential & common-mode signals.

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Common-mode Response:

⇒ Differential amplifier to suppress the effect of common-mode perturbations.

* In reality, neither ckt fully symmetric nor does the current source exhibit an infinite o/p impedance.
* Fraction of the i/p cm variation appears at the o/p.

⇒ Assume, * Circuit is symmetric
* Current source has a finite output impedance, R_{SS}

⇒ Vin c.m changes ⇒ Vp changes
↑ing the drain current of M_1 & M_2 and ↓ing both V_X & V_Y.

⇒ Due to symmetry V_X remains equal to V_Y & two nodes are shorted together.

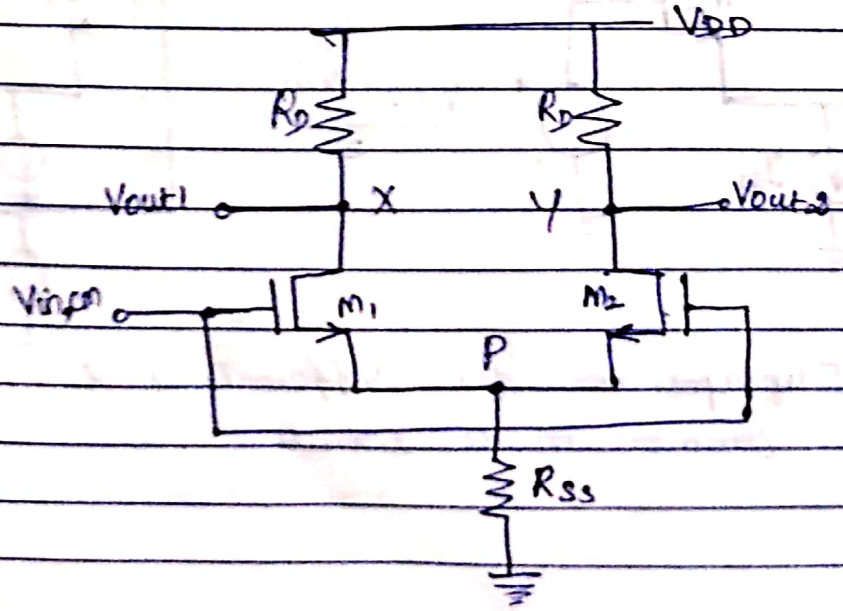

Fig: a ⇒ Differential pair sensing CM input.

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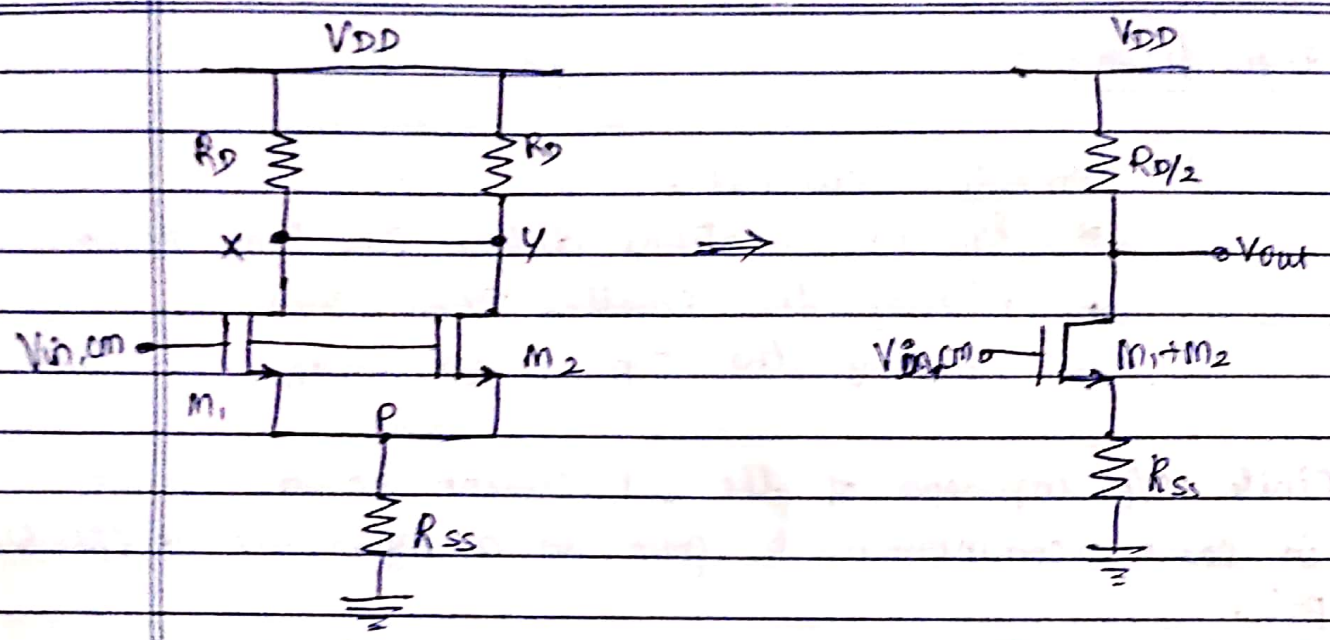

Fig: b simplified version of above figure (a)

Fig: equivalent circuit of (b).

⇒ M_1 & M_2 are "in parallel" ∴ they share all of their respective terminals.

⇒ M_1 & M_2 has twice width & the bias current of each of M_1 & M_2.

* it twice the trans conductance.

⇒ CM gain of the circuit is equal to,

$$A_{v,cm} = \frac{V_{out}}{V_{in,cm}}$$

$$= \frac{R_D/2}{(1/2g_m) + R_{SS}}$$

g_m ⇒ transconductance of each M_1 & M_2, where $\lambda = 0$.

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⇒ Significance :

In symmetric circuit,

* i/p cm variations disturb the bias point.
* Altering the small-signal gain.
* limiting the o/p voltage swing.

⇒ Finite o/p impedance of the tail current source results in some common-mode gain in a symmetric differential pair.

⇒ More trouble is the variation of the differential o/p as a result of a change in $V_{in,cm}$.

* because the circuit is not symmetric in reality.
* two sides suffer from slight mismatch during manufacturing

Study of $V_{in,cm}$ in Asymmetric,

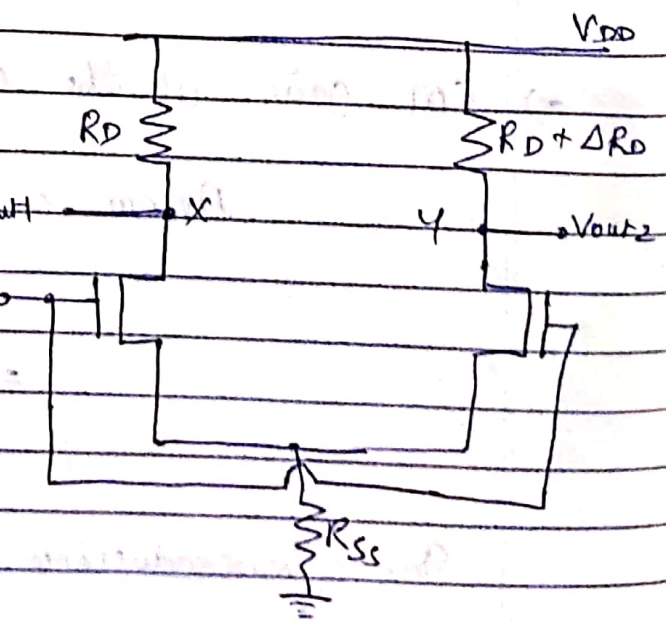
⇒ If circuit is Asymmetric & the tail Ct source suffers from a finite output impedance.

then,

$R_{D1} = R_D$
$R_{D2} = R_D + \Delta R_D$ } assumption

$\Delta R_D \rightarrow$ small mismatch

∴ otherwise CKT is symmetric.



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⇒ Now, V_x & V_y = ? if $V_{in,cm}$ ↑es ?

* M_1 & M_2 are identical,

∴ I_{D1} & I_{D2} ↑ed by $\left[\dfrac{g_m}{1+2g_m R_{SS}}\right] \Delta V_{in,cm}$.

* But V_x & V_y change by different amount,

$$\Delta V_x = -\Delta V_{in,cm} \frac{g_m}{1+2g_m R_{SS}} R_D$$

$$\Delta V_y = -\Delta V_{in,cm} \frac{g_m}{1+2g_m R_{SS}} (R_D + \Delta R_D)$$

(i.e) A common mode change at the i/p introduces a differential component at the o/p.

⇒ The circuit exhibits common mode to differential conversion

* If the i/p of a differential pair includes a differential signal and a common mode noise, the circuit corrupts the amplified differential signal by the input cm change. ⇒ (This is a critical issue)

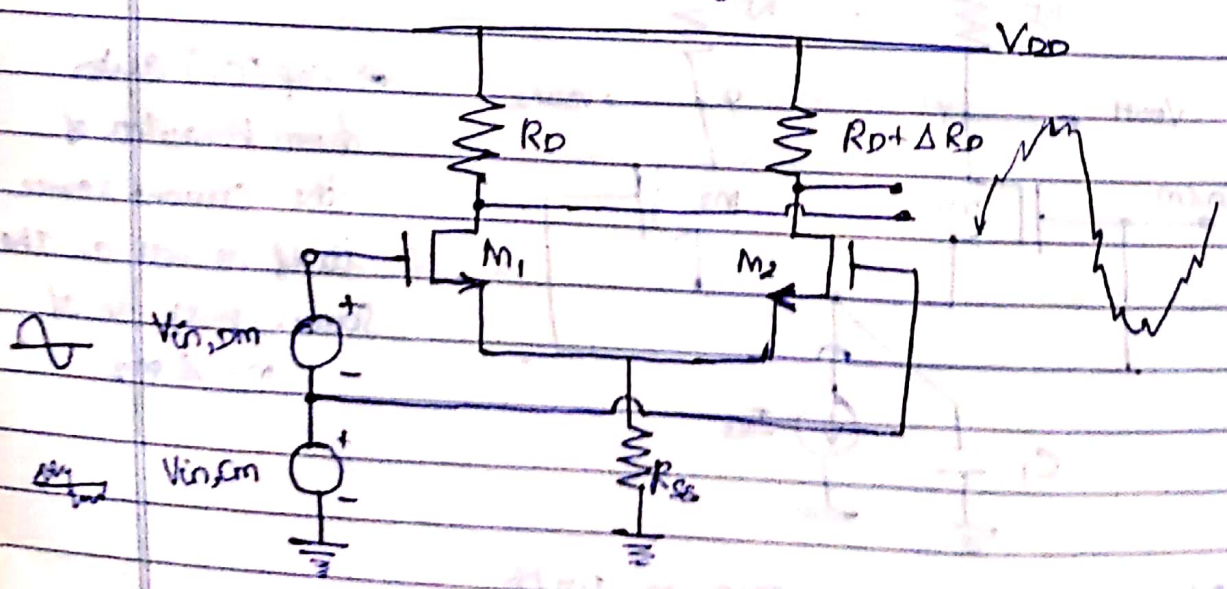

Fig: Effect of CM noise in the presence of resistor mismatch

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⇒ Summary:

The common mode response of differential pairs depends on the o/p impedance of the tail current source and asymmetries in the circuit.

* two effects

(1) Variation of the o/p CM level (in the absence of mismatch)

(2) Conversion of i/p CM variations to differential components at the o/p.

⇒ How significant is common mode to differential conversion?

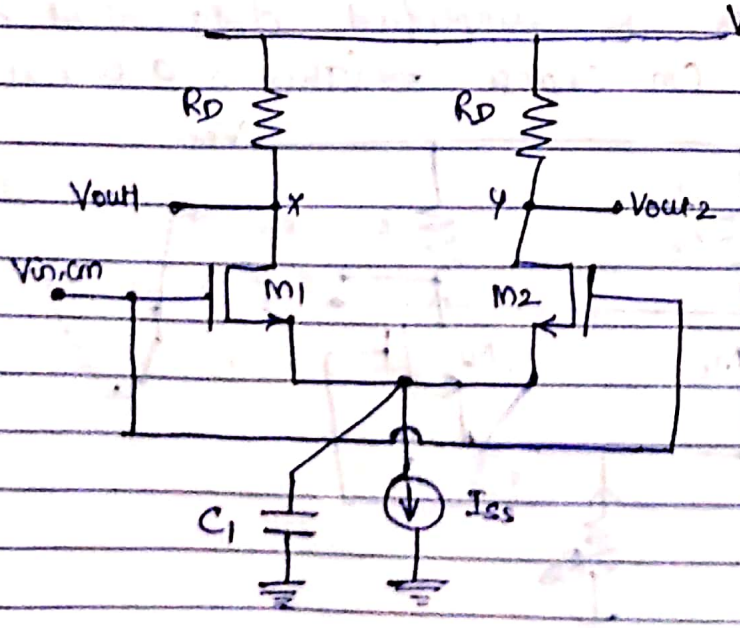
⇒ two observations.

As. (1) frequency of the common mode disturbance increases,

(*) The total capacitance shunting the tail current source introduces larger tail current variations.

(*) o/p resistance of the current source is high

& this conversion becomes significant at high frequencies)



⇒ Cap. (C_1) arises from parasitics of the current source itself as well as the source-bulk jn of M_1 & M_2.

Fig: common mode response with finite tail capacitance.

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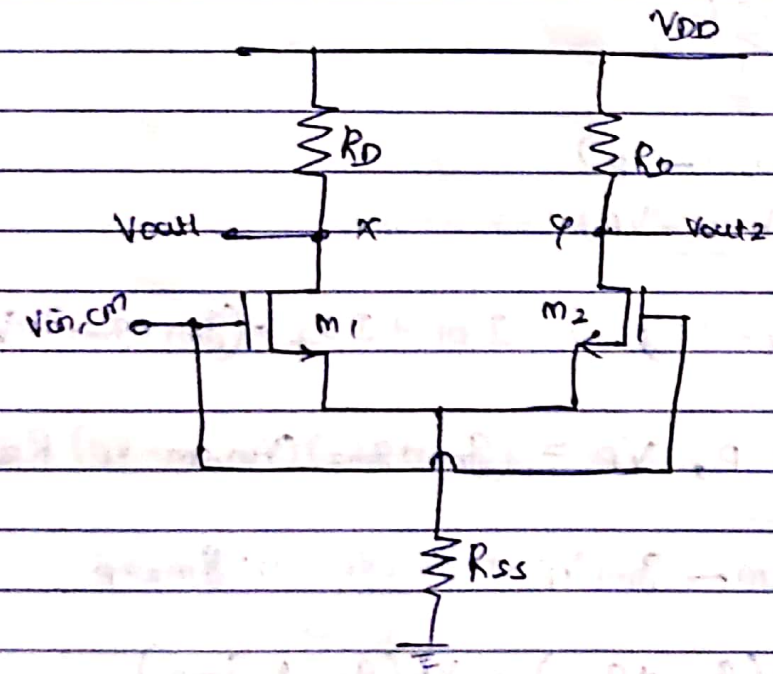
(2) The asymmetry in the CKT stems from both the load resistor and the i/p transistor.

⇒ ~~Study Asymmetry~~

⇒ study of Asymmetry resulting from mismatches b/w M_1 & M_2



* Dimension & threshold voltage mismatches
* 2 transistor carry slightly different currents.
* Exhibit unequal transconductances

⇒ ~~To gain from Vin,cm to x & y~~

⇒ To calculate the gain from Vin,cm to X & Y, use the equivalent circuit.

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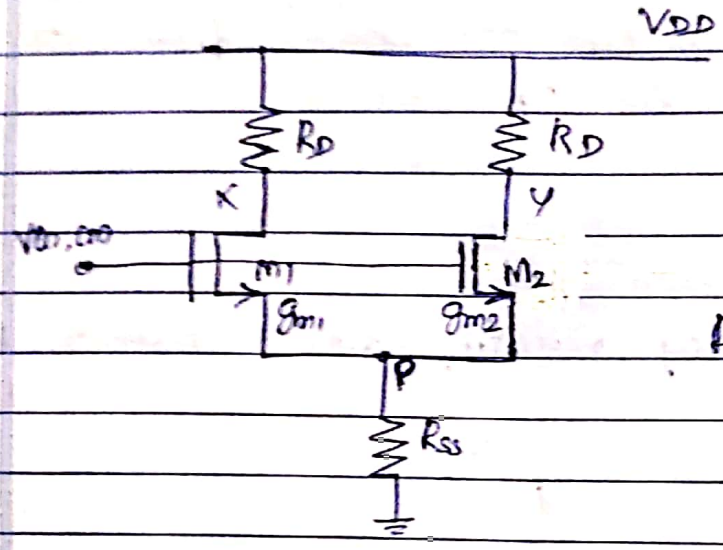

Fig: equivalent circuit.

$I_{D1} = g_{m1}(V_{in,cm} - V_P)$

$I_{D2} = g_{m2}(V_{in,cm} - V_P)$

Total ct at point 'P' ⇒ $I_{D1} + I_{D2} = (g_{m1} + g_{m2})(V_{in,cm} - V_P)$

voltage drop at P, $V_P = (g_{m1} + g_{m2})(V_{in,cm} - V_P) R_{ss}$

$$\frac{V_P}{R_{ss}} = g_{m1} V_{in,cm} - g_{m1} V_P + g_{m2} V_{in,cm} - g_{m2} V_P$$

$$V_P/R_{ss} = V_{in,cm}(g_{m1} + g_{m2}) - V_P(g_{m1} + g_{m2})$$

$$V_{in,cm}(g_{m1} + g_{m2}) = \frac{V_P}{R_{ss}} + V_P(g_{m1} + g_{m2})$$

$$V_{in,cm}(g_{m1} + g_{m2}) = V_P\left(\frac{1 + (g_{m1} + g_{m2}) R_{ss}}{R_{ss}}\right)$$

$$\boxed{V_P = \frac{(g_{m1} + g_{m2}) R_{ss}}{1 + (g_{m1} + g_{m2}) R_{ss}} V_{in,cm}}$$

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⇒ o/p voltages,

$$V_y = -g_{m1}(V_{in,cm} - V_P)R_D$$

$$= -g_{m1}R_D\left(V_{in,cm} - \left[\frac{(g_{m1}R_{SS} + g_{m2}R_{SS})}{1+g_{m1}R_{SS}+g_{m2}R_{SS}} V_{in,cm}\right]\right)$$

$$= -g_{m1}R_D V_{in,cm}\left[1 - \frac{(g_{m1}R_{SS} + g_{m2}R_{SS})}{1+g_{m1}R_{SS}+g_{m2}R_{SS}}\right]$$

$$= -g_{m1}R_D V_{in,cm}\left[\frac{1+\cancel{g_{m1}R_{SS}}+\cancel{g_{m2}R_{SS}}-\cancel{g_{m1}R_{SS}}-\cancel{g_{m2}R_{SS}}}{1+g_{m1}R_{SS}+g_{m2}R_{SS}}\right]$$

$$= \frac{-g_{m1}R_D V_{in,cm}}{1+g_{m1}R_{SS}+g_{m2}R_{SS}}$$

$$\boxed{V_x = \frac{-g_{m1}}{1+(g_{m1}+g_{m2})R_{SS}} \cdot R_D \cdot V_{in,cm}}$$

$$V_y = -g_{m2}(V_{in,cm} - V_P)R_D$$

$$\boxed{V_y = \frac{-g_{m2}}{1+(g_{m1}+g_{m2})R_{SS}} R_D \cdot V_{in,cm}}$$

$$V_{out} = V_x - V_y = -\frac{(g_{m1} - g_{m2})}{1+(g_{m1}+g_{m2})R_{SS}} R_D \cdot V_{in,cm}.$$

$$\boxed{A_{V(cm-dm)} = \frac{V_x - V_y}{V_{in,cm}} = -\frac{(g_{m1} - g_{m2})}{1+(g_{m1}+g_{m2})R_{SS}} R_D}$$

$$A_{dm-cm} = \frac{-\Delta g_m R_D}{1+(g_{m1}+g_{m2})R_{SS}}$$

where, $\Delta g_m = g_{m1} - g_{m2}$

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where,

A_{cm-dm} → common mode to differential mode conversion

$\Delta g_m = g_{m1} - g_{m2}$.

⇒ common mode Rejection Ratio (CMRR) as,

$$CMRR = \left| \frac{A_{DM}}{A_{cm-dm}} \right|$$

* if g_m mismatches,

from page (22),

$$A_{DM} = \frac{R_D}{2} \cdot \frac{g_{m1} + g_{m2} + 4 g_{m1} g_{m2} R_{SS}}{1 + (g_{m1} + g_{m2}) R_{SS}}$$

assume, $V_{in1} = -V_{in2}$,

$$CMRR = \frac{g_{m1} + g_{m2} + 4 g_{m1} g_{m2} R_{SS}}{2 \Delta g_m}$$

$$\boxed{CMRR \simeq \frac{g_m}{\Delta g_m} (1 + 2 g_m R_{SS})}$$

g_m = mean value (i.e) $\frac{g_{m1} + g_{m2}}{2}$

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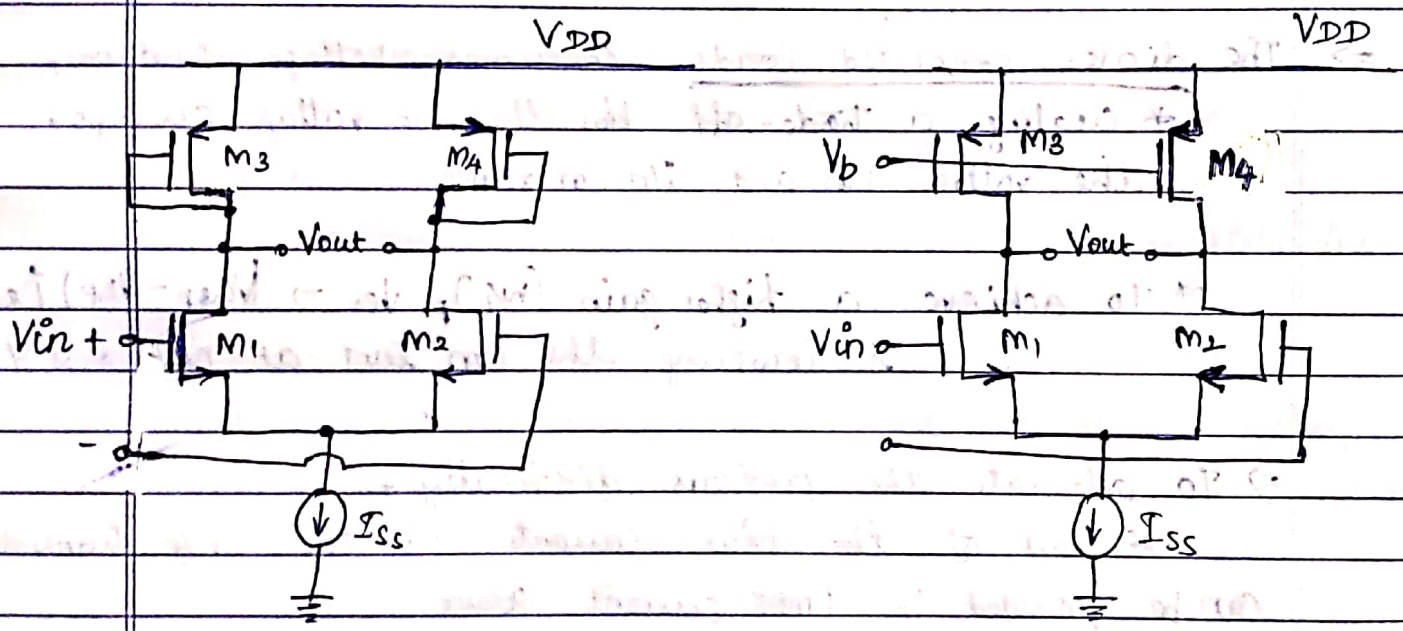
Differential Pair with MOS loads:

⇒ The load of a differential pair need not be implemented by linear resistors.

⇒ Based on common source,
The load for differential pairs can employ diode-connected (or) current source loads.



Fig①: Differential Pair with diode-connected

Fig②: differential pair with current source loads.

⇒ The small signal differential gain can be derived using the half circuit concept,

* For Fig① ⇒

$$A_V = -g_{mN}\left(g_{mP}^{-1} \parallel r_{ON} \parallel r_{OP}\right)$$

$$\boxed{A_V \cong \frac{-g_{mN}}{-g_{mP}}}$$

where, subscripts N & P denote NMOS & PMOS.

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In terms of device dimensions,

$$A_v \simeq -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$

* For Fig② ⇒

$$A_v = -g_{mN}(r_{ON} \| r_{OP})$$

⇒ The diode-connected loads consumes voltage headroom,
* creating a trade-off b/w the o/p voltage swings, the voltage gain and i/p cm range.

* To achieve a higher gain $(W/L)_P$ ↓es ⇒ $|V_{GSP} - V_{THP}|$ ↑es & lowering the cm level at node x & y

⇒ To alleviate the previous difficulty,
* Part of the bias current of the i/p transistors can be provided by PMOS current source.

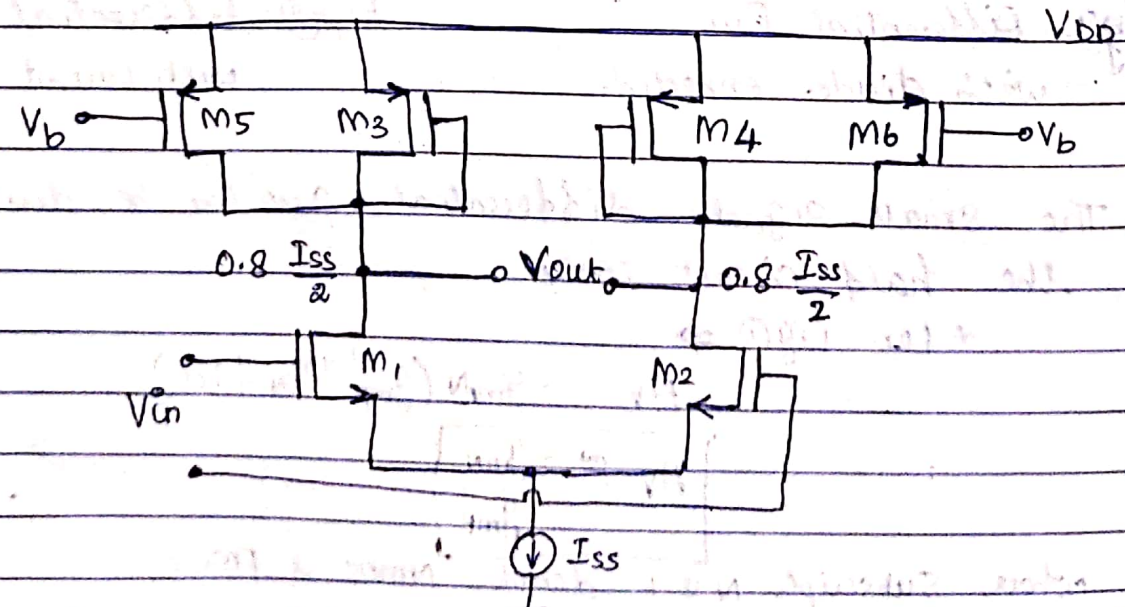

fig: Addition of current source to increase the voltage gain

⇒ The idea is to,
Ring g_m of load devices by reducing their current rather than their aspect ratio.

* Example:
→ If M_5 & M_6 carry 80% of the drain current of M_1 & M_2, then the current through M_3 & M_4 is reduced by a factor of five.
→ $|V_{GSP} - V_{THP}|$ → translates to a factor of five reduction in the transconductance of M_3 & M_4.
∴ W/L of the devices can also be ties the same fact.
⇒ Thus the differential gain is approximately five times that of the case with no pmos current source.

⇒ Small signal gain of the differential pair with current source loads is relatively low in the range of 10 to 20 in submicron technologies.
* How to ries the voltage gain?
⇒ ~~we can~~ by ring the o/p impedance of both PMOS & NMOS devices by cascoding.

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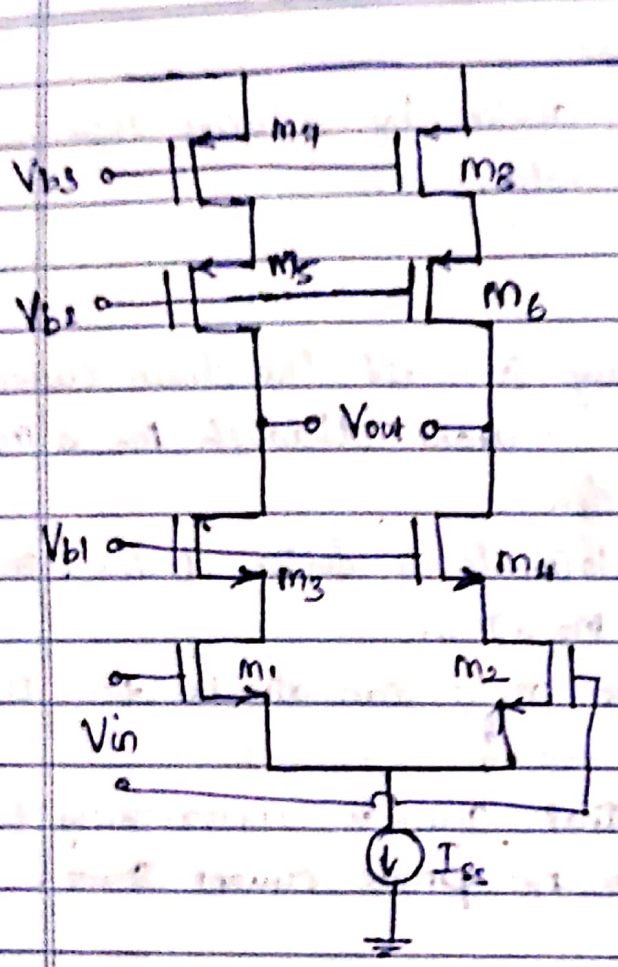

Fig: Cascode differential pair

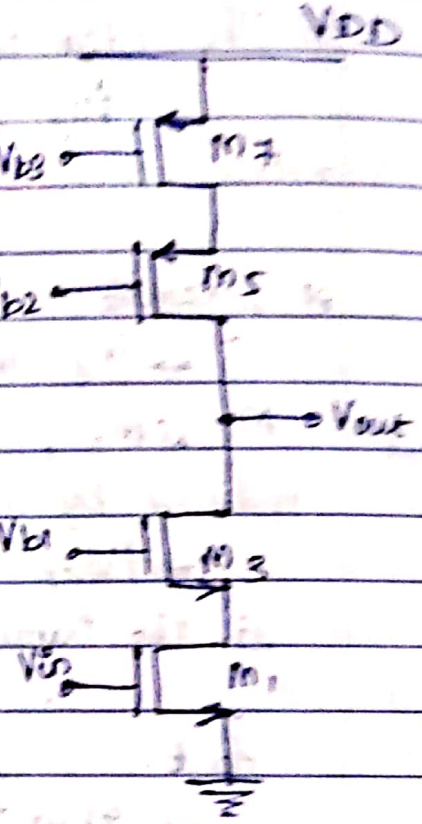

Fig: half circuit of cascode differential pair

⇒ To calculate the gain, we construct the half circuit

$$A_v \cong g_{m1}\left[(g_{m3} r_{o3} r_{o1}) \parallel (g_{m5} r_{o5} r_{o2})\right].$$

* Cascoding ↑es the differential gain, but consuming more voltage headroom.

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Final Note:

→ To maintain high gain in fully differential amplifier requires a means of defining the o/p common-mode level.

* In current source loads, the common-mode level is not well-defined
* In diode connected loads, transistors define the output cm level as $V_{DD} - V_{GSP}$.

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