Steps for Cmos process:

1) Draw the metal (blue) V_{DD} & V_{SS} rails in parallel and creat a demarcation line in b/w. Allowing enough space b/w them for other CKT elements.

2) n-devices are placed below the demarcation line and p-devices are placed above the demarcation line.

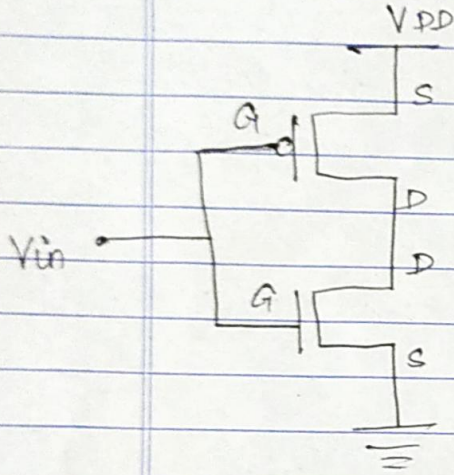
3) n & P devices are then connected using metal and contacts.

4) Finally the remaining interconnections are mad & control signals and data i/p's are added.

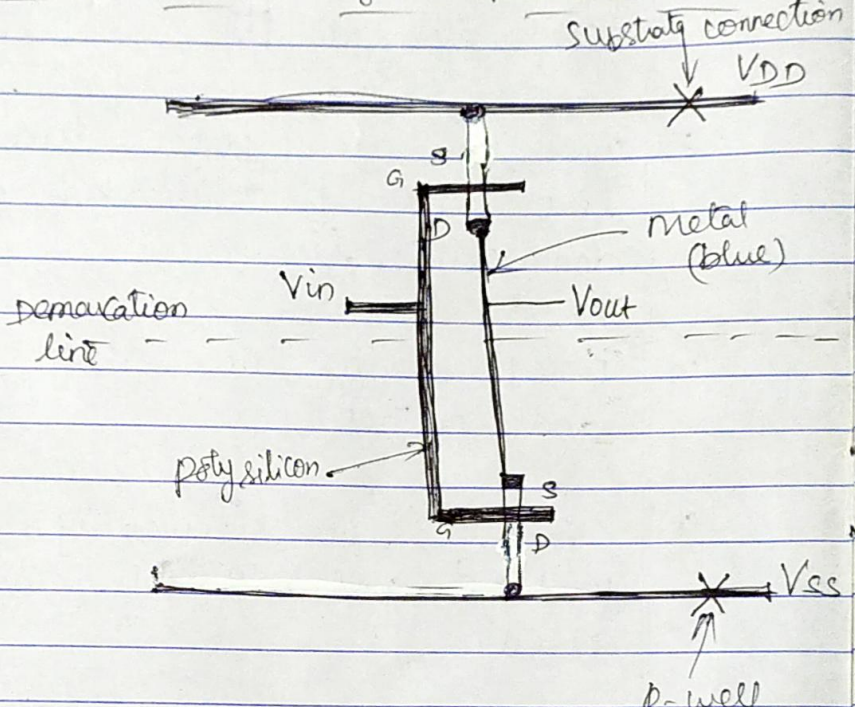
Note: * diffusion paths must not cross the demarcation line
* n&P diffusion wires must not join.
* The metal should be used to connect n & P features
* we must place crosses (x) on V_{DD} & V_{SS} rails to represent the substrate and p-well connection respectively.
* only metal & polysilicon can cross the demarcation line
* represent the V_{SS} & V_{DD} contact cuses — one on V_{DD} line for every 4 P-transistors. & one on V_{SS} line for every 4 n-transistors.

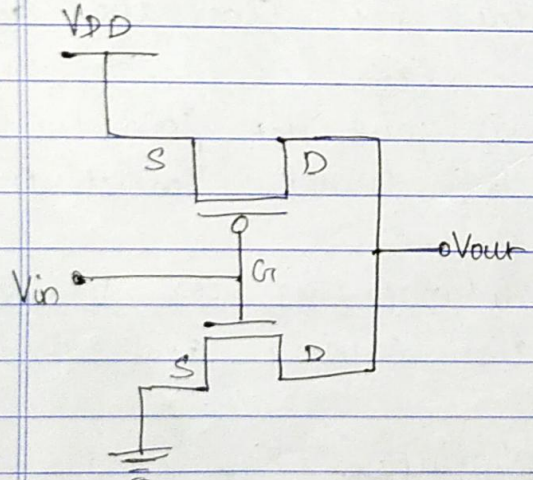
* Metal lines on different layers (metal 1 & metal 2) can cross one another. Contacting 2 metal lines requires a via.

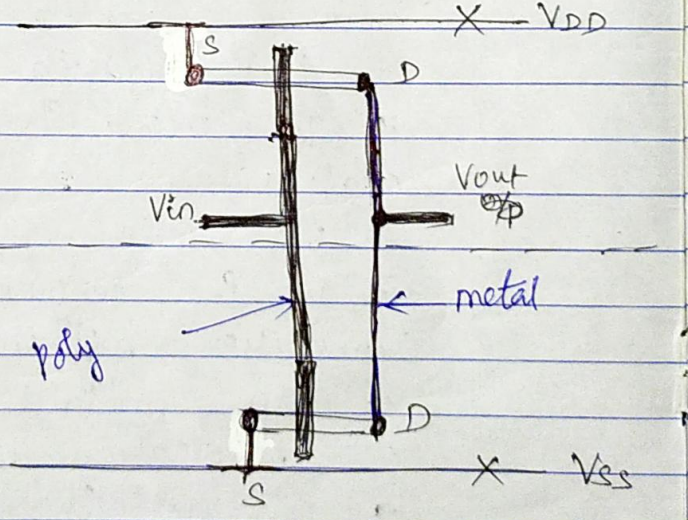
(1) Write the CKT & stick diagram for CMOS inverter.



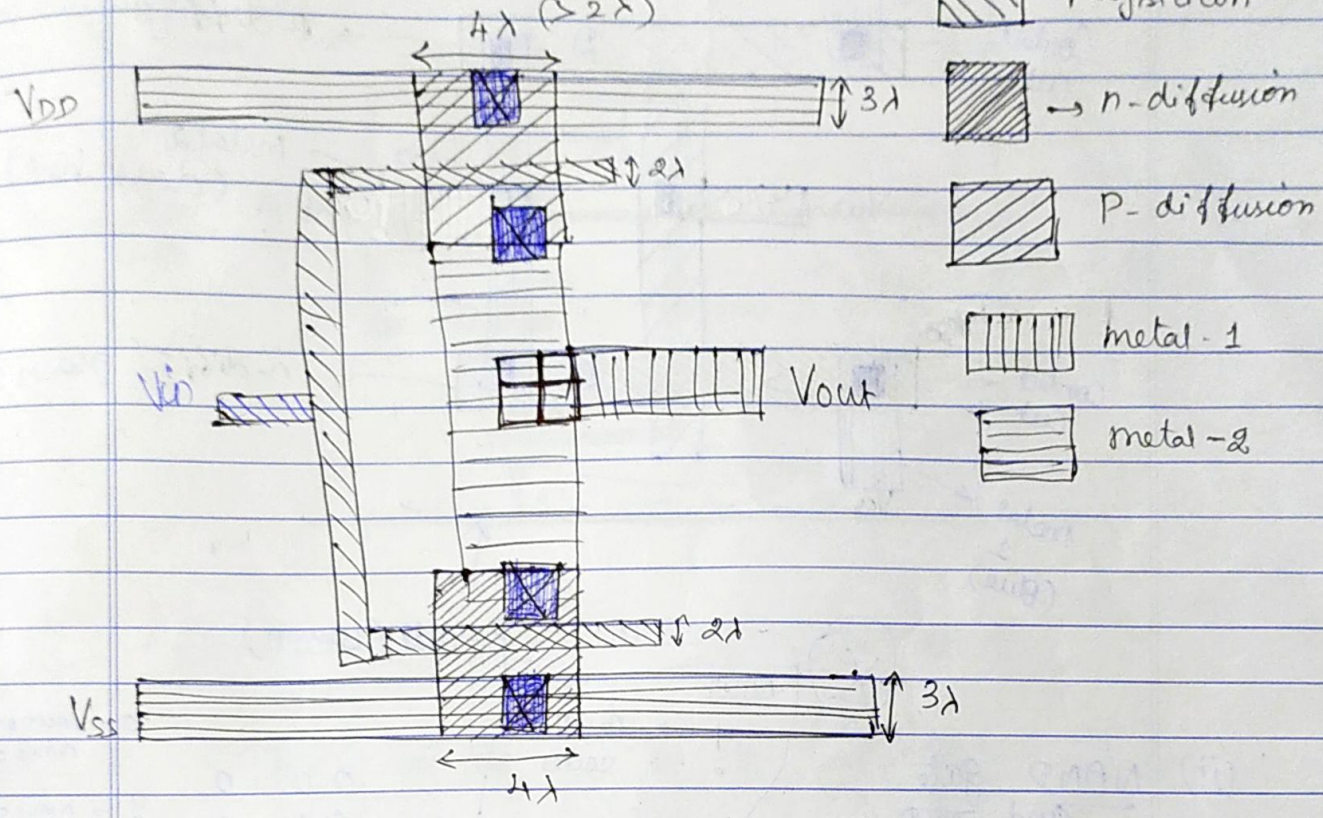
CKT diagram.

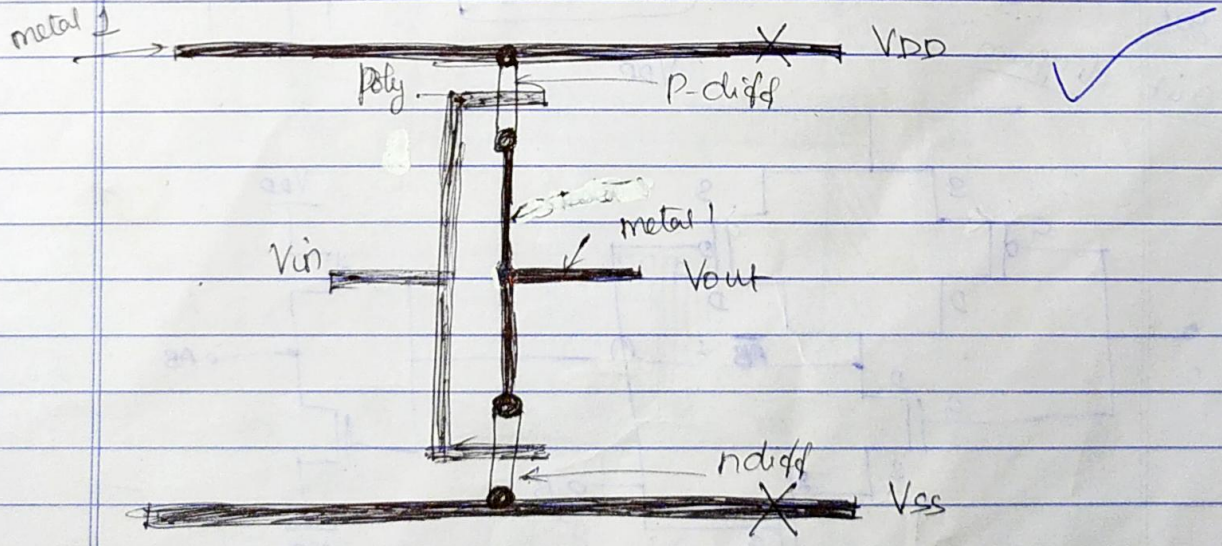


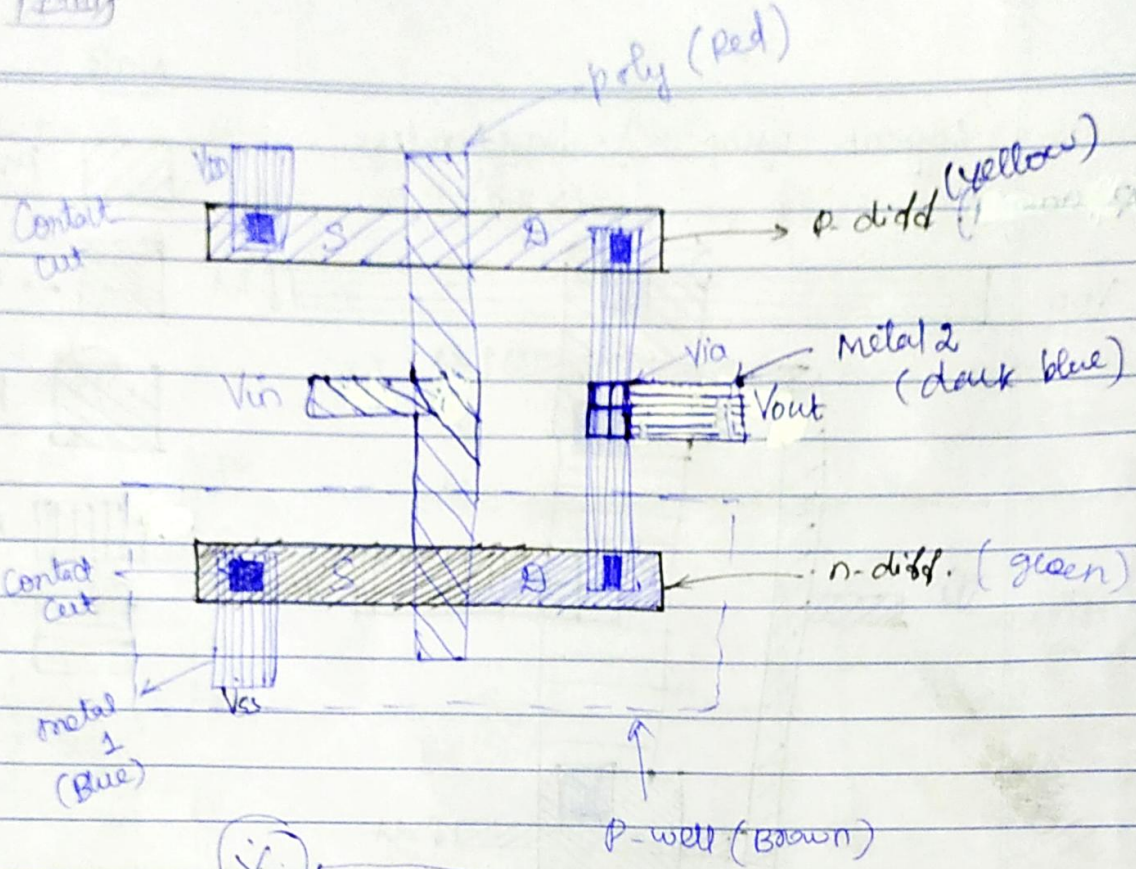




Layout using λ- based rules



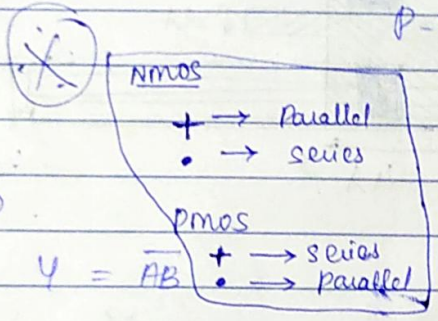




(ii) NAND gate: and AND

and gate

$Y = AB \Rightarrow Y = \overline{AB}$

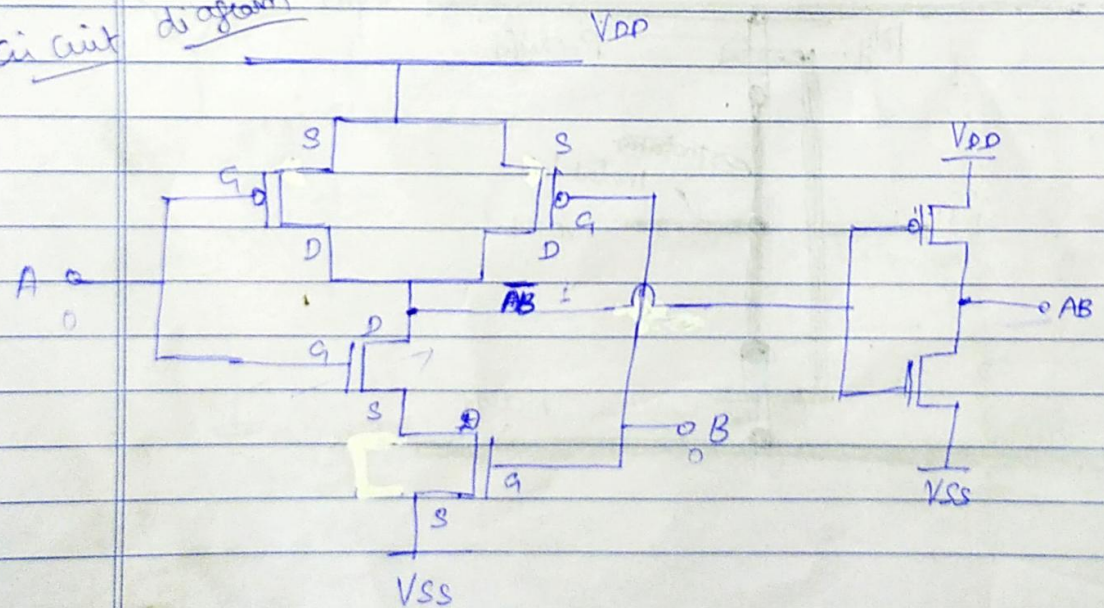


0	0	0
0	1	0
1	0	0
1	1	1

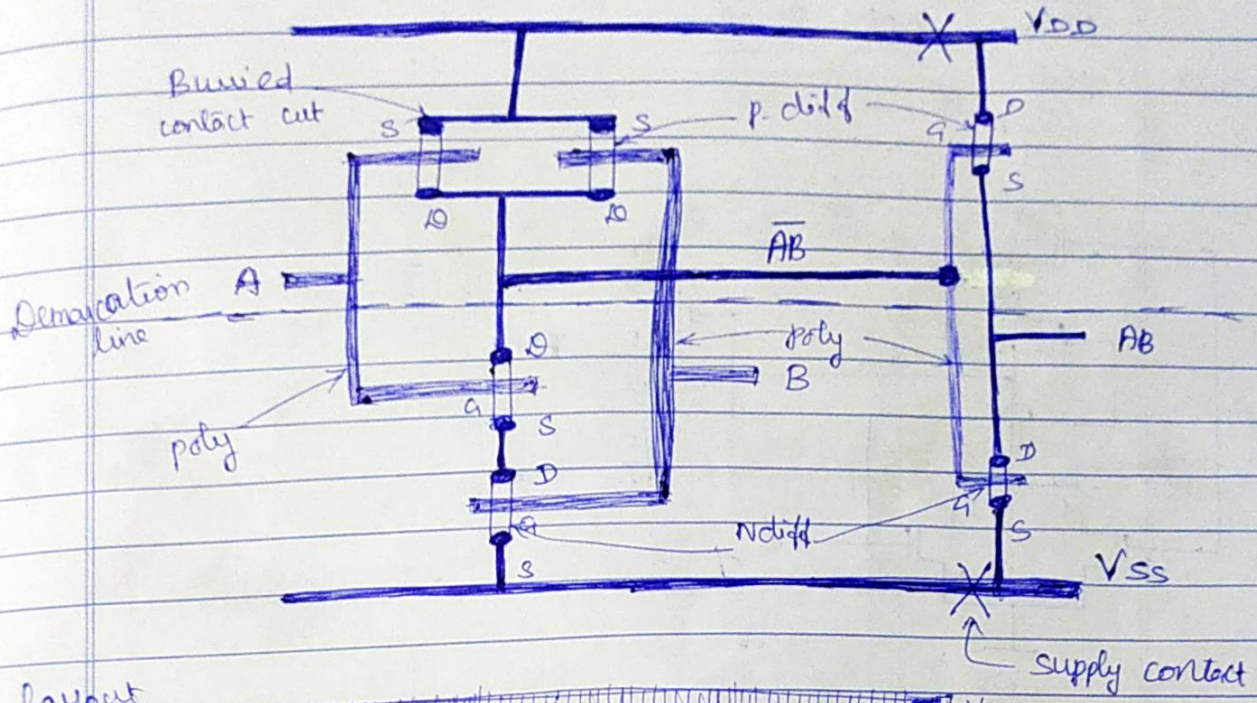
0 → PMOS ON NMOS OFF

1 → NMOS ON PMOS OFF

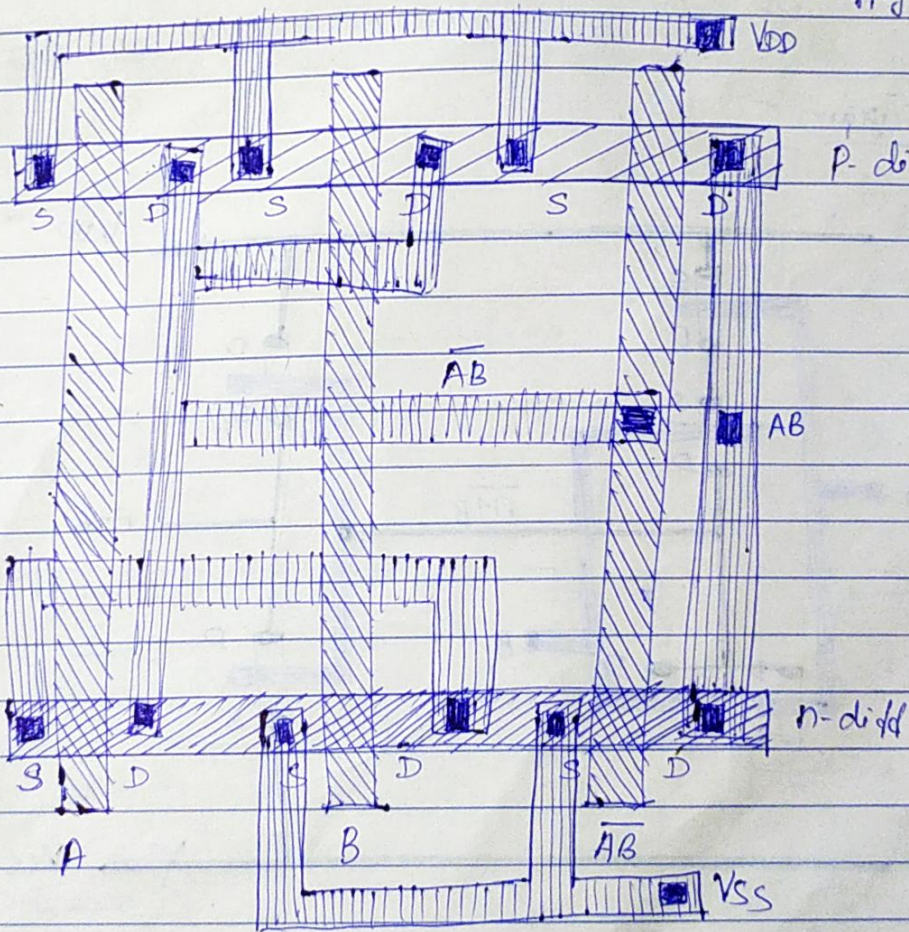
Circuit diagram



Stick diagram

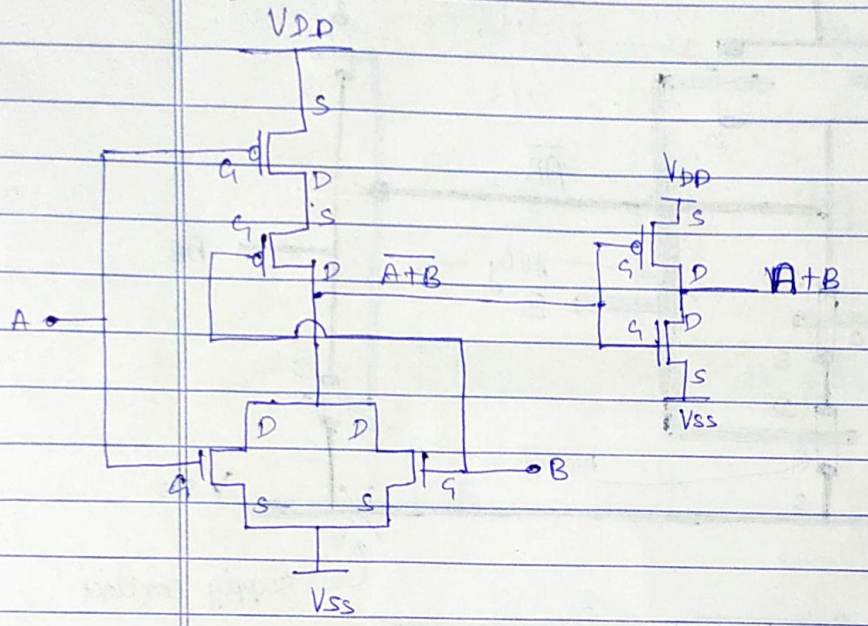


layout

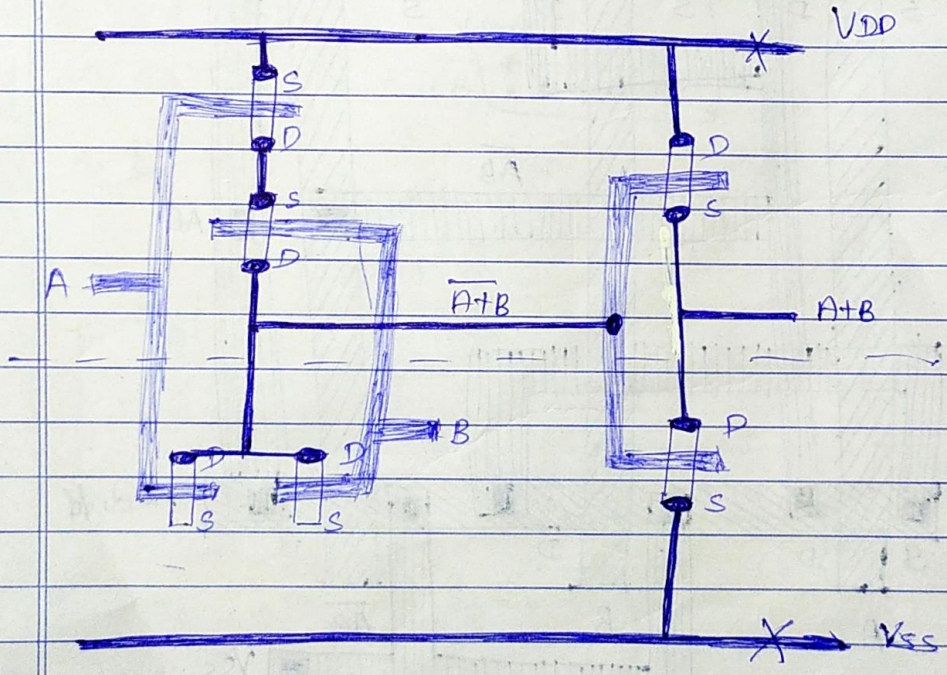


$\overline{A+B}$ = NOR & OR

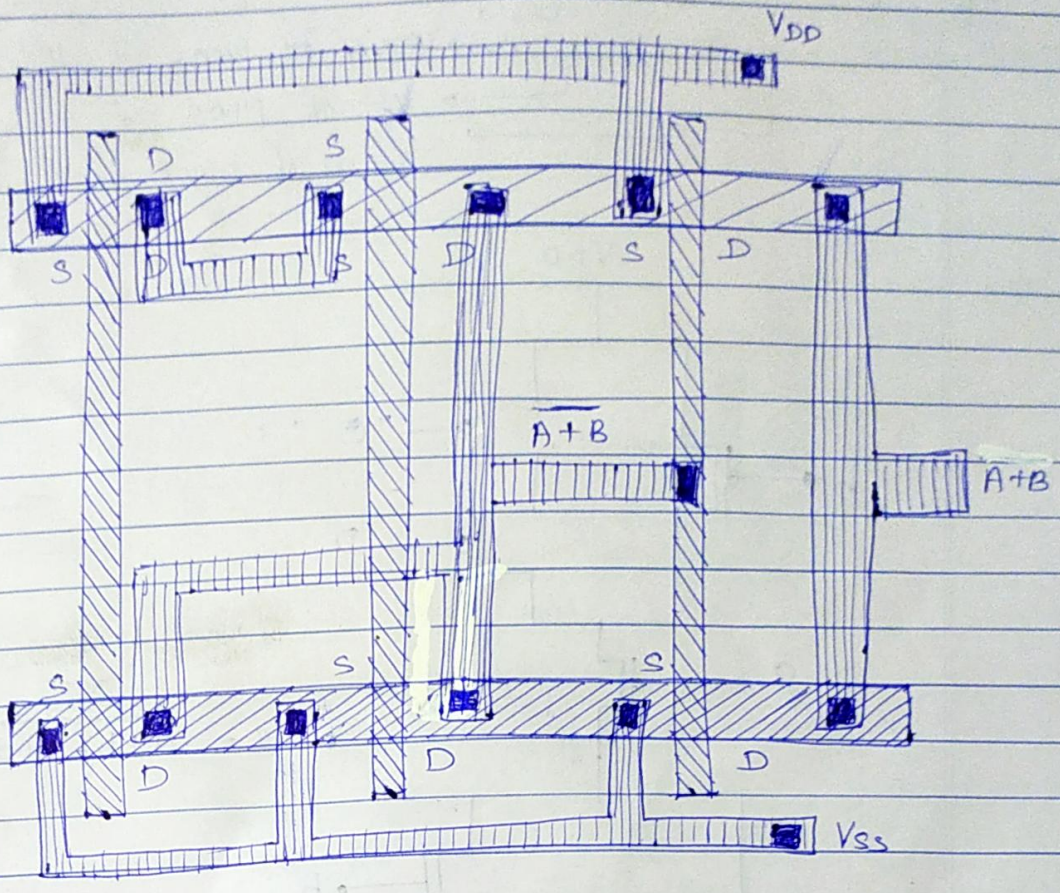
Circuit diagram



Stick diagram



layout

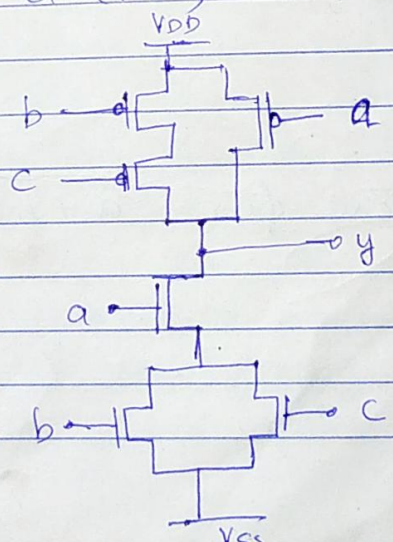


complex logic gates in cmos:

+ ||el
• series NMOS

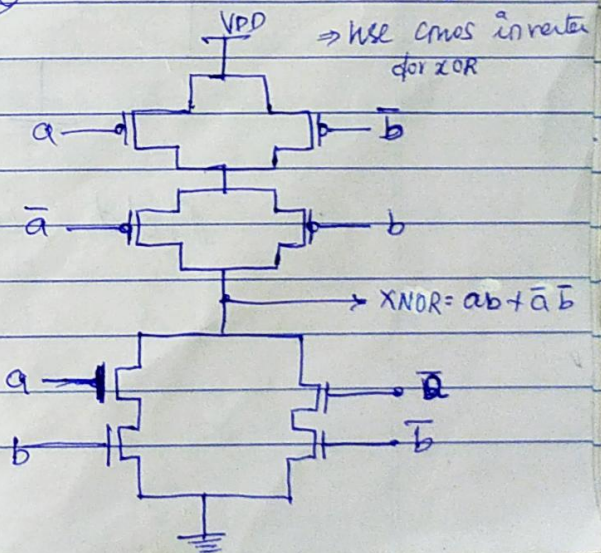
• ||el PMOS
+ series

① $y = \overline{a \cdot (b+c)}$



② XOR = $a \oplus b = \bar{a}b + \bar{a}\bar{b}$

⇒ use cmos inverter for XOR



$L = 2\lambda$

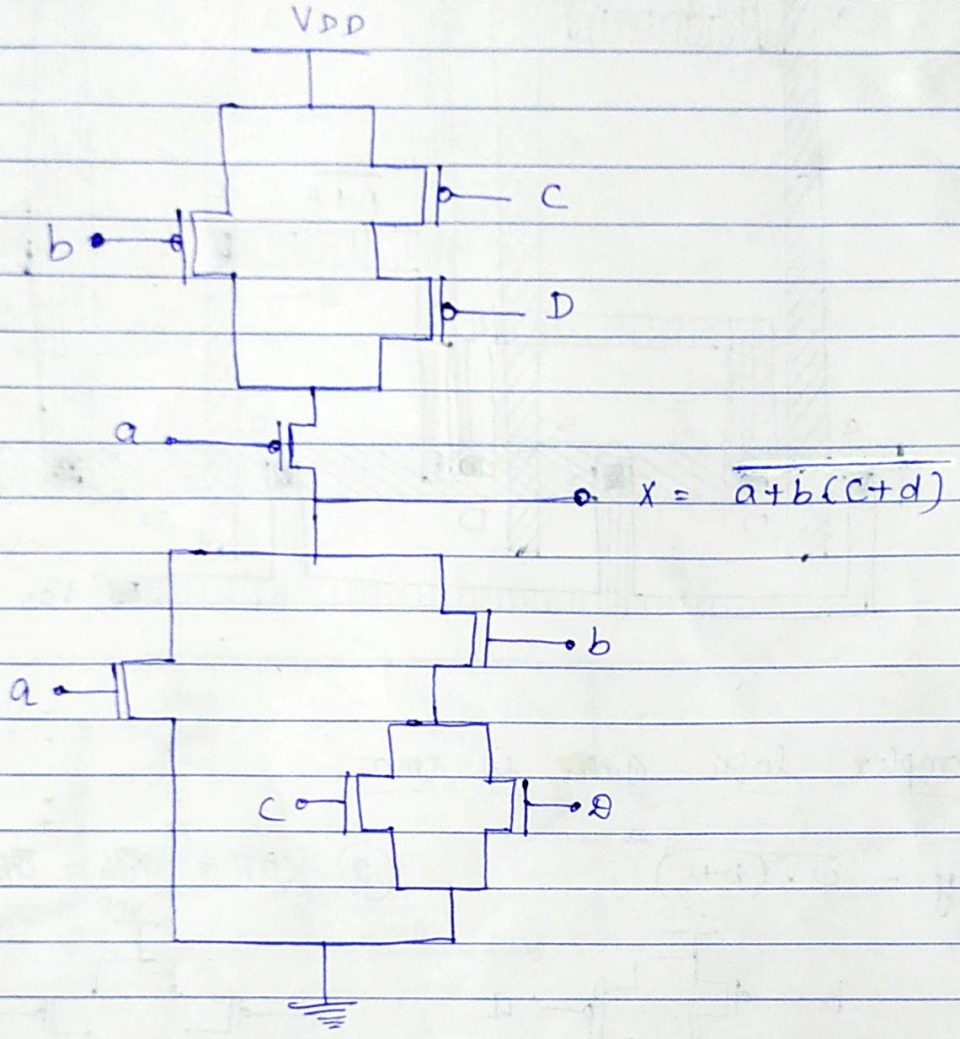
$\lambda = \frac{L}{2}$

(9) $X = \overline{a+b \cdot (c+d)}$

→ series of pmos + ||el of nmos

→ ||el of pmos + series of nmos

series of pmos + ||el of pmos



Add inveter for $a+b(c+d)$