

# **FUNDAMENTALS OF VLSI DESIGN**

*(19EC6DCFOV)*

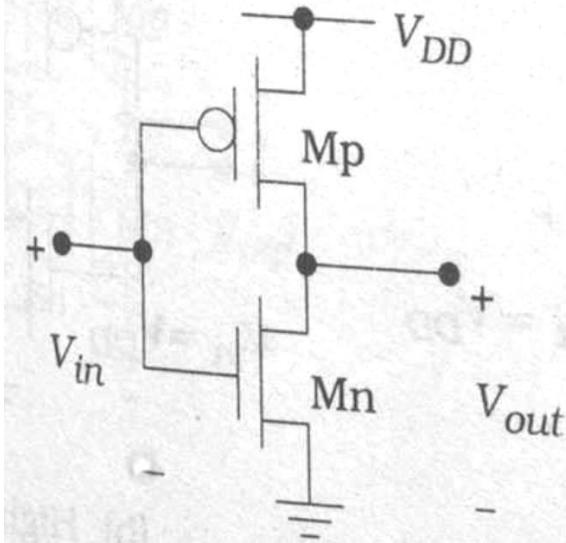
# Module-3

**Electronic Analysis of CMOS Logic gates:** DC Characteristics of CMOS Inverter, Inverter switching characteristics, Power dissipation, DC Characteristics of NAND and NOR gates. NAND and NOR transient response, Analysis of Complex logic gates, Gate design and transient response. (Text book-2) Clocked Latch and Flip Flop circuits (D-Latch, D-FF, MS JK Flip Flop) (Text book -6)

## **Text books:**

2. John P.Uyemura, “Introduction to VLSI Circuits and Systems”, Wiley India Edition, 3rd print, 2007.
6. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH, India, 2007.

# DC Characteristics of CMOS Inverter



$$\text{pFET: } V_{Tp} < 0$$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

$$\text{nFET: } V_{Tn} > 0$$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$

Two types of calculations are needed to characterize a digital logic circuit.

- **DC analysis :** Determines  $V_{out}$  for a given value of  $V_{in}$ . This defines Boolean logic0 and Logic 1 values.
- transient analysis: Input and output voltages are an **explicit function of time**  $V_{in}(t)$  corresponding to a changing logic values.

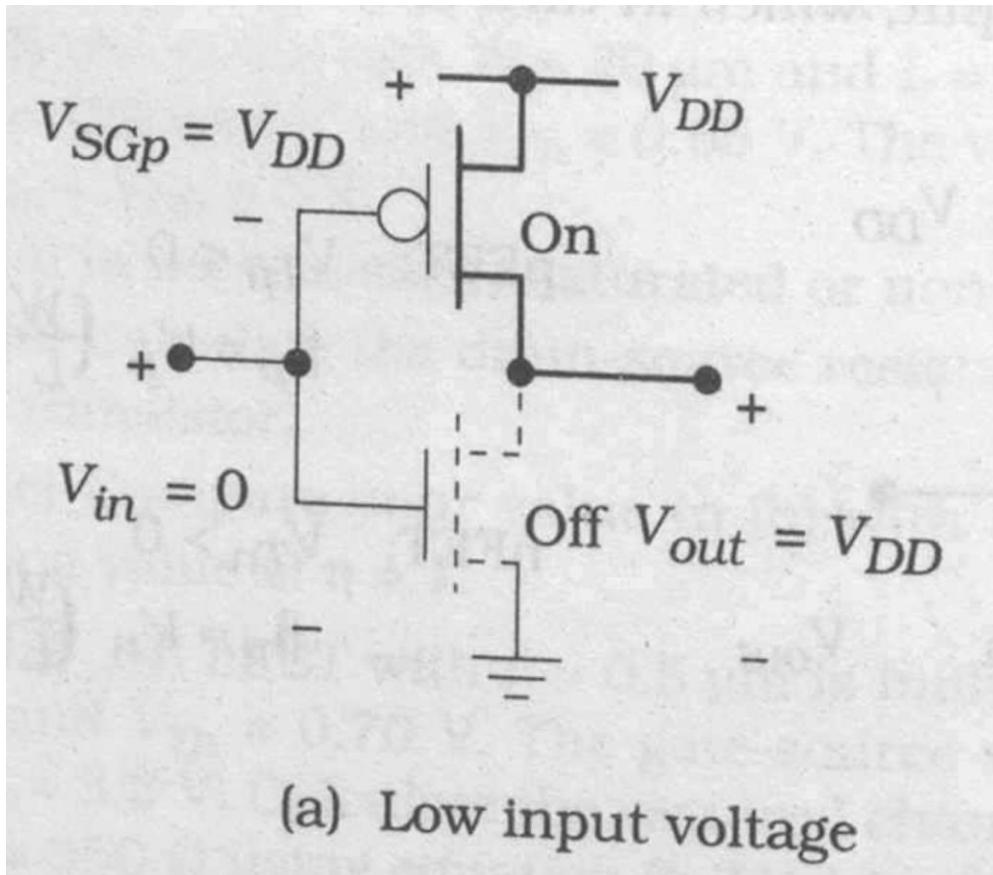
# Voltage transfer characteristic (VTC)

If,  $V_{in}=0$

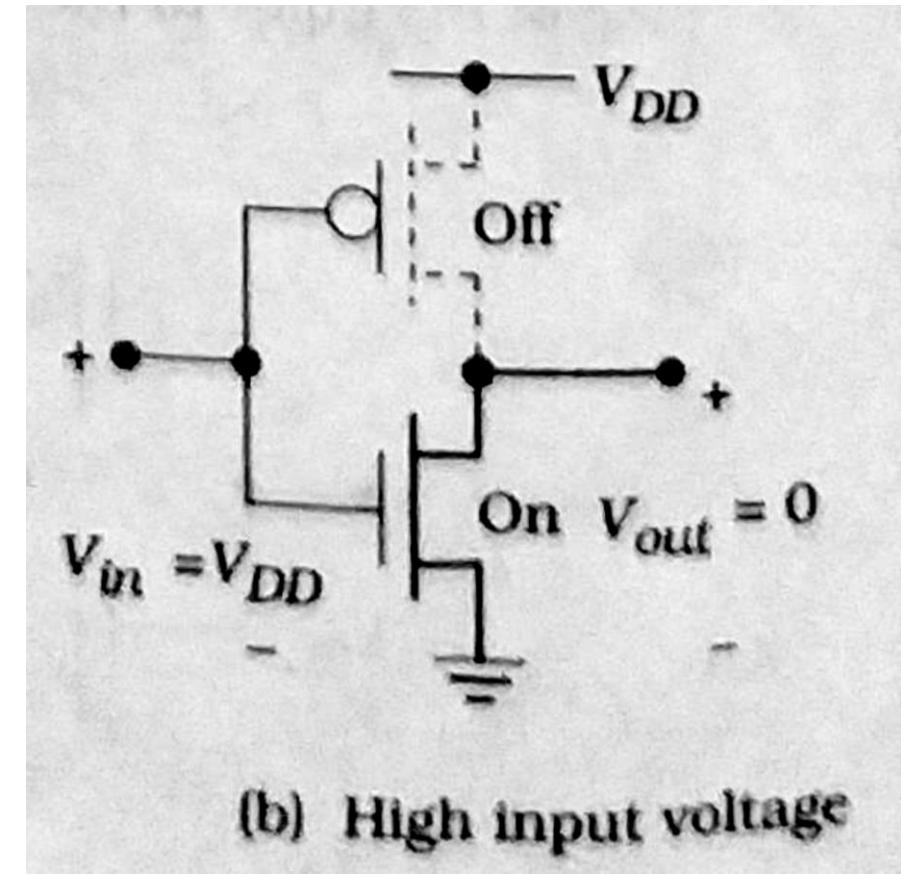
Mn-off & Mp-on ----- defines **output high voltage**

If,  $V_{in}=V_{DD}$

Mn-on & Mp-cutoff ----- defines **output Low voltage**



$$V_{OH} = V_{DD}$$

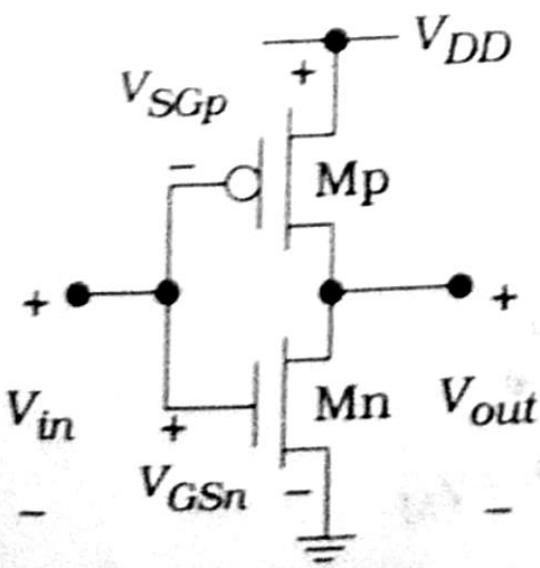


$$V_{OL} = 0 \text{ V}$$

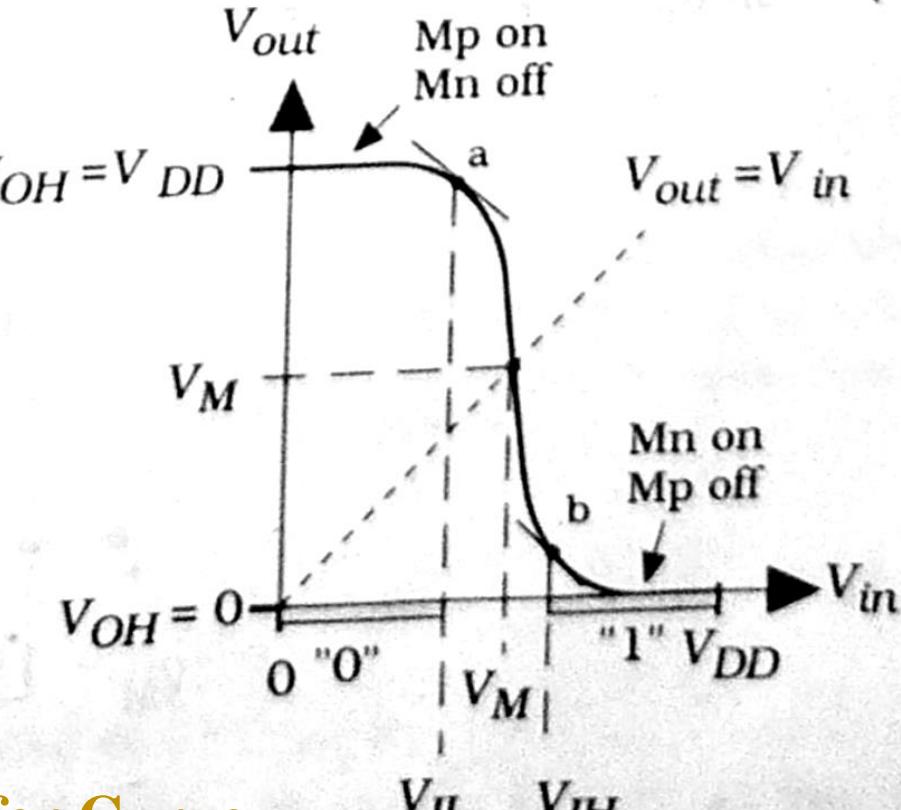
Logic swing of output:

$$V_L = V_{OH} - V_{OL} \\ = V_{DD}$$

## Full rail output



Voltage Transfer Curve



**Logic -0 is defined by**  $0 \leq V_{in} \leq V_{IL}$   
**Logic -1 is defined by**  $V_{IH} \leq V_{in} \leq V_{DD}$

**Voltage Noise Margins are,**

$$VN M_H = V_{OH} - V_{IH} \\ VN M_L = V_{IL} - V_{OL}$$

- Input Voltages:

$$V_{GSn} = V_{in}$$

$$V_{SGp} = V_{DD} - V_{in}$$

- When,  $V_{in}=0$ ,

Mn – Off when  $V_{in} \leq V_{tn}$   
 Mp - On  
 then,  $V_{out}=V_{DD}$

- When, Increasing  $V_{in}$ ,

Downward transition in the VTC  
 Mn-On & Mp- less conductor

- When,  $V_{in} > V_{dd} - V_{tp}$ ,

Mn-On & Mp-Off ; then,  $V_{out}=0$

- The logic 0 and 1 voltage ranges are defined by the **changing slope of the VTC**.

- To calculate the exact voltages for Logic-0 and Logic-1 → midpoint value,
- This is defined as the point where the VTC intersect with the unity gain line.

$$V_{in} = V_{out} = V_M$$

- Drain current,  $I_{Dn} = I_{Dp}$
- Consider nFET,
  - Saturation voltage,  $V_{sat} = V_{GSn} - V_{Tn}$   
 $= V_M - V_{Tn}$

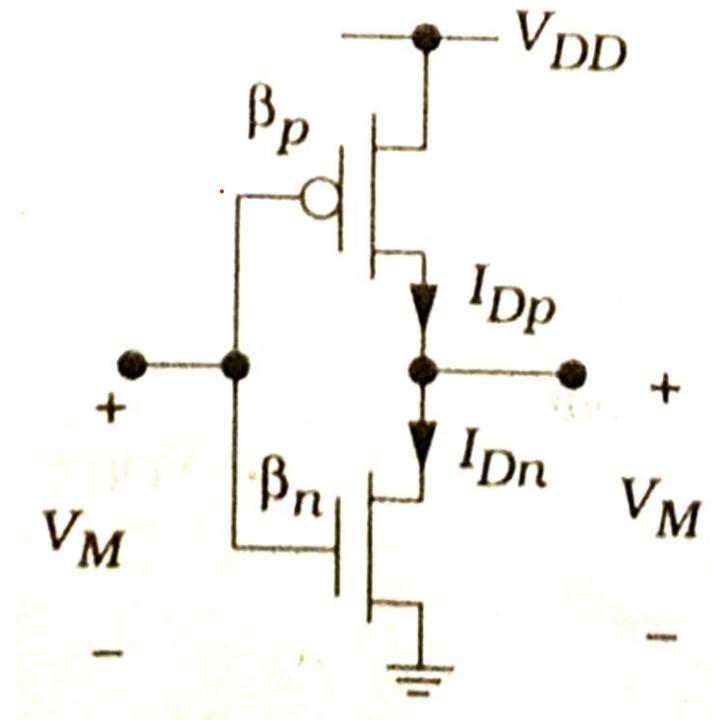
- We used,  $V_{in} = V_{GSn} = V_M$

$$V_{DSn} = V_{out} = V_M$$

- Since  $V_{Tn}$  is Positive,  $V_{DSn} > V_{sat}$  ;  $V_{DSn} > V_M - V_{Tn}$

- **Mn must be saturated.**

- The same can be applied for pFET .  $V_{SGp} = V_{SDp}$ . **Mp also must be saturated**



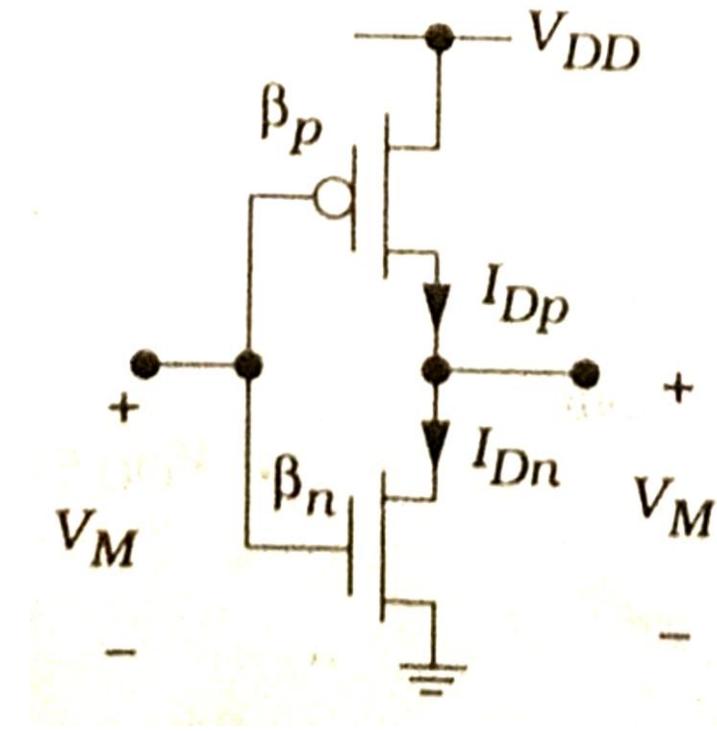
- Drain current,

$$I_{Dn} = I_{Dp}$$

$$I_{Dn} = \frac{\beta_n}{2} (V_{gs} - V_{Tn})^2$$

$$I_{Dp} = \frac{\beta_p}{2} (V_{sg} - |V_{Tp}|)^2$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$



$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$

## Important Observations:

- nFET and pFET have different mobility factors

$$\frac{k'_n}{k'_p} \approx 2 \text{ to } 3$$

- It has significant effect on choices to make both sizes of transistors
- Cox is approximately equal for both the transistors.
- Mobility ratio, r:  $\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r$
- Symmetrical Inverter (equal “0” and “1” input voltages)  $V_M = \frac{1}{2}V_{DD}$

$$\frac{\beta_n}{\beta_p} = \left( \frac{\frac{1}{2}V_{DD} - |V_{Tp}|}{\frac{1}{2}V_{DD} - V_{Tn}} \right)^2$$

Here,  $V_{tn} = |V_{tp}|$  so,  $\beta_n = \beta_p$

**Threshold Voltage, Transconductance** of both the devices are equal

Consider a CMOS process with the following parameters

$$k'_n = 140 \text{ } \mu\text{A}/\text{V}^2$$

$$V_{Tn} = +0.70 \text{ V}$$

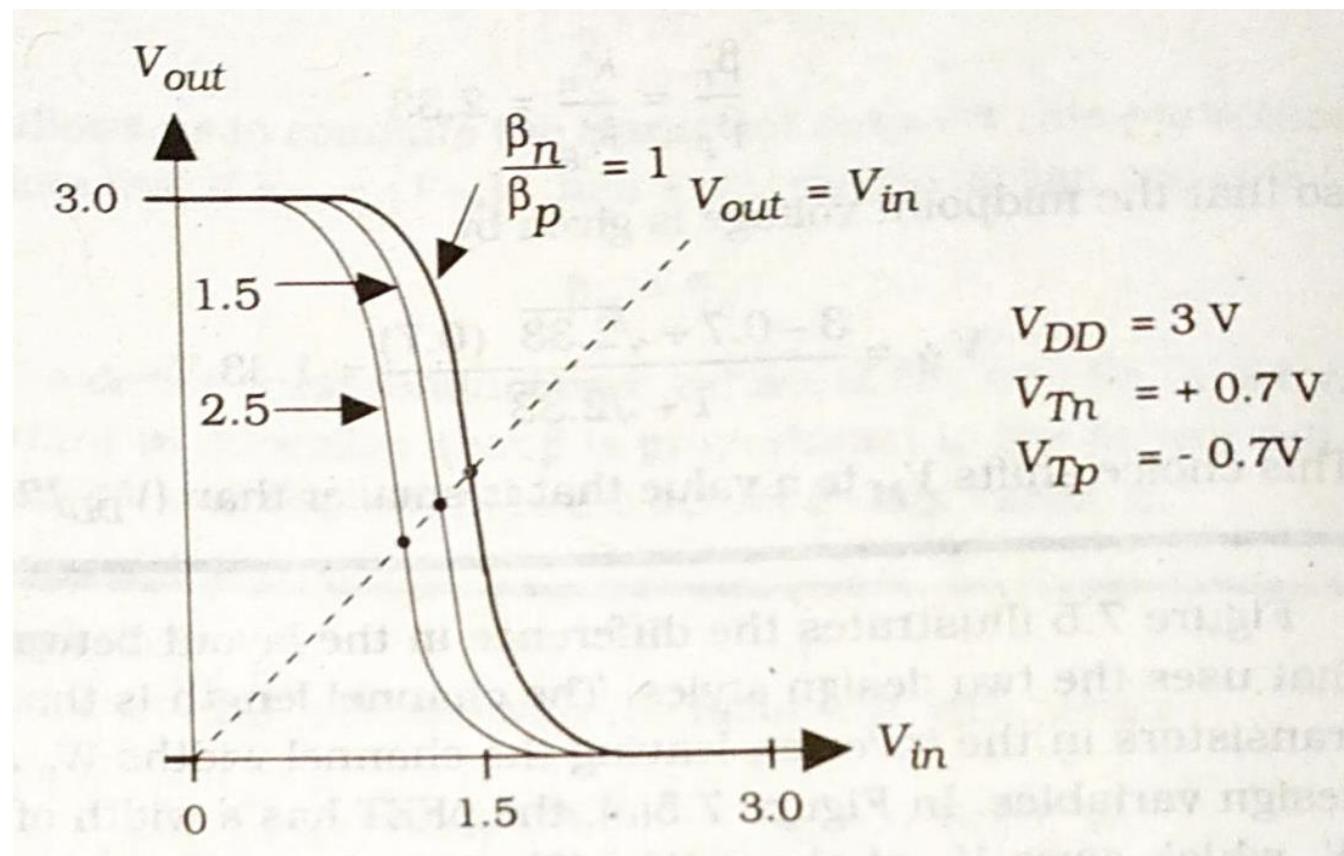
$$k'_p = 60 \text{ } \mu\text{A}/\text{V}^2$$

$$V_{Tp} = -0.70 \text{ V}$$

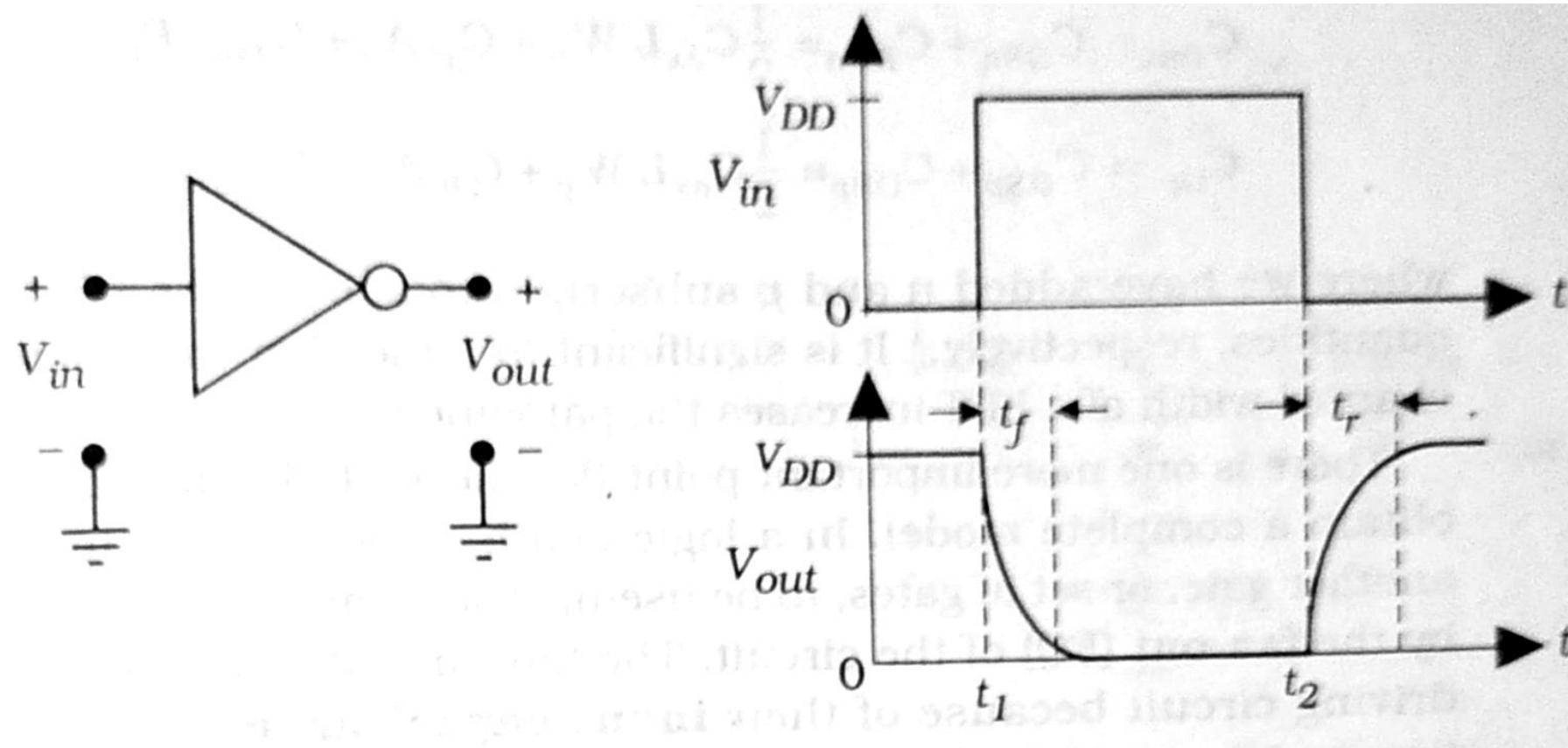
with  $V_{DD} = 3.0 \text{ V}$ .

$$V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

- (i) Verify the symmetrical design
- (ii) Calculate the (W/L) ratio of transistors for symmetrical design
- (iii) Calculate VM value, if both nFET and pFET have same aspect ratio.



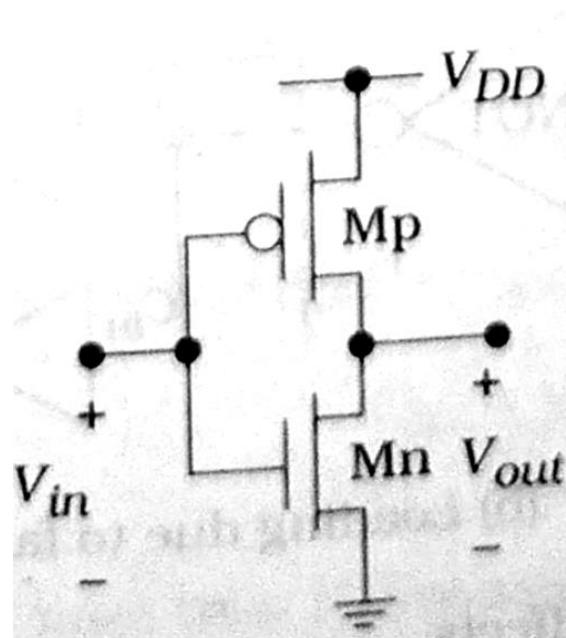
# Inverter Switching Characteristics



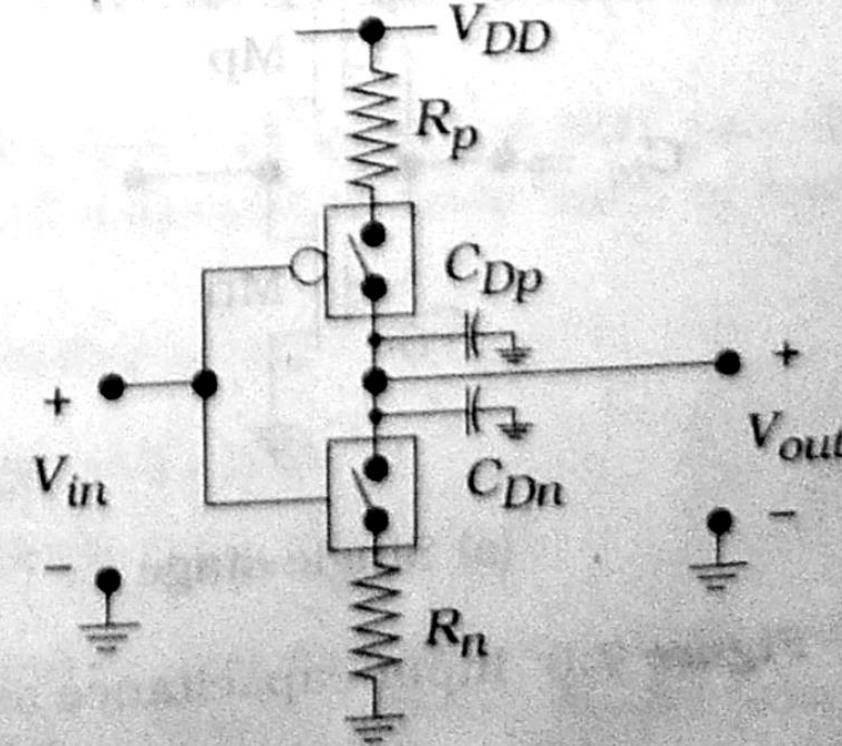
General switching waveforms

**Fall time delay:** 1 to 0 Transition  
**Rise time delay:** 0 to 1 Transition

- **Rise and Fall time delays** : due to Parasitic resistances and Capacitances.



FET Circuit



RC switch model

- once the **aspect ratios (W/L)n and (W/L)p** are specified, we can calculate  $R_n$  and  $R_p$  using equations:

$$R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})} \quad R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)}$$

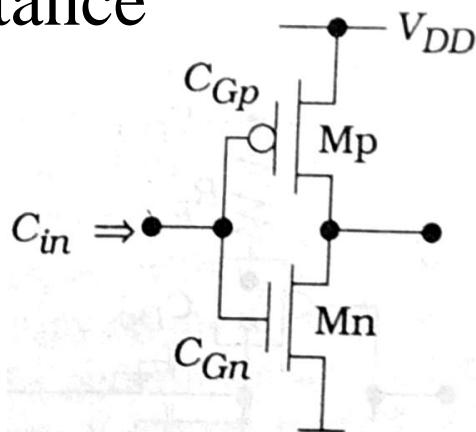
- Knowing the layout dimensions of each FET allows us to find the Parasitic Capacitance  $C_{Dn}$  and  $C_{Dp}$  at the output node as:

$$C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2}C_{ox}L'W_n + C_{jn}A_n + C_{jswn}P_n$$

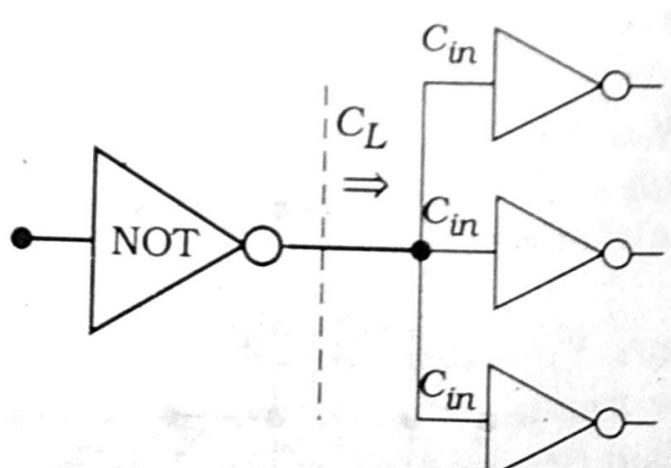
$$C_{Dp} = C_{GSp} + C_{DBp} = \frac{1}{2}C_{ox}L'W_p + C_{jp}A_p + C_{jswp}P_p$$

- Fanout :

- Every logic gate must drive another gate or set of logic gate
- Fanout gates act as a load to the driver circuit because of the input capacitance



(a) Single stage



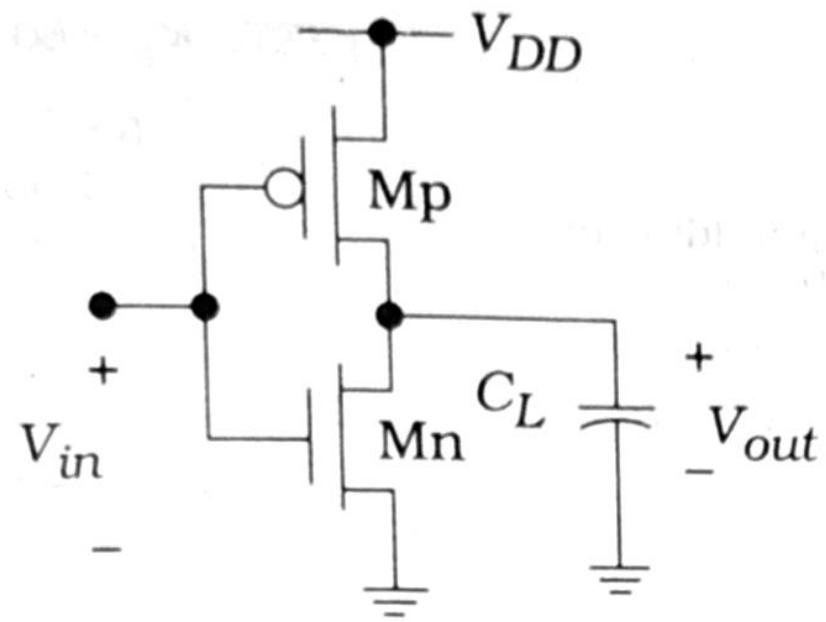
(b) Loading due to fan-out

**Input Cap,  $C_{in}$ :**

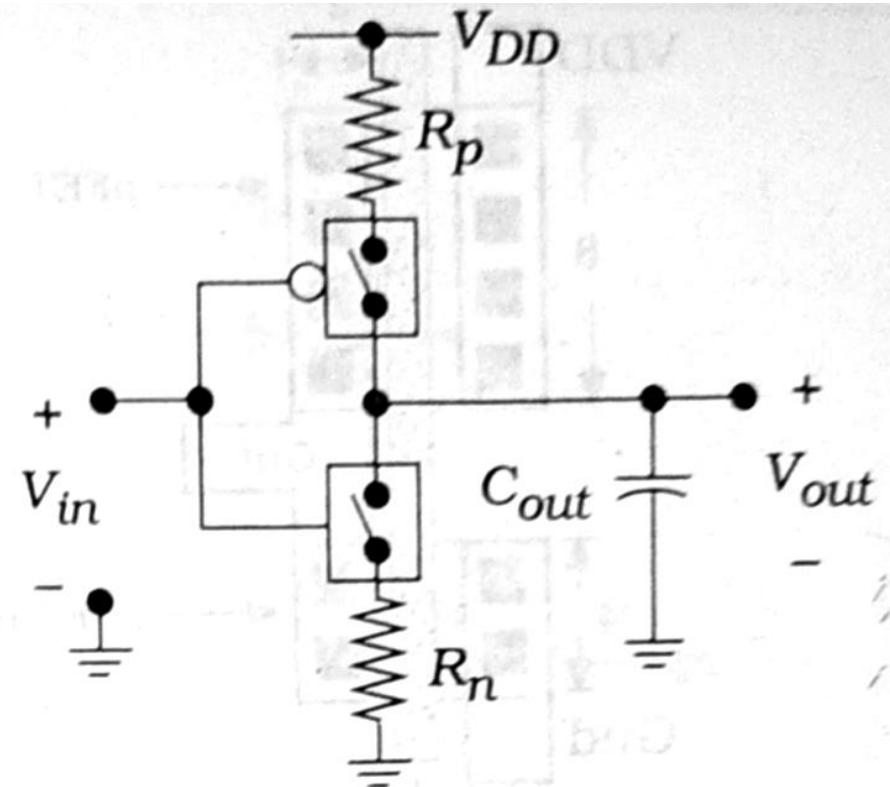
$$C_{in} = C_{Gp} + C_{Gn}$$

**External Load Cap,  $C_L$ :**

$$C_L = 3C_{in}$$



**External load**



**Complete switching model**

- Total output Capacitance,  $C_{out} = C_{FET} + C_L$   
where,  $C_{FET} = C_{Dn} + C_{Dp}$

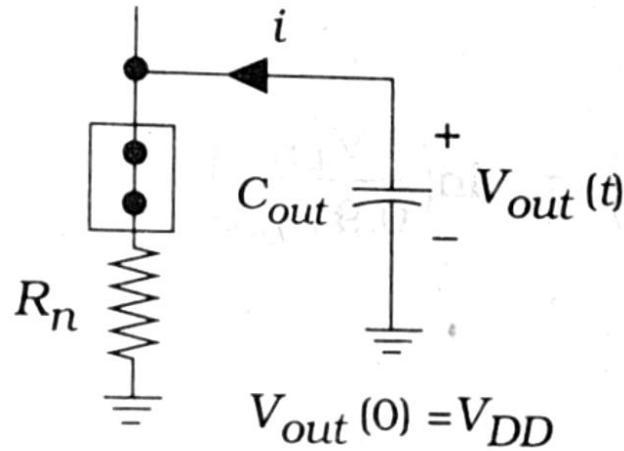
# Fall Time Calculation

When  $V_{in}$  changes from 0 to  $V_{DD}$ ,

PFET- cut-off

NFET - Active

pFET off



$V_{out}(t)$

$V_{DD}$

$V_1$

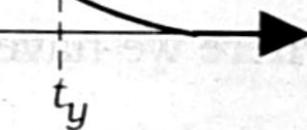
$V_0$

0

$t_x$

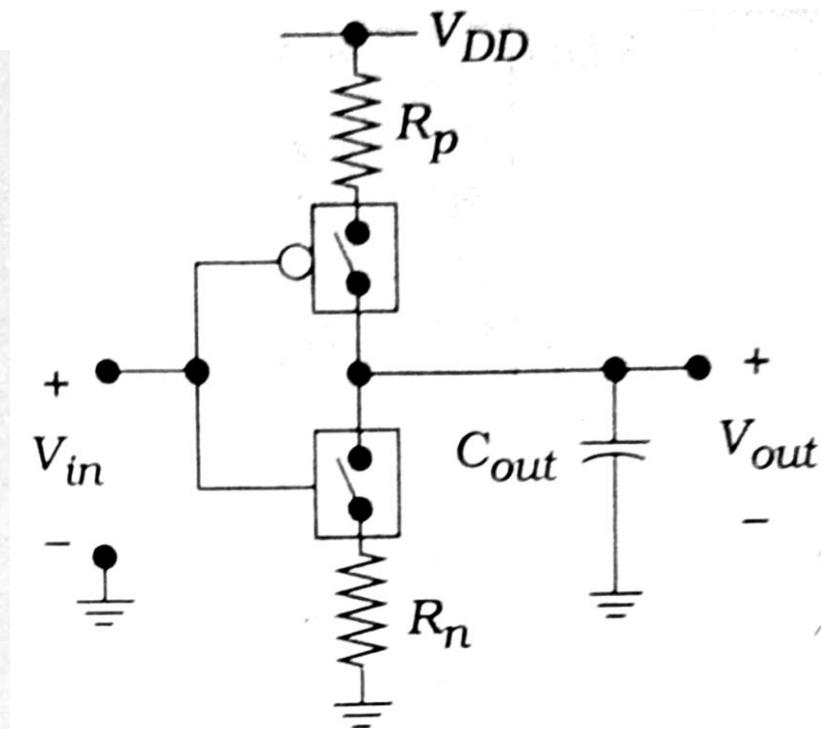
$t_y$

$t_f$



(a) Discharge circuit

(b) Output waveform



- The current leaving the capacitor:  $i = -C_{out} \frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$
- Solving with initial condition,  $V_{out}(0) = V_{DD}$
- We will get,  $V_{out}(t) = V_{DD} e^{-t/\tau_n}$  where,  $\tau_n = R_n C_{out}$  (**time constant**)

- Fall time defined with time interval from  $V_1=0.9V_{DD}$  to  $V_0=0.1V_{DD}$

(90% and 10% of full rail swing of  $V_{DD}$ )

$$V_{out}(t) = V_{DD} e^{-t/\tau_n}$$

$$\frac{V_{out}}{V_{DD}} = e^{-t/\tau_n}$$

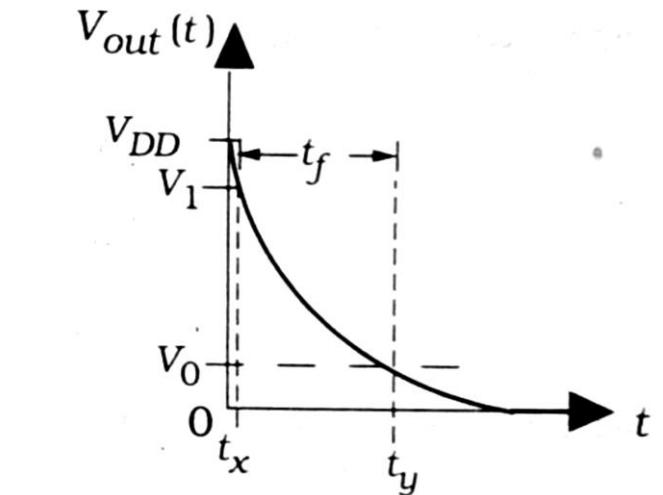
$$\frac{V_{DD}}{V_{out}} = e^{t/\tau_n}$$

$$\ln \left| \frac{V_{DD}}{V_{out}} \right| = t/\tau_n$$

$$\boxed{\tau_n \ln \left| \frac{V_{DD}}{V_{out}} \right| = t}$$

$$t = \tau_n \ln \left( \frac{V_{DD}}{V_{out}} \right)$$

$$\begin{aligned} t_f &= t_y - t_x \\ &= \tau_n \ln \left( \frac{V_{DD}}{0.1V_{DD}} \right) - \tau_n \ln \left( \frac{V_{DD}}{0.9V_{DD}} \right) \\ &= \tau_n \ln(9) \\ t_f &\approx 2.2\tau_n \end{aligned}$$

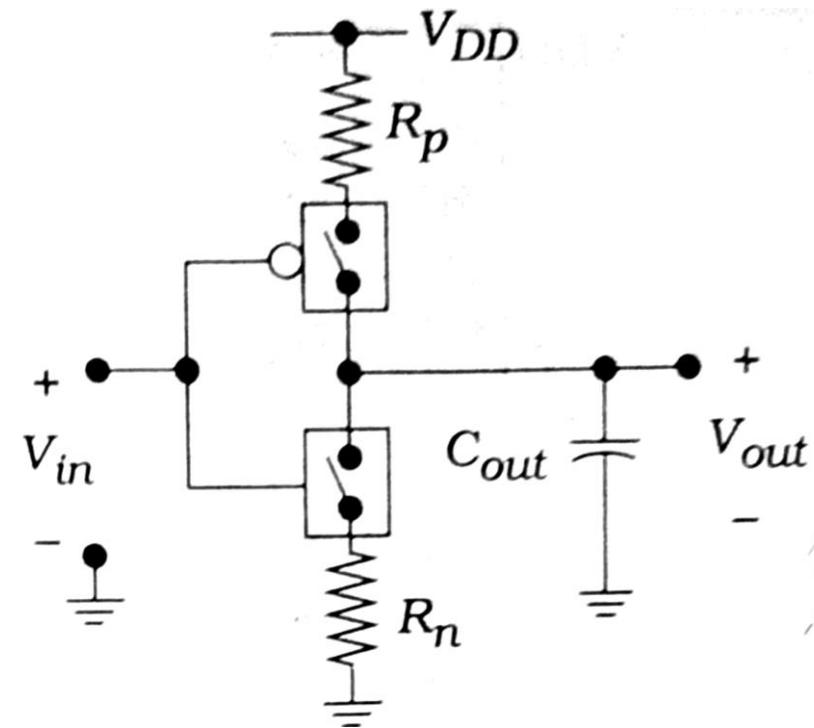
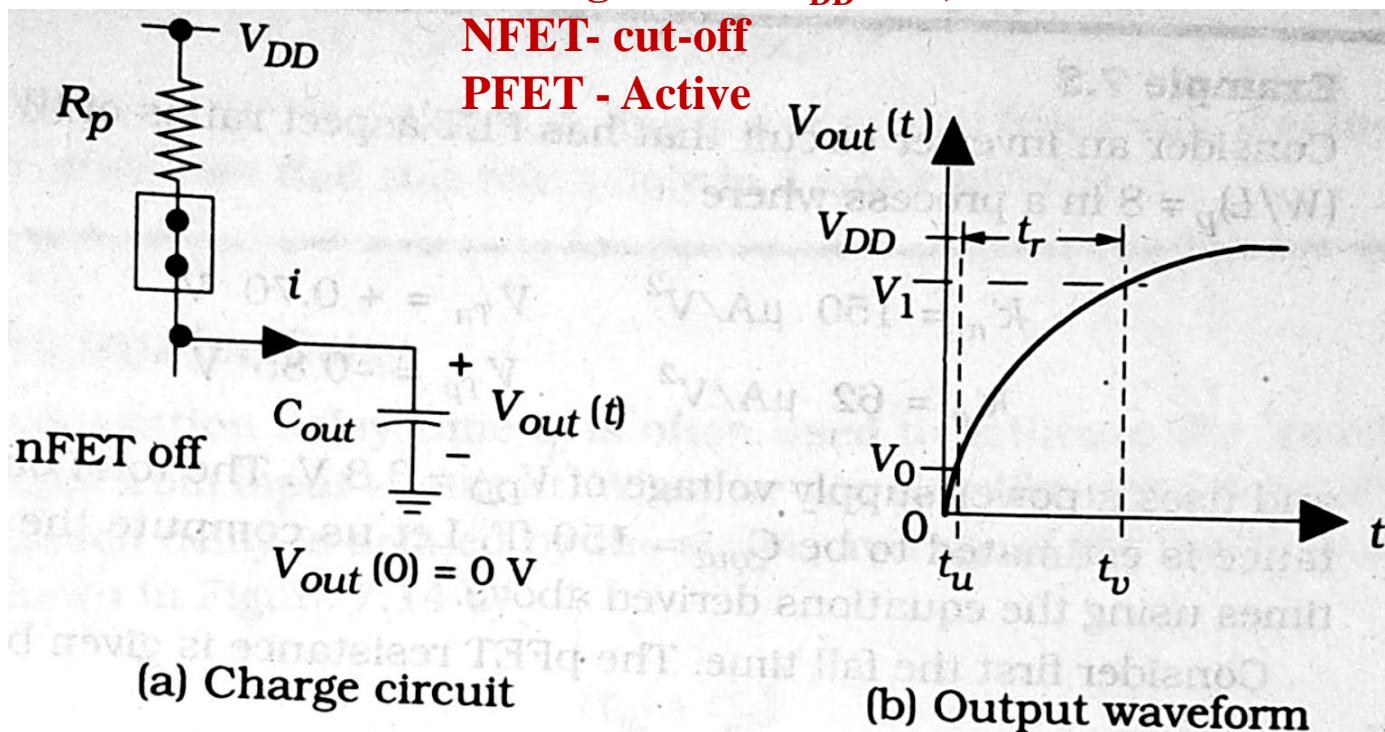


**High to low time,  $t_{HL}$**

$$t_{HL} = t_f$$

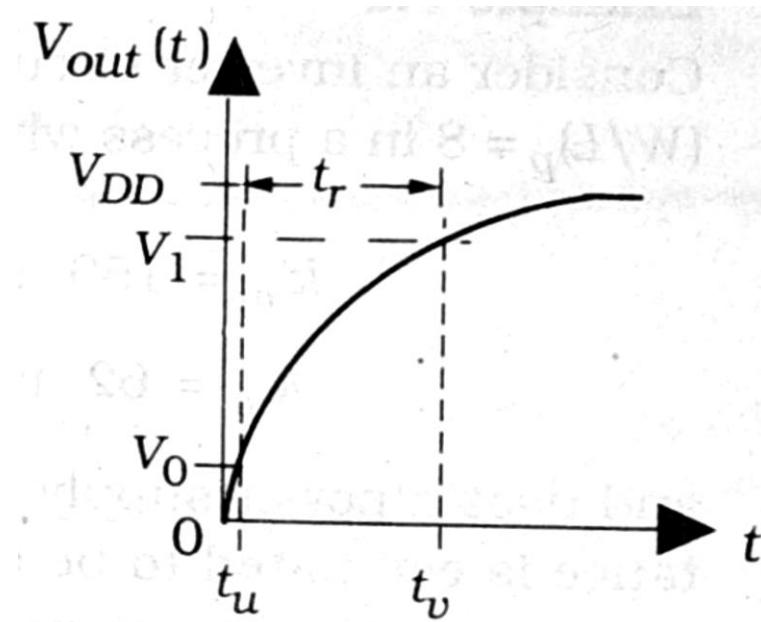
# Rise Time Calculation

When  $V_{in}$  changes from  $V_{DD}$  to 0,



- The current leaving the capacitor:  $i = C_{out} \frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_p}$
- Solving with initial condition,  $V_{out}(0) = V_{DD}$
- We will get,  $V_{out}(t) = V_{DD}[1 - e^{-t/\tau_p}]$  where,  $\tau_p = R_p C_{out}$  (**time constant**)

- Rise time defined with time interval from  $V_1=0.9V_{DD}$  to  $V_0=0.1V_{DD}$



$$t_r = t_v - t_u$$

$$t_r = \ln(9)\tau_p \approx 2.2\tau_p$$

**Low to high time,  $t_{LH}$**

# Maximum Signal Frequency

- Maximum signal frequency is define as,

$$f_{max} = \frac{1}{t_{HL} + t_{LH}} = \frac{1}{t_r + t_f}$$

- Largest frequency applied to the gate
  - Allow the output to settle to a definable state.
- If the Signal frequency exceeds  $f_{max}$ , **Output voltage of the gate will not have sufficient time to stabilize**

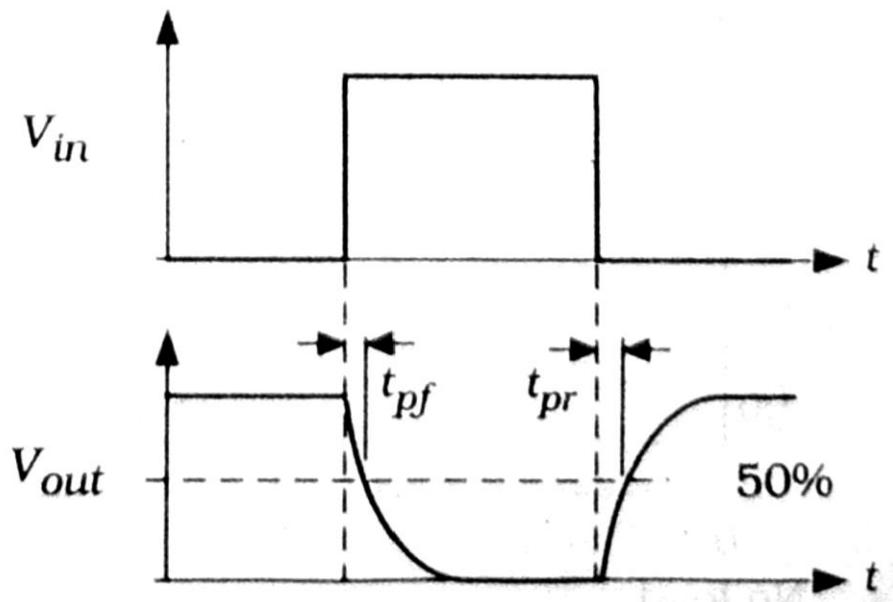
- Consider an inverter circuit that has FET aspect ratios of  $(W/L)_n = 6$  and  $(W/L)_p = 8$  in a process where,  $V_{dd} = 3.3V$ ,  $C_{out} = 150fF$ .

$$k_n = 150 \text{ } \mu\text{A/V}^2 \quad V_{Tn} = + 0.70 \text{ } \text{V}$$
$$k_p = 62 \text{ } \mu\text{A/V}^2 \quad V_{Tp} = -0.85 \text{ } \text{V}$$

- Calculate the rise time, fall time and maximum frequency.

# The Propagation Delay

- $t_p$ , used to estimate the “**reaction**” delay time from input to output.
- When we use step-like input voltages, the **propagation delay is defined by the simple average of the two time intervals**.
- Propagation delay time is a useful **estimate of the basic delay**.



$$t_p = \frac{(t_{pf} + t_{pr})}{2}$$

Where,

$t_{pf}$  = Propagation fall time

$t_{pr}$  = Propagation rise time

$$t_{pf} = \ln(2)\tau_n$$
$$t_{pr} = \ln(2)\tau_p$$

$$t_p \approx 0.35(\tau_n + \tau_p)$$

# General Analysis:

- Output capacitances,  $C_{out}$

$$C_{out} = C_{FET} + C_L$$

- Rise and Fall time equations,

$$t_r \approx 2.2R_p(C_{FET} + C_L)$$

$$t_f \approx 2.2R_n(C_{FET} + C_L)$$

$$t_r = t_{r0} + \alpha_p C_L$$

$$\alpha_p = 2.2R_p = \frac{2.2}{\beta_p(V_{DD} - |V_{TP}|)}$$

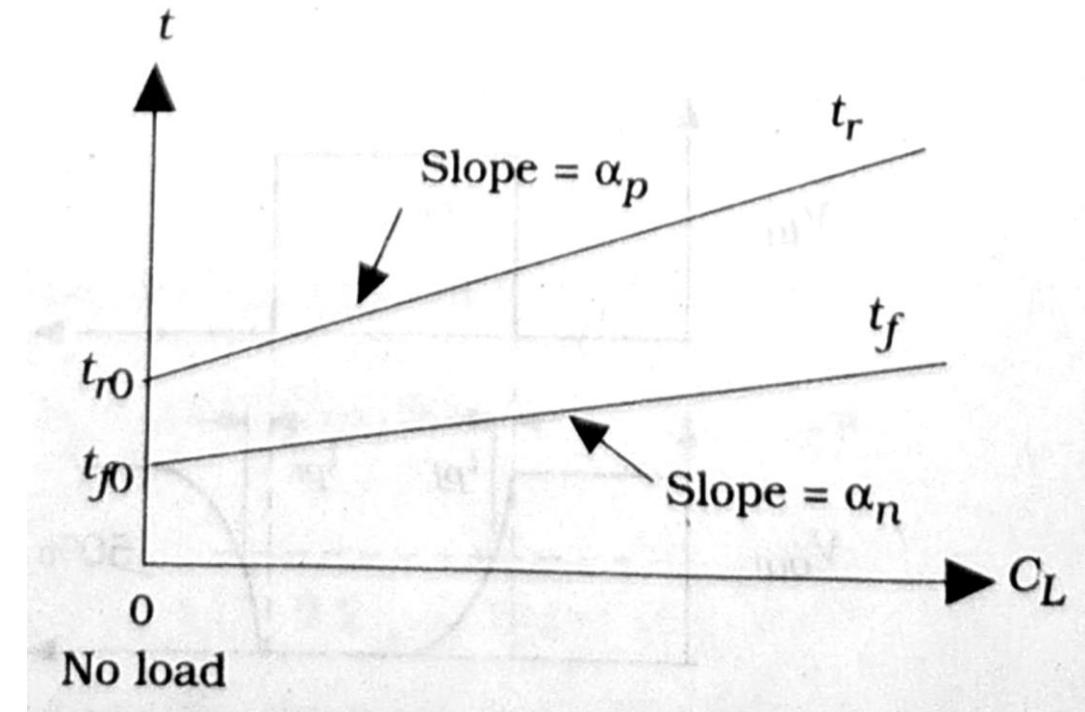
$$t_f = t_{f0} + \alpha_n C_L$$

$$\alpha_n = 2.2R_n = \frac{2.2}{\beta_n(V_{DD} - V_{TN})}$$

- Under zero load conditions ( $C_L=0$ )

$$t_r = t_{r0} \approx 2.2R_p C_{FET}$$

$$t_f = t_{f0} \approx 2.2R_n C_{FET}$$



$$\beta \uparrow \Rightarrow R \downarrow \Rightarrow t \downarrow$$

speed versus area trade-off which says that  
“Fast circuits consume more area than slow circuits”

# Power Dissipation

- Power dissipation calculation

- $P = V_{DD} I_{DD}$

- $P = P_{DC} + P_{dyn}$

- $P_{DC}$ : DC power

- Region A, E:  $I_{DD} = 0$

- Actually, there is leakage current  $I_{DDQ}$ .

- »  $I_{DDQ}$ : quiescent leakage current

- $P_{DC} = V_{DD} I_{DDQ}$

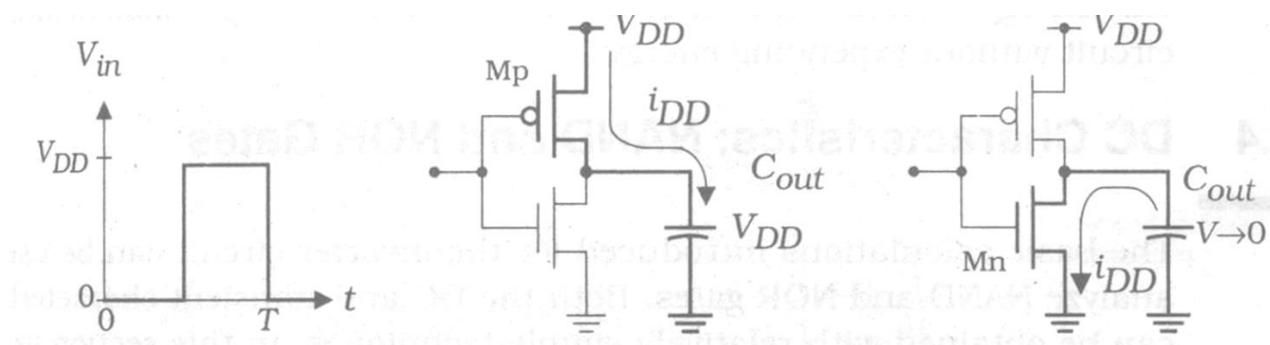
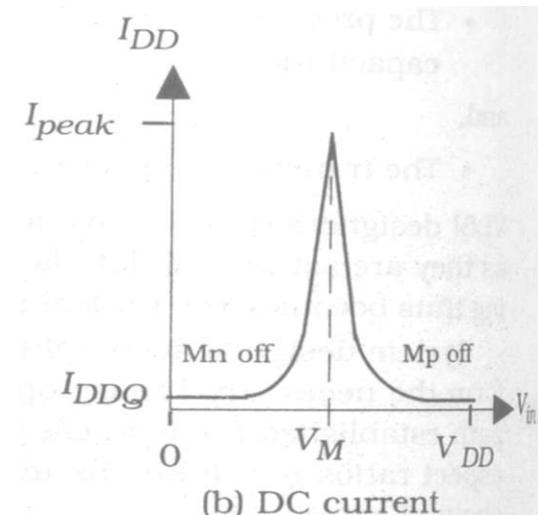
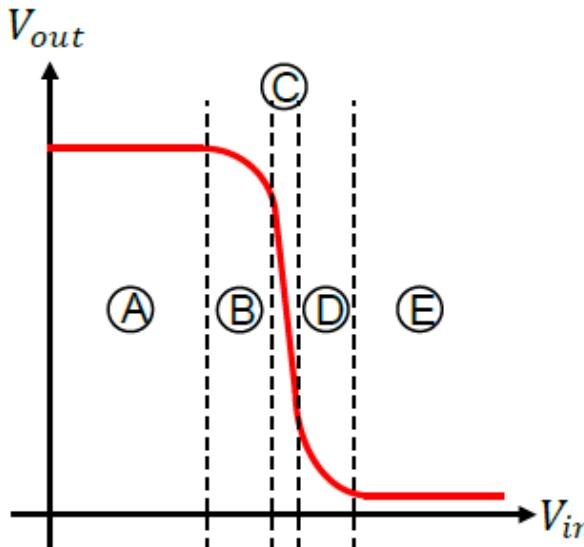
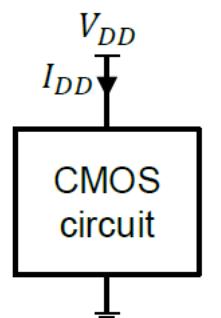
- $P_{dyn}$ : Dynamic power

- Charging/Discharging

Stored electric charge,  $Q_e = C_{out} V_{DD}$

- $P = V_{DD} I_{DD} = V_{DD} \left( \frac{Q_e}{T} \right) = f C_{out} V_{DD}^2$

- $$P = V_{DD} I_{DDQ} + f C_{out} V_{DD}^2$$



(a) Input voltage

(b) Charge injection

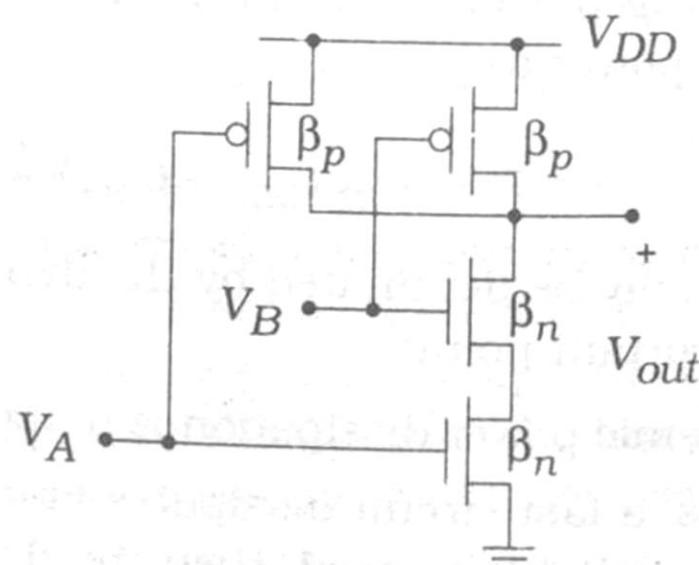
(c) Discharge

The dynamic power dissipation is proportional to the signal frequency

**A fast circuit dissipates more power than slow circuit.**

# DC Characteristics of NAND and NOR gates

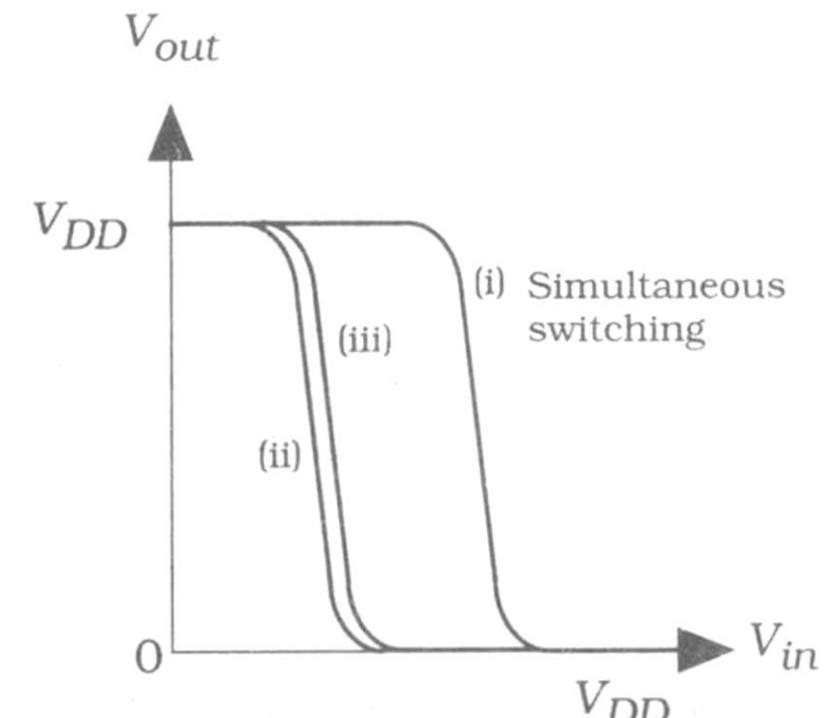
## NAND2 – DC Characteristics:



	$V_A$	$V_B$	$V_{out}$
(i)	0	0	$V_{DD}$
(ii)	0	$V_{DD}$	$V_{DD}$
(iii)	$V_{DD}$	0	$V_{DD}$
	$V_{DD}$	$V_{DD}$	0

(a) Transition table

$V_{out}$  is initially high at  $V_{DD}$  and then falls to 0V



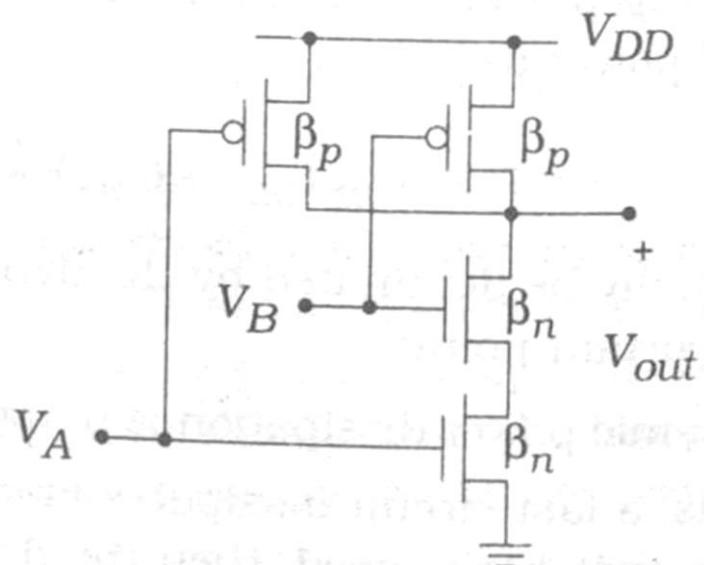
(b) VTC family

simultaneous switching case is “pushed to the right” compared to the single-switched input cases.

- “merge” the two transistors together into one
  - series connected transistors :  $\frac{W}{2L} \rightarrow \frac{\beta}{2}$
  - Parallel connected transistors :  $\frac{2W}{L} \rightarrow 2\beta$

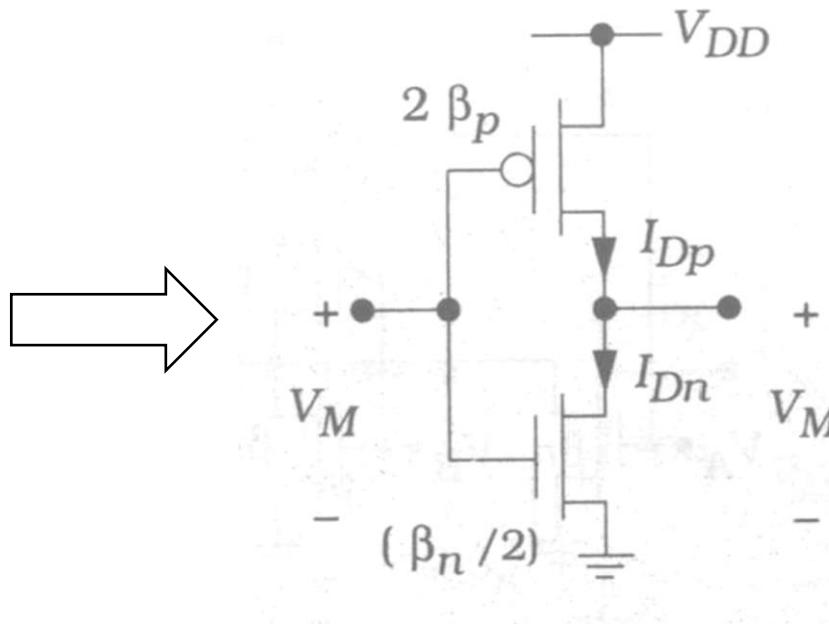
## NAND2 – DC Characteristics:

- To calculate the value of the midpoint voltage,  $V_M$



$$V_M \quad (V_{in} = V_{out} = V_M)$$

- nFET network:  $\frac{\beta_n}{2}$
- pFET network:  $2\beta_p$



$$I_{DSn} = \frac{(\frac{\beta_n}{2})}{2} (V_M - V_{Tn})^2$$

$$I_{SDp} = \frac{(2\beta_p)}{2} (V_{DD} - V_M - |V_{Tp}|)^2$$

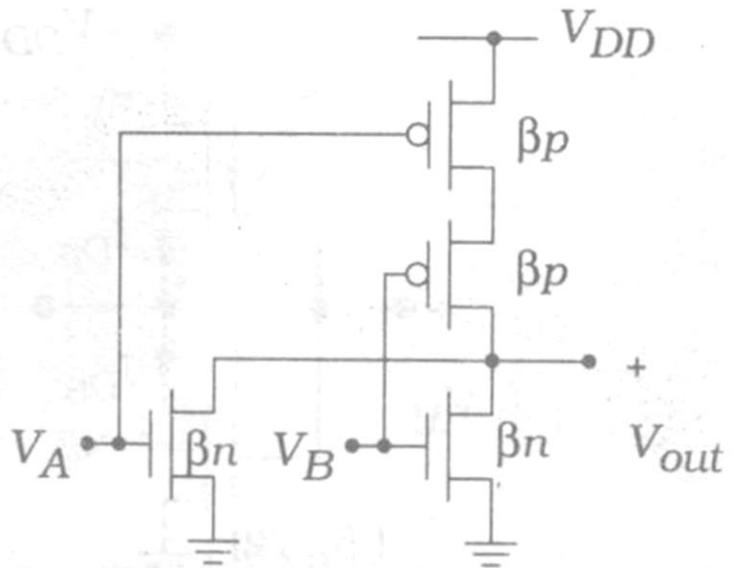
Solve  $I_{DSn} = I_{SDp}$ .

$$V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{2}V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}}$$

- $V_M$  is same form as the NOT gate, except that the square root term is multiplied by a factor of (1/2).
- This reduces the denominator, which is why the **VTC curve is shifted toward the right**.
- For k-input NAND,

$$V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{k}V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{k}\sqrt{\frac{\beta_n}{\beta_p}}}$$

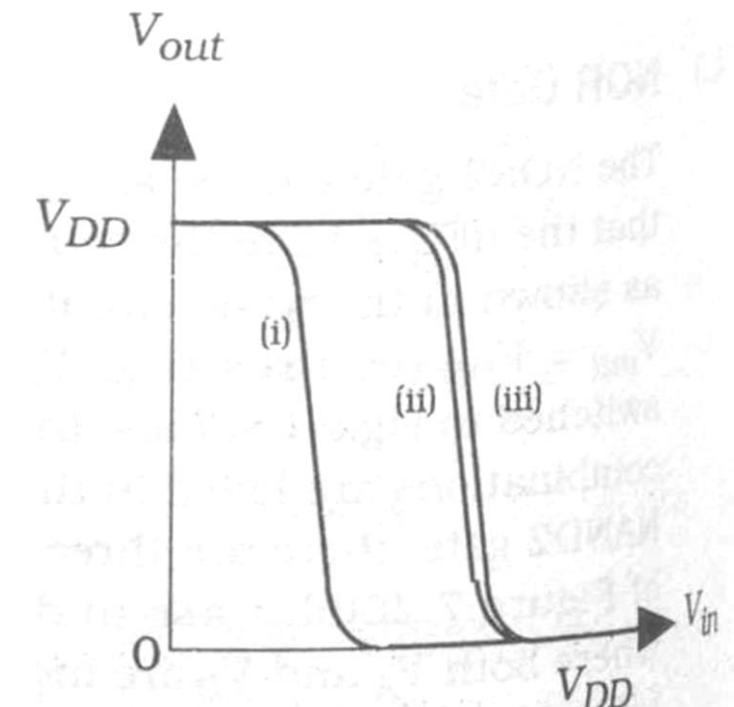
## NOR2 – DC Characteristics:



$V_A$	$V_B$	$V_{out}$
0	0	$V_{DD}$
0	$V_{DD}$	0
$V_{DD}$	0	0
$V_{DD}$	$V_{DD}$	0

(a) Transition table

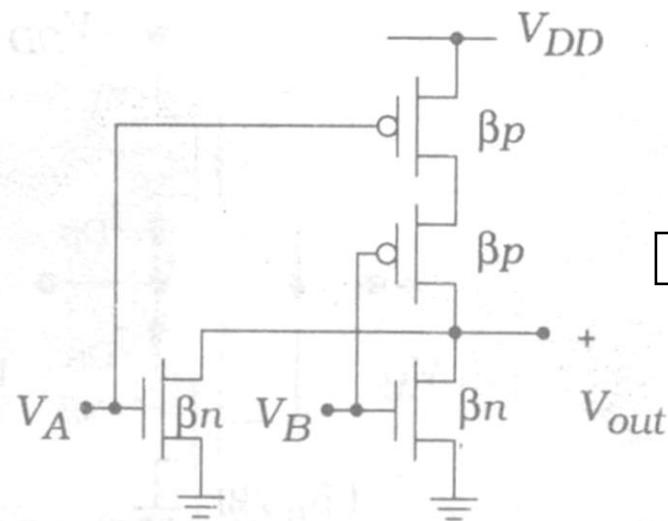
$V_{out}$  is initially low and then rise to  $V_{DD}$



(b) VTC family

simultaneous switching case is “pushed to the left” compared to the single-switched input cases.

- To calculate the value of the midpoint voltage,  $V_M$

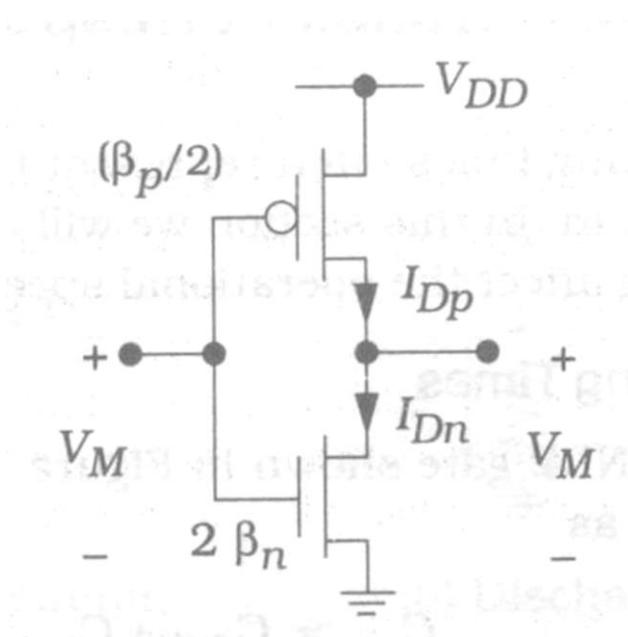


$V_M$  ( $V_{in} = V_{out} = V_M$ )  
 - nFET network:  $2\beta_n$   
 - pFET network:  $\frac{\beta_p}{2}$

$$I_{DSn} = \frac{2\beta_n}{2} (V_M - V_{Tn})^2$$

$$I_{SDp} = \frac{(\frac{\beta_p}{2})}{2} (V_{DD} - V_M - |V_{Tp}|)^2$$

Solve  $I_{DSn} = I_{SDp}$ .



$$V_M = \frac{V_{DD} - |V_{Tp}| + 2V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1+2\sqrt{\frac{\beta_n}{\beta_p}}}$$

- Comparing this with the NOT and NAND expressions shows that the only difference is the factor of 2 multiplying the square root term.
- This increases the denominator, which decreases the value of  $V_M$
- For k-input NAND,

$$V_M = \frac{V_{DD} - |V_{Tp}| + kV_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1+k\sqrt{\frac{\beta_n}{\beta_p}}}$$

# Power dissipation of NAND and NOR gates

- NAND and NOR gates exhibit **low DC power dissipation** values of

$$P_{DC} = V_{DD} I_{DDQ}$$

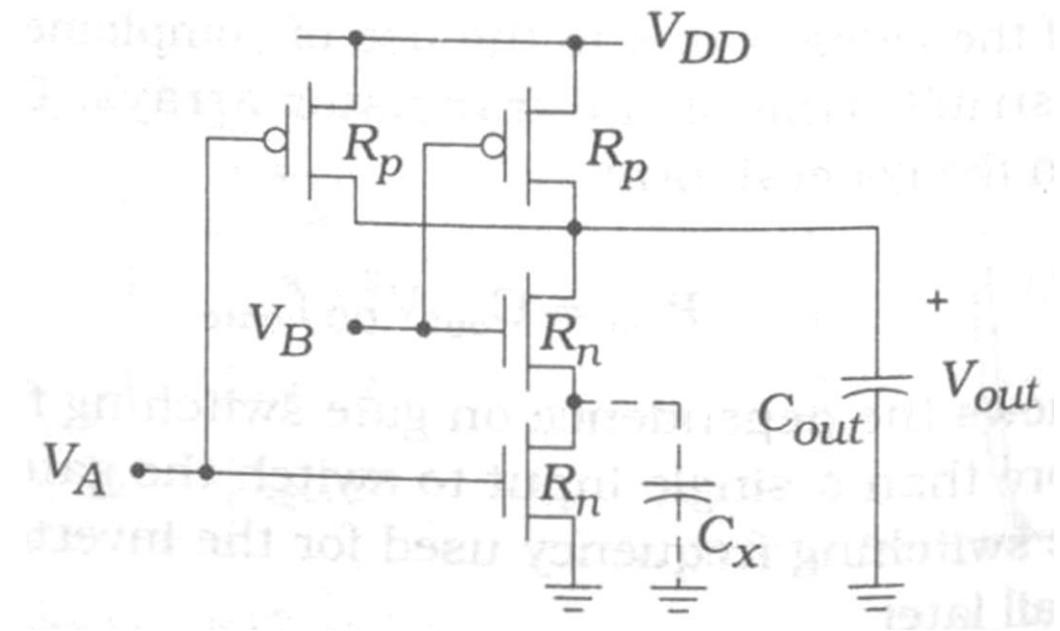
- There is **no direct current flow path from the power supply to ground** when the inputs are stable logic 0 or logic 1 values.
- Dynamic power is still Present in the general form

$$P_{sw} = C_{out} V_{DD}^2 f_{gate}$$

- which shows the **dependence on gate switching frequency gate**.
- Since it takes more than a **single input to switch the gate**,  $f_{gate}$  is different from the basic Switching frequency used for the inverter.

# NAND2 – Switching Characteristics

- $t_r$ : rise time
- $t_f$ : fall time
- $C_{out}$ : total output capacitance
  - $C_{out} = C_{FET} + C_L$ 
    - $C_{FET}$ : FET capacitance
      - $C_{FET} = C_{Dn} + 2C_{Dp}$ 
        - »  $C_{Dn} = C_{GSn} + C_{DBn}$
        - »  $C_{Dp} = C_{GSp} + C_{DBp}$
      - $C_L$ : load capacitance
      - $C_x$ : parasitic capacitance



- **Rise time** The output voltage is initially at 0V and then charged to  $V_{DD}$

- If  $AB: 11 \rightarrow 00$  (best case)

- $V_{out}(t) = V_{DD} \left(1 - e^{-\frac{t}{\tau_p}}\right)$   
 $\tau_p = \frac{R_p}{2} C_{out}$

- $t_r \approx 2.2\tau_p$

If both pFETs are conducting, then the equivalent resistance is lowered to ( $R_p/2$ ) since the two are in parallel; this would be the “best-case” event.

- If  $AB: 11 \rightarrow 10$  or  $AB: 11 \rightarrow 01$  (worst case)

- $V_{out}(t) = V_{DD} \left(1 - e^{-\frac{t}{\tau_p}}\right)$   
 $\tau_p = R_p C_{out}$

- $t_r \approx 2.2\tau_p$

- $t_r = 2.2R_p(C_{FET} + C_L)$

The zero load value,

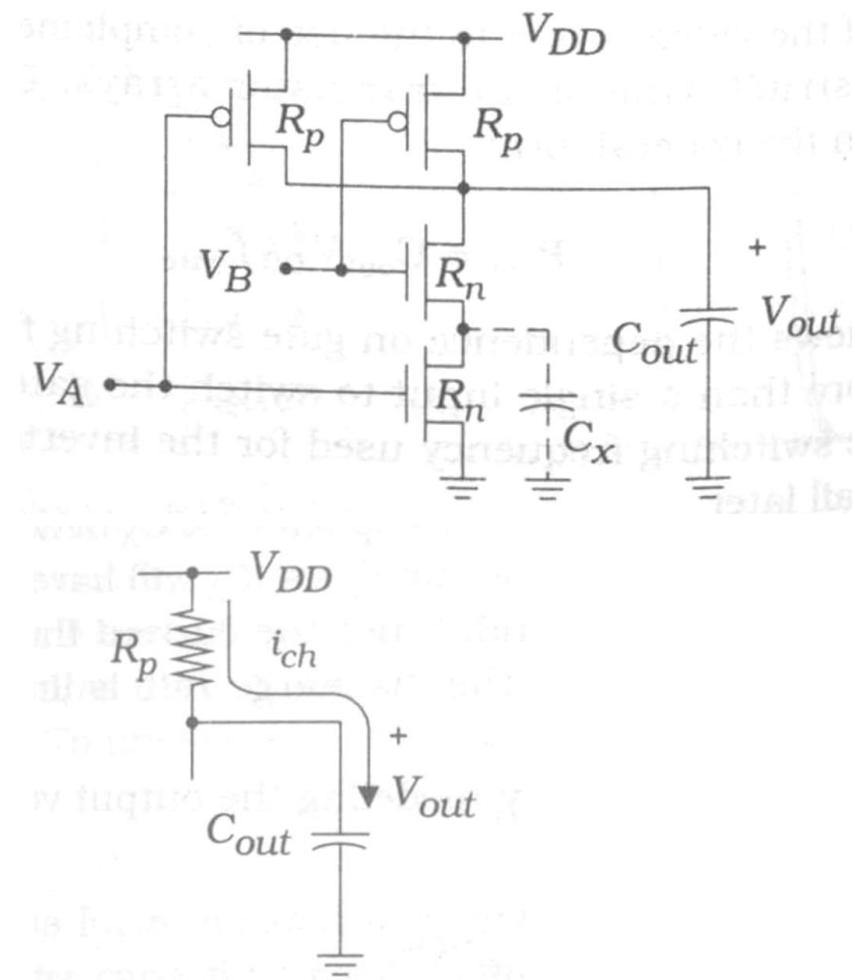
$$t_r = t_{r0} \approx 2.2R_p C_{FET}$$

$$t_r = t_0 + \alpha_0 C_L$$

Where,

$$t_0 = 2.2R_p C_{FET}$$

$$\alpha_0 = 2.2R_p$$



(a) Charging circuit

**Fall time:** The output voltage is initially at  $V_{DD}$  and then discharged to 0V

$$V_{out}(t) = V_{DD} e^{-t/\tau_n}$$

$$\tau_n = C_{out}(R_n + R_n) + C_x R_n$$

$$\tau_n = \tau_{n1} + \tau_{n2}$$

Time constant for  $C_{out}$  discharging through two nFETs,

$$\tau_{n1} = C_{out}(R_n + R_n)$$

Time constant for  $C_x$  discharging through one nFETs,

$$\tau_{n2} = C_x R_n$$

$$\tau_n = R_n(2C_{out} + C_x)$$

$$C_{eff} = 2C_{out} + C_x$$

$$\tau_n = C_{out}(2R_n) + C_x R_n$$

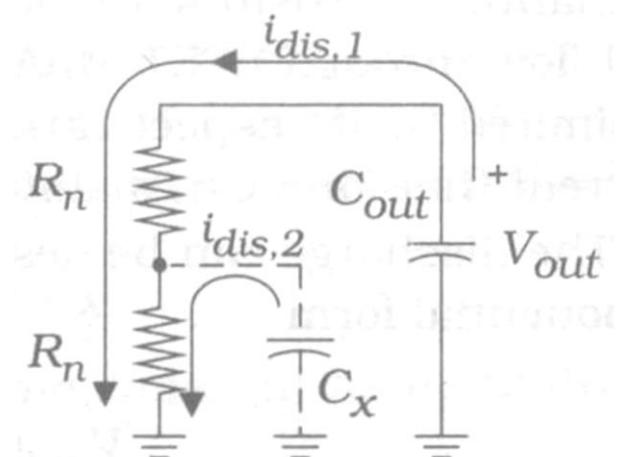
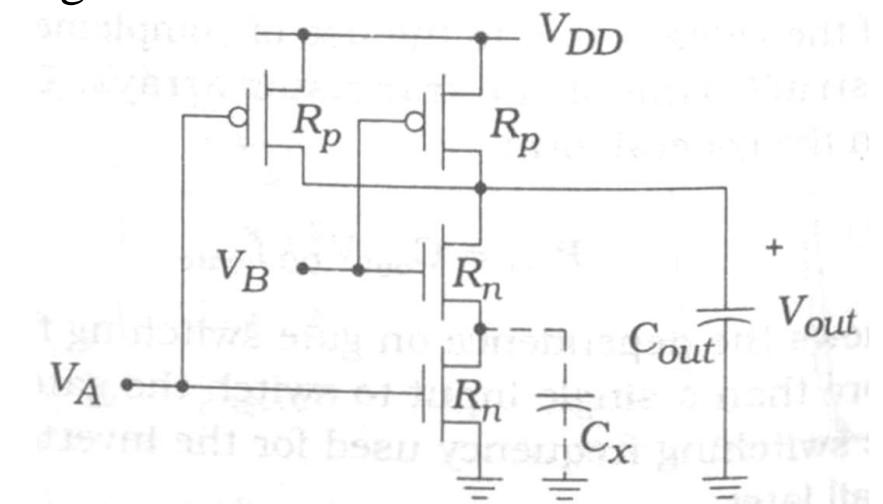
$$t_f \approx 2.2\tau_n$$

$$t_f = 2.2[2R_n(C_{FET} + C_L)] + 2.2R_nC_x$$

$$t_f = t_1 + \alpha_1 C_L$$

$$t_1 = 2.2R_n(2C_{FET} + C_x)$$

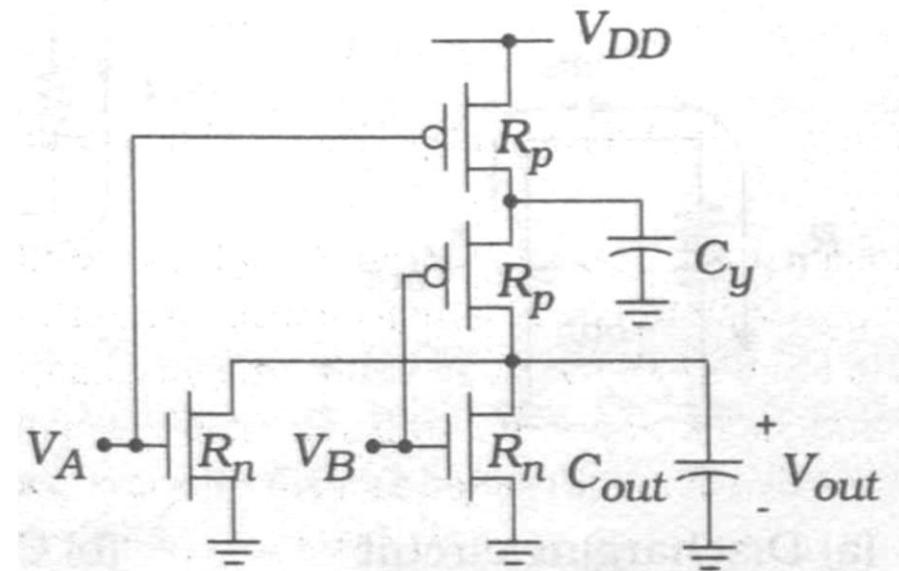
$$\alpha_1 = 4.4 R_n$$



(b) Discharging circuit

# NOR2 – Switching Characteristics

- $t_r$ : rise time
- $t_f$ : fall time
- $C_{out}$ : total output capacitance
  - $C_{out} = C_{FET} + C_L$ 
    - $C_{FET}$ : FET capacitance
      - $C_{FET} = 2C_{Dn} + C_{Dp}$ 
        - »  $C_{Dn} = C_{GSn} + C_{DBn}$
        - »  $C_{Dp} = C_{GSp} + C_{DBp}$
      - $C_L$ : load capacitance
    - $C_y$ : parasitic capacitance



- Fall time

- If  $AB:00 \rightarrow 11$  (best case)

- $V_{out}(t) = V_{DD} e^{-\frac{t}{\tau_n}}$
  - $\tau_n = \frac{R_n}{2} C_{out}$
  - $t_f \approx 2.2\tau_n$

If both nFETs are conducting, then the equivalent resistance is lowered to ( $R_n/2$ ) since the two are in parallel; this would be the “best-case” event.

- If  $AB:00 \rightarrow 10$  or  $AB:00 \rightarrow 01$  (worst case)

- $V_{out}(t) = V_{DD} e^{-\frac{t}{\tau_n}}$
  - $\tau_n = R_n C_{out}$
  - $t_f \approx 2.2\tau_n$

- $t_f = 2.2R_n C_{out}$

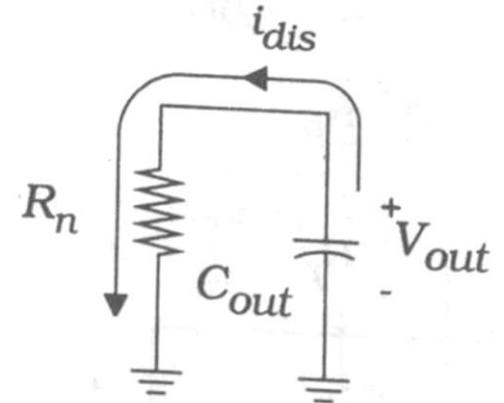
$$t_f = t_1 + \alpha_1 C_L$$

$$t_1 = 2.2R_n C_{FET}$$

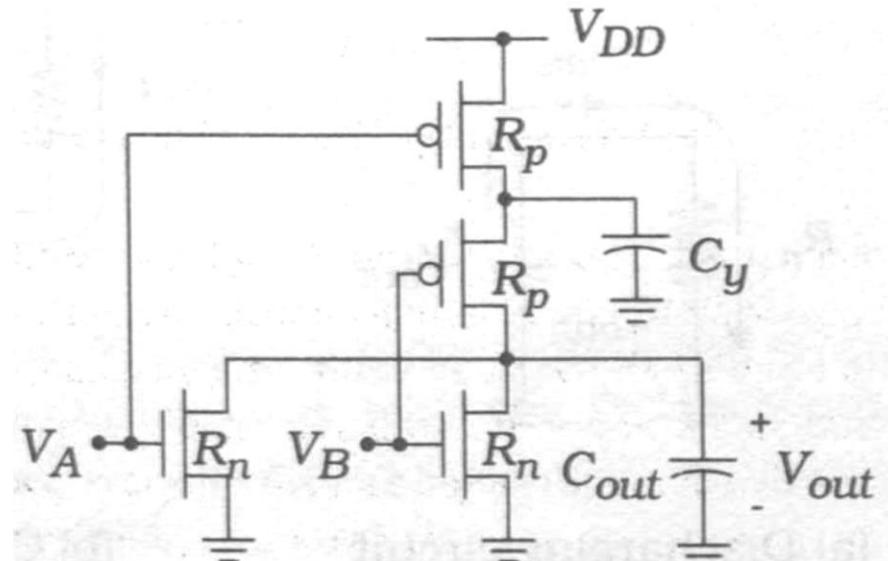
$$\alpha_1 = 2.2R_n$$

The zero load value,

$$t_1 = 2.2R_n C_{FET}$$



(a) Discharging circuit



## Rise time:

$$V_{out}(t) = V_{DD} \left(1 - e^{-\frac{t}{\tau_p}}\right)$$

$$\tau_p = 2R_p C_{out} + R_p C_y$$

time constant for  $C_{out}$  charging through two pFETs

$$\tau_1 = C_{out}(R_p + R_p)$$

time constant for  $C_x$  charging through one pFETs

$$\tau_2 = C_y R_p$$

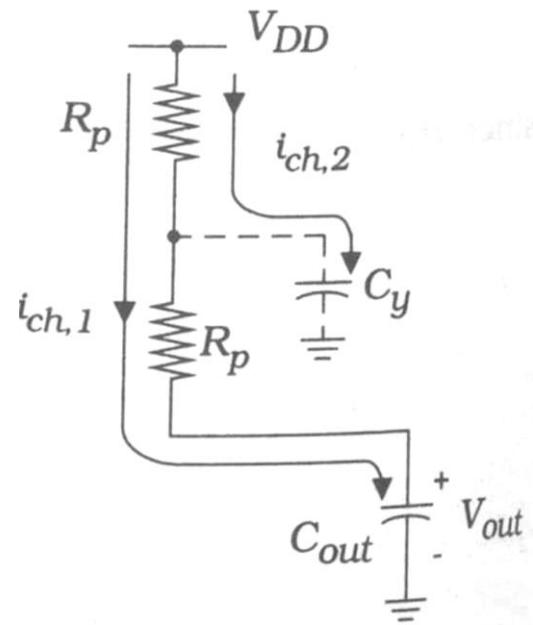
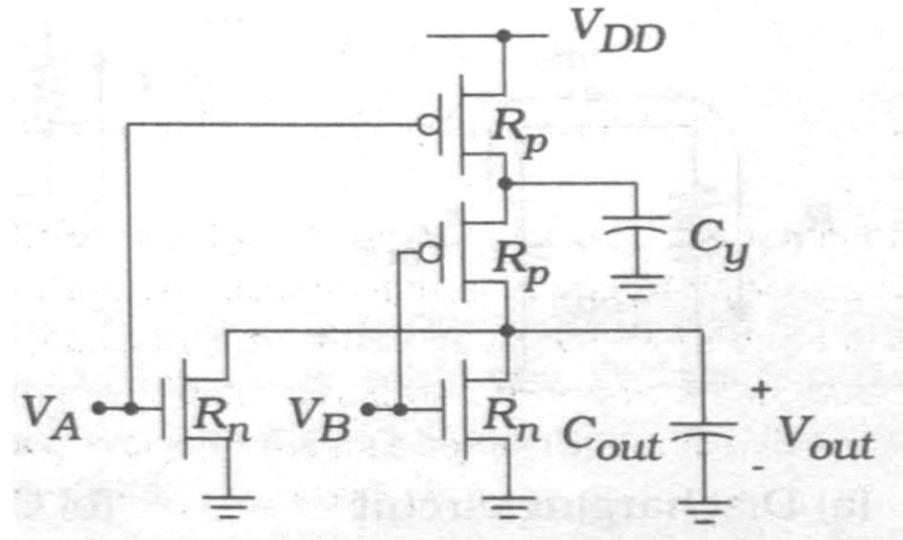
$$\tau_p = \tau_1 + \tau_2$$

$$= C_{out}(2R_p) + C_y R_p$$

$$t_r \approx 2.2\tau_p$$

$$t_r = t_0 + \alpha_0 C_L$$

$$t_0 = 2.2R_p(2C_{FET} + C_y) \quad \alpha_0 = 4.4R_p$$



(b) Charging circuit

## Summary:

$$1. \quad t_r = t_0 + \alpha_0 C_L \quad ; \quad t_f = t_1 + \alpha_1 C_L$$

The constants depend upon the parasitic transistor resistances and capacitances

2. Switching delays increase with the fan-in.

- The number of inputs to a logic gate is called the fan-in (FI).

3. Switching delays increase with the external load.

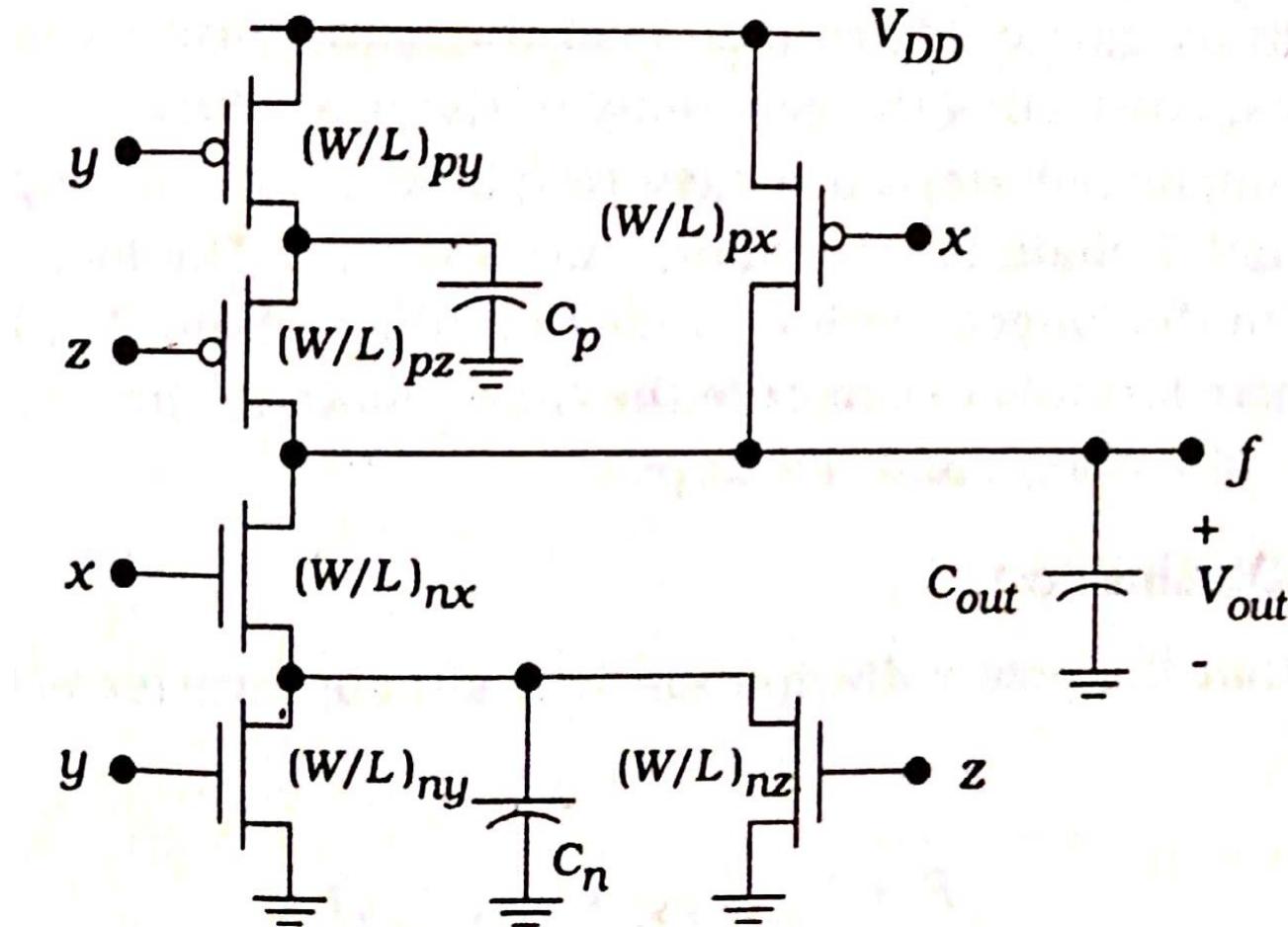
4. The electrical characteristics of these gates are set by,

- The processing variables
- The aspect ratios  $(W/L)_n$  and  $(W/L)_p$  of every FET

5. Series transistors introduced us to the problem of parasitic capacitance between the two devices.

# Analysis of Complex Logic Gates

Consider the logic function  $f = \overline{x \cdot (y + z)}$



$$\left(\frac{W}{L}\right)_{nx} = \left(\frac{W}{L}\right)_{ny} = \left(\frac{W}{L}\right)_{nz}$$

$$\left(\frac{W}{L}\right)_{px} = \left(\frac{W}{L}\right)_{py} = \left(\frac{W}{L}\right)_{pz}$$

- Fall time:  $t_f = 2.2\tau_n$        $\tau_n = R_n C_n + 2R_n C_{out}$   
 $= 2.2R_n[C_n + 2(C_{FET} + C_L)]$   
 $= t_1 + \alpha_1 C_L$

where,

$$t_1 = 2.2R_n(C_n + 2C_{FET}) \quad \alpha_1 = 4.4R_n$$


---

- Rise time:  $t_r \approx 2.2\tau_p$        $\tau_p = R_p C_p + 2R_p C_{out}$   
 $t_r = t_0 + \alpha_0 C_L$

where,

$$t_0 = 2.2R_p(C_p + 2C_{FET}) \quad \alpha_0 = 4.4R_p$$

The important steps are easy to follow:

- 1) The longest series connected nFET chain for the worst-case fall time.
- 2) The longest rise time will be due to the longest series-connected pFET chain.

**Power Dissipation:**  $P = V_{DD} I_{DDQ} + f C_{out} V_{DD}^2$

- To model the number of transitions that take place over a switching period T, we introduce the **activity coefficient,  $\alpha$** .
  - Represents the probability that an output  $0 \rightarrow 1$  transition takes place during one period.
- For a network that consists of N gates, the total dynamic power is more generally written in the form

$$P_{dyn} = \sum_{t=1}^N \alpha_t C_t V_t V_{DD} f$$

where, for the i-th gate,

$\alpha_i$  is the activity coefficient

$C_i$  is the node capacitance that charges to a maximum value of  $V_i$ .

- Activity coefficients can be determined from truth tables.

### NOR2 transitions:

- The activity factor  $\alpha_{NOR2}$  is the probability that the gate makes a  $0 \rightarrow 1$  transition,

$$\alpha = p_0 p_1$$

where,

$p_0$ - Probability that the output is initially at 0 =  $\frac{3}{4}$

$p_1$ - Probability that it makes a transition to 1 =  $\frac{1}{4}$

$$\alpha_{NOR2} = \frac{3}{4} \cdot \frac{1}{4} = \frac{3}{16}$$

### NAND2:

$$p_0 = \frac{1}{4} \text{ and } p_1 = \frac{3}{4}; \alpha_{NAND2} = \frac{3}{16}$$

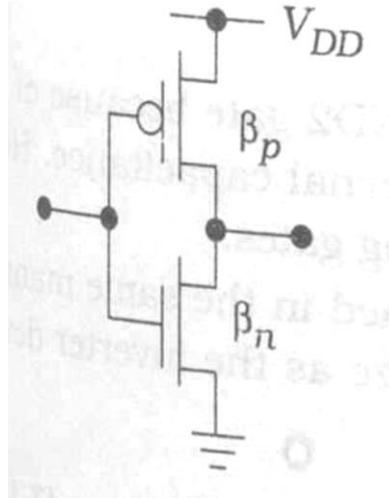
### XNOR2:

$$p_0 = \frac{1}{2} \text{ and } p_1 = \frac{1}{2}; \alpha_{NAND2} = \frac{1}{4}$$

A	B	$\overline{A + B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

# Gate Design for Transient Performance

- The **aspect ratios** are the critical design parameters **for the DC and transient switching times**.
- The **DC switching characteristics** are often **considered less importance** than the switching speed.
- It is **common to design a gate** to have the **desired transient times**, and then **check the DC VTC** to insure that it is acceptable.
- To calculate the switching time the given design, inverter is used as a reference cell.

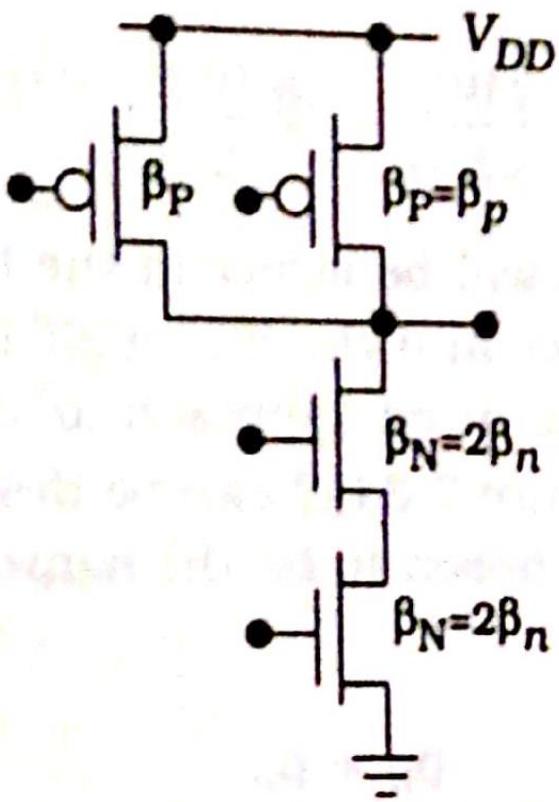


$$R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})} \quad R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)}$$

- For symmetric inverter,

$$\beta_n = \beta_p \quad \frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r \quad \text{Mobility ratio or Transconductance ratio}$$
$$\left(\frac{W}{L}\right)_p = r \left(\frac{W}{L}\right)_n$$

## NAND2:



## parallel pFETs:

- only one transistor contributes to the rise time.
- select the same size as the inverter

$$\beta_P = \beta_p$$

## series nFETs:

- series-connected resistors between the output and ground

$$R = R_N + R_N$$

$$R_N = \frac{1}{\beta_N(V_{DD} - V_{TN})}$$

- Using inverter as reference,

$$R = R_n = 2R_N$$

$$\frac{1}{\beta_n(V_{DD} - V_{TN})} = \frac{2}{\beta_N(V_{DD} - V_{TN})}$$

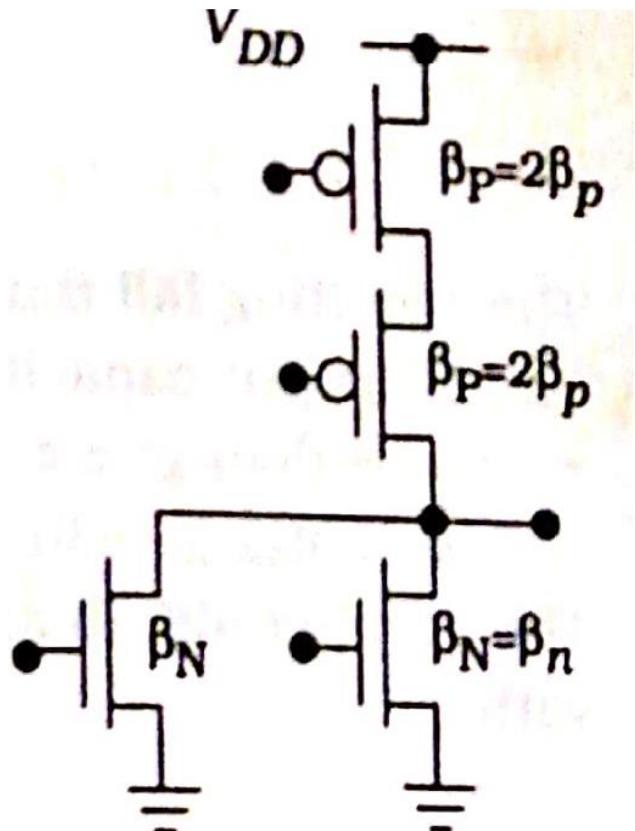
$$\boxed{\beta_N = 2\beta_n}$$

series-connected nFETs are twice as large as the inverter transistor

$$\left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_n$$

**fall time  $t_f$  will be larger in the NAND2 gate**

## NOR2:



- parallel nFETs:

- only one transistor contributes to the rise time.
- select the same size as the inverter

$$\beta_N = \beta_n$$

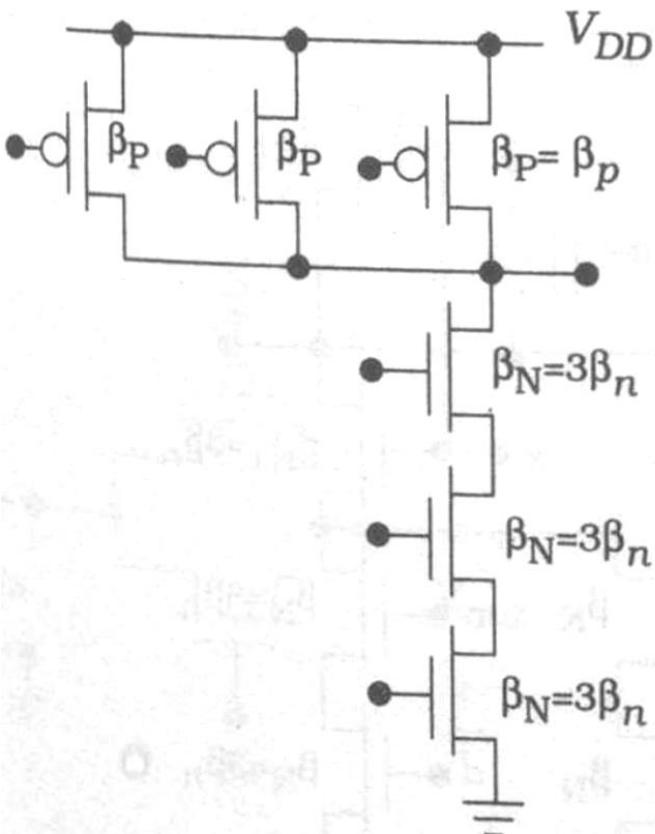
- series nFETs:

- series-connected resistors between the output and ground
- $R_p$  gives as,

$$\frac{1}{\beta_p(V_{DD} - |V_{Tp}|)} = \frac{2}{\beta_P(V_{DD} - |V_{Tp}|)}$$

$$\beta_P = 2\beta_p$$

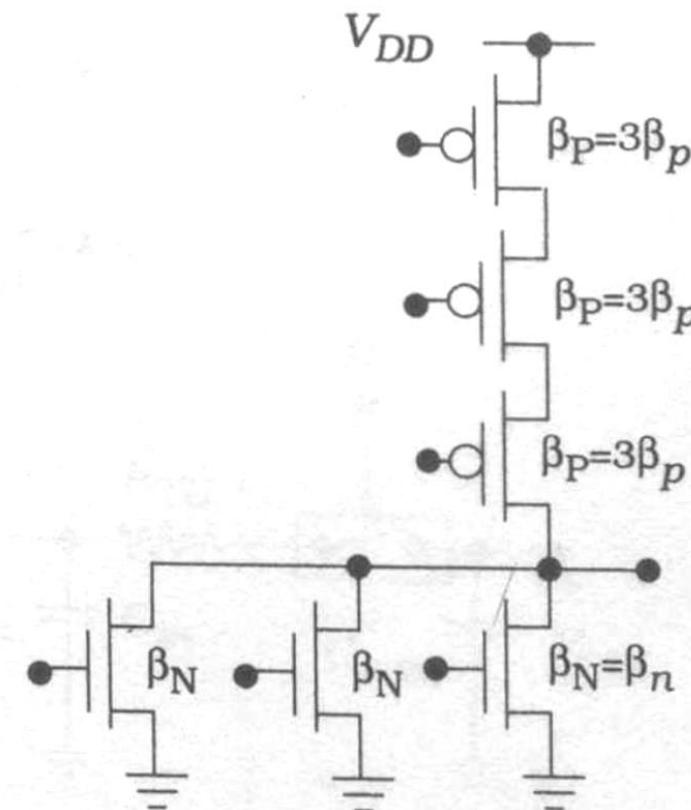
$$\left(\frac{W}{L}\right)_P = 2\left(\frac{W}{L}\right)_p$$



(a) NAND3

$$\beta_N = 3\beta_n, \quad \beta_P = \beta_p$$

$$\left(\frac{W}{L}\right)_N = 3\left(\frac{W}{L}\right)_n, \quad \left(\frac{W}{L}\right)_P = \left(\frac{W}{L}\right)_p$$



(b) NOR3

$$\beta_N = \beta_n, \quad \beta_P = 3\beta_p$$

$$\left(\frac{W}{L}\right)_N = \left(\frac{W}{L}\right)_n, \quad \left(\frac{W}{L}\right)_P = 3\left(\frac{W}{L}\right)_p$$

$$1) F = \overline{x.(y+z)}$$

$$2) F = \overline{(a.b + c.d).x}$$

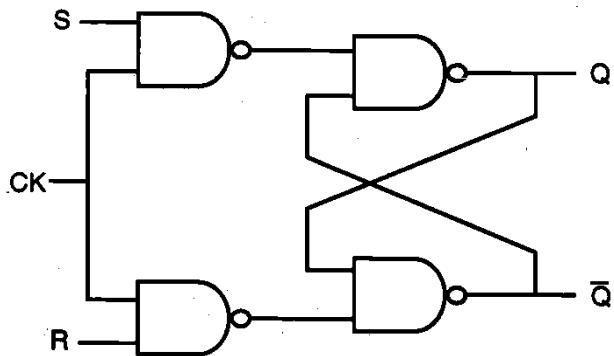
$$3) F = \overline{a.b + c.d.e}$$

$$4) F = \overline{x.(y+z) + x.w}$$

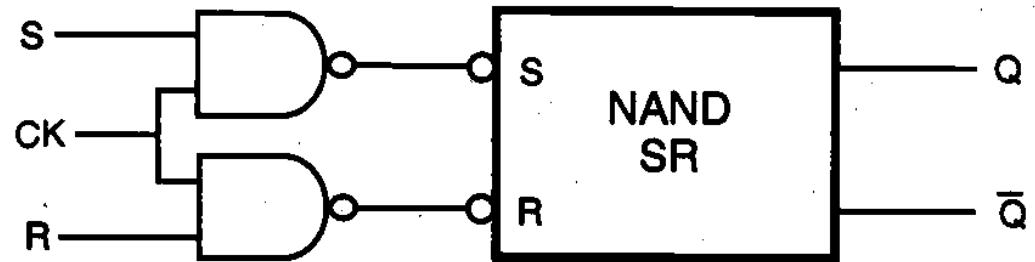
$$5) F = \overline{(a+b).(b+c).d}$$

# Clocked Latch and Flip Flop circuits

## SR latch



Gate-level schematic of the clocked NAND-based SR latch circuit, with active high inputs.

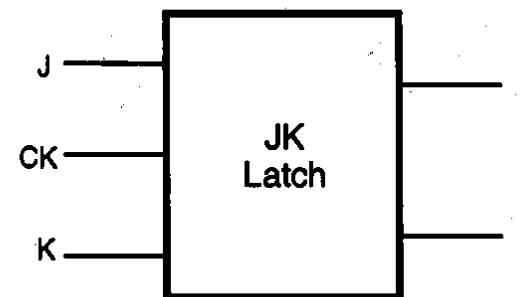
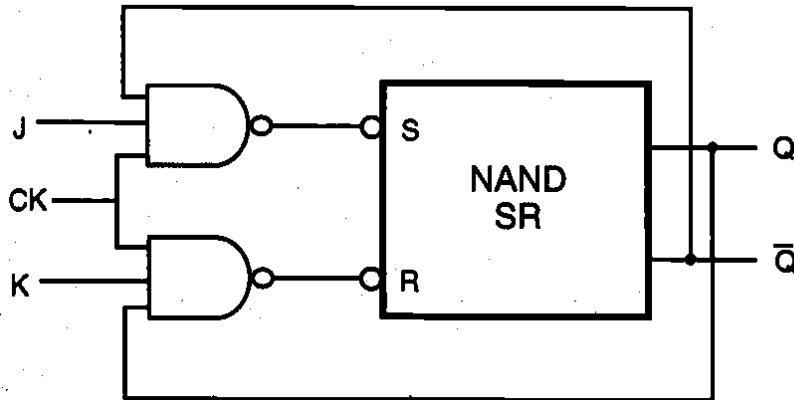


Partial block diagram representation of the same circuit.

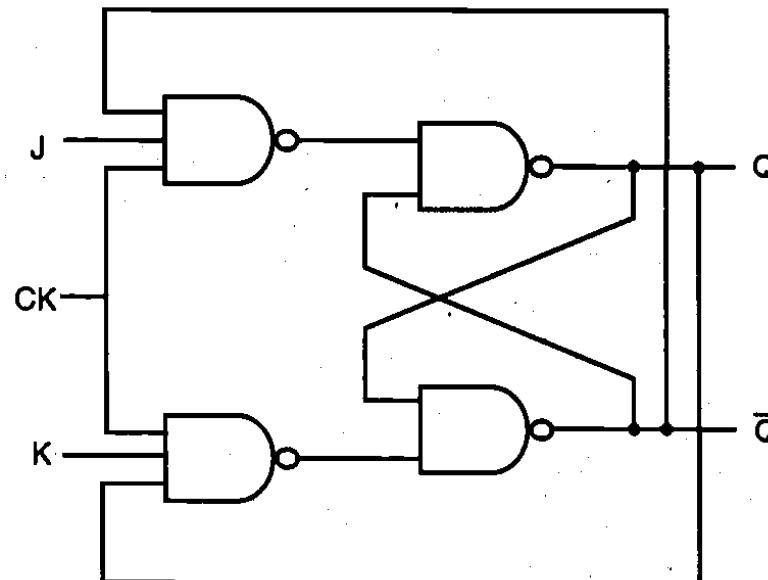
S	R	Q	$Q'$	
0	0	NC	NC	No change. Latch remained in present state.
1	0	1	0	Latch SET.
0	1	0	1	Latch RESET.
1	1	0	0	Invalid condition.

- Both input signals and the CK signal are *active high*,
- Latch output Q will be set when CK = "1," S = "1," and R = "0."
- Latch will be reset when CK = "1," = "0," and R = "1."
- Common Problem: State becomes indeterminate when both inputs S and R are activated at the same time.

- problem can be overcome by **adding two feedback lines from the outputs to the inputs**.- resulting circuit is called a **JK latch**

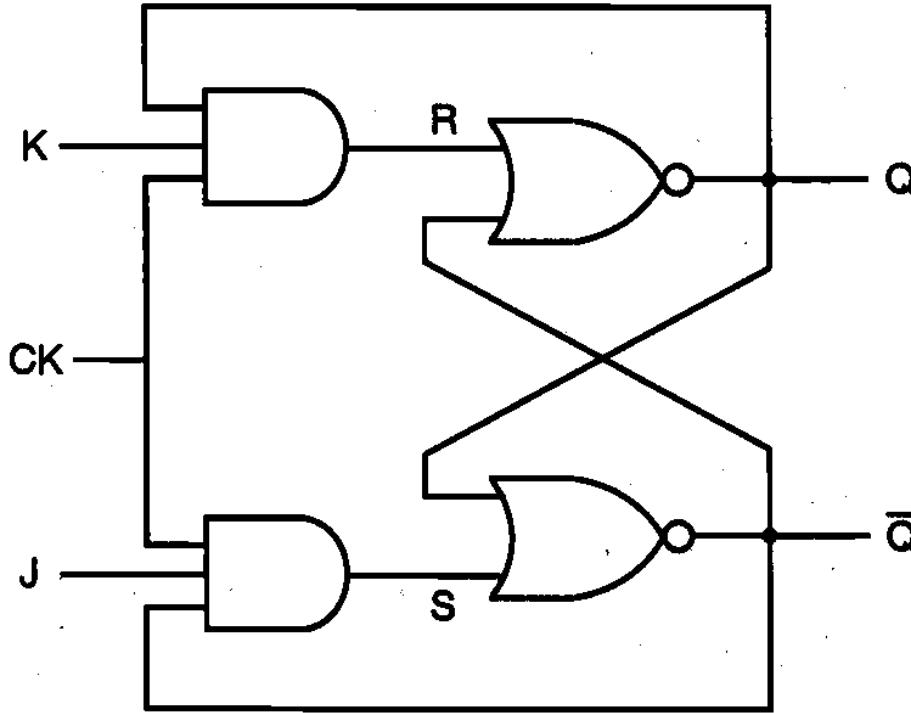


Gate-level schematic of the clocked NAND-based JK latch circuit.



All-NAND implementation of the clocked JK latch circuit.

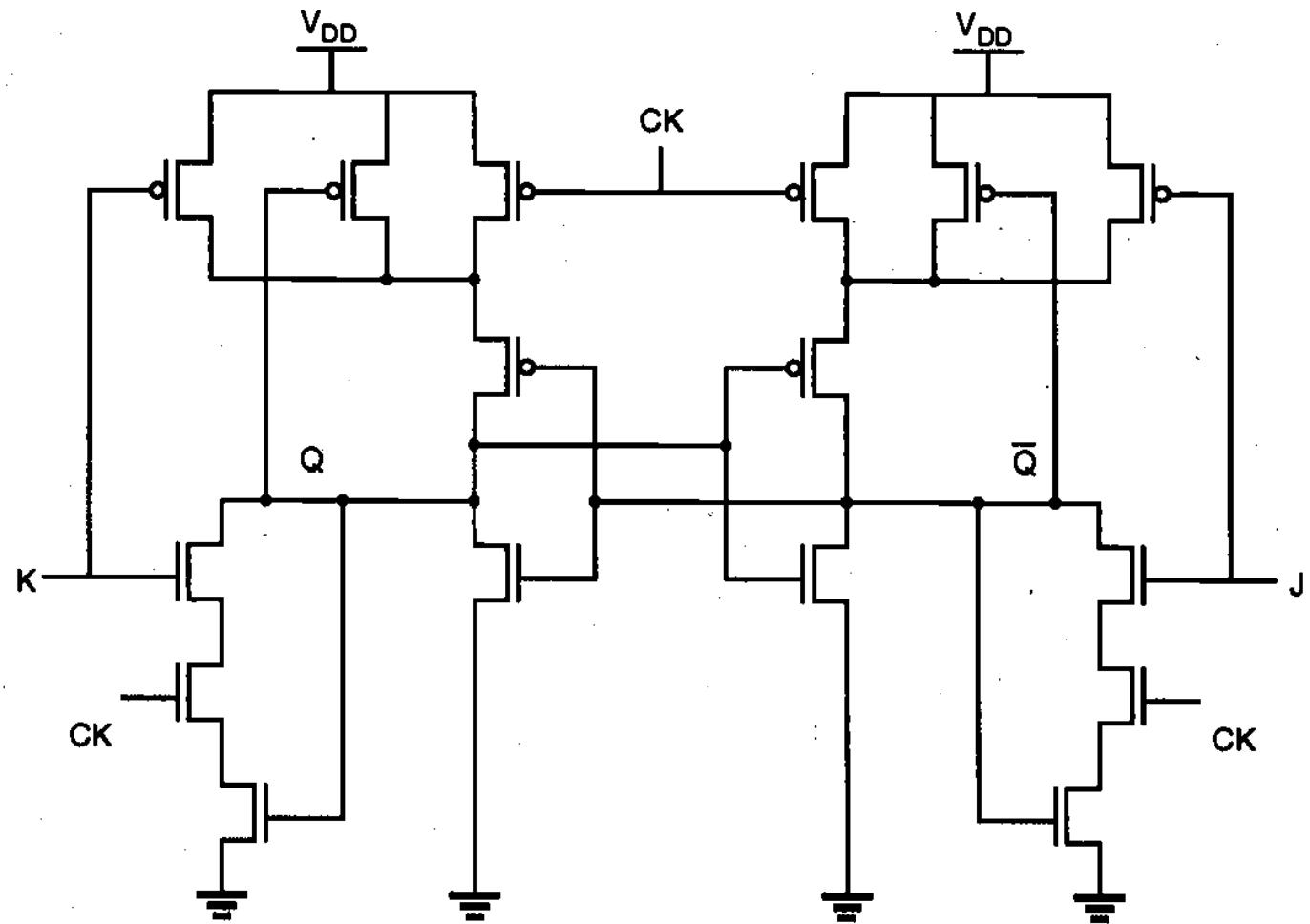
$J$	$K$	$Q_n$	$\bar{Q}_n$	$S$	$R$	$Q_{n+1}$	$\bar{Q}_{n+1}$	<i>Operation</i>
0	0	0	1	1	1	0	1	<i>hold</i>
		1	0	1	1	1	0	
0	1	0	1	1	1	0	1	<i>reset</i>
		1	0	1	0	0	1	
1	0	0	1	0	1	1	0	<i>set</i>
		1	0	1	1	1	0	
1	1	0	1	0	1	1	0	<i>toggle</i>
		1	0	1	0	0	1	



Gate-level schematic of the clocked NOR-based JK latch circuit.

### Problem: Race around condition

If both inputs are equal to logic " 1 " during the active phase of the clock pulse, the output of the circuit will oscillate (toggle) continuously until either the clock becomes inactive (goes to zero), or one of the input signals goes to zero.

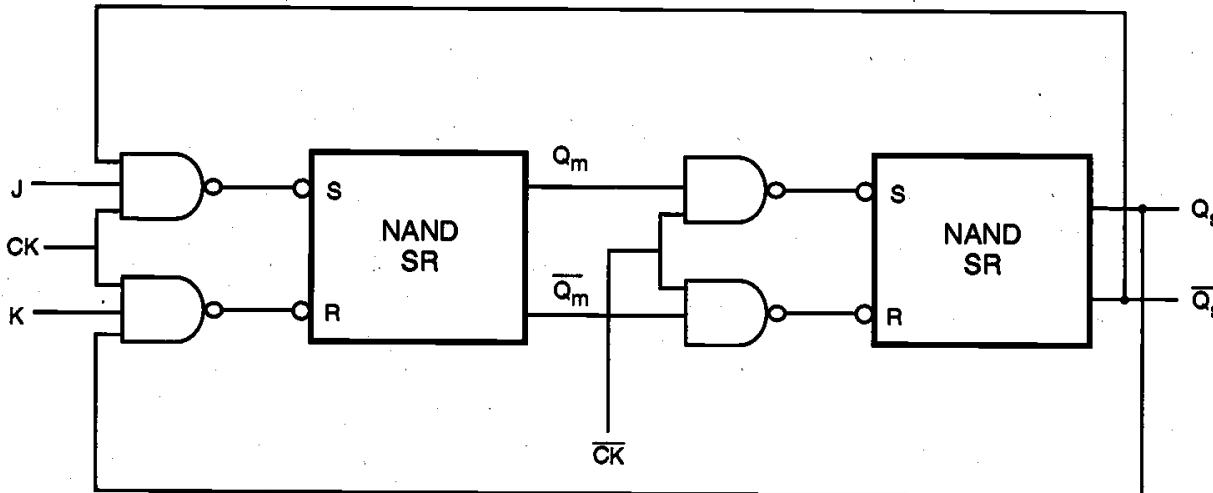


CMOS AOI realization of the JK latch.

- The problem can be prevented by using two latch stages in a cascaded configuration.

## Master-slave flip-flop

- Key operation principle: the two cascaded stages are activated with opposite clock phases.



Master-slave flip-flop consisting of NAND-based JK latches.

### Important property:

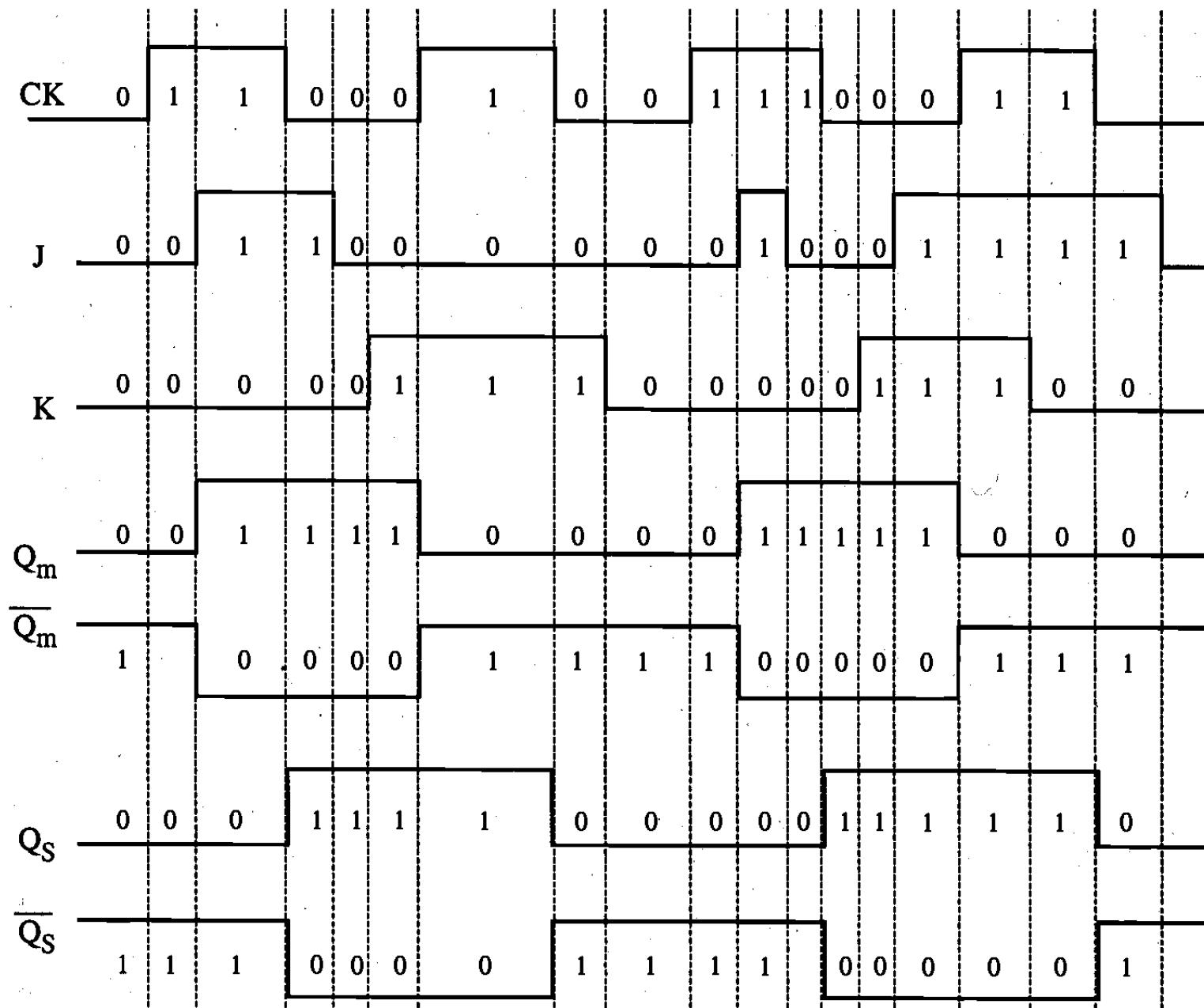
a change occurring in the primary inputs is never reflected directly to the outputs.

**"master," is activated when the clock pulse is high.**

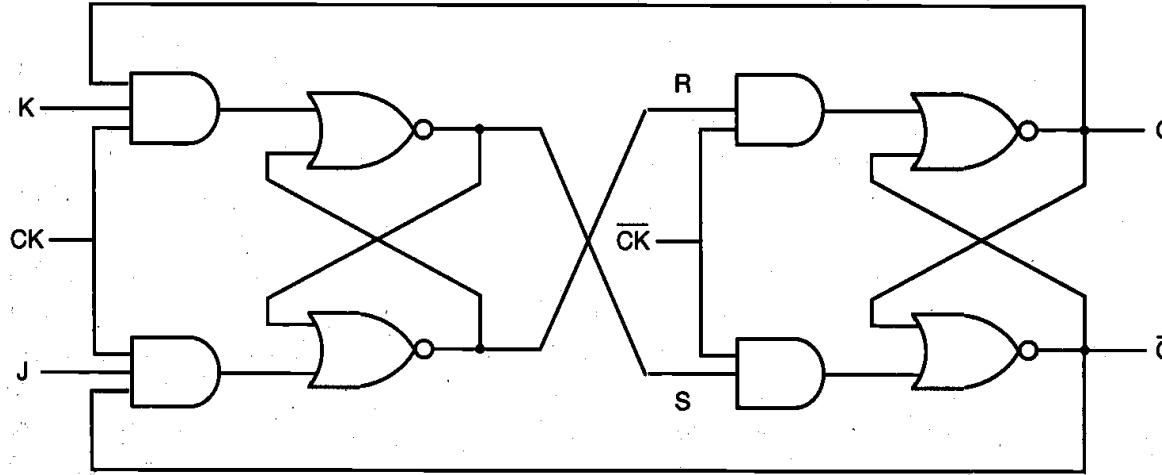
- During this phase, the inputs J and K allow data to be entered into the flip-flop
- First-stage outputs are set according to the primary inputs.

**"Slave," is activated when the clock pulse is low.**

- The output levels of the flip-flop circuit are determined during this second phase based on the master-stage outputs set in the previous phase.



Sample input and output waveforms  
of the master-slave flip-flop circuit.



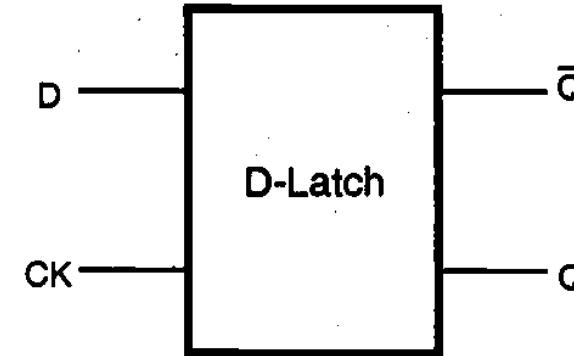
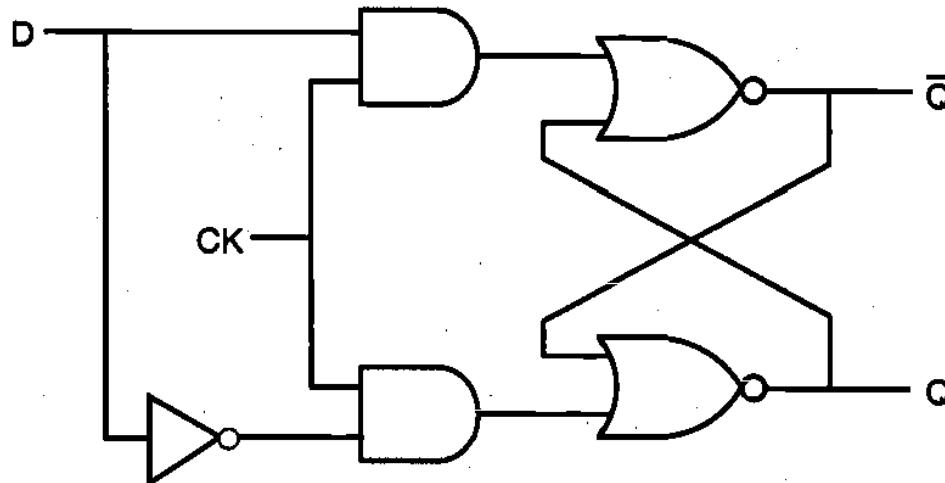
NOR-based realization of the JK master-slave flip-flop.

Problem: "**one's catching.**"

When the clock pulse is high, a narrow spike or glitch in one of the inputs, for instance a glitch in the J line (or K line), may set (or reset) the master latch and thus cause an unwanted state transition, which will then be propagated into the slave stage during the following phase.

problem can be eliminated to a large extent by building an edge-triggered master-slave flip-flop

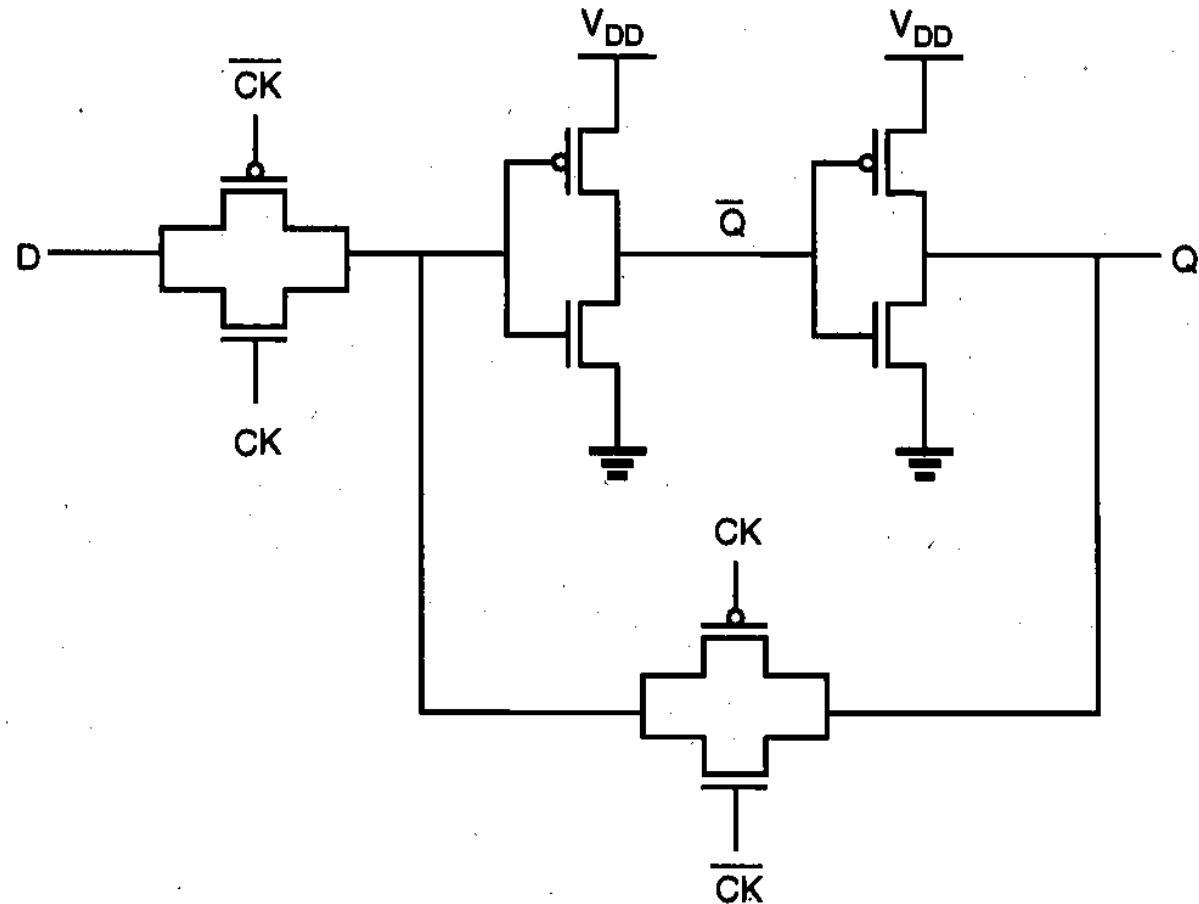
# CMOS D-Latch and Edge-Triggered Flip-Flop



Gate-level schematic and the block diagram view of the D-latch.

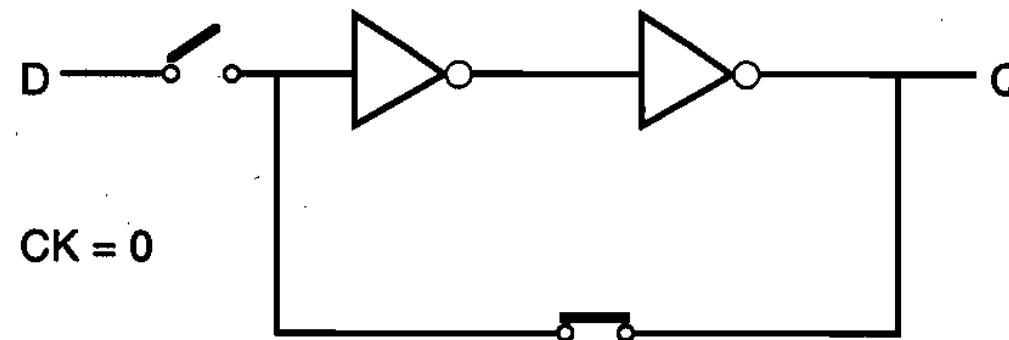
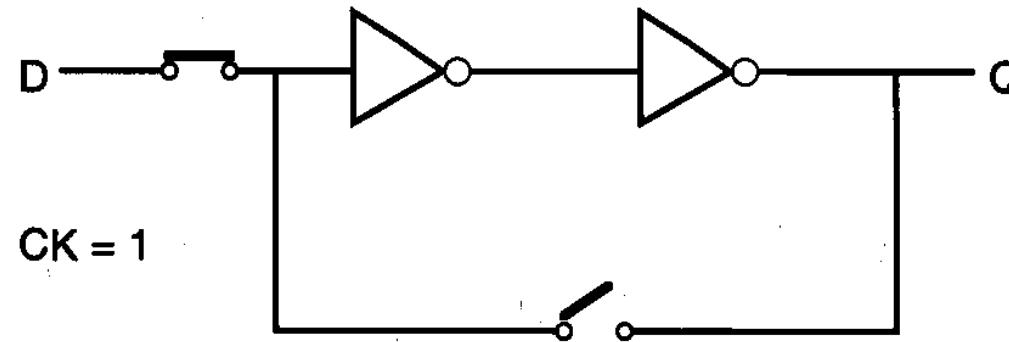
- Output Q assumes the value of the input D when the clock is active, i.e., for  $CK = "1."$
- When the clock signal goes to zero, the output will simply preserve its state.
- **Primarily application:** for temporary storage of data or as a delay element.

- CMOS implementation

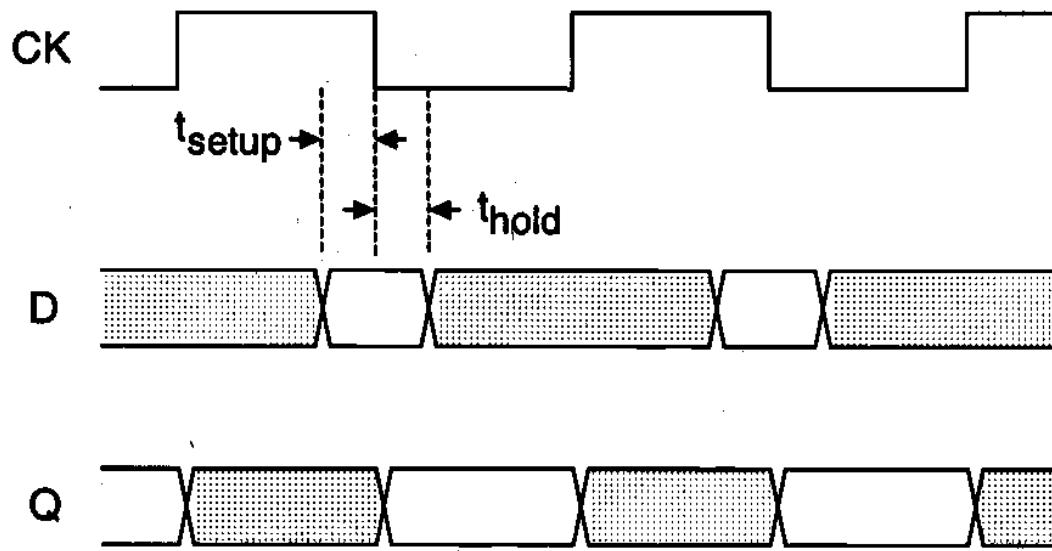


- **two-inverter loop and two CMOS transmission gate (TG) switches.**
- **The input signal is accepted** (latched) into the circuit when the **clock is high**
- the **information is preserved** as the state of the inverter loop when the **clock is low**.

The operation of the CMOS D-latch circuit can be better visualized by replacing the CMOS transmission gates with simple switches.

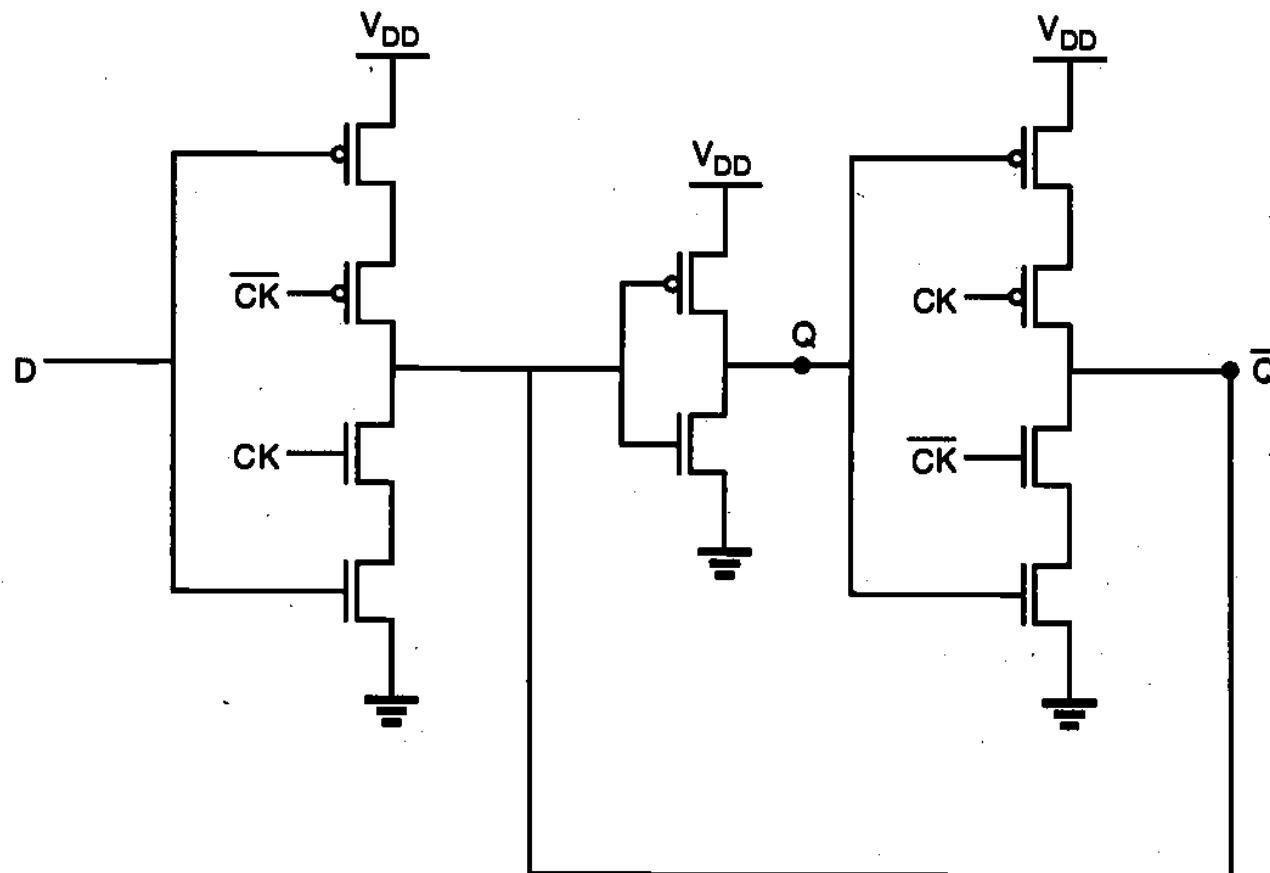


# timing diagram



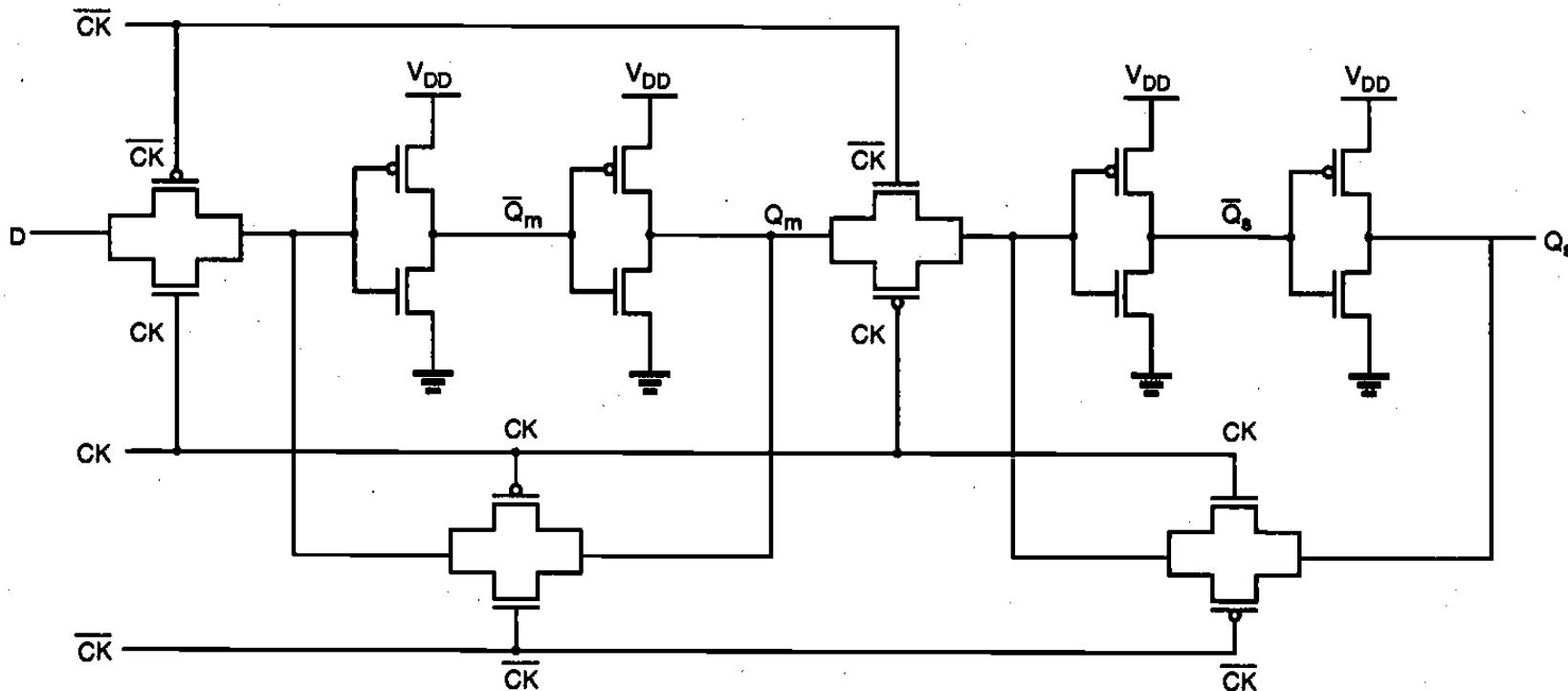
- **D input must be stable for a short time** before (*setup time*,  $t_{setup}$ ) and after (*hold time*,  $t_{hold}$ ) the negative clock transition
- In the D-latch design, **the requirements for setup time and hold time should be met carefully.**
- Any violation of such specifications can cause **metastability** problems which lead to seemingly chaotic transient behavior.
- result in an **unpredictable state** after the transitional period.

# CMOS implementation of the D-latch (version 2)



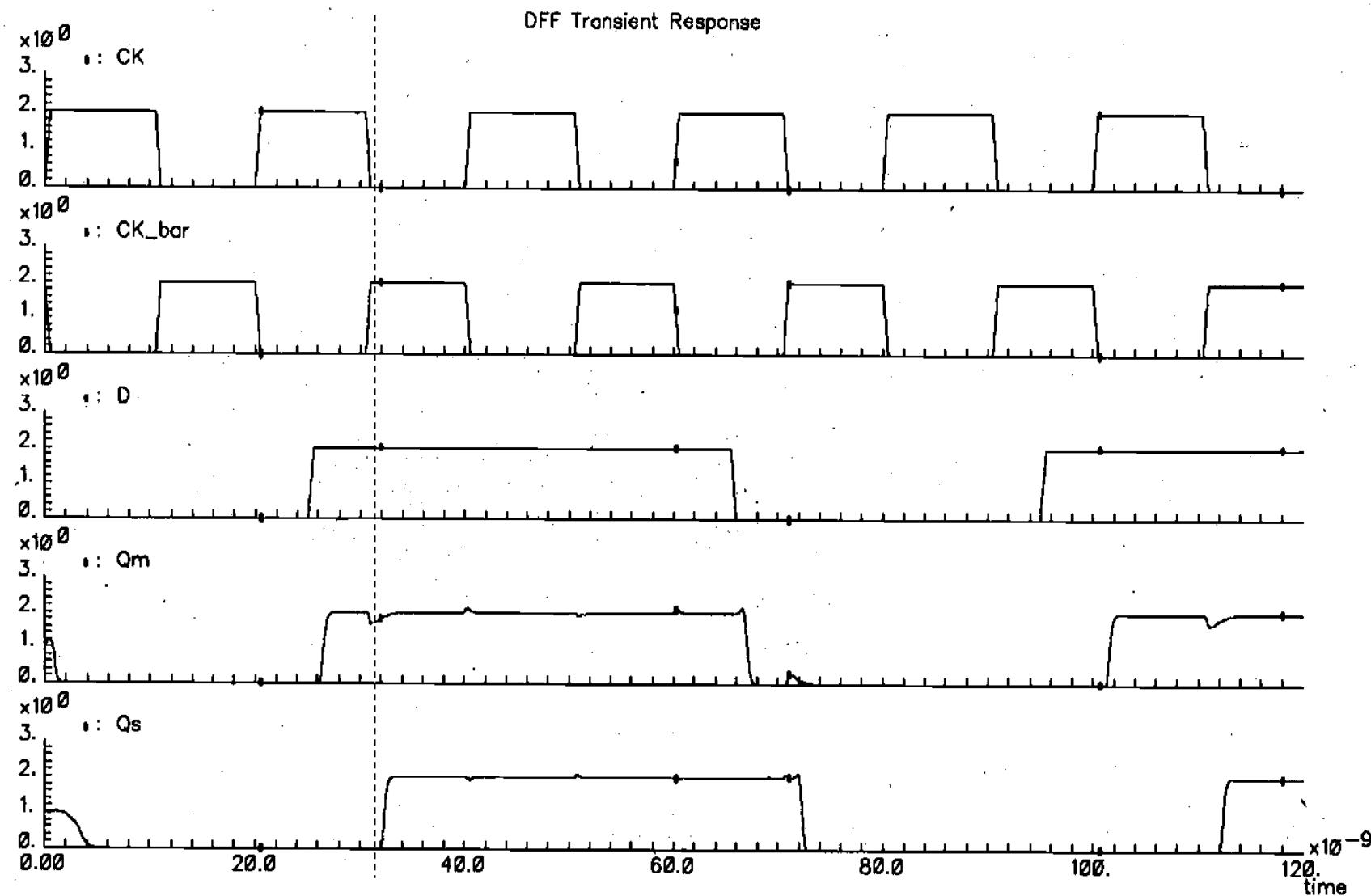
- circuit contains **two tristate inverters**, driven by the clock signal and its inverse.
- when the **clock is high**
  - The first tri-state inverter acts as the input switch, accepting the input signal.
  - The second tristate inverter is at its high-impedance state, and the output Q is following the input signal.
- When the clock goes low,
  - input buffer becomes inactive, and the second tristate inverter completes the two-inverter loop, which preserves its state until the next clock pulse.

## two-stage master-slave flip-flop circuit

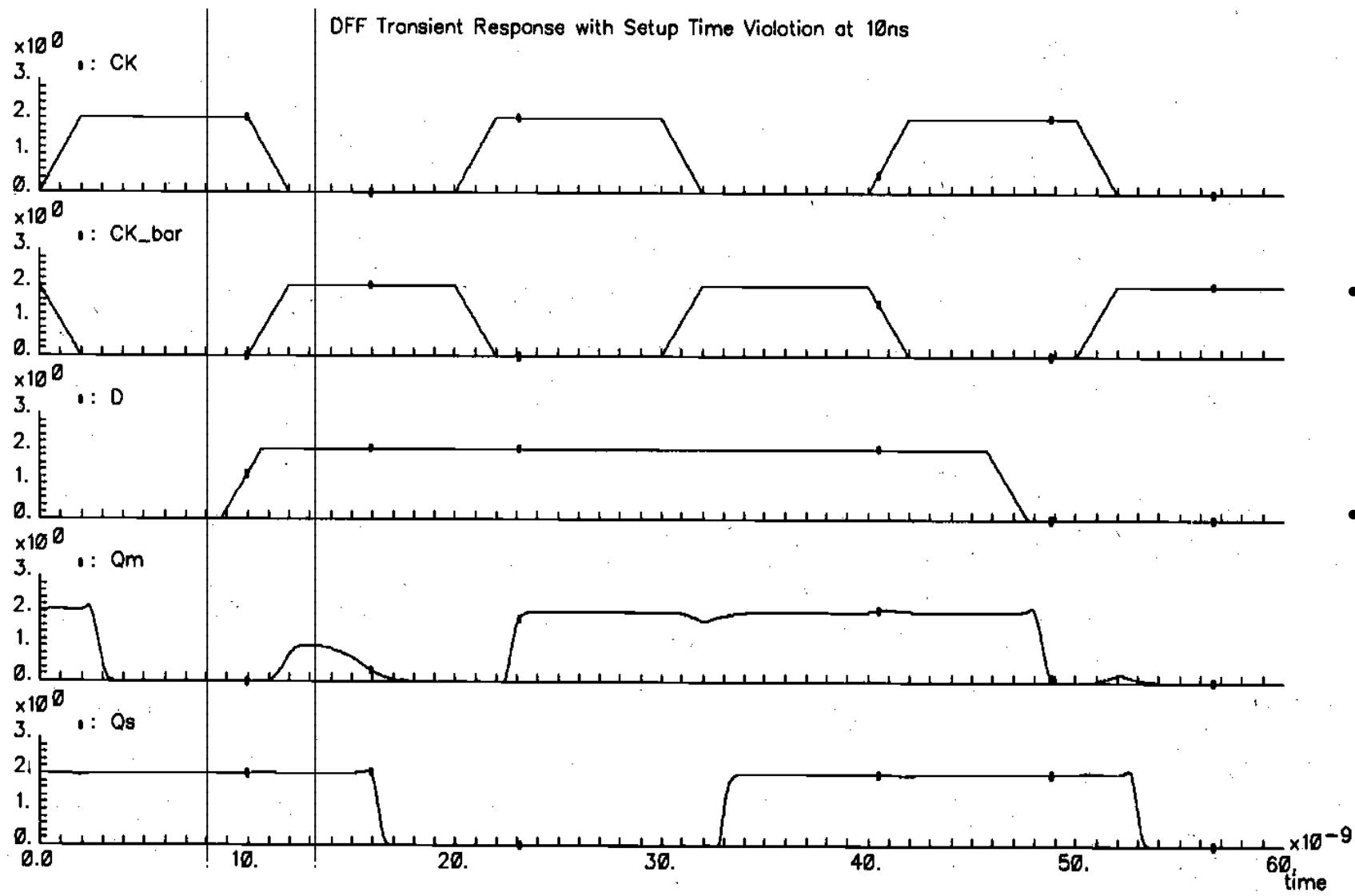


- The first stage (master) is driven by the clock signal (master stage is positive level-sensitive)
- The second stage (slave) is driven by the inverted clock signal (slave stage is negative level-sensitive)

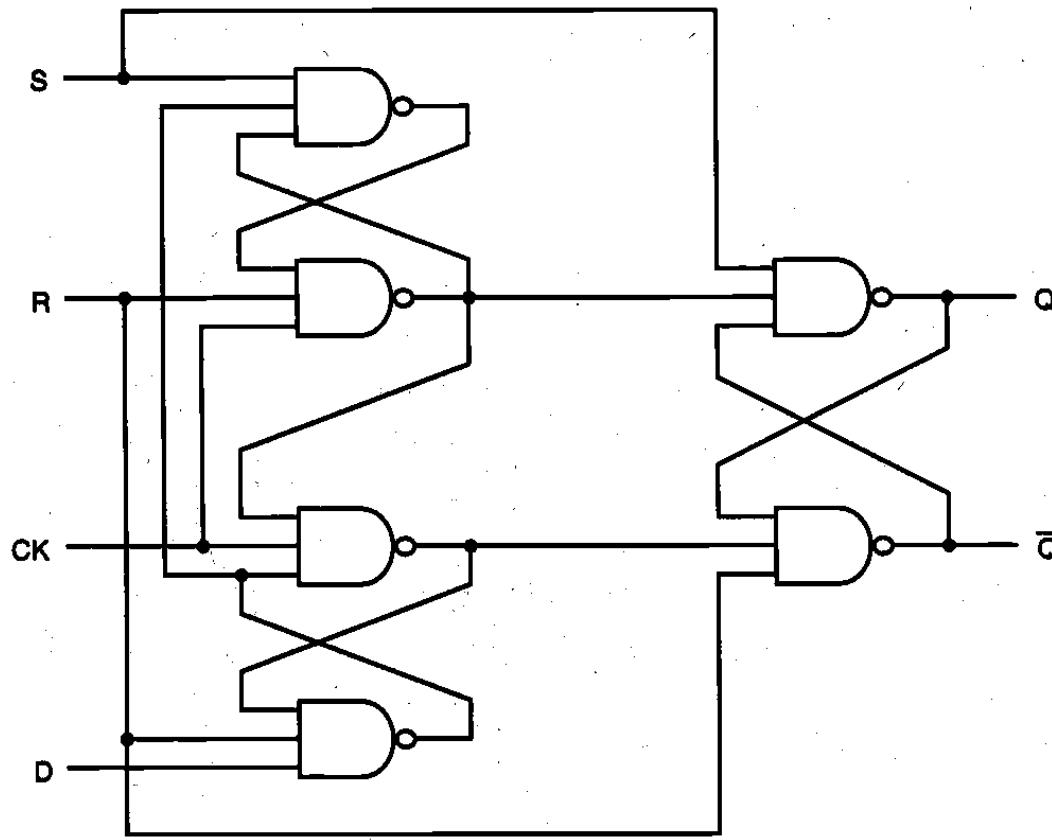
- When the clock is, **high**,
  - the **master stage follows the D input**
  - the **slave stage holds the previous value**.
- When the clock **changes from logic "1" to logic "0"**
  - the **master latch ceases to sample the input and stores the D value** at the time of the clock transition.
  - the **slave latch becomes transparent**, passing the stored master value **Qm** to the output of the slave stage, **Qs**



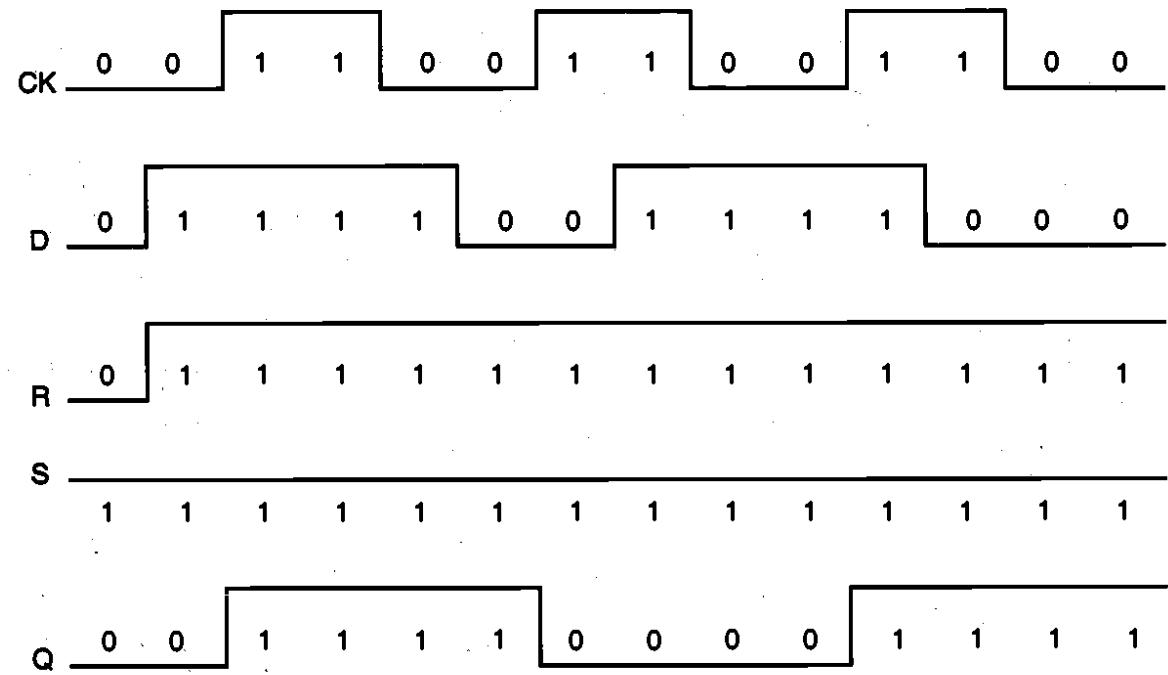
Simulated input and output waveforms of the CMOS DFF circuit



- Simulated waveforms of the CMOS DFF circuit, showing a set-up time violation for the master stage input at 10 ns.
- The output of the master stage fails to settle at the correct level.



NAND3-based positive edge-triggered D flip-flop circuit.



Timing diagram of the positive edge-triggered D flip-flop.