FUNDAMENTALS OF VLSI DESIGN

(19EC6DCFOV)

Module-5

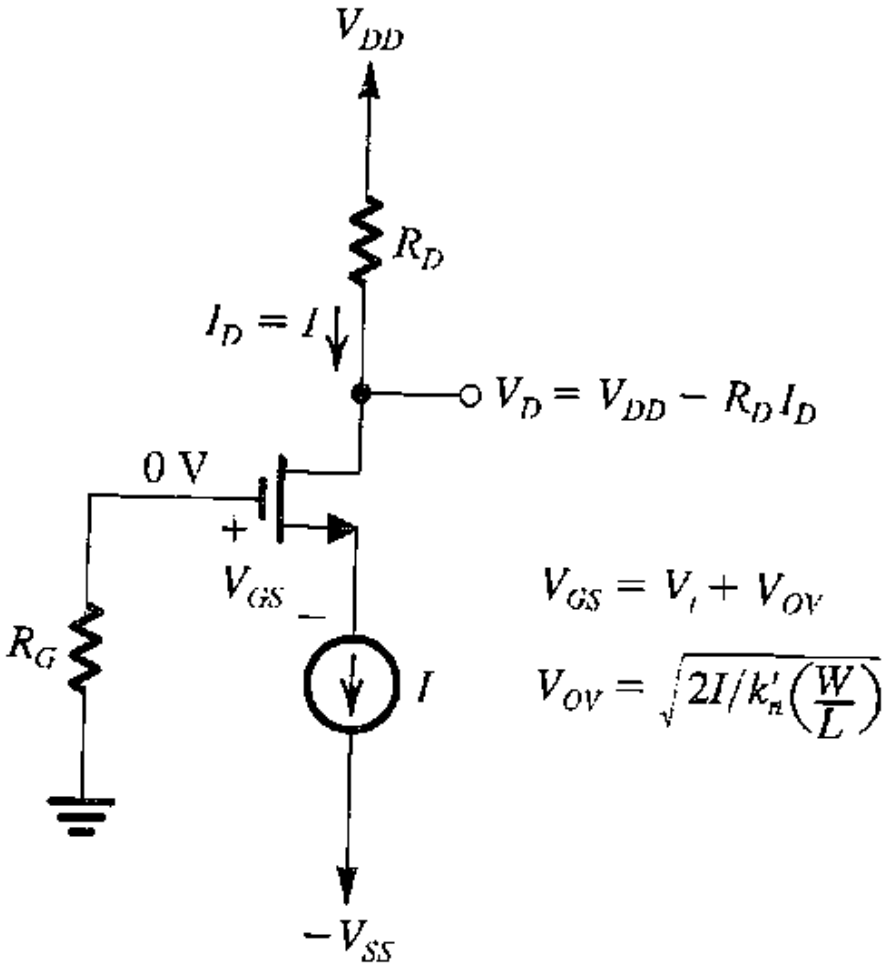
The MOS Amplifiers: Single-Stage MOS Amplifiers : The basic structure, Characterizing amplifiers, Common-Source (CS) Amplifier , The Common-Source Amplifier resistive load , The Common-Gate (CG) Amplifier ,The Common-Drain or Source-Follower Amplifier (Text book-4)

Differential amplifier : Differential Amplifiers, Basic difference pair, common mode/differential mode responses, Differential pair with MOS loads, basic current mirrors (Text book-6)

Text books:

4. Adel A. Sedra and K.C. Smith, “Microelectronics Circuits Theory and Applications”, 5th edition, Oxford University Press, International Version, 2009.
6. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH, India, 2007.

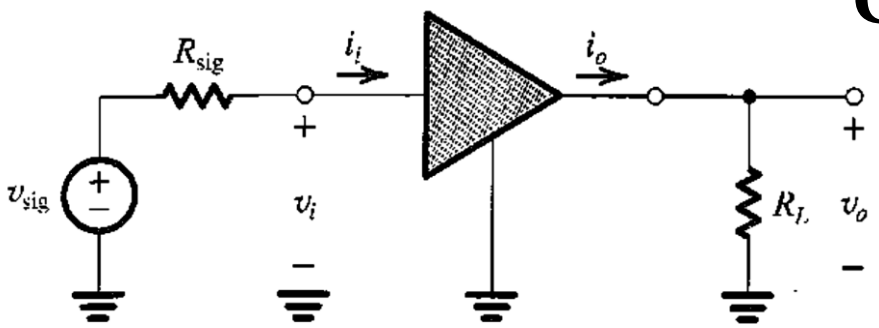
Single-Stage MOS Amplifiers



Basic circuit

- utilize to implement the various configurations of discrete-circuit MOS amplifiers.
- Figure indicates the dc current and the dc voltages resulting at various nodes.

Characterizing amplifiers



Definitions

- Input resistance with no load:

$$R_i \equiv \left.\frac{v_i}{i_i}\right|_{R_L=\infty}$$

- Input resistance:

$$R_{in} \equiv \frac{v_i}{i_i}$$

- Open-circuit voltage gain:

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

- Voltage gain:

$$A_v \equiv \frac{v_o}{v_i}$$

- Short-circuit current gain:

$$A_{is} \equiv \left.\frac{i_o}{i_i}\right|_{R_L=0}$$

- Current gain:

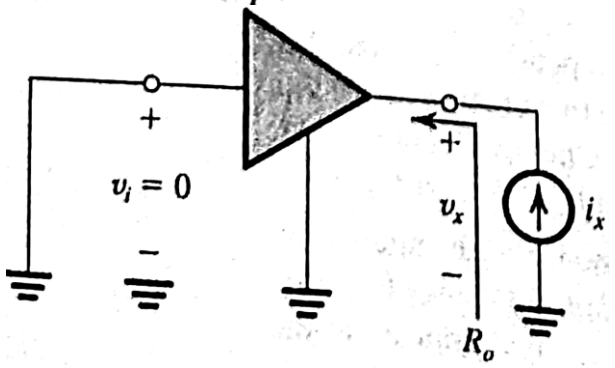
$$A_i \equiv \frac{i_o}{i_i}$$

- Short-circuit transconductance:

$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{R_L=0}$$

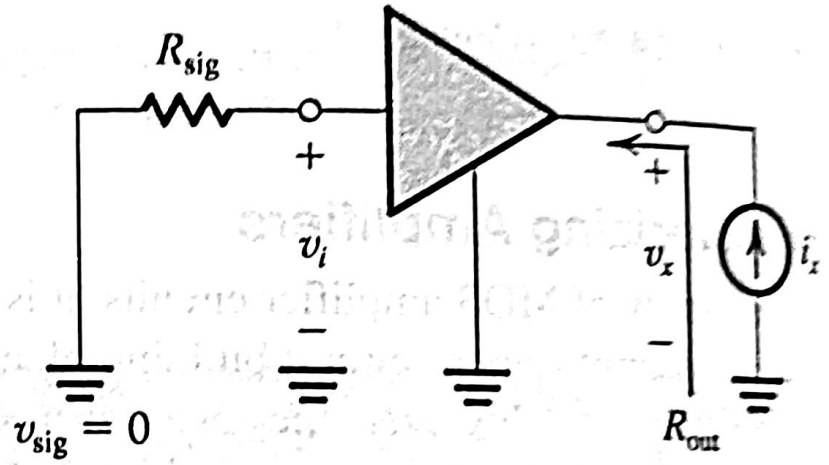
- Output resistance of amplifier proper

$$R_o \equiv \left.\frac{v_x}{i_x}\right|_{v_i=0}$$



- Output resistance:

$$R_{out} \equiv \left.\frac{v_x}{i_x}\right|_{v_{sig}=0}$$



- Open-circuit overall voltage gain:

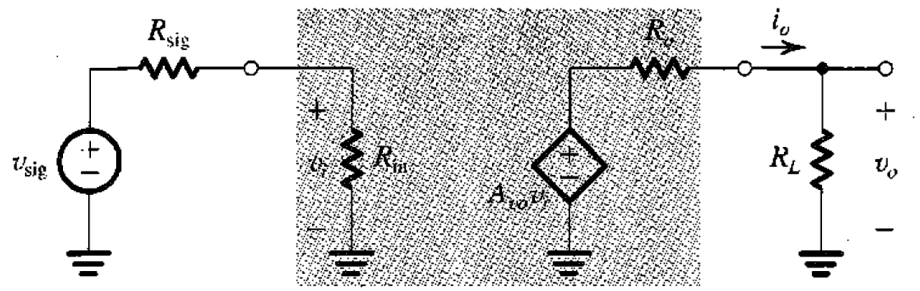
$$G_{vo} \equiv \left.\frac{v_o}{v_{sig}}\right|_{R_L=\infty}$$

- Overall voltage gain:

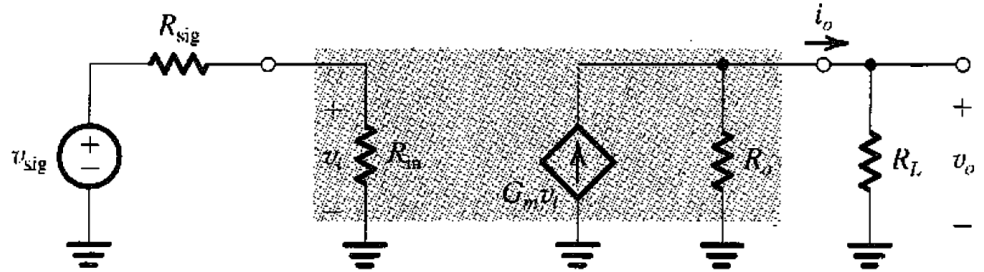
$$G_v \equiv \frac{v_o}{v_{sig}}$$

Equivalent Circuits

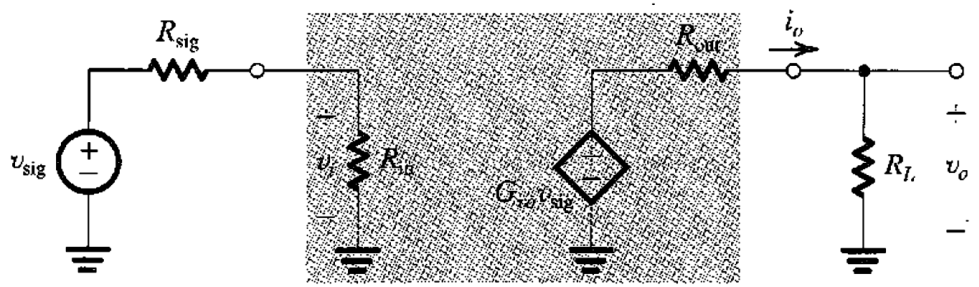
- A:



- B:

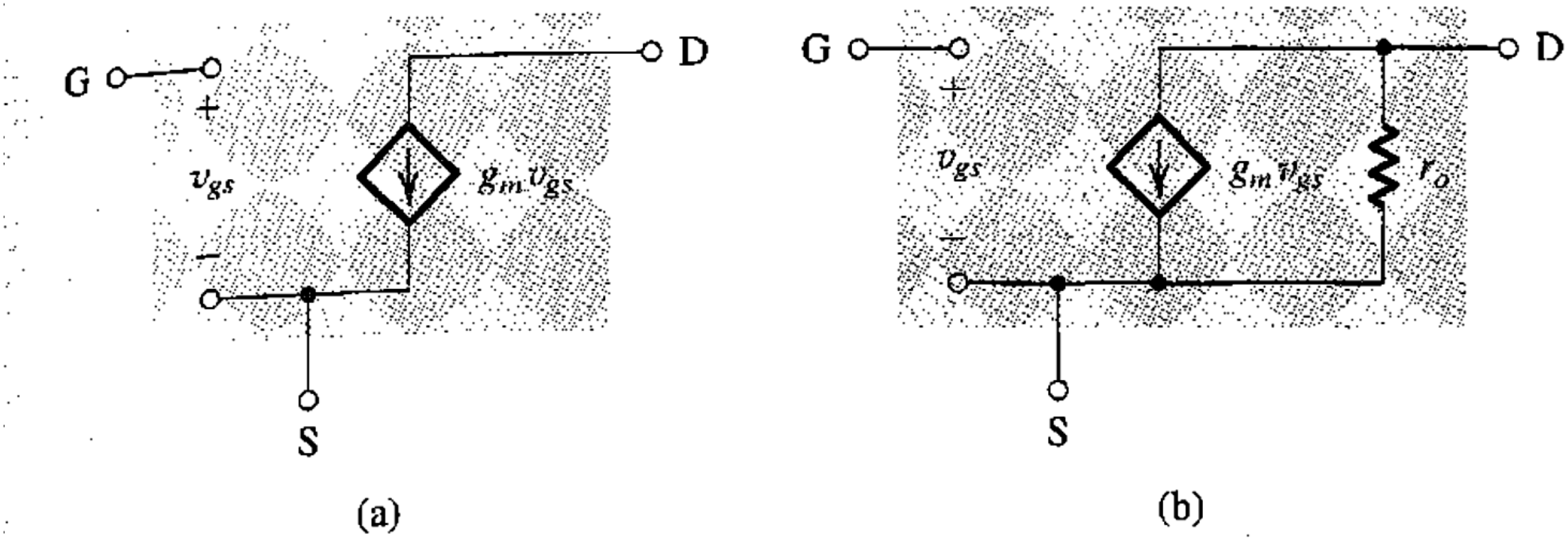


- C:



Relationships

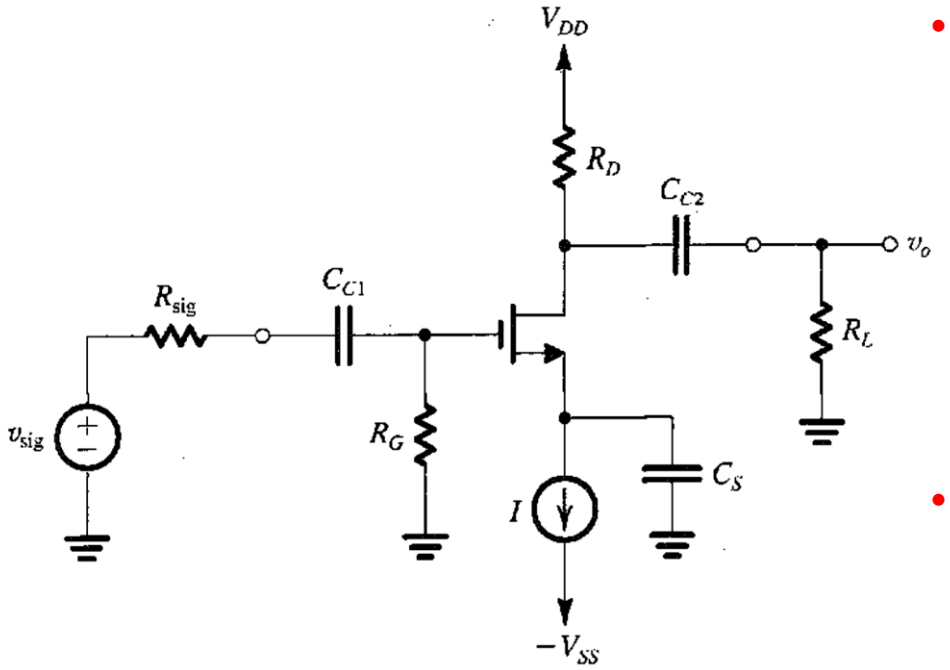
- $\dfrac{v_i}{v_{sig}} = \dfrac{R_{in}}{R_{in} + R_{sig}}$
- $A_v = A_{vo}\dfrac{R_L}{R_L + R_o}$
- $A_{vo} = G_m R_o$
- $G_v = \dfrac{R_{in}}{R_{in} + R_{sig}} A_{vo} \dfrac{R_L}{R_L + R_o}$
- $G_{vo} = \dfrac{R_i}{R_i + R_{sig}} A_{vo}$
- $G_v = G_{vo}\dfrac{R_L}{R_L + R_{out}}$



Small-signal models for the MOSFET

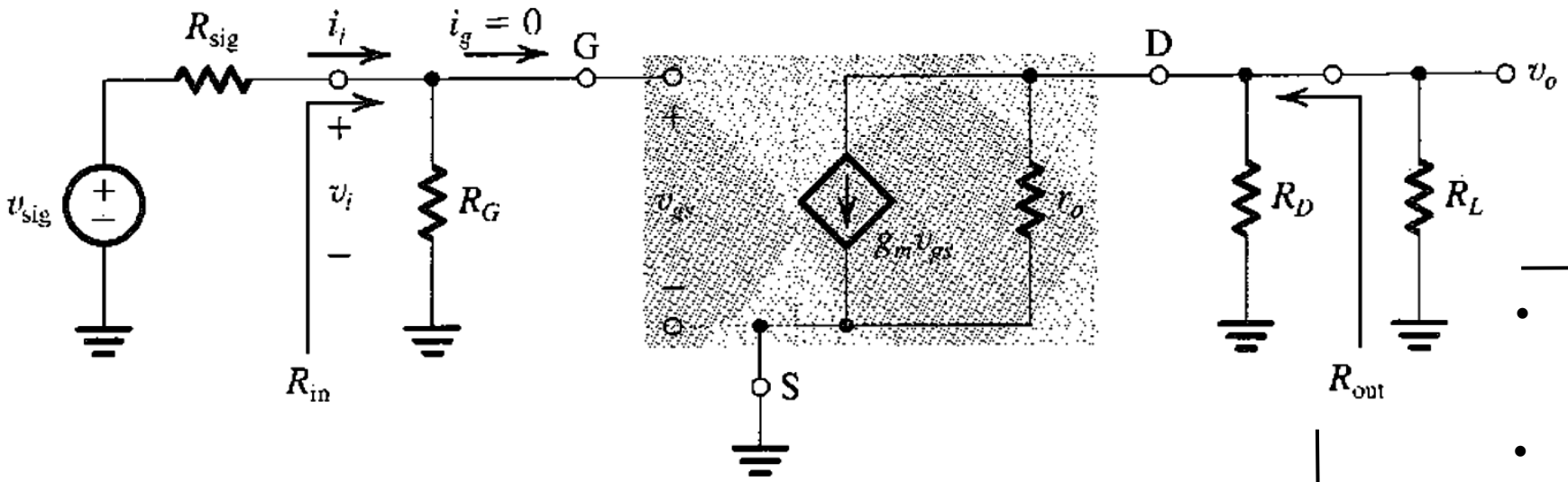
The Common-Source (CS) Amplifier

- The common-source (CS) or grounded-source configuration is the most widely used of all MOSFET amplifier circuits.



- **signal ground,** or an **ac ground** as it is sometimes called, at the source
- ***Cs:* bypass capacitor**
  - between the source and ground.
  - usually in the *pF* range
  - to provide a very small impedance at all signal frequencies of interest. In this way, the signal current passes through *Cs* to ground and thus *bypasses* the output resistance of current source *I.*
- ***C_{c1} : coupling capacitor***
  - required to act as a perfect short circuit at all signal frequencies of interest while blocking dc.
  - At low signal frequency, the impedance of C_{cl} (i.e., $l/j(\omega C_{cl})$ will increase its effectiveness as a coupling capacitor will be correspondingly reduced.
- ***C_{c2} : coupling capacitor***
  - acts as a perfect short circuit at all signal frequencies of interest and thus that the output voltage *vo = vd.*

- Terminal characteristics of the CS amplifier— input resistance, voltage gain, and output resistance
- replace the MOSFET with its small-signal model.



Unilateral amplifier:

- *Rin* does not depend on *RL* thus *Rin = Ri.*
- *Rout* will not depend on *Rsig* thus *Rout = R0.*

At the input,

$$i_g = 0$$

$$R_{in} = R_G$$

$$v_i = v_{sig}\frac{R_{in}}{R_{in} + R_{sig}} = v_{sig}\frac{R_G}{R_G + R_{sig}}$$

- R_G is selected very large (e.g., in the M Ω range) with the result that in many applications $R_G > R_{sig}$

$$v_i \cong v_{sig}$$

$$v_{gs} = v_i$$

$$v_o = -g_m v_{gs}(r_o \| R_D \| R_L)$$

- voltage gain A_v is

$$A_v = -g_m(r_o \| R_D \| R_L)$$

- open-circuit voltage gain A_{vo} is

$$A_{vo} = -g_m(r_o \| R_D)$$

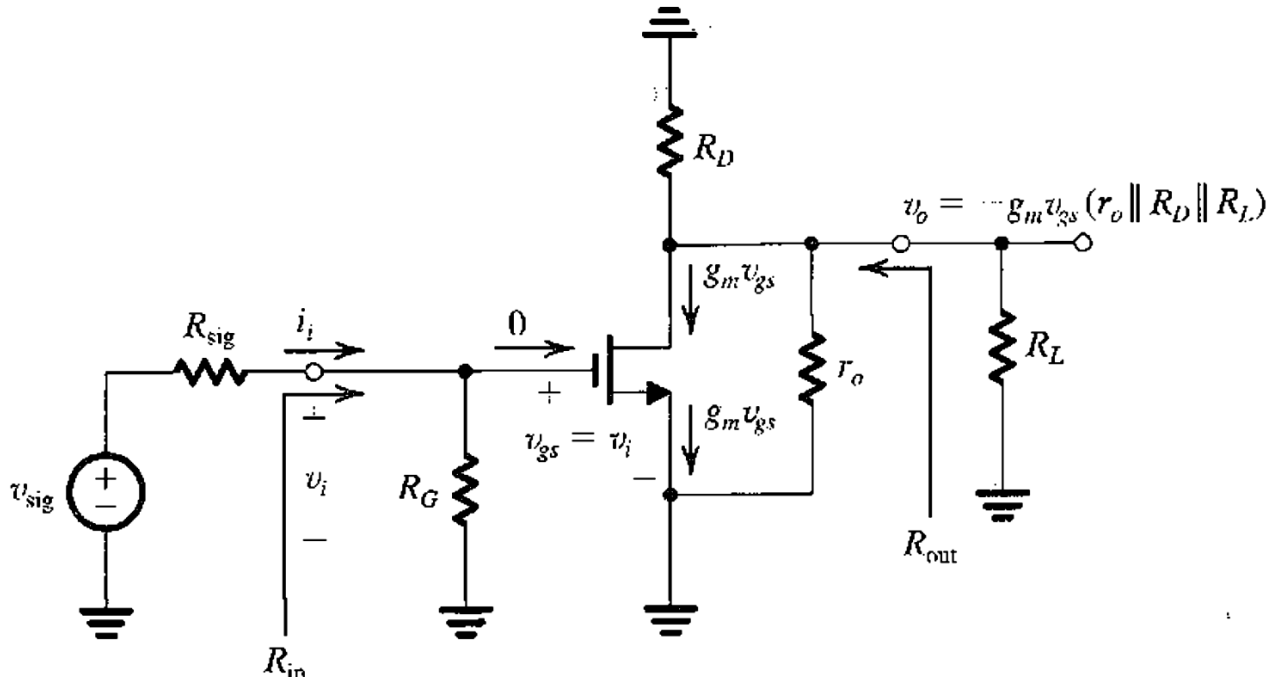
- overall voltage gain from the signal-source to the load will be, $G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_v$

$$= -\frac{R_G}{R_G + R_{sig}} g_m(r_o \| R_D \| R_L)$$

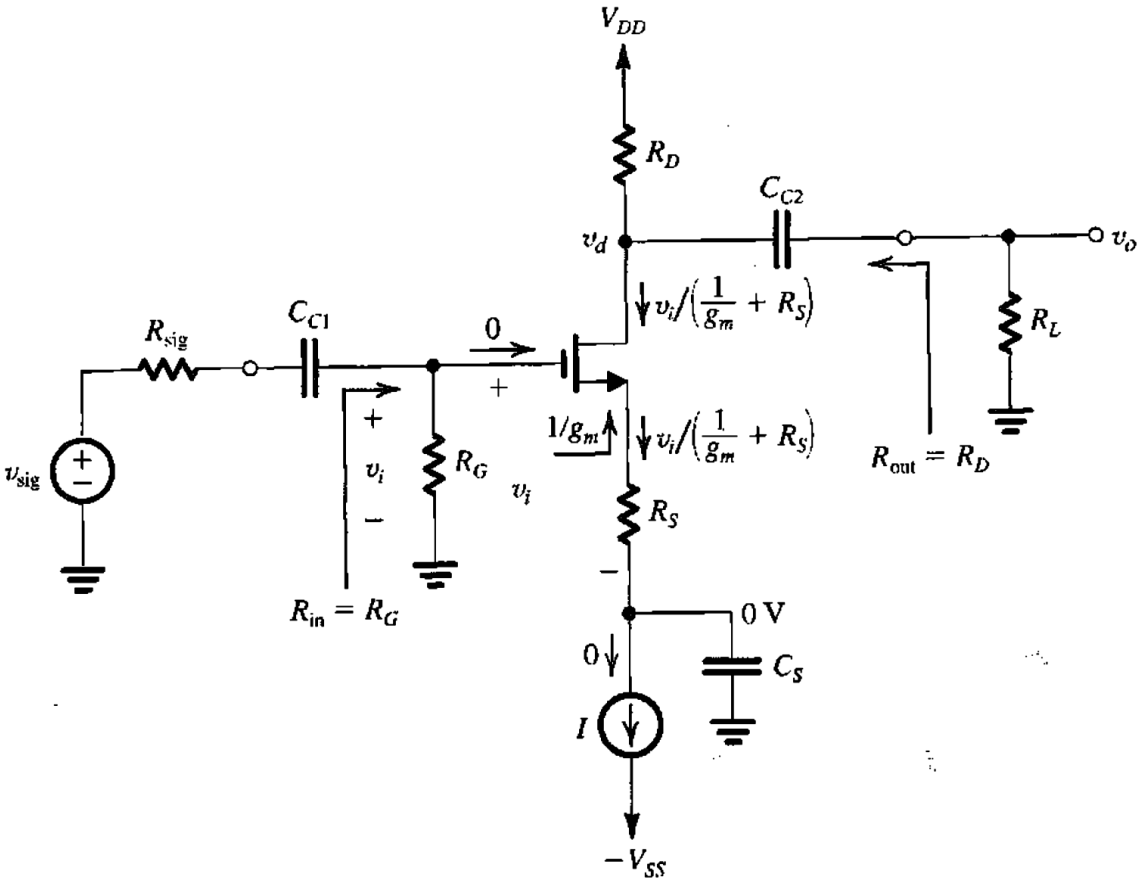
- output resistance R_{out}

$$R_{out} = r_o \| R_D$$

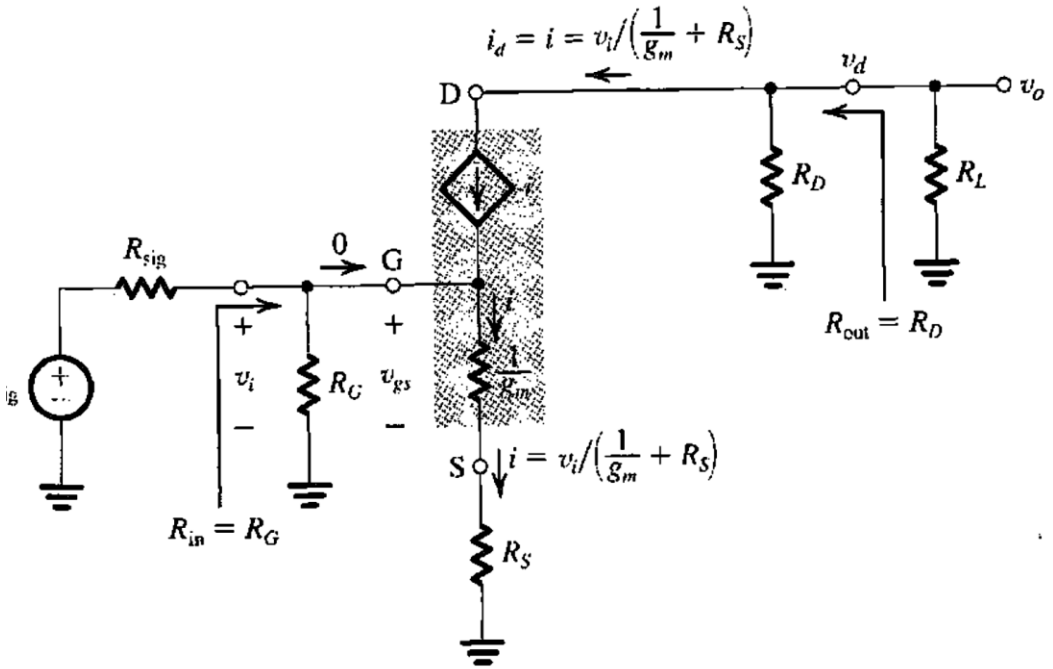
simplified version of the circuit



The Common-Source Amplifier with a Source Resistance



Common-source amplifier with a resistance ***Rs*** in the source lead



Small-signal equivalent circuit with r0 neglected.

- transistor has been replaced by its T equivalent-circuit model.
- not included *r0*
- *r0* would connect the output node of the amplifier to the input side
- Without *r0*, amplifier **nonunilateral.**

1) $R_{in} = R_i = R_G$

2) $v_i = v_{sig}\dfrac{R_G}{R_G + R_{sig}}$

3) *vgs* can be determined from the voltage divider composed of *l/gm* and *Rs*

$$v_{gs} = v_i\frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_S} = \frac{v_i}{1 + g_m R_S}$$

- value of *Rs* to control the magnitude of the signal *vgs*

4) The current *id* is equal to the current *i* flowing in the source lead

$$i_d = i = \frac{v_i}{\frac{1}{g_m} + R_S} = \frac{g_m v_i}{1 + g_m R_S}$$

including *Rs* reduces i_d by the factor (1+*gmRs)*

5) The output voltage

$$v_o = -i_d(R_D \parallel R_L)$$

$$= -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S} v_i$$

6) The voltage gain is

$$A_v = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$$

7) open-circuit voltage gain A_{vo} is

$$A_{vo} = -\frac{g_m R_D}{1 + g_m R_S}$$

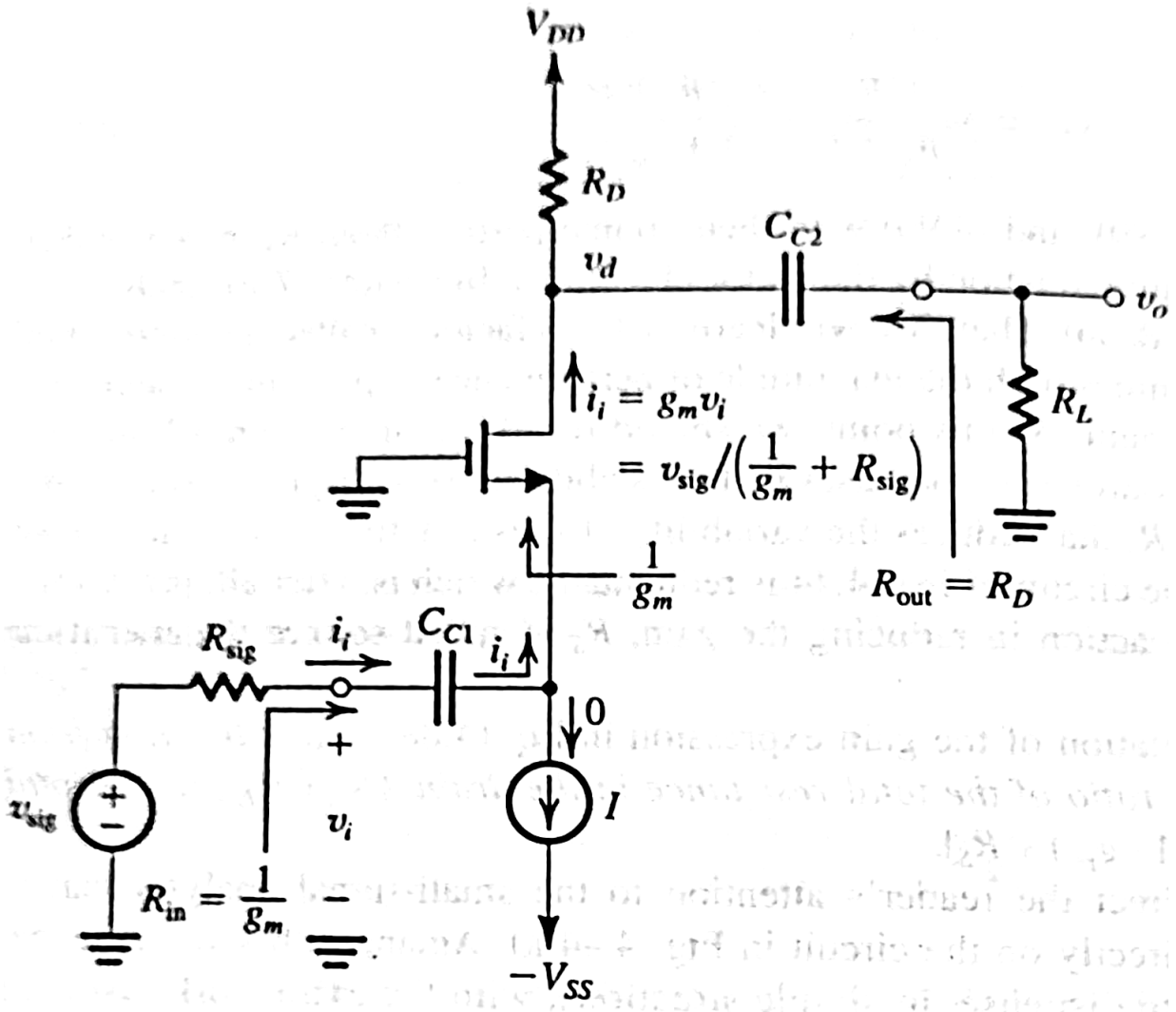
8) The overall voltage gain *Gv* is

$$G_v = -\frac{R_G}{R_G + R_{sig}}\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$$

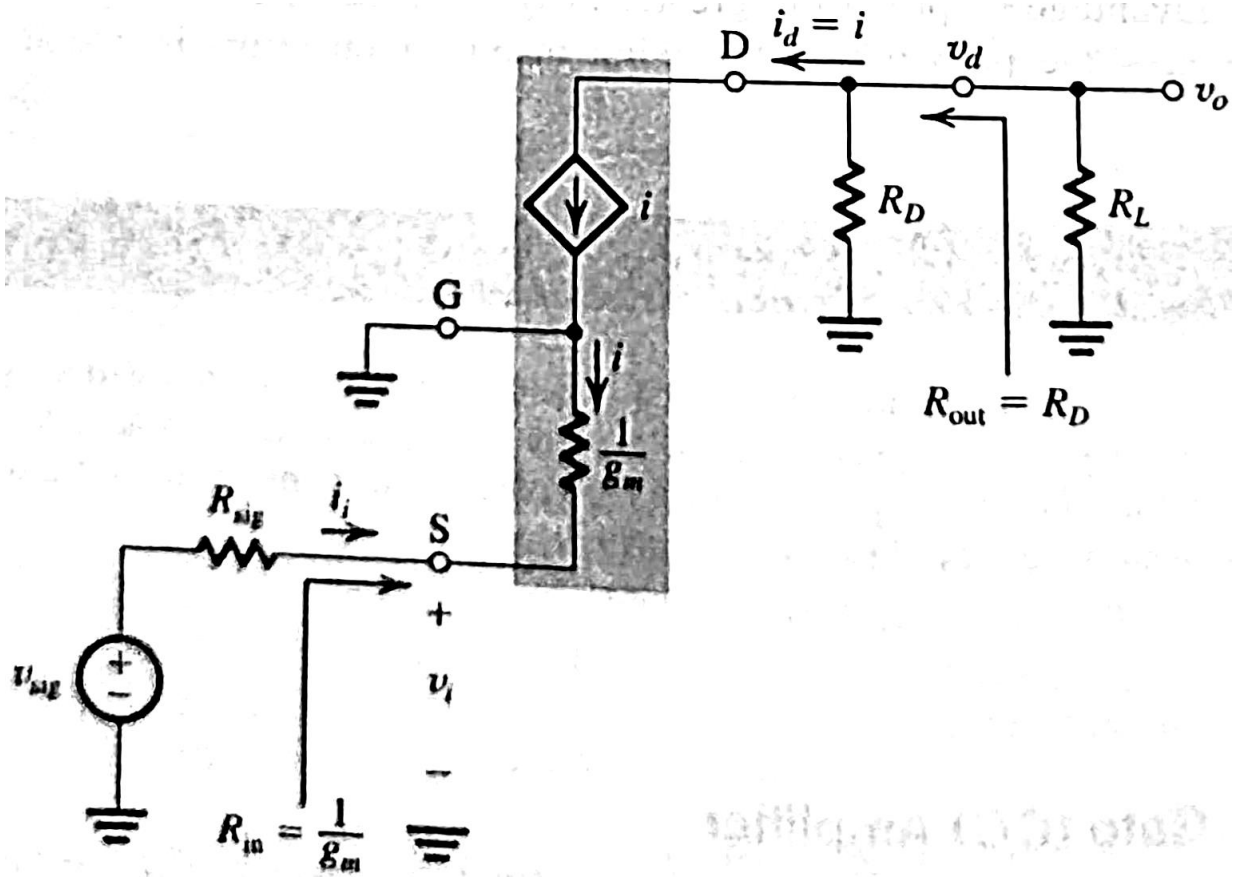
Including *Rs* results in a gain reduction by the factor (1+*gmRs).*

Because of the action in reducing the gain, *Rs* is called **source degeneration resistance.**

The Common-Gate (CG) Amplifier



- Signal ground on the MOSFET gate terminal - **common-gate (CG)** or **grounded-gate amplifier**
- The input signal is applied to the source, and the output is taken at the drain, with gate forming common terminal between the input and output ports.
- Coupling capacitors C_{cl} and C_{C2} perform similar functions to those in the CS circuit.



1) $$R_{in} = \frac{1}{g_m}$$

2) $$v_i = v_{sig}\frac{R_{in}}{R_{in} + R_{sig}}$$

$$v_i = v_{sig}\frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_{sig}} = v_{sig}\frac{1}{1 + g_m R_{sig}}$$

To keep the loss in signal strength small, the source resistance *RS* should be small,

$$R_{sig} \ll \frac{1}{g_m}$$

3) The current i_i

$$i_i = \frac{v_i}{R_{in}} = \frac{v_i}{1/g_m} = g_m v_i$$

4) drain current *id* is

$$i_d = i = -i_i = -g_m v_i$$

5. The output voltage

$$v_o = v_d = -i_d(R_D \| R_L) = g_m(R_D \| R_L)v_i$$

6. The voltage gain

$$A_v = g_m(R_D \| R_L)$$

7. The open-circuit voltage gain

$$A_{vo} = g_m R_D$$

8. The overall voltage gain

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_v = \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_{sig}} A_v = \frac{A_v}{1 + g_m R_{sig}}$$

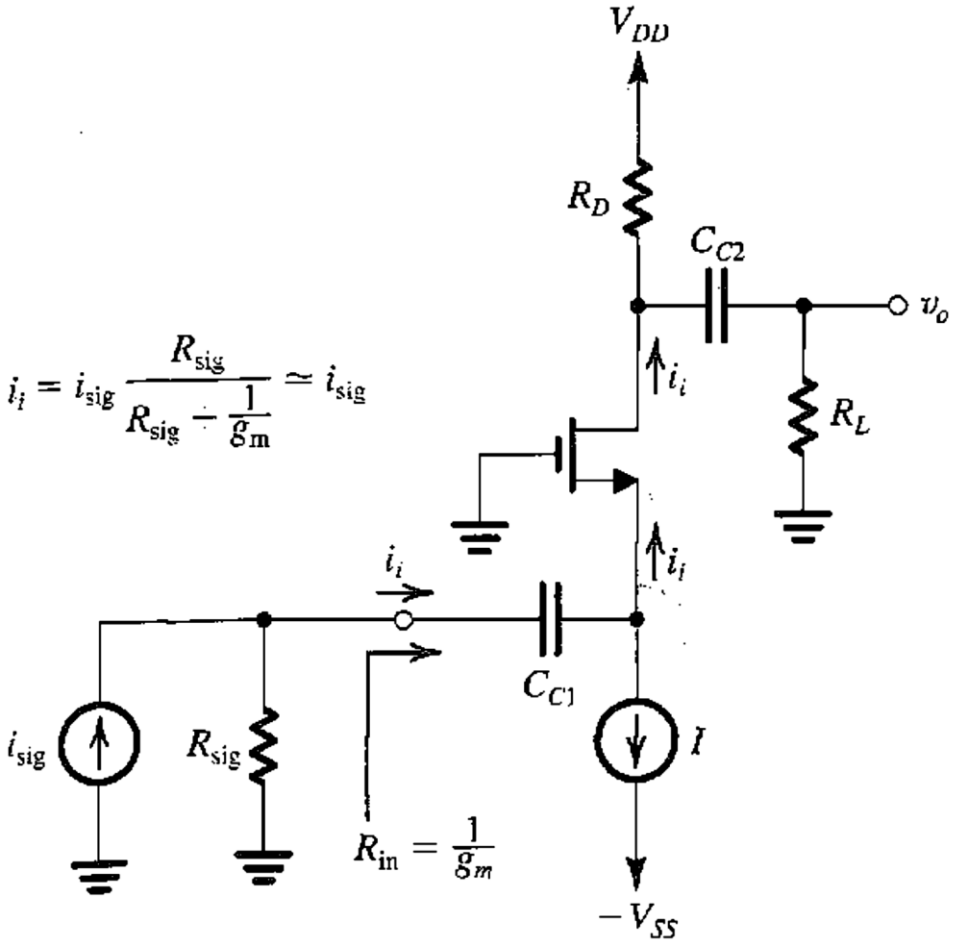
$$G_v = \frac{g_m(R_D \| R_L)}{1 + g_m R_{sig}}$$

9. The output resistance

$$R_{out} = R_o = R_D$$

observations:

1. Unlike the CS amplifier, which is inverting, the CG amplifier is **noninverting**.
2. CS amplifier has a very high input resistance, the **input resistance of the CG amplifier is low.**
3. ***Av*** values of both CS and CG amplifiers are **nearly identical,** the **overall voltage gain** of the CG amplifier is **smaller by the factor 1 + *gmRsig*** , which is due to t he low input resistance of the CG circuit.



Rin = 1/gm and based on the current-divider rule

$$i_i = i_{sig}\frac{R_{sig}}{R_{sig} + R_{in}} = i_{sig}\frac{R_{sig}}{R_{sig} + \frac{1}{g_m}}$$

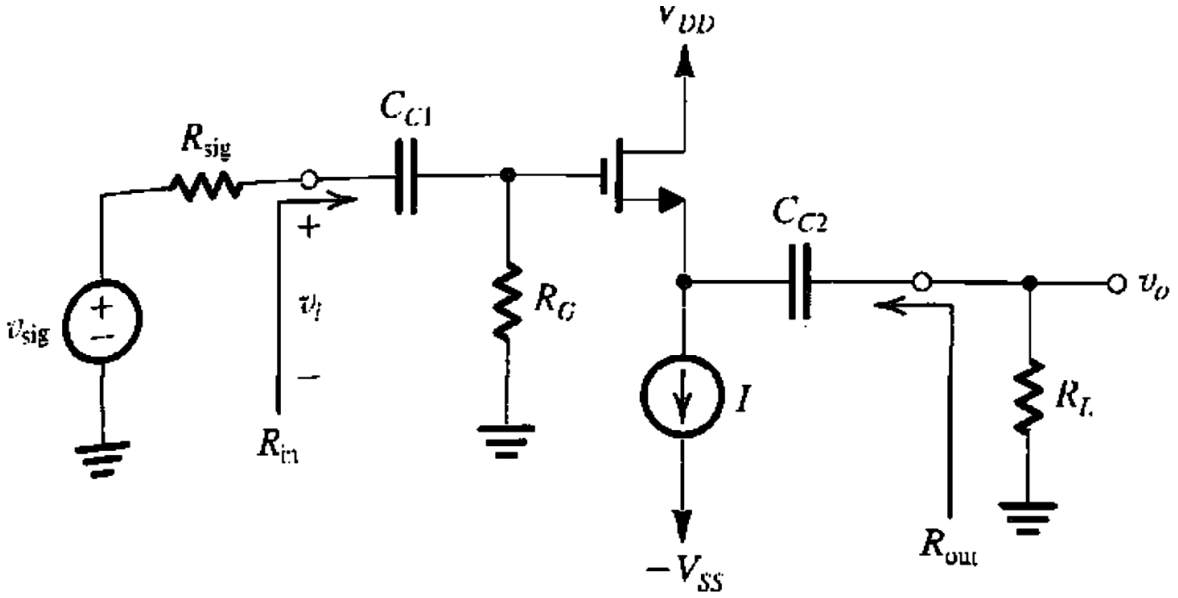
Normally, $R_{sig} \ll \frac{1}{g_m}$

$$i_i \cong i_{sig}$$

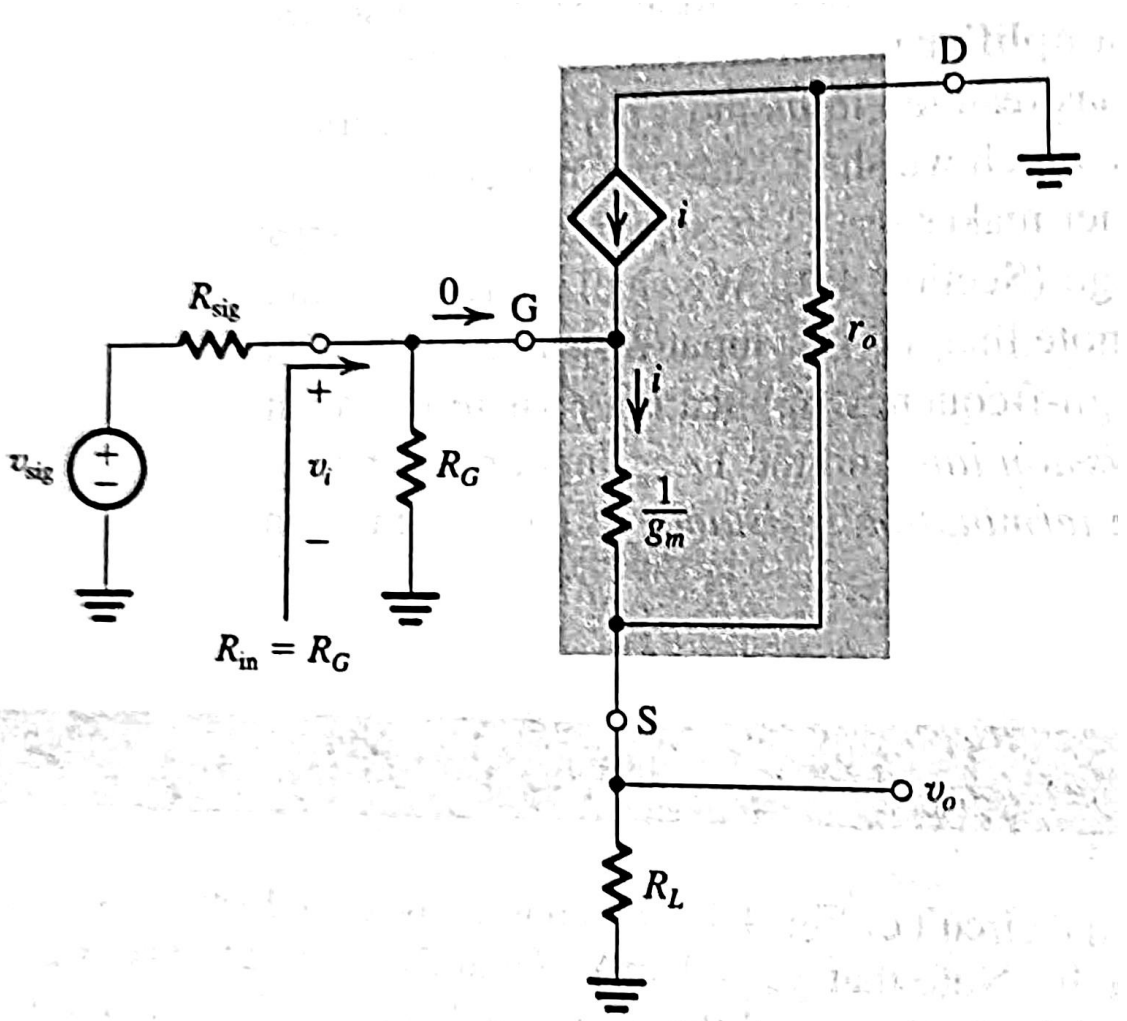
The MOSFET then reproduces this current in the drain terminal at a much higher output resistance. The circuit thus acts in effect as a **unity-gain current amplifier** or a **current follower.**

The common-gate amplifier fed with a current-signal input.

The Common-Drain or Source-Follower Amplifier



A common drain circuit



Small signal Equivalent circuit

1. $R_{in} = R_G$

$$v_i = v_{sig}\frac{R_{in}}{R_{in} + R_{sig}} = v_{sig}\frac{R_G}{R_G + R_{sig}}$$

2. Usually R_G is selected to be much larger than R_{sig} with the result that

$$v_i \cong v_{sig}$$

3. $$v_o = v_i\frac{R_L \| r_o}{(R_L \| r_o) + \frac{1}{g_m}}$$

4. The voltage gain A_v

$$A_v = \frac{R_L \| r_o}{(R_L \| r_o) + \frac{1}{g_m}}$$

5. The open-circuit voltage gain,

$$A_{vo} = \frac{r_o}{r_o + \frac{1}{g_m}}$$

- Normally $r_0 > 1/g_m$, A_{v0} become nearly unity.
- Thus the voltage at the source follows that at the gate, giving the circuit its popular name of **source follower.**

6. The overall voltage gain G_v

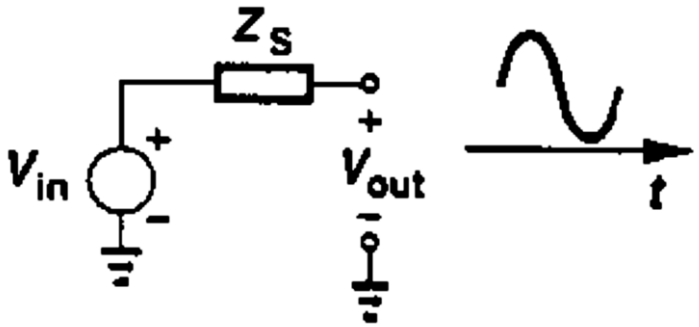
$$G_v = \frac{R_G}{R_G + R_{sig}}\frac{R_L \| r_o}{(R_L \| r_o) + \frac{1}{g_m}}$$

which approaches unity for $R_G > R_{sig}$, $r_0 > 1/g_m$, and $r_0 > R_L$.

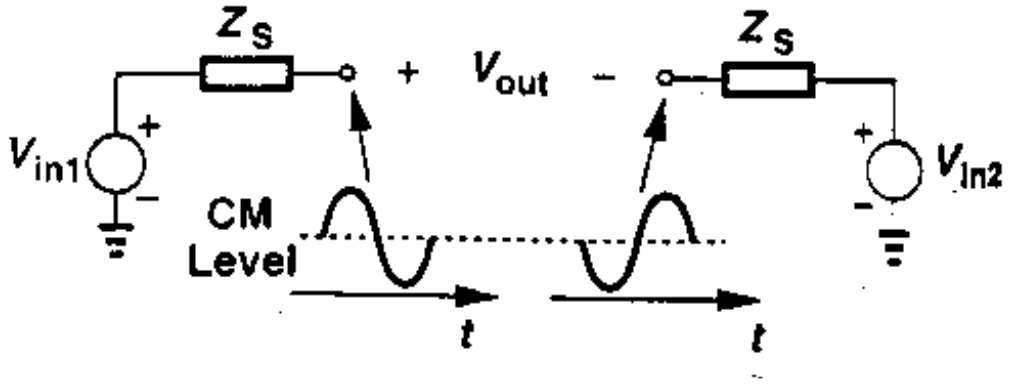
Differential Amplifiers

- Dominant choice in high-performance analog and mixed-signal circuits.

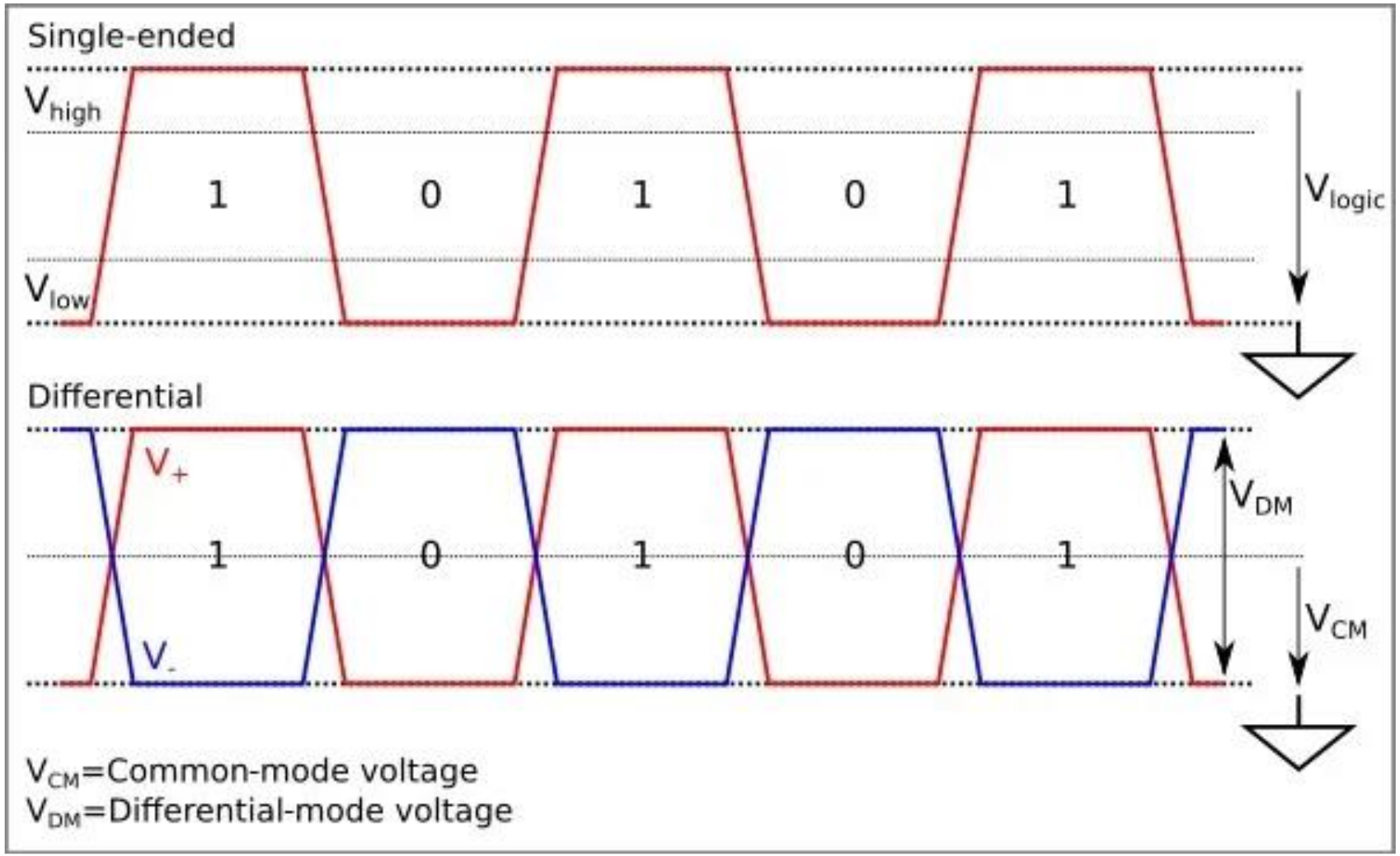
Single-Ended and Differential Operation:



- A single-ended signal is defined as one that is **measured with respect to a fixed potential**, usually the ground.



- A differential signal is defined as one that is **measured between two nodes** that **have equal and opposite signal** excursions around a **fixed potential.**
- The "**center" potential** in differential signaling is called the **"common-mode"** (CM) level.


Single-ended
V_{high}
1
0
1
0
1
V_{low}
V_{logic}
Differential
V_+
1
0
1
0
1
V_-
V_{DM}
V_{CM}
V_{CM}=Common-mode voltage
V_{DM}=Differential-mode voltage

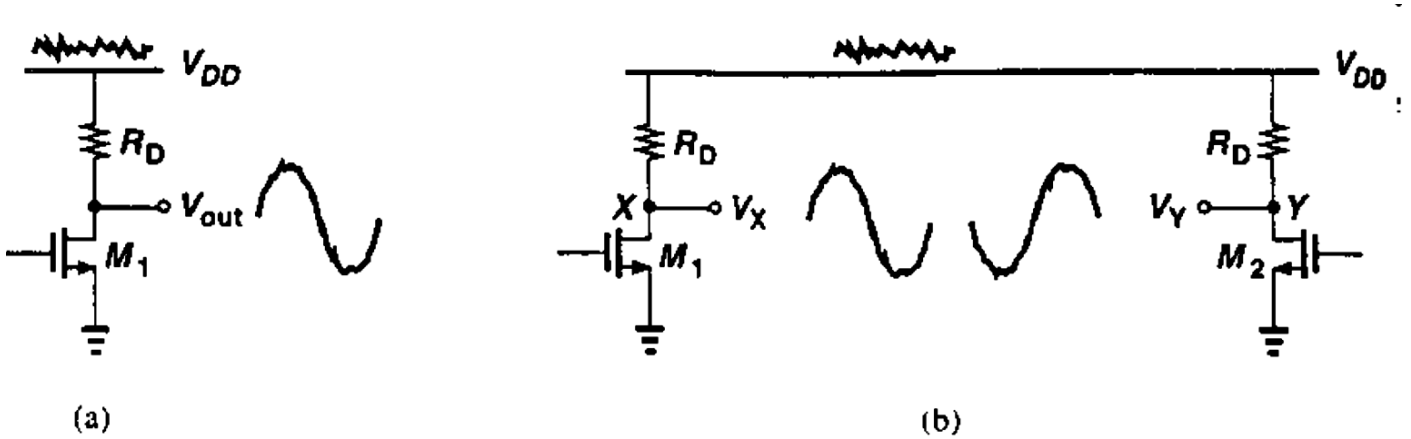
advantages of differential operation:

1) higher immunity to environmental noise.
2) **increase in maximum achievable voltage swings.**
3) simpler biasing and higher linearity

Disadvantages of differential operation:

- circuits **occupy twice** as much **area** as single-ended

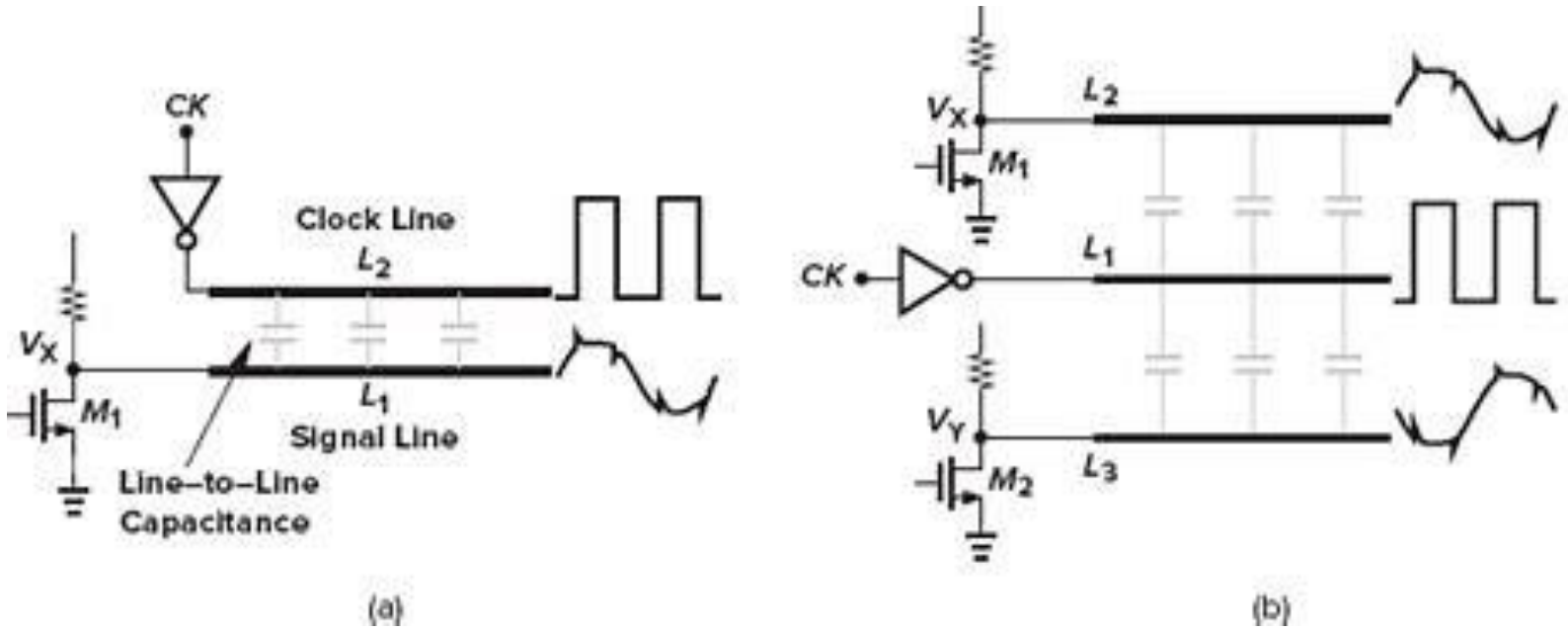
The suppression of nonideal effects by differential operation makes this as minor disadv/drawback



- Maximum output swing at X or Y is equal to VDD - (Vgs - V*th*)
- Where as for Vx - Vy, the peak-to-peak swing is equal to 2(V*DD* - (Vgs – VT)).

1) **higher immunity to environmental noise.**

Example-1:



a) Corruption of a signal due to coupling, b) reduction of coupling by differential operation.

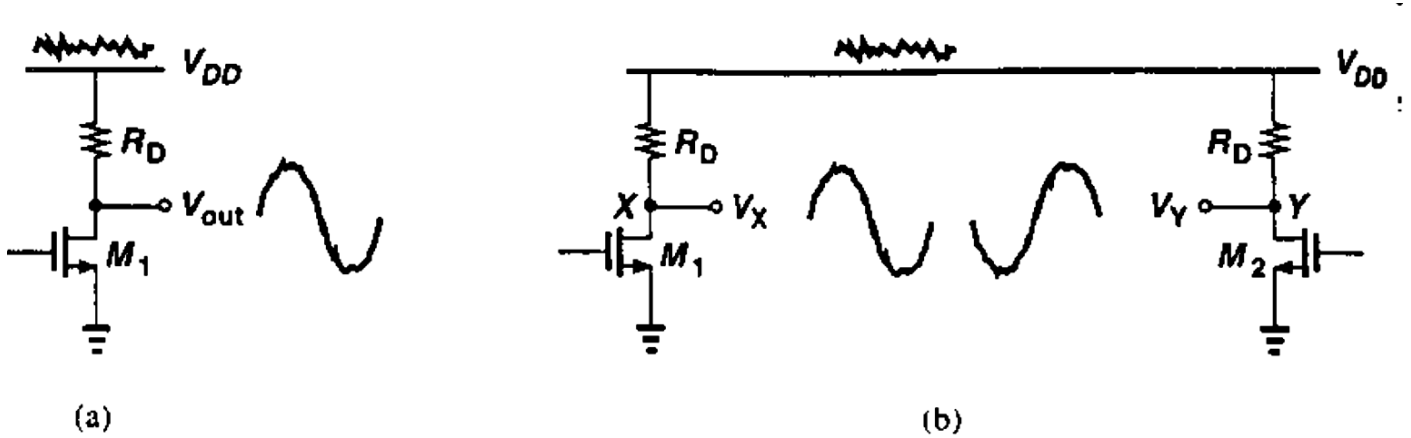
Fig.(a):

- Due to **capacitive coupling** between the lines, transitions on line *L2* **corrupt the signal** on line *L1.*

Fig.(b):

- sensitive signal is distributed as **equal and opposite phases.**
- **common mode level** of the two phases is **disturbed** but the **differential output is not corrupted**
- we say this arrangement **"rejects'** common-mode noise.

- **Example-2 :** common-mode rejection occurs with noisy supply voltages.



Effect of supply noise on (a) a single-ended circuit, (b) a differential circuit.

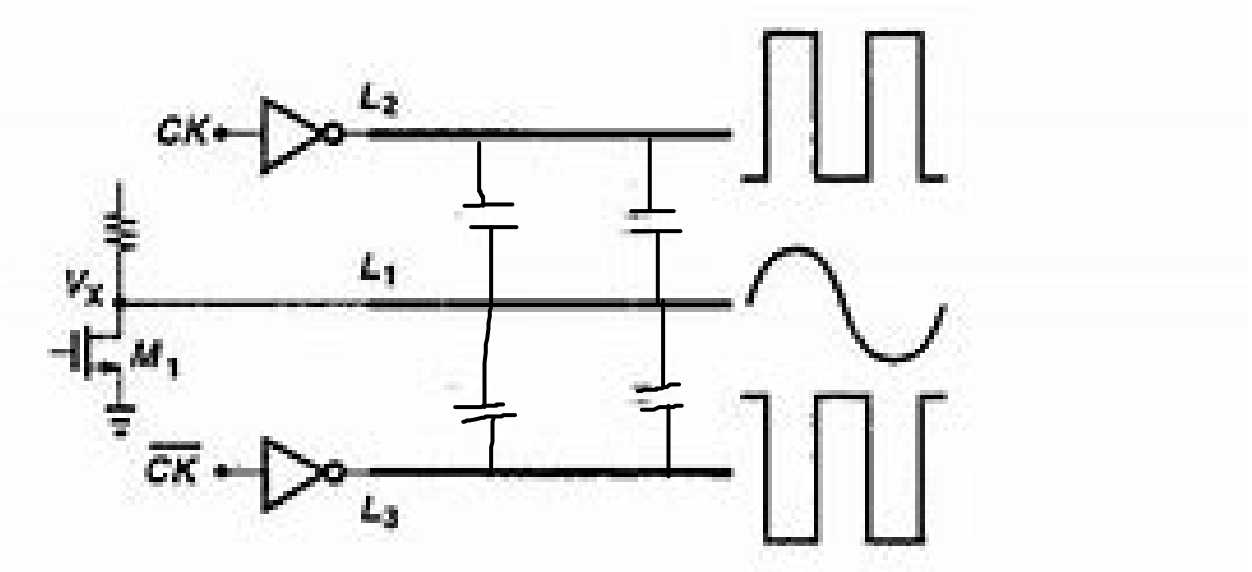
In Fig.(a):

- if VDD varies by ΔV, then Vout changes by approximately the same amount.

In Fig.(b):

- circuit is symmetric, noise on VDD affects Vx and Vy but not Vx - Vy = Vout

- **Example-3 :** beneficial to employ differential distribution for *noisy lines*.



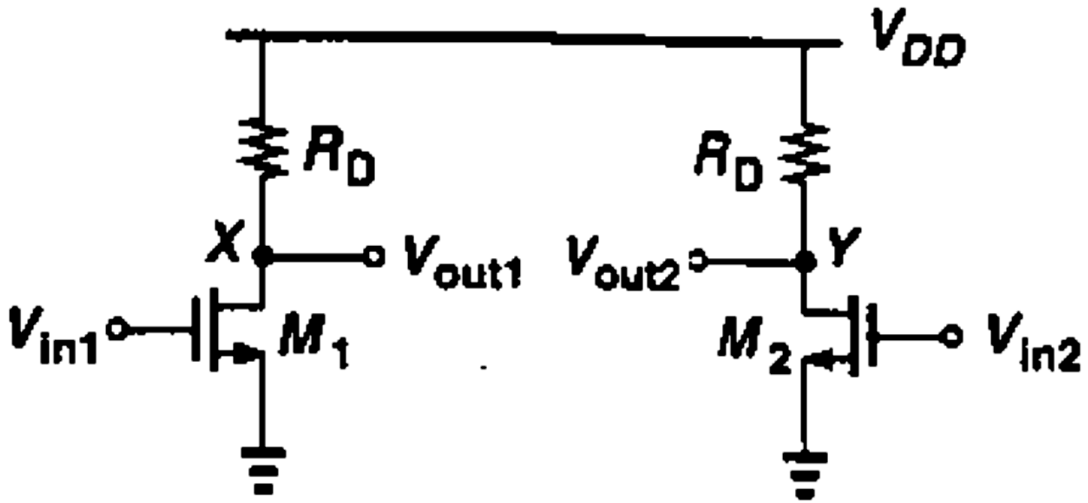
- The clock signal is distributed in differential form on two lines.

- Then, with perfect symmetry, the components coupled from CK and $\overline{CK}$ to the signal line cancel each other.

Basic Differential Pair

- How do we amplify a differential signal?

incorporate **two identical single-ended signal paths** to process the two phases



Simple differential circuit.

circuit offers the advantages of differential signaling:

- high rejection of supply noise, higher output swings, etc.

Example:

But what happens if,

- common-mode disturbance is large for *V*in1 and Vin2 ?

(or)

- i/p common-mode level is not well defined*?*
  - bias currents of M1 and M2 changes
  - varying both the transconductance of the devices
  - Varying the output CM level.
  - The variation of the transconductance leads to a change in the small-signal gain

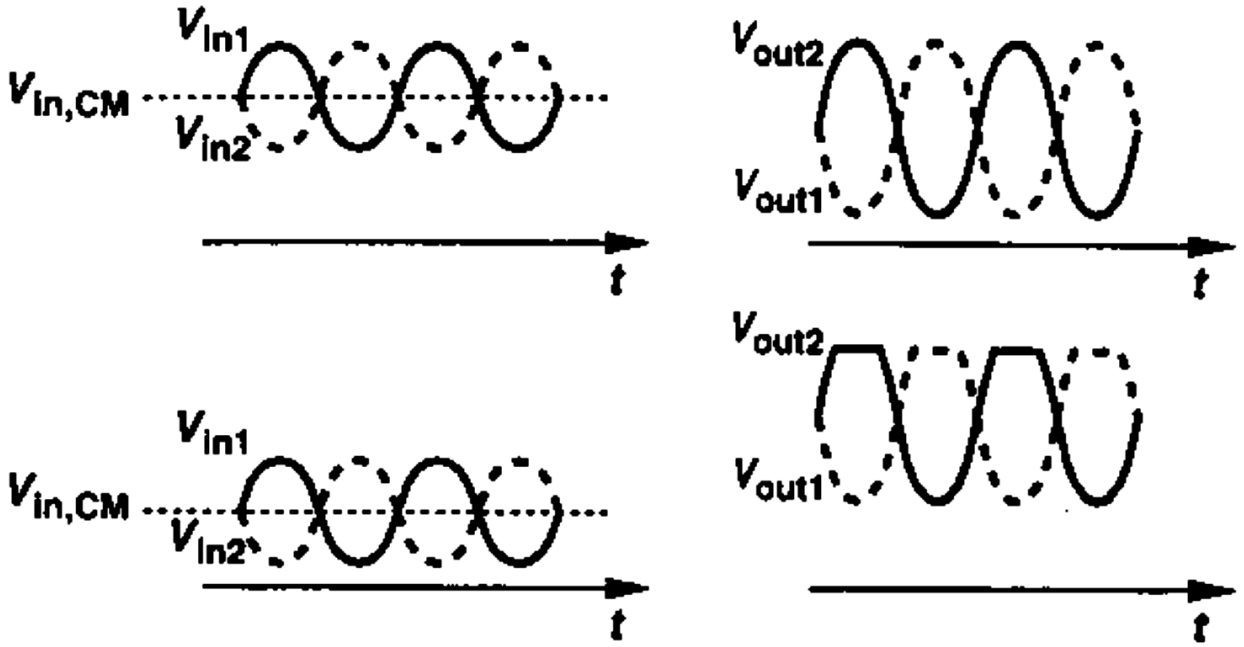
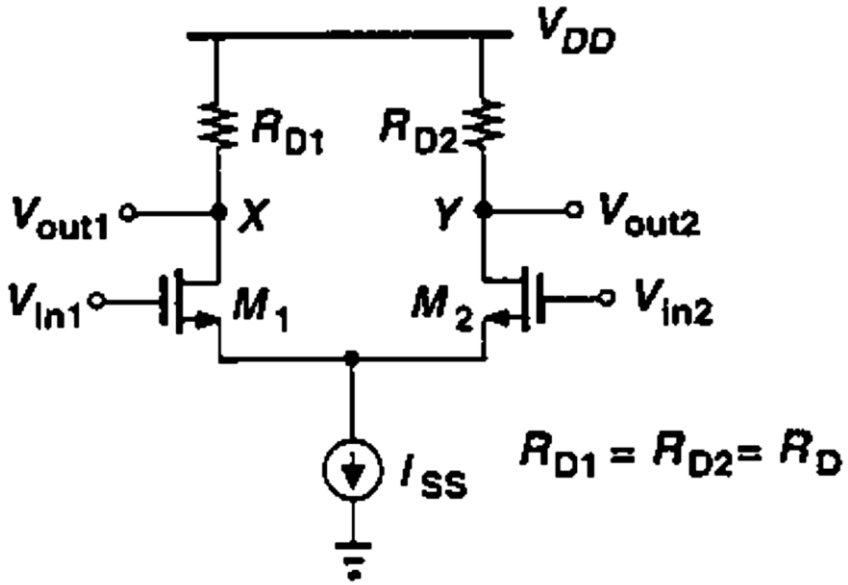


illustration of sensitivity to the input common-mode level.

- If the **input CM level is excessively low**, the minimum values of Vin1 and Vin2 may turn off M1nand M2 → **leading to clipping at the output.**
- Thus, it is important that the bias currents of the devices have minimal dependence on the input CM level.

A simple modification can resolve the above issue - employs a current source *Iss*

- make $I_{D1}+I_{D2}$ independent of $V_{in,CM}$
- If $V_{in1}=V_{in2}$, the bias current of each transistor equal to Iss/2
- $V_{out,CM}$ level is $V_{DD} - R_D I_{SS}/2$



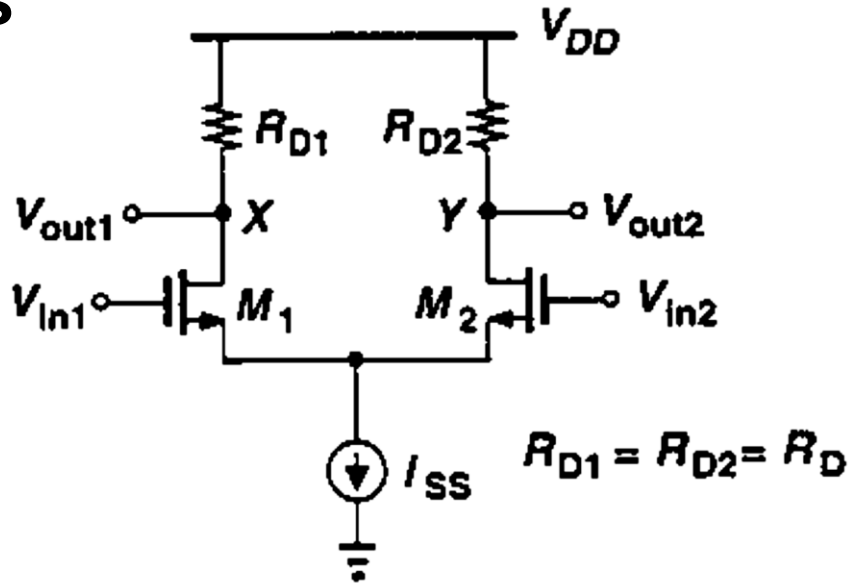
Basic differential pair

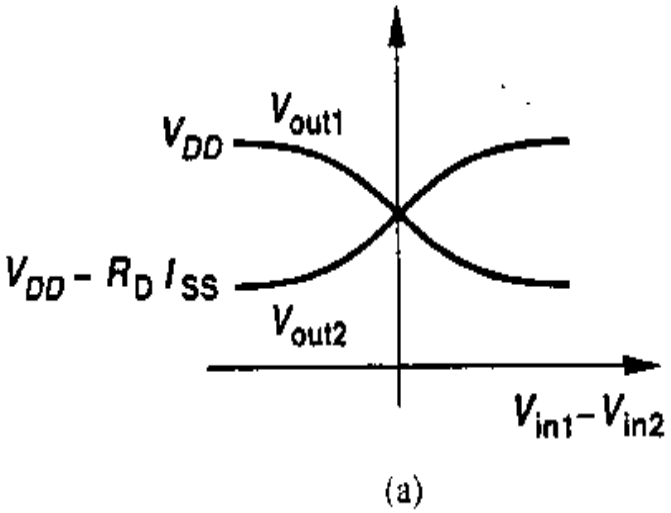
Qualitative Analysis

Differential behaviour:

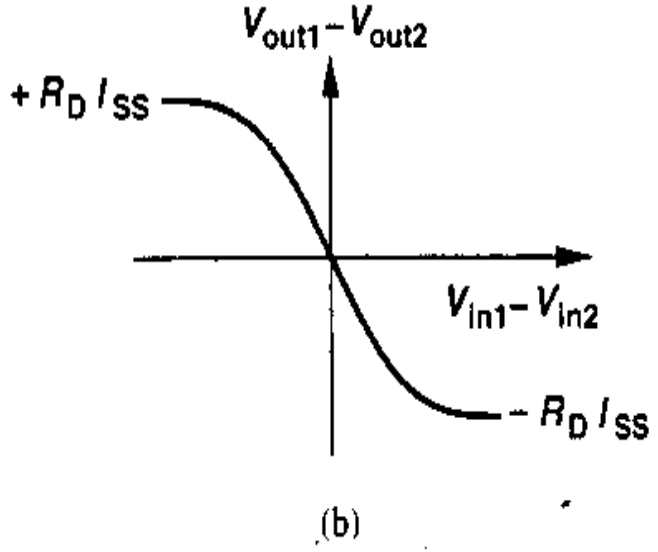
Vin1 – Vin2 varies from -∞ to + ∞

1. Vin1 is much more negative than Vin2
2. Vin1 is brought closer to Vin2
3. Vin1= Vin2
4. Vin1 becomes more positive than Vin2





(a)



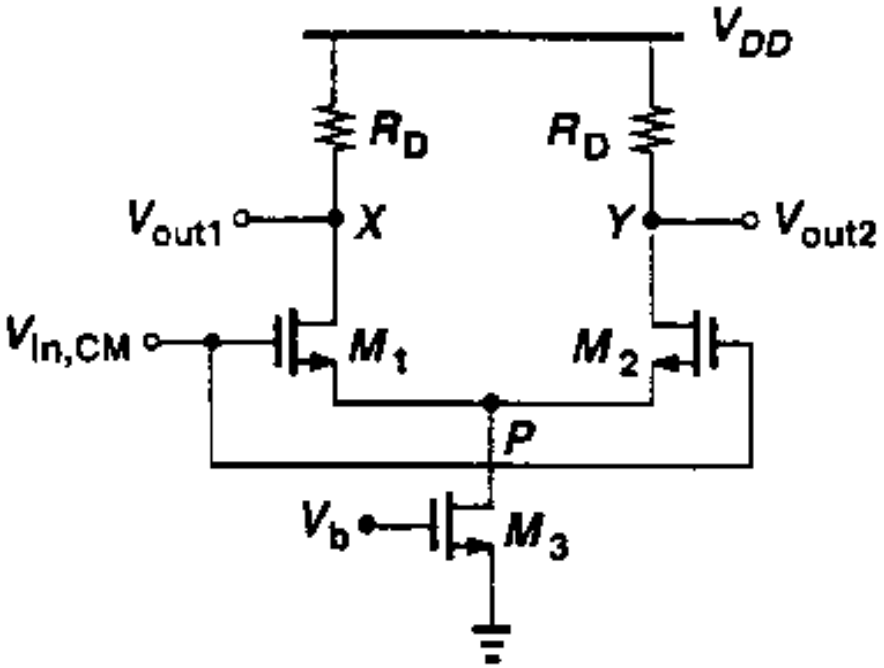
(b)

Two important attributes:

- maximum and minimum levels at the output are well-defined (V_{DD} and $V_{DD} - R_D I_{ss}$. respectively) and independent of the input CM level.
- small-signal gain is maximum for Vin1=Vin2 and gradually falling to zero as Vin1– Vin2 increases.

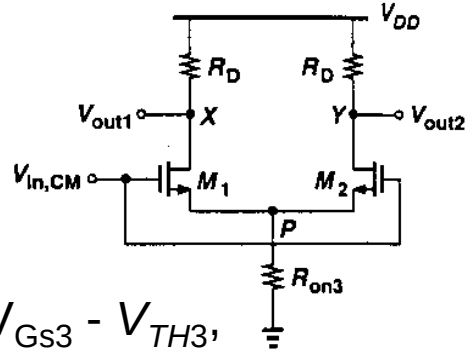
Common- mode behaviour:

Vin1 = Vin2 = $V_{in,CM}$



Differential pair sensing an input common-mode change

1. **$V_{in,CM}$ =0**
   - M1 &M2 → off ; M3 → deep triode region
   - $I_{D1}=I_{D2}=0$;
   - $V_{out1}=V_{out2}=V_{DD}$
   - circuit is incapable of signal amplification



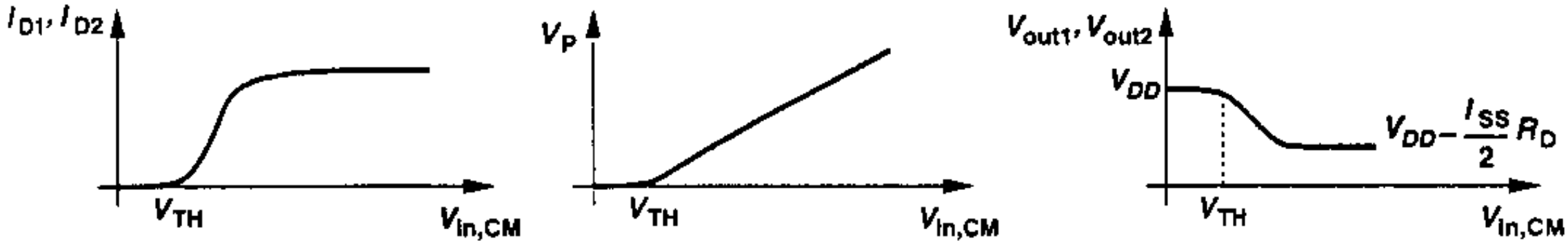
2. **$V_{in,CM}$ becomes more positive**
   - Modeling *M*3 by a resistor as in Fig
   - M1 & M2 → turn on Beyond this point.
   - For high $V_{in,CM}$, the V_{ds3} of *M*3 exceeds V_{Gs3} - V_{TH3}, allowing the device to operate in saturation.
   - The total cu**rrent** through M1 & M2 remains constant.
   - For proper operation: $V_{in,CM} \geq V_{Gs}+(V_{Gs3}-V_{TH3})$.

3. **$V_{in,cm}$ rises further**
   - M1 & M2 → deep triode region if,

$$V_{in.CM} > V_{out1} + V_{TH} = V_{DD} - R_D I_{SS}/2 + V_{TH}$$

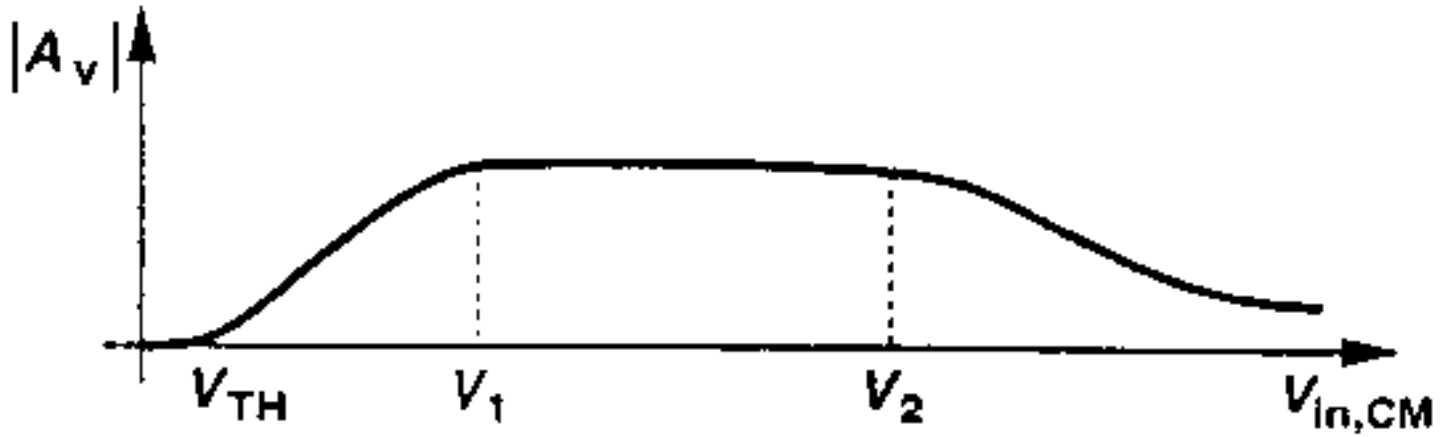
   - This sets an upper limit on the input CM level.
   - The allowable value of $V_{in,cm}$ is bounded as,

$$V_{GS1} + (V_{GS3} - V_{TH3}) \leq V_{in.CM} \leq \min\left[V_{DD} - R_D\frac{I_{SS}}{2} + V_{TH},\ V_{DD}\right].$$



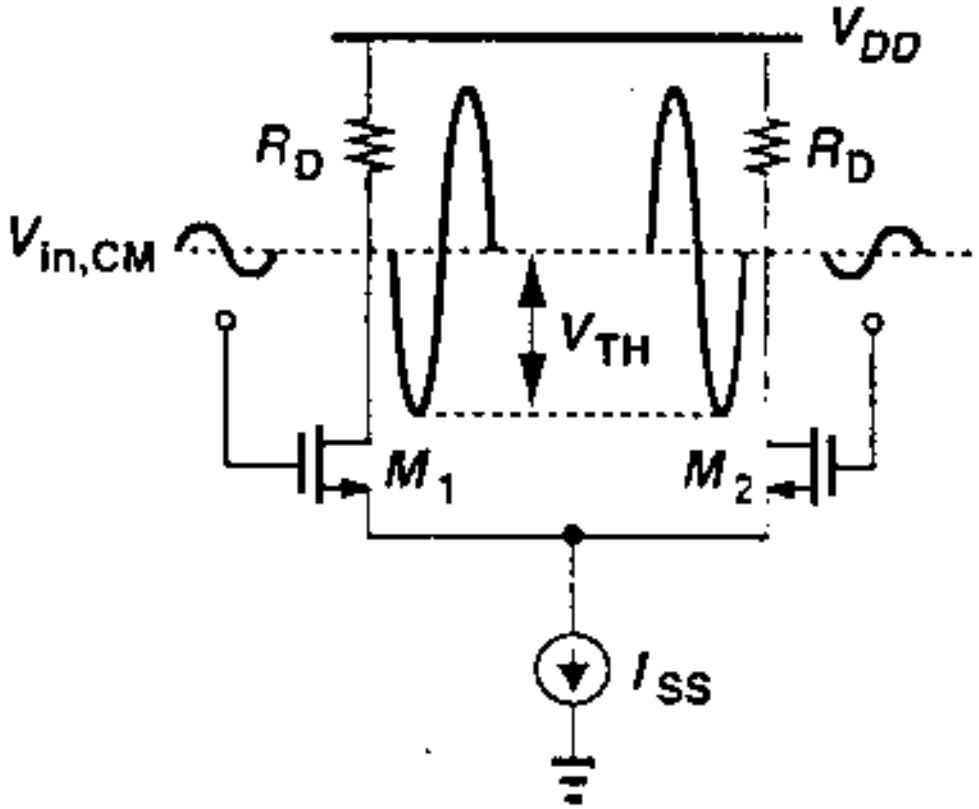
common-mode input-output characteristics.

Sketch the small-signal differential gain of a differential pair as a function of the input CM level.



- The gain begins to increase as $V_{in,cm}$ exceeds V_{TH}.
- After the tail current source enters saturation ($V_{in,cm} = V_1$), the gain remains relatively constant.
- Finally, if $V_{in,cm}$ is so high → input transistors enter the triode region ($V_{in,cm} = V_2$), the gain begins to fall.

How large can the output voltage swings of a differential pair be?

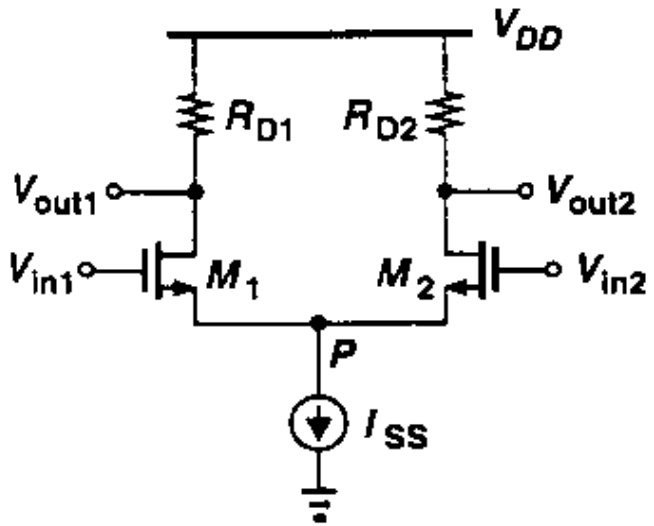


- *M*1 & *M*2 → to be saturated,
- Each output can go as high as V_{DD} but as low as approximately $V_{in,CM} - V_{TH}$.
- **The higher the input CM level, the smaller the allowable output swing**
- **T**he gain of a differential pair is a function of the dc drop across the load resistors.
- **Thus, if $R_D I_{ss}/2$ is large, $V_{in,CM}$ must remain close to ground potential.**

Quantitative Analysis

- Quantify the behavior of a MOS differential pair as a function of the input differential voltage.

large-signal analysis:



$$V_{out1} = V_{DD} - R_{D1} I_{D1}$$

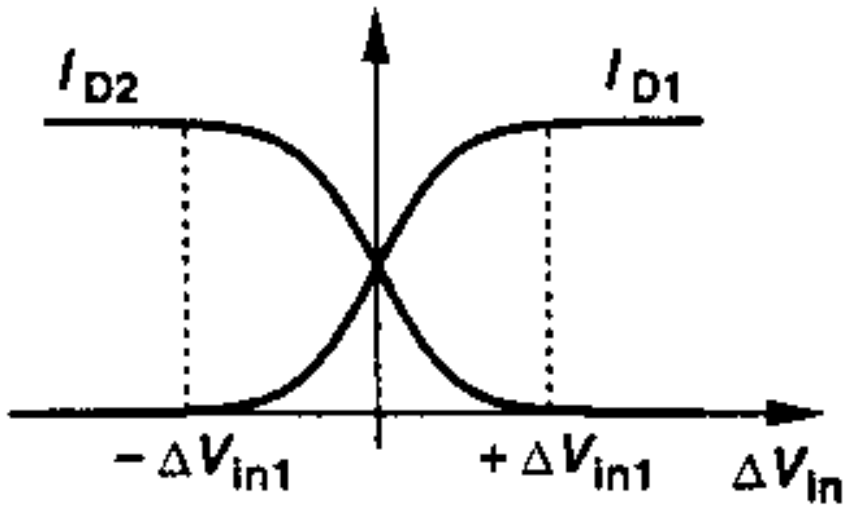
$$V_{out2} = V_{DD} - R_{D2} I_{D2}$$

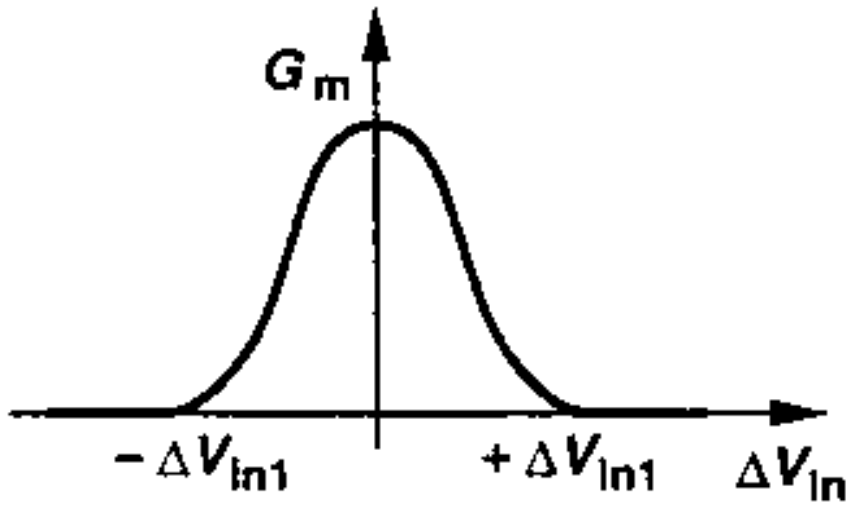
$$V_{out1} - V_{out2} = R_{D2} I_{D2} - R_{D1} I_{D1} = R_D (I_{D2} - I_{D1})$$

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{\dfrac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\dfrac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}.$$

$$G_m = \sqrt{\mu_n C_{ox} (W/L) I_{SS}}.$$

$$A_v = R_D \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS} \mu_n}$$





Variation of drain currents and overall transconductance of a differential pair versus input voltage.

$$\Delta V_{in1} = V_{GS1} - V_{TH}$$