User's Manual

Totally Not SECON's processor is built upon a Python library called MyHDL. MyHDL turns Python into a hardware description and verification language. Using this library gave us the ability to create our processor using hardware descriptions with Python syntax. The library also outputs a .vcd file which allowed us to view all the signals in GTKWave.

1. MyHDL must first be installed. To do so follow the instructions here.
2. To simulate the processor run "processor.py"
3. The processor has several execution modes which are presented in a menu when "processor.py" is ran.
    a. Typing a number will run that many clock cycles
    b. Typing 'a' will run just enough clock cycles to complete the sample program.
    c. Typing 't' will enter a loop where every time the user hits enter, another clock cycle will be run. This will continue until the user enters 'q' or the entire program has been executed.
    d. Typing 'l' will run all the instructions up to the first loop then run a loop each time the user hits enter. After all of the loops have been executed it will run the rest of the program then print out the results.
    e. Typing 'q' will terminate the program.

The processor prints out all of the data stored by each pipeline stage with every clock cycle. After the program executes any input by the user the contents of the register file and the data memory are printed out. Lastly, whenever the program is finished running or the user quits the contents of the register file and the data memory are compared predetermined values to check if everything was executed properly.