# Object:

To design and study 555 timers as: 1. Astable multivibrator, 2. Mono stable multivibrator,

**Introduction**: Oscillators are broadly classified into two categories namely sinusoidal and non-sinusoidal oscillators. Sinusoidal oscillators produce a sine wave output and the non-sinusoidal oscillators produce a square or pulsed output.

A multivibrator circuit is basically a non-sinusoidal oscillator with a regenerative feedback. It is a two state circuit that has zero, one or two stable output states. Depending on the number of stable output states there are three basic types of multivibrator circuits namely Bistable multivibrator having two stable states, Monostable multivibrator having one stable state and Astable multivibrator having zero stable states. In the case of Monostable and Bistable multivibrator an external trigger pulse is required for their operation whereas in the case of Astable multivibrator it has automatic built in triggering which switches it continuously between its two unstable states both SET and RESET. There are two main components in every multivibrator namely the bistable circuit and the two passive networks that are connected in a basic feedback loop. The networks in the circuit can be Monostable (resistive), Astable (resistive-capacitive) or bistable. Astable multivibrator is built of two amplifying stages that are connected in a positive feedback loop using two resistive-capacitive coupling networks. The elements used for amplification may be junction field effect transistors, bipolar junction transistors, operational amplifiers or any other type of amplifier.

**IC 555 TIMER:** The 555 timer is widely used as IC timer circuit and it is the most commonly used general purpose linear integrated circuit. It can run in either one of the two modes: Monostable (one stable state) or Astable (no stable state). In the Monostable mode it can produce accurate time delays from microseconds to hours. In the Astable mode it can produce rectangular waveforms with a variable Duty cycle. The simplicity and ease with which both the multivibrator circuits can be configured around this IC is one of the main reasons for its wide use. Design of an Astable multivibrator using 555 timer IC, generating non-sinusoidal waveform in the form of Rectangular waveform as well as capacitor voltage waveform in the form of ramp waveform.

The 555 timer IC was first introduced around 1970 by the Signetics Corporation as the SE555/NE555 and was called "The IC Time Machine" and was also the very first and only commercial timer IC available. It provided circuit designers with a relatively cheap, stable, and user-friendly integrated circuit for timer and multivibrator applications. The IC comprises of 23 transistors, 2 diodes and 16 resistors with built-in compensation for component tolerance and temperature drift. There are three resistors in the voltage divider net work section in it and all have the same value 5  $K\Omega$  in the bipolar version of this IC and hence the name 555.

#### Block diagram of 555 Timer IC:

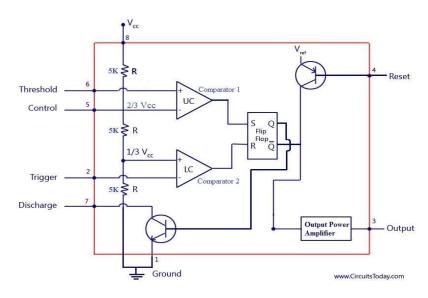
The block diagram of a 555 timer is shown in the figure. A 555 timer has two comparators (which are basically Two op-amps), an R-S flip-flop, two transistors and a resistive network. The Resistive network consists of three equal resistors (5K Ohms each R) and acts as a voltage divider. Notice that the resistor network is designed in such a way that the voltage at the Inverting terminal of Comparator 1 (Upper comparator) will be 2/3Vcc and the voltage at the Non Inverting terminal of Comparator 2 (Lower comparator) will be 1/3Vcc.

Comparator 1 – compares the threshold voltage (at pin 6) with the reference voltage  $+ 2/3 V_{CC}$  volts.

Comparator 2 – compares the trigger voltage (at pin 2) with the reference voltage +  $1/3\ V_{CC}$  volts.

In most applications, the control input is not used, so that the control voltage equals +(2/3) VCC.

555 IC Timer Block Diagram



Upper comparator has a threshold input (pin 6) and a control input (pin 5). Output of the upper comparator is applied to set (S) input of the flip-flop. Whenever the threshold voltage exceeds the control voltage, the upper comparator will set the flip-flop and its output is high. A high output from the flip-flop when given to the base of the discharge transistor saturates it and thus discharges the transistor that is connected externally to the discharge pin 7. The complementary signal out of the flip-flop goes to pin 3, the output. The output available at pin 3 is low. These conditions will prevail until lower comparator triggers the flip-flop. Even if the voltage at the threshold input falls below (2/3) VCC that is upper comparator cannot cause the flip-flop to change again. It means that the upper comparator can only force the flip-flop's output high.

To change the output of flip-flop to low, the voltage at the trigger input must fall below + (1/3) Vcc. When this occurs, lower comparator triggers the flip-flop, forcing its output low. The low output from the flip-flop turns the discharge transistor off and forces the power amplifier to output a high. These conditions will continue independent of the voltage on the trigger input. Lower comparator can only cause the flip-flop to output low.

From the above discussion it is concluded that for the having low output from the timer 555, the voltage on the threshold input must exceed the control voltage or +(2/3) VCC. This also turns the discharge transistor on. To force the output from the timer high, the voltage on the trigger input must drop below +(1/3) VCC. This turns the discharge transistor off.

A voltage may be applied to the control input to change the levels at which the switching occurs. When not in use, a 0.01 nF capacitor should be connected between pin 5 and ground to prevent noise coupled onto this pin from causing false triggering. Connecting the reset (pin 4) to a logic low will place a high on the output of flip-flop. The discharge transistor will

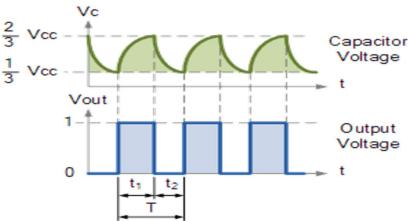
go on and the power amplifier will output a low. This condition will continue until reset is taken high. This allows synchronization or resetting of the circuit's operation. When not in use, reset should be tied to +VCC.

You can see the output wave forms in the side diagrams. The two important parameters that we should understand from the output of timer is ON Time  $(T_{LOW}=T1)$  and OFF Time  $(T_{LOW}=T2)$ .

**ON Time** – is the time for which the timer output Vout has remained in HIGH State. We notate this with  $T_{HIGH}$ .

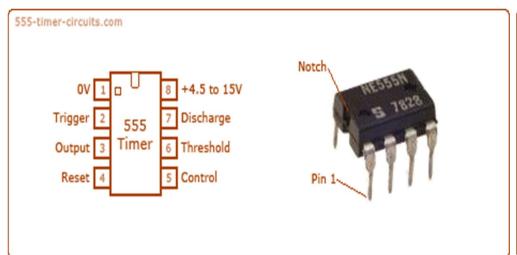
**OFF Time** – is the time for which the timer output Vout has remained in LOW state. We notate this with  $T_{LOW}$ .

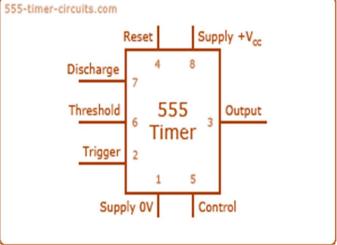
(ON Time and OFF Time are dependent on the values of  $R_{A}$ ,  $R_{B}$  and C in Astable Multivibrator. So we can obtain the desired ON Time and OFF Time at the timer output with the proper calculation of  $R_{A}$ ,  $R_{B}$  and C values.)



Although the timer <u>555</u> has been used in a wide variety of often unique applications it is very hard on its power supply lines, requiring quite a bit of current, and injecting many noise transients. This noise will often be coupled into adjacent ICs falsely triggering them. The 7555 is a CMOS version of the 555. Its quiescent current requirements are considerably lower than that of 555, and the 7555 does not contaminate the power supply lines. It is pin compatible with the 555. So this CMOS version of the 555 should be the first choice when a 555 timer IC is to be used.

**IC Package:** These ICs come in two packages, either the round metal-can called the 'T' package or the more familiar 8-pin DIP 'V' package. DIP package is shown in figure below.





# The Timer IC 555's pin details are as follows:

PIN 1: Ground Pin: Connects to the OV power supply, All voltages are measured with respect to this terminal.

**PIN 2: Trigger input**: The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. When a negative going pulse of amplitude greater than 1/3 VCC is applied to this pin the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage. If Pin 2 is low and pin 6 LOW, output goes and stays HIGH, If pin 6 high and pin 2 goes low, output goes low while pin 2 low.

This pin has a very high impedance about 10 M $\Omega$  and will trigger with about 1  $\mu$ A.

**PIN 3: Output:** The output of the timer is measured here with respect to ground. There are two ways by which a load can be connected to the output terminal: either between pin 3 and ground or between pin 3 and supply voltage +VCC. When the output is low the load current flows through the load connected between pin 3 and +VCC into the output terminal and is called *sink current*. The current through the grounded load is zero when the output is low. For this reason the load connected between pin 3 and +VCC is called normally off-load. On the other hand, then the output is high the current through the load connected between pin 3 and +VCC is zero. This current is called *source current*. The maximum value of sink or source current is up to 200mA. (Pin 3 and 7 are in phase) goes HIGH (about 2 V less than rail) and LOW (about 0.5 V less than 0 V)

**PIN 4: Reset input:** The timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +VCC to avoid any possibility of false triggering. Reset pin is internally connected HIGH via 100 K $\Omega$ , must be taken below 0.8 V to reset the IC chip.

**PIN 5: Control voltage.** A voltage applied to this pin will vary the timing of the RC network (quite considerably). An external voltage applied to this terminal changes the threshold as well as trigger voltage. Thus by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a  $0.01\mu$  F Capacitor to prevent any noise problems.

**PIN 6: Threshold input:** When the voltage at this pin is greater than or equal to the threshold voltage 2/3VCC, the output of the timer low. Means Detects 2/3 of rail voltage to make output Low only if pin 2 is High, This pin has a very high impedance (about  $10 \text{ M}\Omega$ ) and will trigger with about 0.2 A.

**PIN 7: Discharge Pin.** This pin is connected internally to the collector of transistor Q. When the output is high Q is OFF and acts as an open circuit to external capacitor C connected across it. On the other hand, when the output is low, Q is saturated and acts as a short circuit, shorting out the external capacitor C to ground. i.e. discharge pin goes low when pin 6 detect 2/3 rail voltage but pin 2 must be high. If pin 2 is high and pin 6 can be high or low than pin 7 remains low. Discharge pin goes OPEN (high) and stay HIGH when pin 2 detects 1/3 rail voltage (even as a LOW pulse) when pin 6 is low. Pin 7 and 3 are in phase. (Pin 7 is equal to pin 3 but pin 7 does not go high- it goes open. But it goes low and will sink about 200 mA.

**PIN 8: +VCC.** The supply voltage of +5V to + 18V is applied to this pin with respect to ground. But is commonly 5 V DC when working with digital IC circuits.

**Astable Multivibrator**: These circuits are not stable in any state and switch outputs after predetermined time periods. The result of this is that the output is a continuous square/rectangular wave with the properties depending on values of external resistors and capacitors. Thus, while designing these circuits following parameters need to be determined:

- 1. Frequency (or the time period) of the wave.
- 2. The duty cycle of the wave.

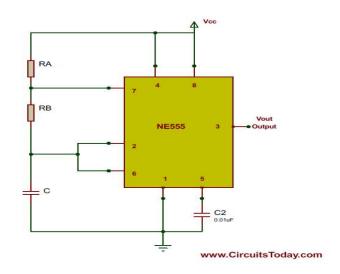
We are explaining an astable multivibrator, often called a free-running multivibrator. An astable multivibrator can be designed using different types of components, say using transistors (and associated components) alone or by using op amps (and associated components) or can be design using 555 Timer IC. If you are wondering what all are the practical applications of an astable multivibrator, let's begin by seeing a few. One of the most common application for an astable multivibrator is to **generate time delays**. Let's say you want to turn an LED "**ON**" for 1 second and keep it "**OFF**" for 0.5 seconds, and then an astable multivibrator is the best circuit you could use to build this application. This circuit does not require any external trigger to change the state of the output, hence the name free-running. Before going to make the circuit, make sure your 555 IC is working.

# 555 Timer Astable Multivibrator Circuit Diagram

An Astable Multivibrator can be designed by adding two resistors a capacitor (RA, RB and C in circuit diagram) to the 555 Timer IC. These two resistors and the capacitor (values) are selected appropriately so as to obtain the desired 'ON' and 'OFF' timings at the output terminal (pin 3). So basically, the ON and OFF time at the output (i.e. the 'HIGH' and 'LOW' state at the output terminal) is dependent on the values chosen for RA, RB and C.

Note: - The capacitor C2 (0.01uF) is connected to pin number 5 (Control Voltage Terminal) in all 555 IC based circuits in which that particular pin (pin 5 – control voltage terminal) is not used. This capacitor is used to avoid noise problems that could arise in the circuit if that pin is left open.

#### Astable Multivibrator using 555 Timer



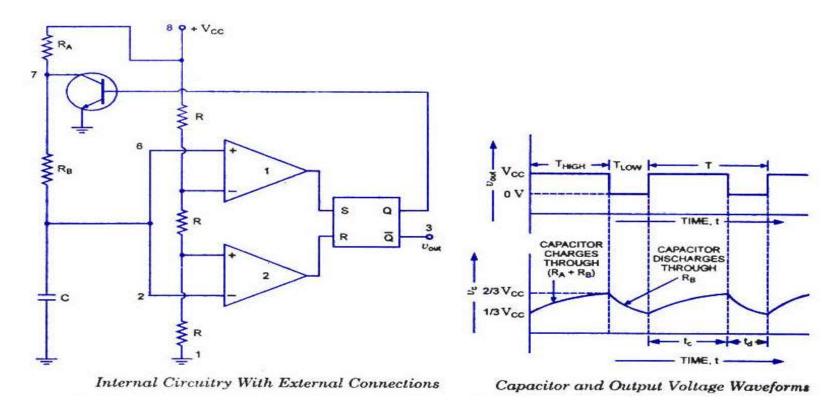
#### The 555 timer Connections as Astable Multivibrator and it's operation

Let's see how the 555 timer astable multivibrator connections are made in the circuit diagram.

Pin 1 is grounded; pins 4 and 8 are shorted and then tied to supply +Vcc, Output (Vout) is taken from pin 3; pin 2 and 6 are shorted and then connected to ground terminal through the capacitor C, pin 7 is connected to supply + VCC through a resistor RA, and between pin 6 and 7 a resistor RB is connected. At pin 5 a bypass capacitor of 0.01uF is connected (this capacitor is for bypass the noise signals created by resistance divider).

# **Astable Multivibrator Working**

To explain the 555 timer astable multivibrator working, we have drawn an internal circuit diagram of 555 timer IC (consisting of two Op Amps, an SR Flip Flop and the transistor connected at the discharging terminal – pin 7) along with the necessary external connections (Ra, Rb and C). A Wave form from the output terminal (Vout – pin 3) is shown towards the right side of the circuit diagram. Carefully observe the circuit diagram and the output waveforms before we begin the explanation.



For the sake of explanation, let's assume the circuit is powered up and right now the status at non inverting flip flop output – Q is LOW. When Q is LOW, Vout will be HIGH (which we call as Timer Output). You see that Q is directly connected to base of transistor (at the discharge terminal). So when Q is LOW, transistor will be in its cut off state (OFF state). In this state, capacitor C is directly connected to power supply Vcc through resistors  $R_A$  and  $R_B$ . So the capacitor will start charging towards the supply voltage Vcc and the charging time constant will be defined by  $R_A$  and  $R_B$  values as  $(R_A + R_B) * C$ . The capacitor will charge towards Vcc and this will increase the threshold voltage (voltage across pin 6) of 555 IC. When the capacitor charges up to 2/3Vcc and beyond, the threshold voltage will also surpass 2/3Vcc level and this will force the op amp output (comparator 1) to go HIGH (take note that the reference voltage at – terminal of comparator 1 is 2/3Vcc). Since

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the op amp output of comparator 1 is connected 'S' (SET input) of SR flip flop, the flip flop will be triggered and the Q output (non inverting output) of flip flop will turn HIGH. You got up to this? You may recall that we have begun this explanation by assuming Q is LOW initially. Now as a result of capacitor charging, Q has turned HIGH automatically from LOW. When Q goes HIGH, Vout will automatically go to LOW as Vout is nothing but a compliment of Q.

When Q is HIGH, the transistor at pin 7 (the discharge terminal) will be turned ON and the transistor will get saturated. When the transistor gets saturated, the pin 7 (discharge terminal) will act as a ground for the capacitor. As a result, a new path is available for the capacitor to discharge from 2/3Vcc level to zero volts. The capacitor will start discharging through the new path (through Rb) and this will result in decrease in voltage across the trigger terminal (pin 2) of 555 IC. The discharging time constant is defined by Rb\*C. Once the capacitor discharges to a level below 1/3Vcc, resulting in the same voltage (voltage of capacitor) across the trigger terminal (notice that the reference input voltage at + terminal of comparator 2 is 1/3Vcc), the op amp output of comparator 2 will go HIGH. Since the output of comparator 2 is connected to R' – the RESET input terminal of SR flip flop, the Q output of flip flop will go from HIGH to LOW. When Q goes to LOW, Vout will automatically go to HIGH. Thus an automatic transition from HIGH to LOW and then from LOW to HIGH is achieved in an Astable Multivibrator. The cycle repeats.

Inside the 555 IC, this discharge terminal (pin 7) is connected to the collector terminal of a transistor whose base is directly connected to the output terminal (non inverting terminal – Q) of SR flip flop. You have to notice that Vout (pin 3 – output terminal of 555 IC) is taken from the inverting output terminal (Q complimentary terminal) of SR flip flop. So when flip flop output (non inverting) Q is HIGH, Vout will be LOW and when flip flop output Q is LOW, Vout will be HIGH.

The key external component of the astable timer is the capacitor.

The time during which the capacitor C charges from 1/3 V<sub>CC</sub> to 2/3 V<sub>CC</sub> is equal to the time the output is high and is given  $T_{HIGH} = 0.693$  (R<sub>A</sub> + R<sub>B</sub>) C, which is proved below.

Voltage across the capacitor at any instant during charging period is given as, V<sub>c</sub>=V<sub>CC</sub> (1<sup>-et/RC</sup>)

The time taken by the capacitor to charge from 0 to  $\pm 1/3$  V<sub>CC</sub>

$$t1=1/3 V_{CC} = V_{CC} (1^{-et/RC})$$

The time taken by the capacitor to charge from 0 to  $\pm 2/3$  V<sub>CC</sub>

or  $t2 = RC \log^{6} 3 = 1.0986 RC$ 

So the time taken by the capacitor to charge from +1/3 V<sub>CC</sub> to +2/3 V<sub>CC</sub>

tc = (t2 - t1) = (1.0986 - 0.405) RC = 0.693 RC

Substituting  $R = (R_A + R_B)$  in above equation we have

 $T_{HIGH} = tc = 0.693 (R_A + R_B) C$ 

Where  $R_A$  and  $R_B$  are in ohms and C is in farads.

The time during which the capacitor discharges from +2/3 V<sub>CC</sub> to +1/3 V<sub>CC</sub> is equal to the time the output is low and is given as

td or  $T_{LOW} = 0.693 R_B C$  where  $R_B$  is in ohms and C is in farads The above equation is worked out as follows:

Voltage across the capacitor at any instant during discharging period is given as

 $vc = 2/3 V_{CC} e-td/R_BC$ 

Substituting vc = 1/3 V<sub>CC</sub> and t = td in above equation we have

 $+1/3 V_{CC} = +2/3 V_{CC} e^{-td}/RBC$ 

Or td = 0.693 RBC

Overall period of oscillations,  $T = T_{HIGH} + T_{LOW} = 0.693$  ( $R_A + 2R_B$ ) C, The frequency of oscillations being the reciprocal of the overall period of oscillations T is given as  $f = 1/T = 1.414/(R_A + 2R_B)C$ 

Equation indicates that the frequency of oscillation / is independent of the collector supply voltage +V<sub>CC</sub>.

Often the term duty cycle is used in conjunction with the astable multivibrator.

The duty cycle, the ratio of the time thigh during which the output is high to the total time period T is given as

% duty cycle, D = thigh / T \* 100 =  $(R_A + R_B)$  /  $(R_A + 2R_B)$  \* 100

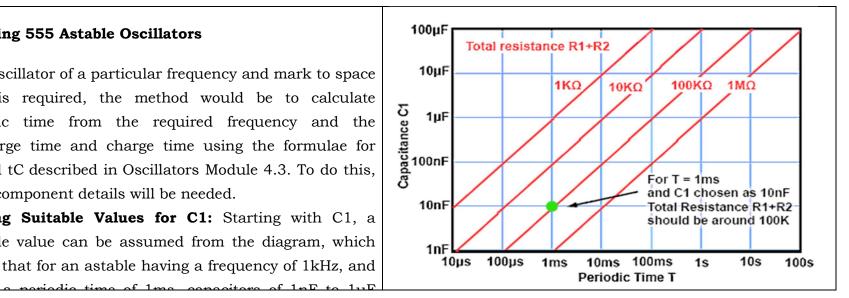
From the above equation it is obvious that square wave (50 % duty cycle) output cannot be obtained unless  $R_A$  is made zero. However, there is a danger in shorting resistance  $R_A$  to zero. With  $R_A$  = 0 ohm, terminal 7 is directly connected to +  $V_{CC}$ . During the discharging of capacitor through  $R_B$  and transistor, an extra current will be supplied to the transistor from  $V_{CC}$  through a short between pin 7 and + $V_{CC}$ . It may damage the transistor and hence the timer.

There is a possibility to construct a symmetrical square wave can be obtained if a diode is connected across resistor  $R_B$ , as illustrated in dotted lines in figure below. The capacitor C charges through  $R_A$  and diode D to approximately +  $2/3V_{CC}$  and discharges through resistor  $R_B$  and terminal 7 (transistor) until the capacitor voltage drops to  $1/3~V_{CC}$ . Then the cycle is repeated. To obtain a square wave output,  $R_A$  must be a combination of a fixed resistor R and a pot, so that the pot can be adjusted to give the exact square wave.

## **Designing 555 Astable Oscillators**

If an oscillator of a particular frequency and mark to space ratio is required, the method would be to calculate periodic time from the required frequency and the discharge time and charge time using the formulae for tD and tC described in Oscillators Module 4.3. To do this, some component details will be needed.

Finding Suitable Values for C1: Starting with C1, a suitable value can be assumed from the diagram, which shows that for an astable having a frequency of 1kHz, and

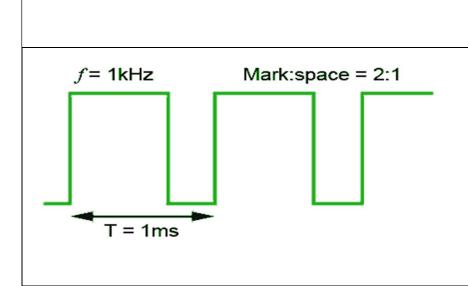


#### **Advantages and Disadvantages of Astable Multivibrators**

These multivibrators are changes between one stable state to another continuously. This permits multivibrators to power themselves & achieve work at a constant rate without impact from any external forces or actions. Also, these multivibrators are low cost to produce, and simple to design

These multivibrators do not transfer the whole o/p signal to the i/p. This is due to resistance in the circuit, nonexistence of a totally closed loop at the o/p terminals, and the leaning of one transistor/capacitor to absorb energy at a somewhat different rate than the other. Although the amplifier restores the lost energy when it amplifies the signal, the signal will finally be too small to be of any use.

# To design a 555 astable with a frequency of 1 kHz and a mark to space ratio (Duty cycle ratio\*\*) of 2:1



Manufacturers specify the maximum total resistance usually around 10 to  $20M\Omega$  that may be used with their particular variant of the 555, however using such high values can increase the error between calculated and actual frequencies, so for many uses a  $1M\Omega$  maximum can be recommended. The minimum total resistance value for the combination of R1 and R2 depends largely on the value of R1. The junction of R1/R2 is connected to pin 6 and to the trigger input pin 2. If the value of R1 is less than about  $1K\Omega$ , there is a danger that the trigger input may not be able reach a low enough voltage to trigger comparator 1, and so oscillations cannot take place. From this it can be assumed that if R1 must be  $1K\Omega$  or above and R1 + R2 should be kept below  $1M\Omega$ ; a 10nF capacitor would allow a suitable total resistance of around  $100K\Omega$  to be calculated.

## Calculation:

Periodic time (Frequency) T = 1/f = 1/1000 = 1 ms

Charge time  $tC = 2/3T = 667\mu s$ 

Discharge time  $tD = 1/3T = 333\mu s$ 

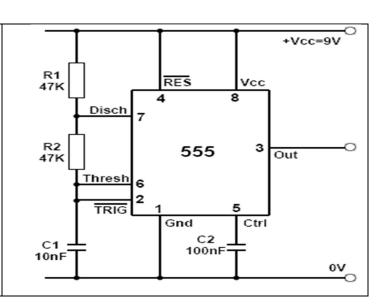
Assuming (from Fig. ) a 10nF capacitor will be used, which discharges via R2 only:

$$tD = 0.7 \times R2 \times C1$$

Re-arranging the formula to find R2 gives:

$$R2 = \frac{tD}{0.7xC1} = 47.6 \text{ k}\Omega$$

During the charge time C1 charges via R1 + R2, therefore:



$$tC = 0.7 \times (R1+R2) \times C1$$

Rearranging the formula to find (R1+R2) gives:

$$(R1+R2) = \frac{tc}{0.7XC1} = 95.3 \text{ k}\Omega$$

As 
$$R1 = (R1+R2) - R2$$
 then:

$$R1 = 95.3K\Omega - 47.6K\Omega = 47.7K\Omega$$

Choosing the nearest preferred values (available in Lab) for R1 and R2 gives the value  $47K\Omega$  for both resistors.

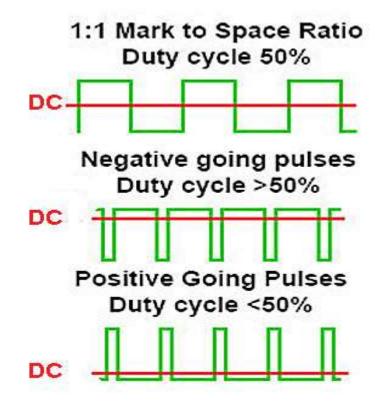
Check that two  $47K\Omega$  will give the required frequency of 1kHz? Simply apply the frequency formula for a 555 astable using the calculated values:

$$F_{Osc} = \frac{1.414}{(R1+2R2)C1}$$
 993 Hz (approx 1 kHz)

#### \*\* Duty Cycle (Space Ratio)

The mark to space ratio of a square wave or pulse oscillator is often referred to as the Duty Cycle. This is a more useful term when the purpose of an output wave is to drive some device such as a motor. It gives a more useful comparison to the power supplied to the motor than describing the mark to space ratio of the output. Changing the duty cycle changes the average DC voltage or DC current level of the output, as shown in Fig. 4.4.5 and hence the power supplied to control the speed of the motor. This is also important in driving output devices such as lamps, heaters and many others.

The Duty Cycle is a term that describes the percentage of each cycle taken up by the active or high period. For example a square wave with a mark to space ratio of 1:1 has a duty cycle of 50% so the high period takes up 50% of the total period. In the waveform illustrating negative going pulses the duty cycle may be about 80% while in the positive going pulse waveform, the duty cycle may be around 20%.



# Monostable Multivibrator using a 555 timer

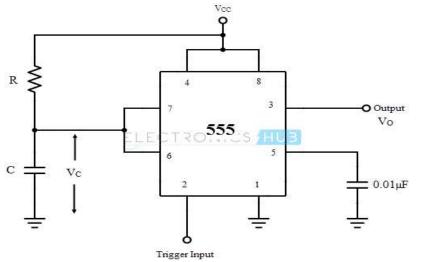
We now discuss another important application of 555 timers that is as a monostable multivibrator. A monostable multivibrator is a pulse generating circuit having one stable and one quasi-stable state. Since there is only one stable state, the circuit is known as "monostable multivibrator". The duration of the output pulse is determined by the RC network connected externally to the 555 timer. The stable state output is approximately zero or at logic-low level. An external trigger pulse forces the output to become high or approximately VCC. After a predetermined length of time, the output automatically switches back to the stable state and remains low until a trigger pulse is again applied. The cycle then repeats, That is, each time a trigger pulse is applied; the circuit produces a single pulse. Hence, it is also called "one-shot multivibrator".

# **Circuit and Operation**

The following figure is the schematic of IC 555 as a Monostable Multivibrator. This is the basic mode of operation of the IC 555. It requires only two extra components to make it work as a monostable multivibrator: a resistor and a capacitor.

As the name specifies, a monostable multivibrator has only one stable state. When a trigger input is applied, a pulse is produced at the output and returns back to the stable state after a time interval. The duration of time for which the pulse is high will depend on the timing circuit that comprises of a resistor (R) and a capacitor (C).

The details of the connection are as follows. The pins 1 and 8 are connected to ground and supply (VCC) respectively. Output is taken at pin 3. To avoid accidental reset of the circuit, pin 4 is connected to the VCC. Pin 5, which is the control voltage input, should be grounded when not in use. To filter the noise, it is connected to the ground via a small capacitor of capacitance  $0.01\mu F$ .



# **Applications of Monostable Multivibrator**

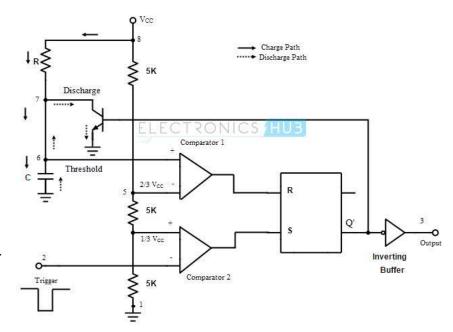
Frequency Divider, Pulse Width Modulation,

Linear Ramp Generator , Switching the Relay ON Missing Pulse Detector

#### Operation

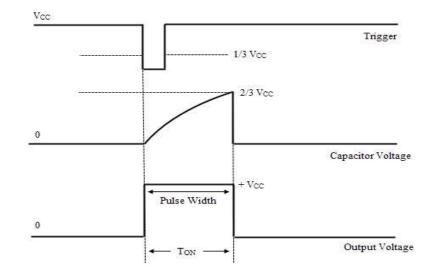
The monostable mode is also called "one-shot" pulse generator. The sequence of events starts when a negative going trigger pulse is applied to the trigger comparator. When this trigger comparator senses the short negative going trigger pulse to be just below the reference voltage (1/3 VCC), the device triggers and the output goes HIGH.

The discharge transistor is turned OFF and the capacitor C that is externally connected to its collector will start charging to the max value through the resistor R. The HIGH output pulse ends when the charge on the capacitor reaches 2/3 VCC. The internal connection of the IC 555 in monostable mode along with the RC timing circuit is shown below.



The detailed operation can be explained as follows. Initially, the flip-flop is RESET. This will allow the discharge transistor to go to saturation. The capacitor C, which is connected to the open collector (drain in case of CMOS) of the transistor, is provided with a discharge path. Hence the capacitor discharges completely and the voltage across it is 0. The output at pin 3 is low (0).

When a negative going trigger pulse input is applied to the trigger comparator (comparator 2), it is compared with a reference voltage of 1/3 VCC. The output remains low until the trigger input is greater than the reference voltage. The moment trigger voltage goes below 1/3 VCC, the output of comparator goes high and this will SET the flip-flop. Hence the output at pin 3 will become high. At the same time, the discharge transistor is turned OFF and the capacitor C will begin to charge and the voltage across it rises exponentially.



This is nothing but the threshold voltage at pin 6. This is given to the comparator 1 along with a reference voltage of 2/3 VCC. The output at pin 3 will remain HIGH until the voltage across the capacitor reaches 2/3 VCC.

The instance at which the threshold voltage (which is nothing but the voltage across the capacitor) becomes more than the reference voltage, the output of the comparator 1 goes high. This will RESET the flip-flop and hence the output at pin 3 will fall to low (logic 0) i.e. the output returns to its stable state. As the output is low, the discharge transistor is driven to saturation and the capacitor will completely discharge. Hence it can be noted that the output at pin 3 is low at start, when the trigger becomes less than 1/3 VCC the output at pin 3 goes high and when the threshold voltage is greater than 2/3 VCC the output becomes low until the occurrence of next trigger pulse. A rectangular pulse is produced at the output. The time for which the output stays high or the width of the rectangular pulse is controlled by the timing circuit i.e. the charging time of the capacitor which depends on the time constant RC.

### Monostable Multivibrator Design Using 555 timer IC

The capacitor C has to charge through resistance  $R_A$ . The larger the time constant  $R_A$ .C, the longer it takes for the capacitor voltage to reach +2/3VCC.

In other words, the RC time constant controls the width of the output pulse. The time during which the timer output remains high is given as

$$tp = 1.0986 R_A C$$

where R<sub>A</sub> is in ohms and C is in farads. The above relation is derived as below.

We know that the voltage across the capacitor C rises exponentially. Voltage across the capacitor at any instant during charging period is given as

$$VC = VCC (1 - e-t/RC)$$

When the capacitor voltage is 2/3 VCC,

then 
$$2/3$$
 VCC = VCC  $(1 - e-t/RC)$ 

Substituting vc = 2/3 VCC in above equation we get the time taken by the capacitor to charge from 0 to +2/3 VCC.

So 
$$+2/3$$
VCC. = VCC.  $(1 - e - t/R_AC)$ 

or 
$$t - R_A C \log 3 = 1.0986 R_A C$$

So pulse width,  $tP = 1.0986 R_AC$ 

∴ 
$$t \approx 1.1 R_AC$$

The pulse width of the circuit may range from micro-seconds to many seconds. This circuit is widely used in industry for many different timing applications.

The **Monostable 555 Timer** circuit triggers on a negative-going pulse applied to pin 2 and this trigger pulse must be much shorter than the output pulse width allowing time for the timing capacitor to charge and then discharge fully. Once triggered, the 555 Monostable will remain in this "HIGH" unstable output state until the time period set up by the R1 x C1 network has elapsed. The amount of time that the output voltage remains "HIGH" or at a logic "1" level, is given by the following time constant equation.

T = 1.1 RC

Where, t is in seconds, R is in  $\Omega$ 's and C in Farads.

# Example No1

Take time delay T = 10 Sec

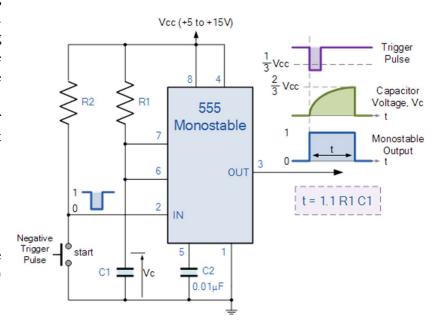
If a 100 uF timing capacitor is used, calculate the value of the resistor required to produce a minimum output time delay of 10 Sec.

 $R = 10 \text{ Sec} / 1.1 \times 100 \text{ uF} = 90.90909 \text{ k}\Omega$ 

The calculated value for the timing resistor R required to produce the required time constant of 10 Sec is therefore, 90.90909 k $\Omega$ . However, this resistor value does not exist as a standard value resistor, so we would need to select the nearest preferred value resistor of 100 k $\Omega$  which is available in all the standard ranges. Calculate exect time with 100 k and 100 uF.

If long time delays are required as above 10's of seconds, it is not always advisable to use high value timing capacitors as they can be physically large, expensive and have large value tolerances, e.g, ±20%.

One alternative solution is to use a small value timing capacitor and a much larger value resistor up to about  $1M\Omega$ 's to produce the require time delay.



#### **Questions:**

How is an Astable multivibrator connected into a pulse position modulator?

Explain the function of reset?

Derive the expression of time delay of a monostable multivibrator

Which among the following can be used to detect the missing heart beat?

a) Monostable multivibrator, b) Astable multivibrator, c) Schmitt trigger, d) None of the mentioned

The output waveform of a 555 timer is always a) sinusoidal b) triangular c) rectangular d) square.

A multivibrator circuit having one stable state and other quasi-stable state is known as a) monostable multivibrator b) bistable multivibrator c) astable multivibrator d) free-running multivibrator.

A monostable multivibrator is also called a "one-shot multivibrator" because a) each time a trigger pulse is applied, the circuit produces a single pulse. b) the circuit has to be triggered only once c) the output pulse duration is very small.

The output of a monostable multivibrator remains high a) while the external capacitor is charging b) while the external capacitor is discharging c) while the trigger is held high d) a and c

The output of a monostable multivibrator remains low a) while the external capacitor is charging b) while the external capacitor is discharging c) while the trigger is held high d) a and c

When a 555 timer is connected in monostable mode, the voltage across the external capacitor is used for the threshold to pin 6. (True/False)

Once the circuit is triggered and the output becomes high, it remains so for the time interval tp and will not change even if an input trigger is applied during this time interval. (True / False)

Is it possible to achieve a stable state output within the time interval tp using a reset terminal? (Yes / No)

The output state of a 555 timer connected in a monostable mode with a high trigger input is a) low b) high c) either high or low d) not stable.

The pulse-width of the wave generated by a monostable multivibrator with RA =  $68 \text{ k}\Omega$  and C =  $0.1 \mu\text{F}$  is a) 3.74 ms b) 7.48 ms c)  $7.48 \mu\text{s}$  d) none of the above.

The pulse-width of the wave generated by a one-shot multivibrator decreases when the a) supply voltage decreases b) timing resistor increases c) UTP increases d) timing capacitance decreases.

For the proper functioning of a monostable multivibrator, what must be the relative magnitude of the pulse-width of the trigger input in comparison to the expected pulse-width of the output waveform? a) It must be smaller b) It must be larger c) It must be the same d) It can have any magnitude.

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The trigger input may be a) driven by the output of a stable multivibrator with high Duty Cycle. b) supplied manually by grounding the trigger input for a fraction of a second. c) both a and b d) only a.

Once the output of the monostable multivibrator has switched to the stable low state, it remains low until a trigger pulse is again applied. (True / False)

What is the time of a monostable timer for which the output remains high?