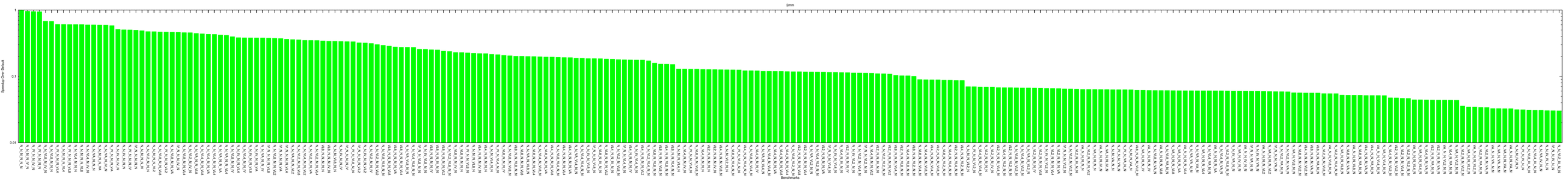
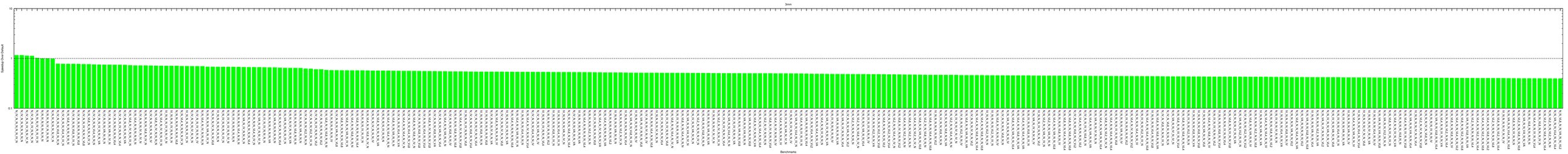
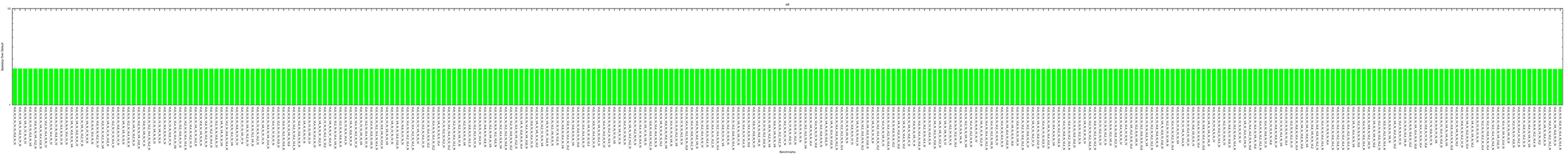
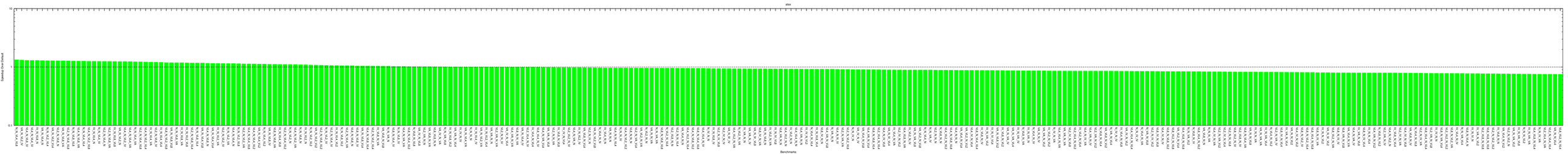
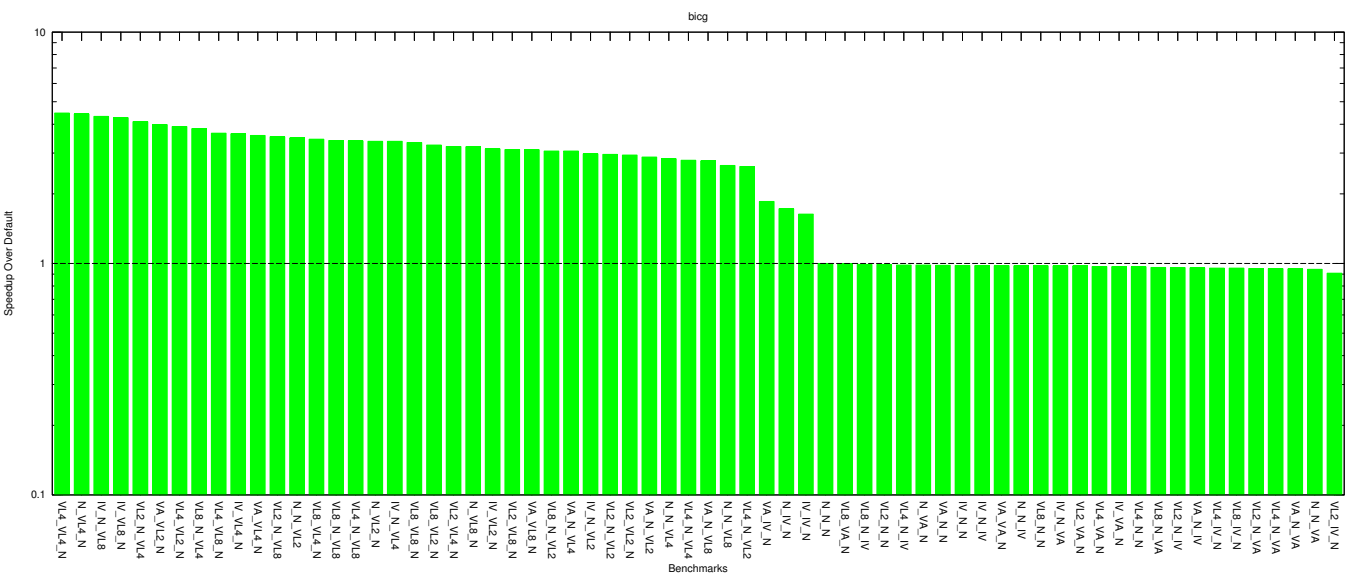
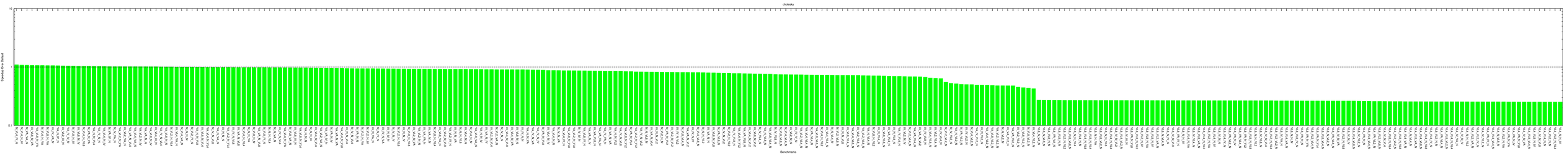

2mm
Speedup Over Default
1
0.1
0.01
Benchmarks

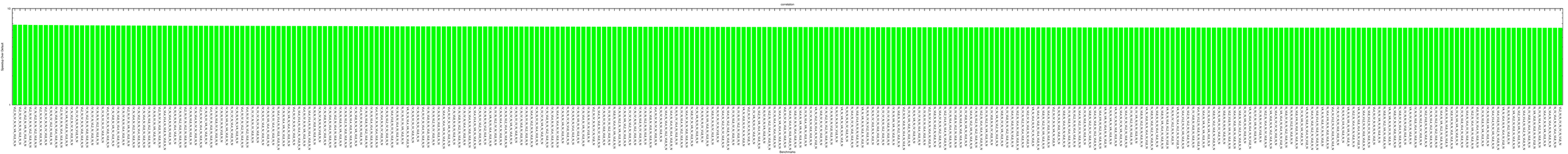

3mm
Speedup Over Default
1.0
0.5
0.0
Benchmarks

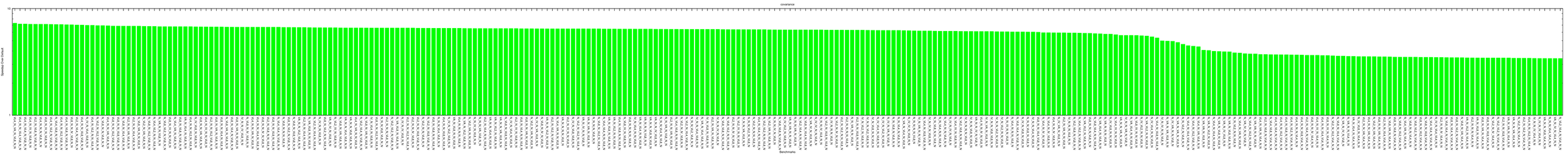

adi
Speedup Over Default
1.0
0.0
Benchmarks

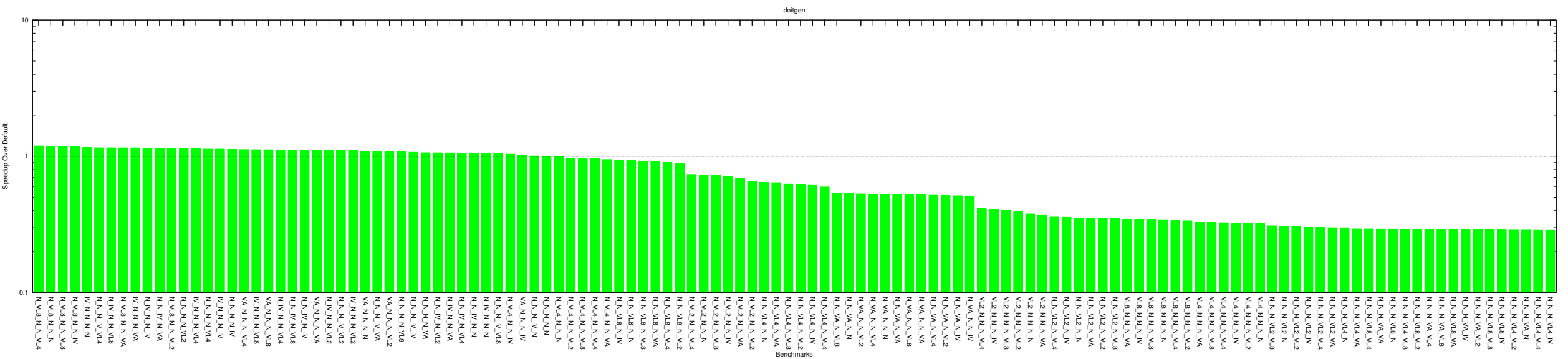

jstax
Speedup Over Default
Benchmarks

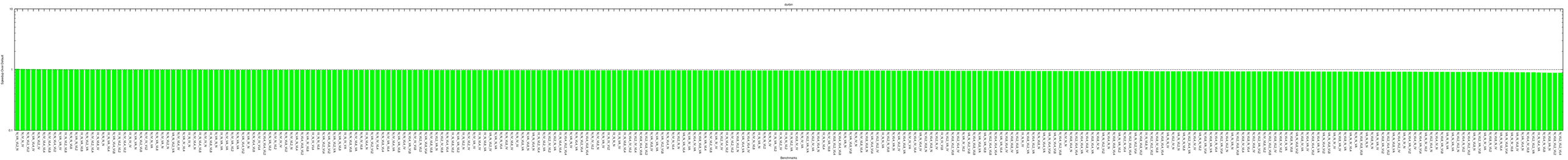

bicg
Speedup Over Default
10
1
0.1
Benchmarks
VL4_VL4_N
N_VL4_N
IV_N_VL8
IV_VL8_N
VL2_VL4
VA_VL2_N
VL4_VL2_N
VL8_N_VL4
VL4_VL8_N
IV_VL4_N
VA_VL4_N
VL2_N_VL8
N_N_VL2
VL8_VL4_N
VL8_N_VL8
VL4_N_VL8
N_VL2_N
IV_N_VL4
VL8_VL8_N
VL8_VL2_N
VL2_VL4_N
N_VL8_N
IV_VL2_N
VL2_VL8_N
VA_VL8_N
VL8_N_VL2
VA_N_VL4
IV_N_VL2
VL2_N_VL2
VL2_VL2_N
VA_N_VL2
N_N_VL4
VL4_N_VL4
VA_N_VL8
N_N_VL8
VL4_N_VL2
VA_IV_N
N_IV_N
IV_IV_N
N_N_N
VL8_VA_N
VL8_N_IV
VL2_N_N
VL4_N_IV
N_VA_N
VA_N_N
IV_N_N
IV_N_IV
VA_VA_N
N_N_IV
VL8_N_N
IV_N_VA
VL2_VA_N
VL4_VA_N
IV_VA_N
VL4_N_N
VL8_N_VA
VL2_N_IV
VA_N_IV
VL4_IV_N
VL8_IV_N
VL2_N_VA
VL4_N_VA
VA_N_VA
N_N_VA
VL2_IV_N

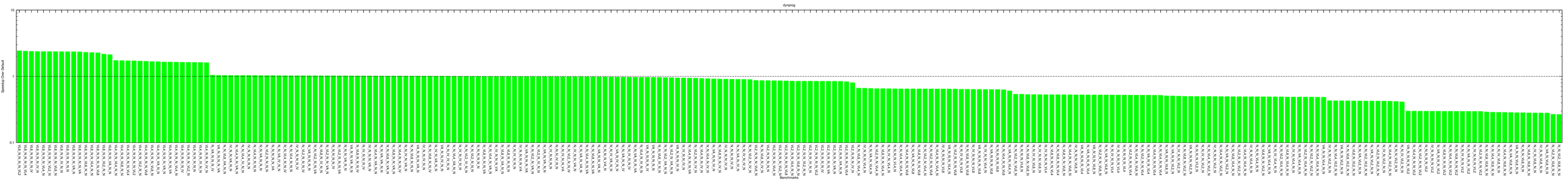

cholesky
Speedup Over Default
Benchmarks

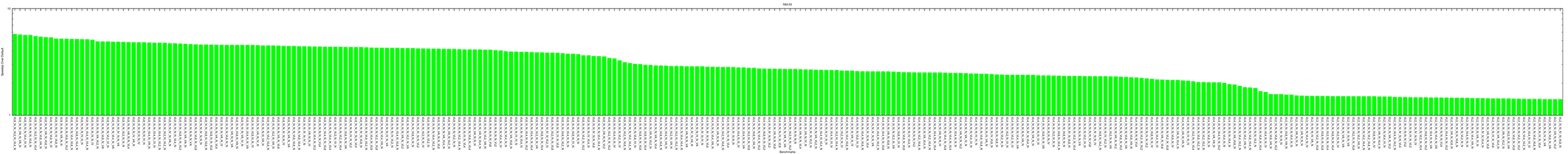

correlation
Speedup Over Default
1.0
Benchmarks

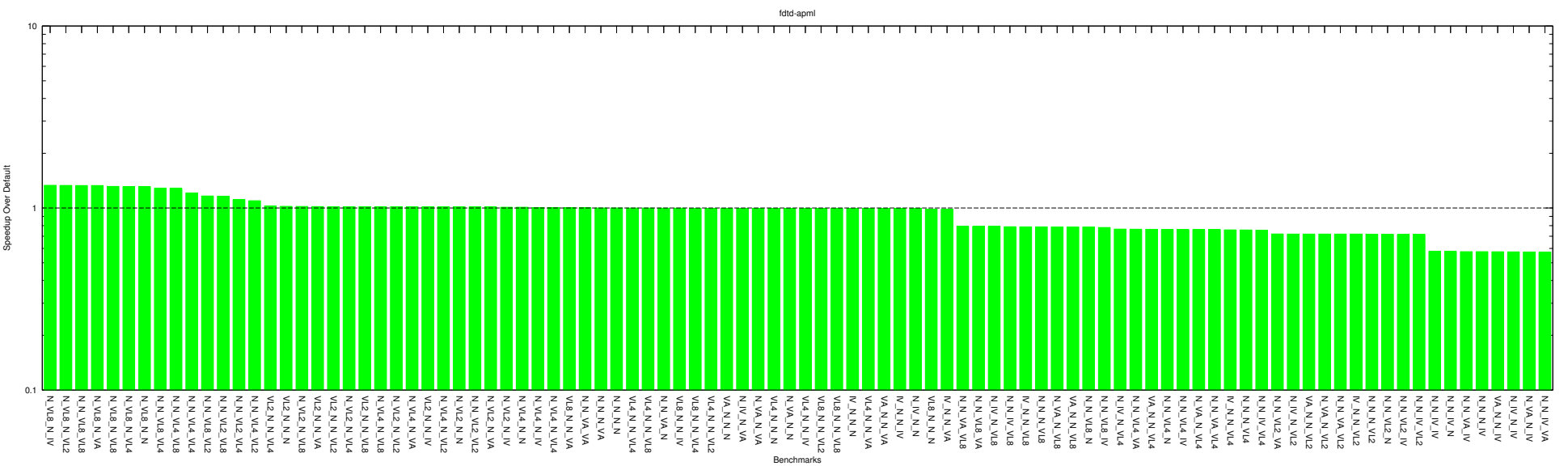

covariance
Speedup Over Default
1.0
0.0
Benchmarks

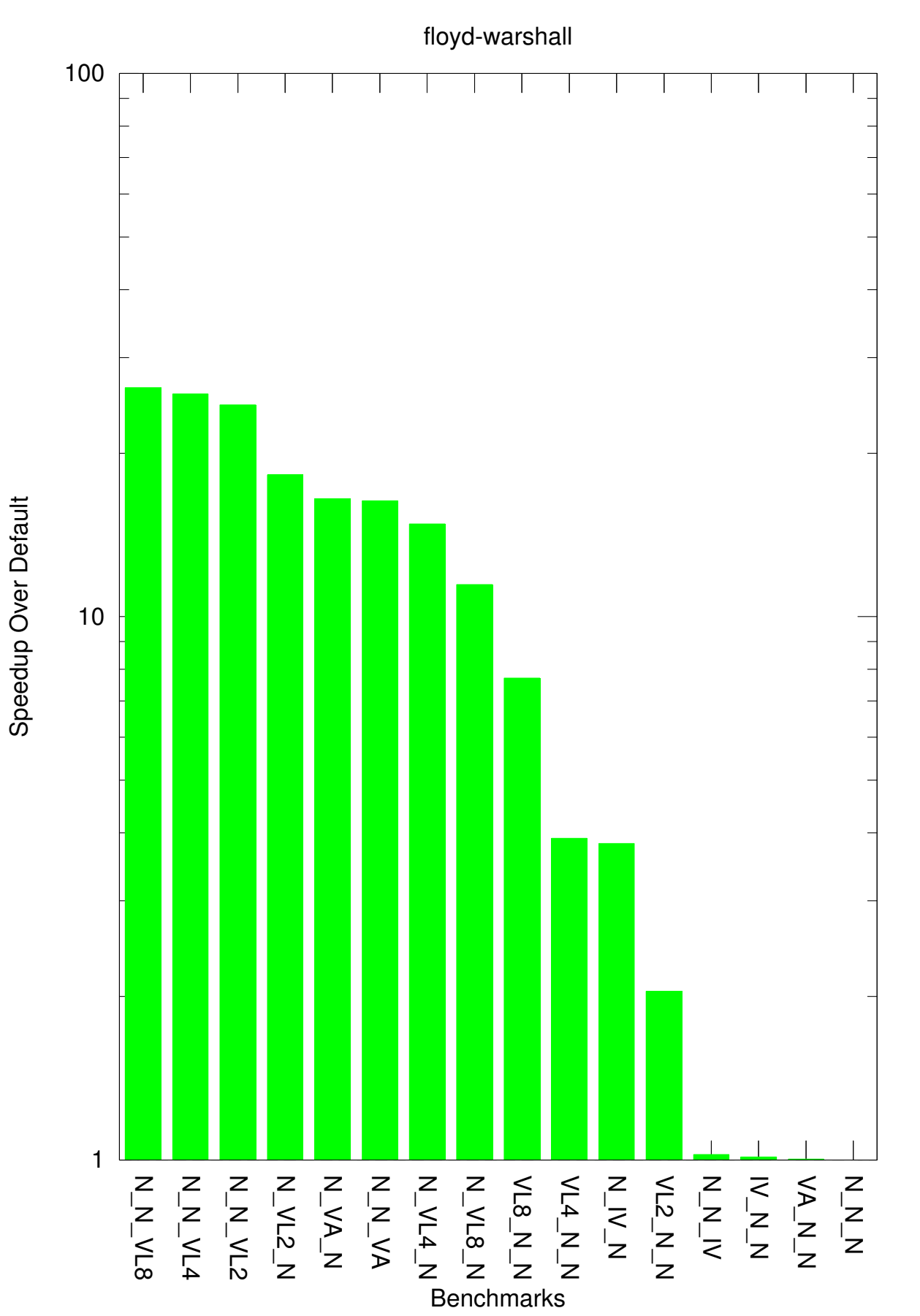

doitgen
Speedup Over Default
10
1
0.1
Benchmarks
N_VL8_N_N_VL4
N_VL8_N_N_N
N_VL8_N_N_VL8
N_VL8_N_N_IV
IV_N_N_N_N
N_N_N_IV_VL4
N_IV_N_N_VL8
N_VL8_N_N_VA
IV_N_N_N_VA
N_IV_N_N_IV
N_N_IV_N_VA
N_VL8_N_N_VL2
N_N_N_N_VL2
IV_N_N_N_VL4
N_N_N_N_IV
N_N_N_N_IV
VA_N_N_N_VL4
IV_N_N_N_VL8
VA_N_N_N_VL8
N_IV_N_N_VL4
N_N_IV_N_VL8
N_N_IV_N_IV
VA_N_N_N_VA
N_IV_N_N_VL2
N_N_N_IV_VL2
IV_N_N_N_VL2
VA_N_N_N_N
N_N_N_IV_VA
VA_N_N_N_VL2
N_N_N_N_VL8
N_N_N_IV_N
N_N_N_IV_IV
N_N_N_N_VA
N_N_N_IV_VL2
N_N_N_N_VL4
IV_N_N_N_VA
N_N_IV_N_VL4
N_N_N_N_IV
VA_N_N_N_IV
N_N_N_IV_VL8
N_N_N_IV_N
N_N_N_N_N
N_VL4_N_N_VL8
N_VL4_N_N_VL4
N_VL4_N_N_VA
N_N_VL8_N_IV
N_N_VL8_N_N
N_N_VL8_N_VA
N_N_VL8_N_VL4
N_N_VL8_N_VL2
N_VL2_N_N_VL4
N_VL2_N_N_N
N_VL2_N_N_VL8
N_VL2_N_N_IV
N_VL2_N_N_VA
N_VL2_N_N_VL2
N_VL2_N_N_VL4
N_VA_N_N_VL4
N_VA_N_N_N
N_VA_N_N_VL2
N_VA_N_N_IV
N_VA_N_N_VL8
N_VA_N_N_VA
N_VA_N_N_VL4
N_N_VA_N_VL2
N_N_VA_N_IV
N_VA_N_N_IV
VL2_N_N_N_VL4
VL2_N_N_N_IV
VL2_N_N_N_VL8
VL2_N_N_N_VL2
VL2_N_N_N_N
VL2_N_N_N_VA
N_N_VL2_N_IV
N_N_VL2_N_N
N_N_VL2_N_VA
N_N_VL2_N_VL2
N_N_VL2_N_VL8
VL8_N_N_N_VA
VL8_N_N_N_IV
VL8_N_N_N_VL8
VL8_N_N_N_N
VL8_N_N_N_VL4
VL8_N_N_N_VL2
VL4_N_N_N_VA
VL4_N_N_N_VL8
VL4_N_N_N_IV
VL4_N_N_N_VL2
VL4_N_N_N_N
N_N_N_VL2_N
N_N_N_VL2_VL2
N_N_N_VL2_IV
N_N_N_VL2_VL4
N_N_N_VL2_VA
N_N_N_VL4_N
N_N_N_VL4_VA
N_N_N_VL8_VL4
N_N_N_VA_VA
N_N_N_VL8_N
N_N_N_VL4_VL8
N_N_N_VL8_VL2
N_N_N_VA_VL4
N_N_N_VL8_IV
N_N_N_VA_IV
N_N_N_VL4_VL4
N_N_N_VL4_IV

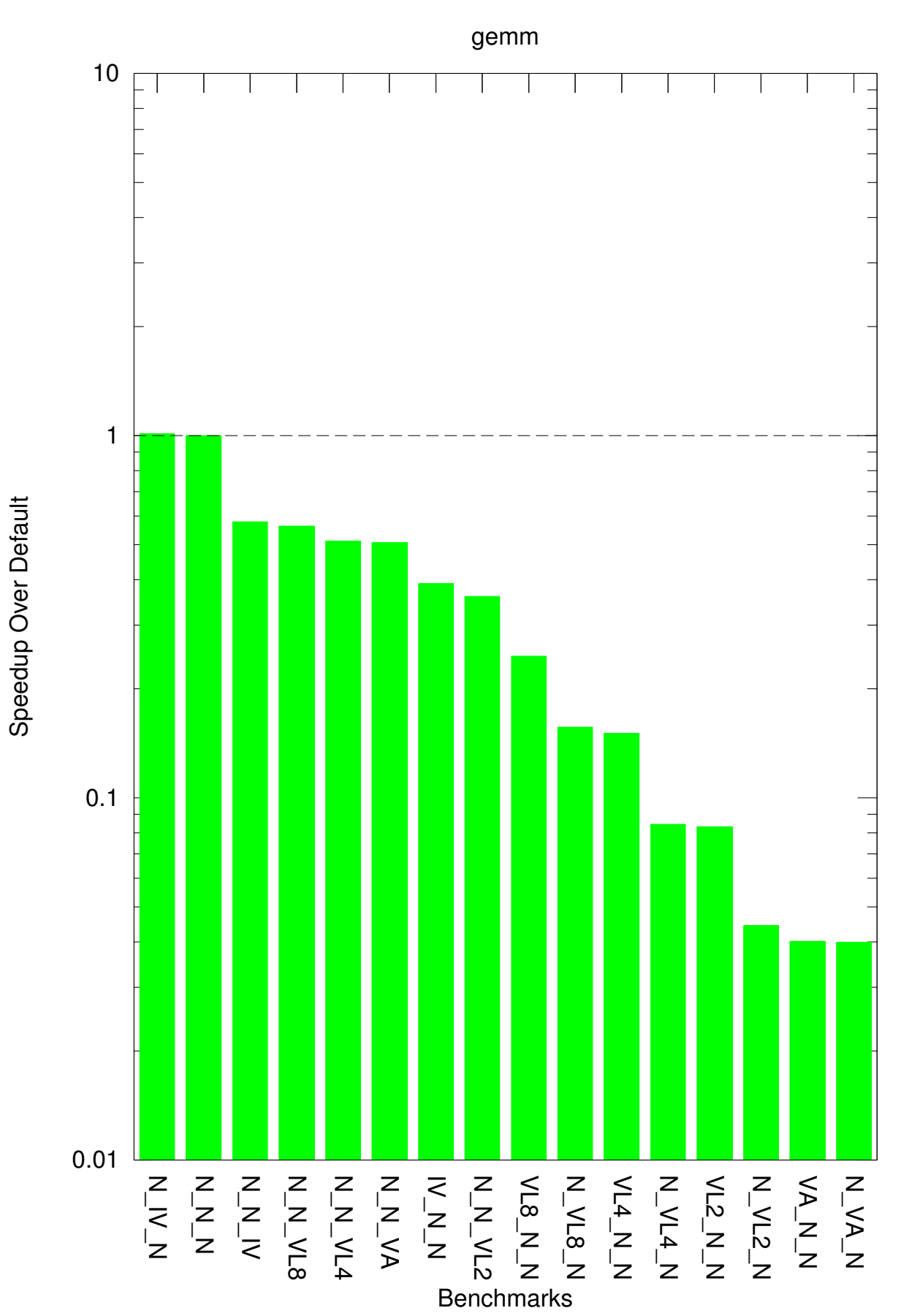

durbin
Speedup Over Default
Benchmarks
2
1
0.5

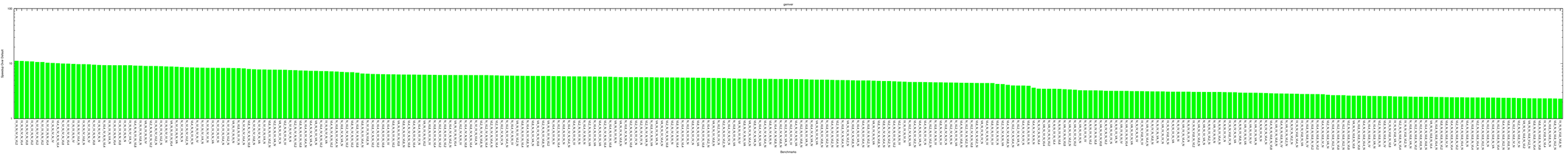

dynprog
Speedup Over Default
10
1
0.1
Benchmarks

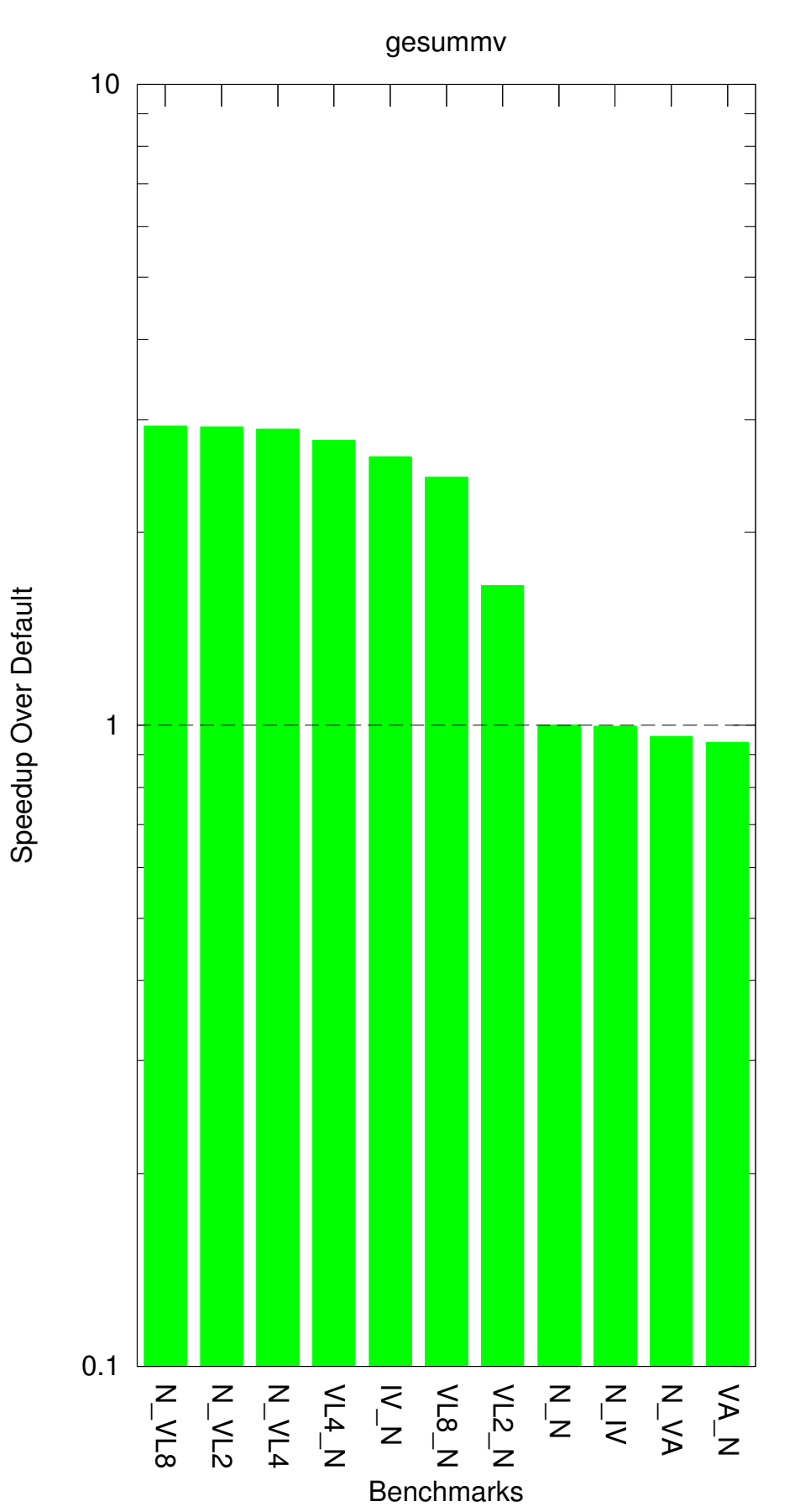

fdtd-2d
Speedup Over Default
1.2
1
Benchmarks

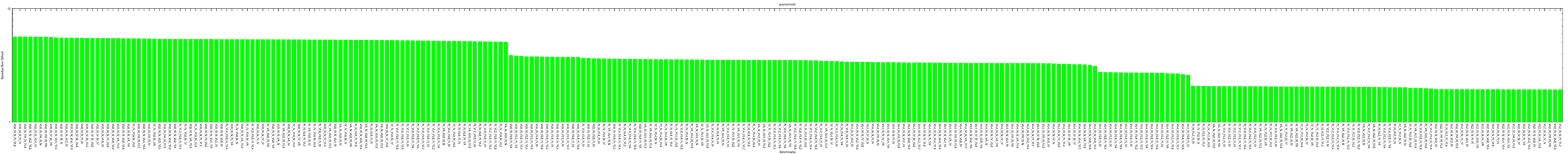

fdtd-apml
Speedup Over Default
10
1
0.1
Benchmarks
N_VL8_N_IV
N_VL8_N_VL2
N_N_VL8_VL8
N_N_VL8_N_VA
N_VL8_N_VL8
N_VL8_N_VL4
N_VL8_N_N
N_N_VL8_VL4
N_N_VL4_VL8
N_N_VL4_VL4
N_N_VL8_VL2
N_N_VL2_VL8
N_N_VL2_VL4
N_N_VL4_VL2
VL2_N_N_VL4
VL2_N_N_N
N_VL2_N_VL8
VL2_N_N_VA
VL2_N_N_VL2
N_VL2_N_VL4
VL2_N_N_VL8
N_VL4_N_VL8
N_N_VL2_VL2
N_VL4_N_VA
VL2_N_N_IV
N_VL2_N_VL2
N_VL4_N_VL2
N_VL2_N_N
N_N_VL2_VL2
N_VL2_N_VA
N_VL2_N_IV
N_VL4_N_N
N_VL4_N_IV
N_VL4_N_VL4
VL8_N_N_VA
N_N_N_N
N_N_N_VA
VL4_N_N_VA
N_N_N_VA
VL4_N_N_VL4
VL4_N_N_VL8
N_N_VA_N
VL8_N_N_IV
VL8_N_N_VL4
VL4_N_N_VL2
VA_N_N_N
N_IV_N_VA
N_VA_N_VA
VL4_N_N_N
N_VA_N_N
VL4_N_N_IV
VL8_N_N_VL2
VL8_N_N_VL8
IV_N_N_N
VL4_N_N_VA
VA_N_N_VA
IV_N_N_IV
N_IV_N_N
IV_N_N_VA
N_N_VA_VL8
N_N_VL8_VA
N_IV_N_VL8
N_N_IV_VL8
IV_N_N_VL8
N_N_N_VL8
N_VA_N_VL8
VA_N_N_VL8
N_N_VL8_N
N_N_VL8_IV
N_IV_N_VL4
VA_N_N_VL4
N_IV_N_VL4
N_N_N_VL4
N_N_IV_VL4
N_N_VL2_VA
N_IV_N_VL2
VA_N_N_VL2
N_N_VA_VL2
IV_N_N_VL2
N_N_VL2_N
N_N_VL2_IV
N_N_IV_VL2
N_N_IV_IV
N_N_IV_N
N_N_VA_IV
VA_N_N_IV
N_N_N_IV
N_IV_N_IV
N_VA_N_IV
N_IV_N_VA

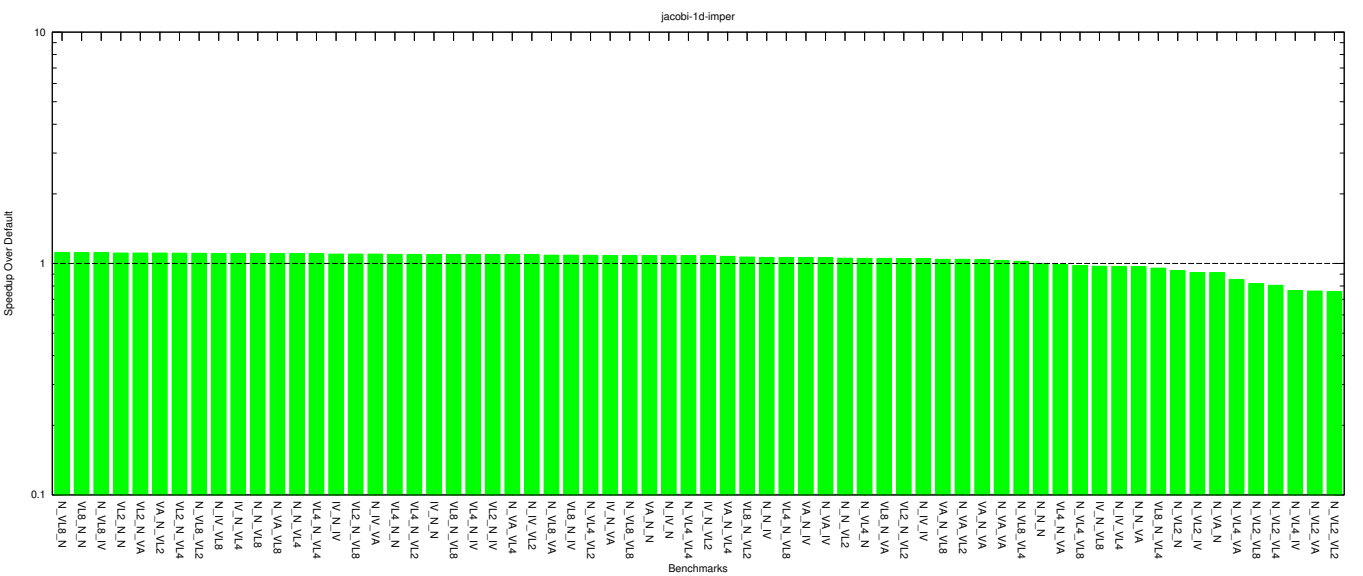

floyd-warshall
100
10
1
Speedup Over Default
N_N_VL8
N_N_VL4
N_N_VL2
N_VL2_N
N_VA_N
N_N_VA
N_VL4_N
N_VL8_N
VL8_N_N
VL4_N_N
N_IV_N
VL2_N_N
N_N_IV
IV_N_N
VA_N_N
N_N_N
Benchmarks

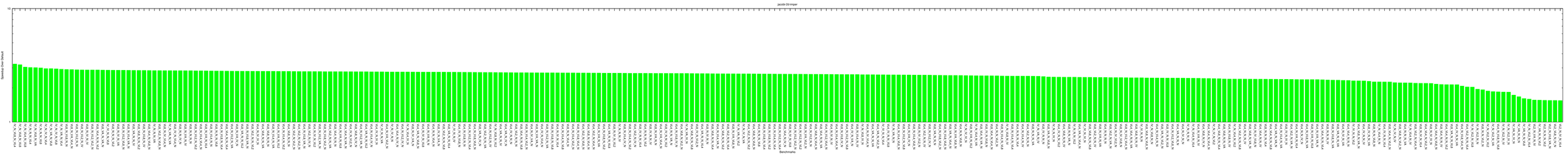

gemm
10
1
0.1
0.01
Speedup Over Default
N_IV_N
N_N_N
N_N_IV
N_N_VL8
N_N_VL4
N_N_VA
IV_N_N
N_N_VL2
VL8_N_N
N_VL8_N
VL4_N_N
N_VL4_N
VL2_N_N
N_VL2_N
VA_N_N
N_VA_N
Benchmarks

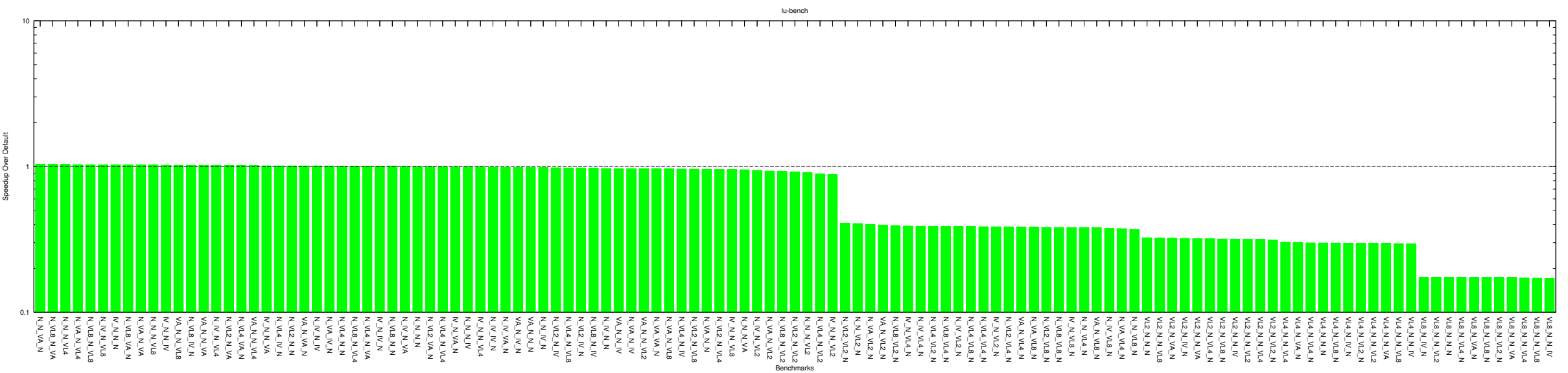

gemver
Speedup Over Default
100
0
-
Benchmarks


gesummv
10
1
0.1
Speedup Over Default
N_VL8
N_VL2
N_VL4
VL4_N
IV_N
VL8_N
VL2_N
N_N
N_IV
N_VA
VA_N
Benchmarks


gramschmidt
Speedup Over Default
1.0
Benchmarks


jacobi-1d-imper
Speedup Over Default
10
1
0.1
Benchmarks
N_VL8_N
VL8_N_N
N_VL8_IV
N_VL8_VA
VL2_N_N
VL2_N_VA
VA_N_VL2
VL2_N_VL4
N_VL8_VL2
N_IV_VL8
IV_N_VL4
N_N_VL8
N_VA_VL8
N_N_VL4
VL4_N_VL4
IV_N_IV
VL2_N_VL8
N_IV_VA
VL4_N_N
VL4_N_VL2
IV_N_N
VL8_N_VL8
VL4_N_IV
VL2_N_IV
N_VA_VL4
N_IV_VL2
N_VL8_VA
VL8_N_IV
N_VL4_VL2
IV_N_VA
N_VL8_VL8
VA_N_N
N_IV_N
N_VL4_VL4
IV_N_VL2
VA_N_VL4
VL8_N_VL2
N_N_IV
VL4_N_VL8
VA_N_IV
N_VA_IV
N_N_VL2
N_VL4_N
VL8_N_VA
VL2_N_VL2
N_IV_IV
VA_N_VL8
N_VA_VL2
VA_N_VA
N_VA_VA
N_VL8_VL4
N_N_N
VL4_N_VA
N_VL4_VL8
IV_N_VL8
N_IV_VL4
N_N_VA
VL8_N_VL4
N_VL2_N
N_VL2_IV
N_VA_N
N_VL4_VA
N_VL2_VL8
N_VL2_VL4
N_VL4_IV
N_VL2_VA
N_VL2_VL2


jacobi-2d-imper
Speedup Over Default
Benchmarks
1.0
0.0


lu-bench
Speedup Over Default
10
1
0.1
Benchmarks
N_N_VA_N
N_VL8_N_VA
N_N_N_VL4
N_VA_N_VL4
N_VL8_N_VL8
N_IV_N_VL8
IV_N_N_N
N_VL8_VA_N
N_VA_N_VA
N_N_N_VL8
IV_N_N_IV
VA_N_N_VL8
N_VL8_IV_N
VA_N_N_VA
N_IV_N_VL4
N_VL2_N_VA
N_VL4_VA_N
VA_N_N_VL4
IV_N_N_VA
N_VL2_N_N
N_VL4_IV_N
VA_N_VA_N
N_IV_N_IV
N_VL8_N_N
N_N_N_N
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VA_N_N_IV
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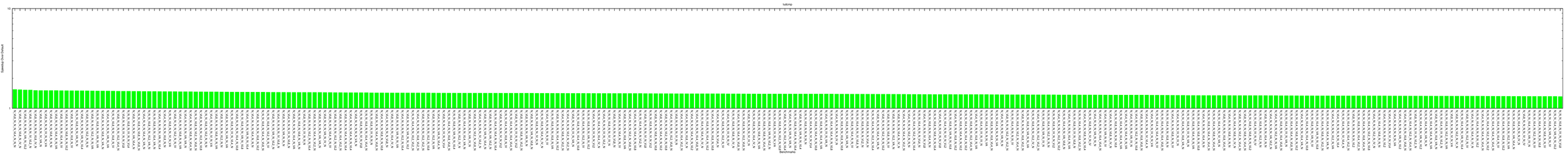
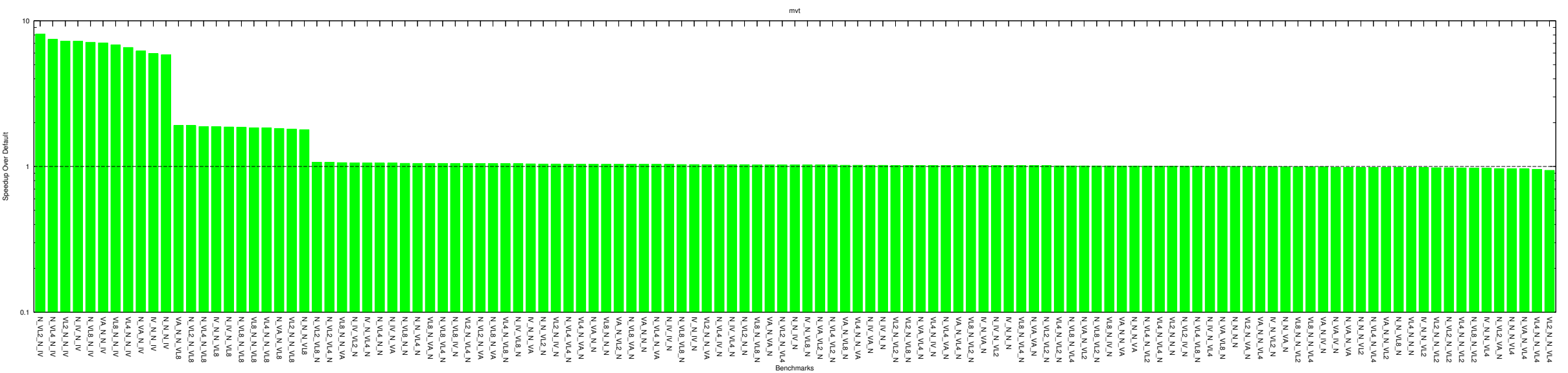
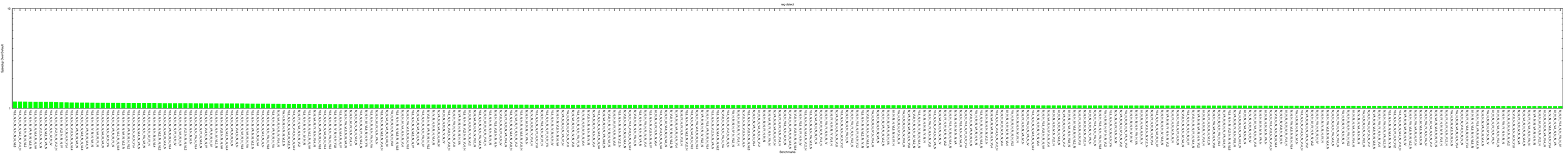
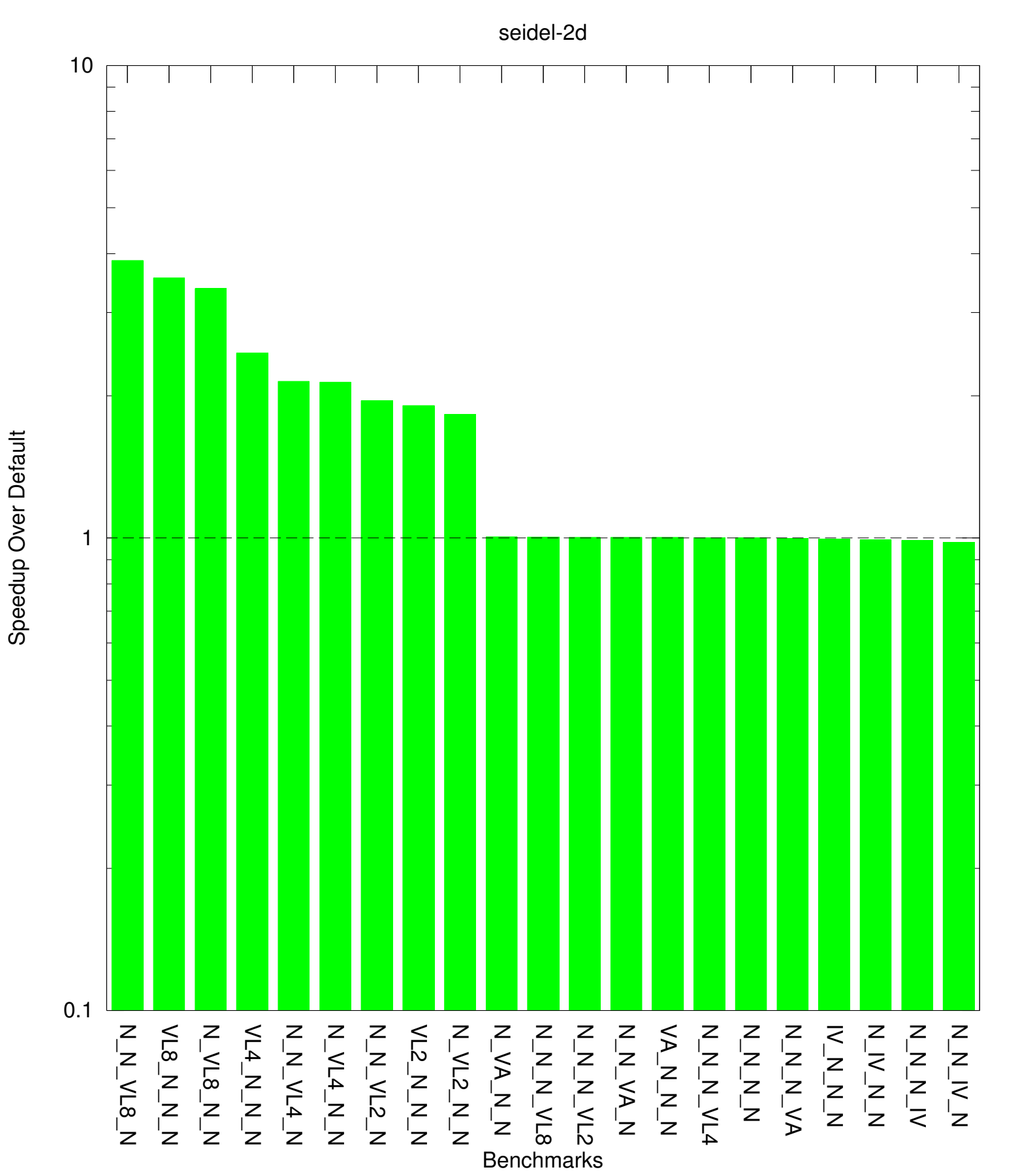
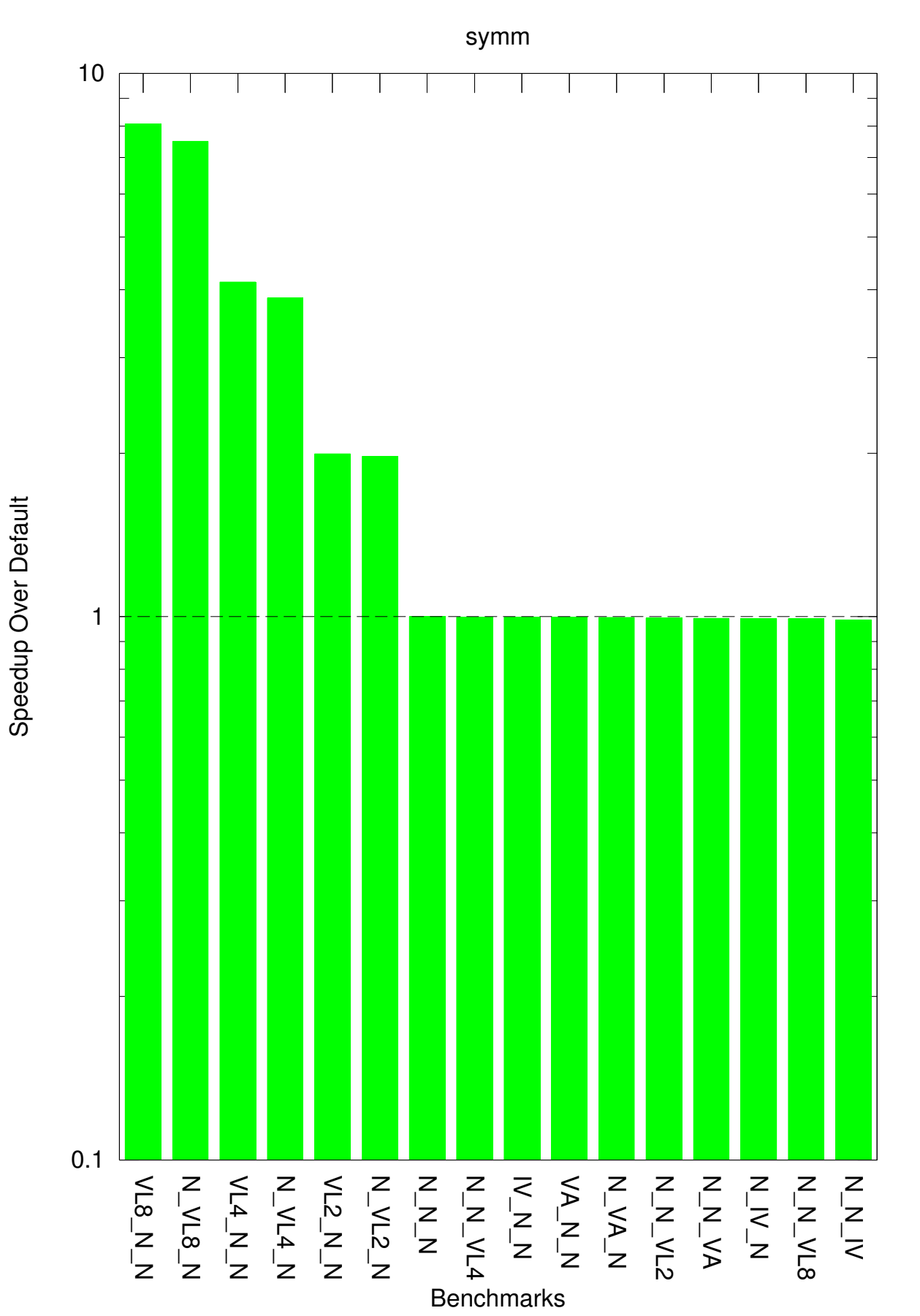
N_IV_N_N
VA_N_N_IV
N_VL4_N_N
N_VL8_N_IV
N_VL4_N_VL8
N_VL2_N_VL8
N_VA_N_N
N_VL2_N_VL4
N_IV_N_VL8
N_IV_N_VL2
N_N_N_VA
N_VA_N_VL2
N_VL8_N_VL2
N_IV_N_VL4
N_IV_VL4_N
N_VL8_VL4_N
N_IV_VL2_N
N_VL4_VL8_N
N_VL4_VL2_N
IV_N_N_VL2
N_VL2_VL2_N
N_N_VL2_N
N_VA_VL2_N
VA_N_VL2_N
N_VL8_VL2_N
N_VL4_VL2_N
IV_N_VL2_N
N_VL2_VL4_N
VA_N_VL4_N
N_VA_VL8_N
N_VL2_VL8_N
N_VL8_VL8_N
IV_N_VL8_N
N_N_VL4_N
VA_N_VL8_N
N_IV_VL8_N
N_VA_VL4_N
N_N_VL8_N
VL2_N_N_N
VL2_N_VA_N
VL2_N_VL8_N
VL2_N_IV_N
VL2_N_VA_N
VL2_N_VL4_N
VL2_N_N_IV
VL2_N_VL8_N
VL2_N_N_VL2
VL2_N_N_VL4
VL4_N_VL2_N
VL4_N_N_VA
VL4_N_N_VL8
VL4_N_N_IV
VL4_N_N_VL2
VL4_N_N_VL4
VL4_N_N_VL8
VL4_N_N_IV
VL8_N_IV_N
VL8_N_N_VL2
VL8_N_N_N
VL8_N_VL4_N
VL8_N_VA_N
VL8_N_VL8_N
VL8_N_VL2_N
VL8_N_N_VA
VL8_N_VL4_N
VL8_N_N_VL8
VL8_N_N_IV

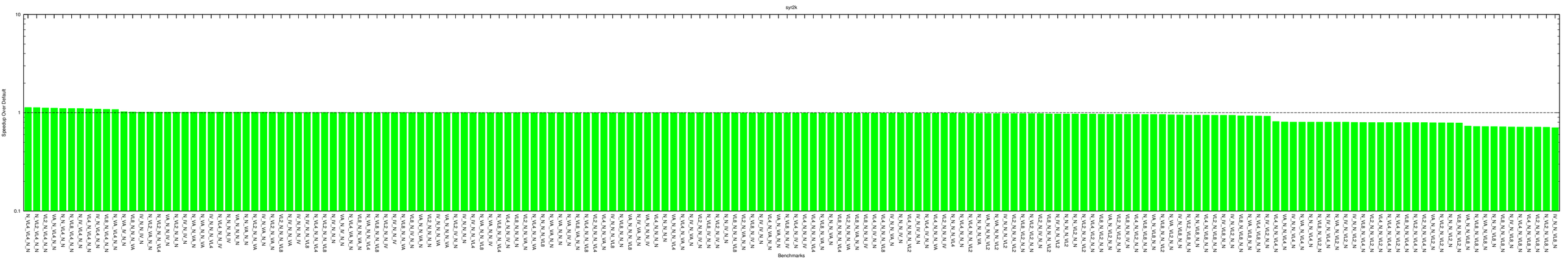

fuzzcmp
Speedup Over Default
1.0
0.0
Benchmarks

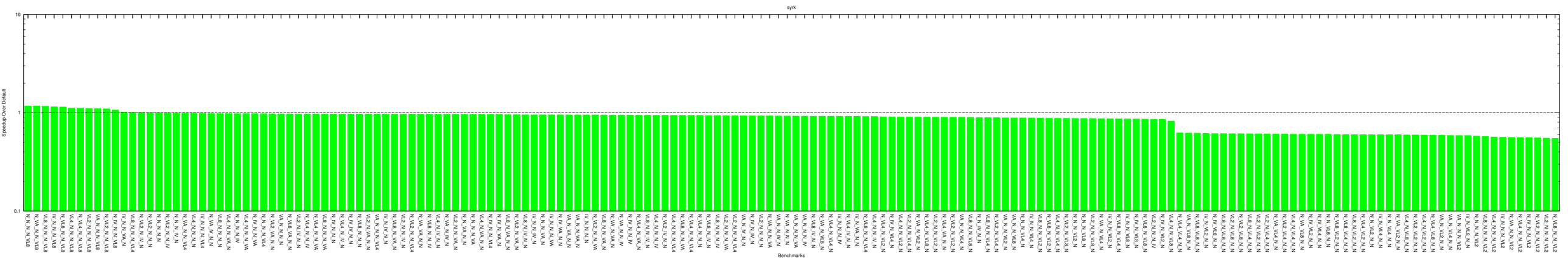

mvt
Speedup Over Default
10
1
0.1
Benchmarks
N_VL2_N_IV
N_VL4_N_IV
VL2_N_N_IV
N_IV_N_IV
N_VL8_N_IV
VA_N_N_IV
VL8_N_N_IV
VL4_N_N_IV
N_VA_N_IV
N_N_N_IV
N_N_N_IV
VA_N_N_VL8
N_VL2_N_VL8
N_VL4_N_VL8
N_N_N_VL8
N_IV_N_VL8
N_VL8_N_VL8
VL8_N_N_VL8
VL4_N_N_VL8
VL2_N_N_VL8
N_VA_N_VL8
N_N_N_VL8
N_VL2_VL4_N
N_VL2_VL8_N
VL8_N_N_VA
N_IV_VL2_N
IV_N_VL4_N
N_VL4_N_N
N_IV_N_VA
N_VL8_N_N
N_N_VL4_N
N_VL8_N_VA
N_VL8_VL4_N
N_VL8_IV_N
VL2_N_VL4_N
N_VL2_N_VA
N_VL8_N_VA
VL4_N_VL8_N
N_IV_VL8_N
IV_N_N_VA
N_N_VL2_N
VL4_N_VA_N
N_VL4_VL4_N
VL4_N_VA_N
N_VA_N_N
VL8_N_N_N
VA_N_VL2_N
N_VL8_VA_N
VA_N_N_N
N_VL4_N_VA
N_IV_N_N
N_VL8_VL8_N
IV_N_IV_N
VL2_N_N_VA
N_VL4_IV_N
N_IV_VL4_N
N_VL2_N_N
VL8_N_VL8_N
VA_N_VA_N
N_VL2_N_VL4
N_IV_N_VL8_N
IV_N_VL8_N
N_VL4_VA_N
N_VA_N_VL4_N
VL8_N_VL2_N
N_VL4_VL2_N
N_IV_N_VA_N
IV_N_N_N
N_VA_VA_N
N_VL2_VL2_N
VL4_N_VL2_N
N_VA_N_VL2
VL8_N_VL4_N
N_VL8_N_VL2_N
VL8_N_IV_N
VA_N_N_VA
N_N_N_VA
N_VL4_N_VL2
VL4_N_VL4_N
VL2_N_N_N
N_VL2_IV_N
N_VL4_VL8_N
N_IV_N_VL4
N_VA_VL8_N
N_N_N_N
VL2_N_VA_N
VA_N_N_VL2
N_VL8_N_VL2
N_VA_N_VL4
VL8_N_VL4_N
VA_N_IV_N
N_VA_IV_N
N_VA_N_VA
N_N_N_VL2
VA_N_N_VL2
N_VL4_N_N
N_N_VL8_N
VL4_N_N_N
N_IV_N_VL2
VL2_N_N_VL2
N_N_N_VL4
N_VA_N_VL4
N_N_VA_N
N_VA_N_VL4
VL4_N_N_VL4
VL2_N_N_VL4

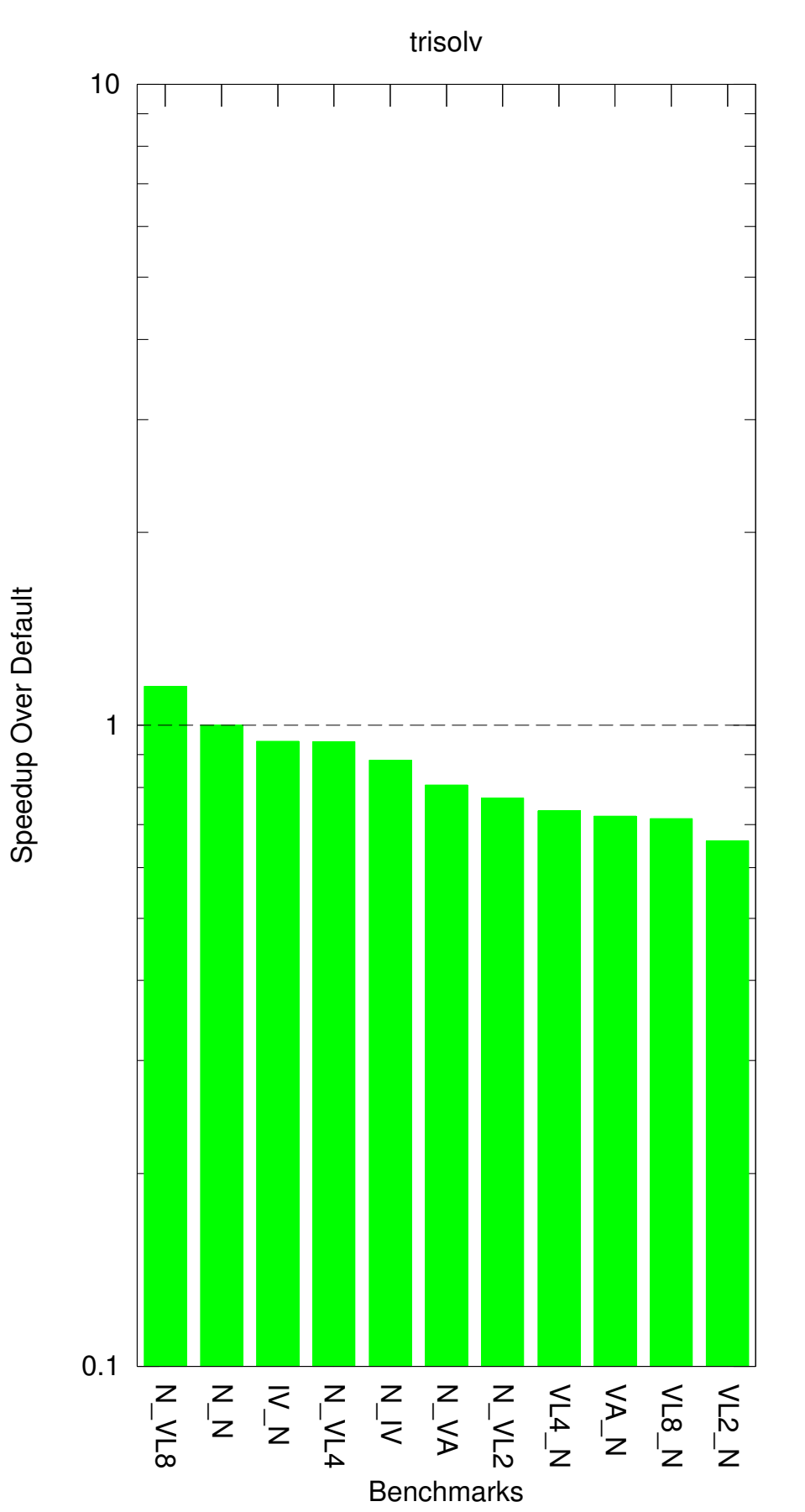

reg-detect
Speedup Over Default
Benchmarks
1.0
1

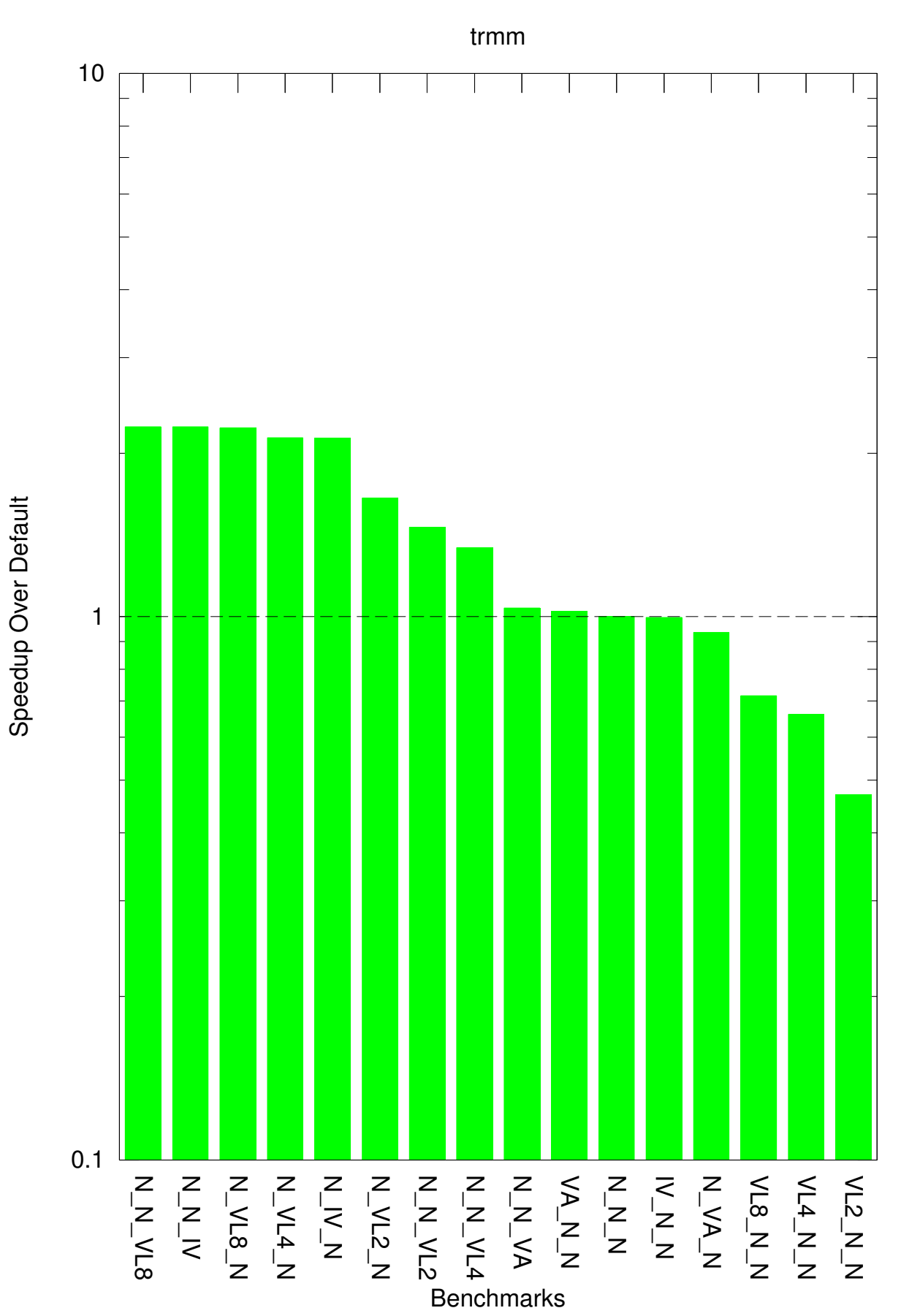

seidel-2d
10
1
0.1
Speedup Over Default
N_N_VL8_N
VL8_N_N_N
N_VL8_N_N
VL4_N_N_N
N_N_VL4_N
N_VL4_N_N
N_N_VL2_N
VL2_N_N_N
N_VL2_N_N
N_VA_N_N
N_N_N_VL8
N_N_N_VL2
N_N_N_VA_N
VA_N_N_N
N_N_N_VL4
N_N_N_N
N_N_N_VA
IV_N_N_N
N_IV_N_N
N_N_N_IV
N_N_IV_N
Benchmarks


symm
10
1
0.1
Speedup Over Default
VL8_N_N
N_VL8_N
VL4_N_N
N_VL4_N
VL2_N_N
N_VL2_N
N_N_N
N_N_VL4
IV_N_N
VA_N_N
N_VA_N
N_N_VL2
N_N_VA
N_IV_N
N_N_VL8
N_N_IV
Benchmarks


syr2k
Speedup Over Default
10
1
0.1
Benchmarks


syrk
Speedup Over Default
10
1
0.1
Benchmarks


trisolv
10
1
0.1
Speedup Over Default
N_VL8
N_N
IV_N
N_VL4
N_IV
N_VA
N_VL2
VL4_N
VA_N
VL8_N
VL2_N
Benchmarks


trmm
10
1
0.1
Speedup Over Default
N_N_VL8
N_N_IV
N_VL8_N
N_VL4_N
N_IV_N
N_VL2_N
N_N_VL2
N_N_VL4
N_N_VA
VA_N_N
N_N_N
IV_N_N
N_VA_N
VL8_N_N
VL4_N_N
VL2_N_N
Benchmarks