

# Software Design Document for the **Core Flight System SP0-VxWorks6.9 Platform Support Package – Version 1.5.1.0**

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Engineering Directorate  
Software, Robotics and Simulation Division

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National Aeronautics and  
Space Administration  
**Lyndon B. Johnson Space Center**  
Houston, Texas

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# Software Design Document for the **Core Flight System SP0-VxWorks6.9 Platform Support Package** **Version 1.5.1.0**

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**National Aeronautics and Space Administration**  
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## Change Record

<i>Revision</i>	<i>Date</i>	<i>Originator</i>	<i>Description</i>
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## 1 INTRODUCTION

The Software Design Document (SDD) details the Computer Software Units (CSUs), including their identities, attributes, static relationships, dynamic interactions and design requirements. The SDD includes enough structural and behavioral information sufficient to (1) specify the internal and external behavior of the primitive software components, and (2) be translated straightforwardly into the chosen programming language(s). The SDD includes information sufficient to enable sustaining engineering of the software by programmers other than the original developers. This includes the software structure, module definitions and functionality, high-level interface descriptions, threads of control, major data structures, and important algorithms.

This SDD defines the requirements and design of the software for the Core Flight System SP0-VxWorks6.9 Platform Support Package.

### 1.1 Scope

This Software Design Document (SDD) documents the requirements and design of the Core Flight System SP0-VxWorks6.9 Platform Support Package. This document includes the selected design of the software, including its decomposition into software components, their relationships, and the design of interfaces.

### 1.2 Responsibility and Change Authority

This document is prepared in accordance with EA-WI-025, “GFE Flight Project Software and Firmware Development”. The responsibility for the development of this document lies with the Spacecraft Software Engineering Branch. Change authority is the Software, Robotics and Simulation Division of the Johnson Space Center.

## 2 RELATED DOCUMENTATION

The following documents are referenced in this specification. Unless otherwise specified, the exact issue shown is the applicable version.

### 2.1 Applicable Documents

The following documents, of the exact issue and revision shown, form a part of this SDD to the extent specified herein.

**Table 2-1: Applicable Documents**

<i>Document Number</i>	<i>Document Title</i>	<i>Revision / Release Date</i>
NPR 7150.2	NASA Software Engineering Procedural Requirements	Rev C / Aug 2019
EA-WI-025	GFE Flight Project Software and Firmware Development	Rev D / Sep 2013
GP-10021	Core Flight Software Certification Software Development Plan	Baseline / May 2020

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## 2.2 Reference Documents

The following documents are referenced within this SDD. These documents do not form a part of this SDD and are not controlled by their reference herein.

**Table 2-2: Reference Documents**

<i>Document Number</i>	<i>Document Title</i>	<i>Revision / Release Date</i>
GSFC 582-2007-001	cFE Application Developer's Guide	Rel. 5.4 / Sep 2014
GSFC 582-2008-012	cFS Deployment Guide	Rel. 3.0 / Sep 2014
GSFC 582-2007-00	OSAL Configuration Guide	Rel. 4.2.1 / Aug 2016
TBD	SP0-VxWorks6.9 PSP Software Developer's Guide	TBD

## 2.3 Order of Precedence

In the event of a conflict between the text of this SDD and an applicable document cited herein, the text of this SDD takes precedence.

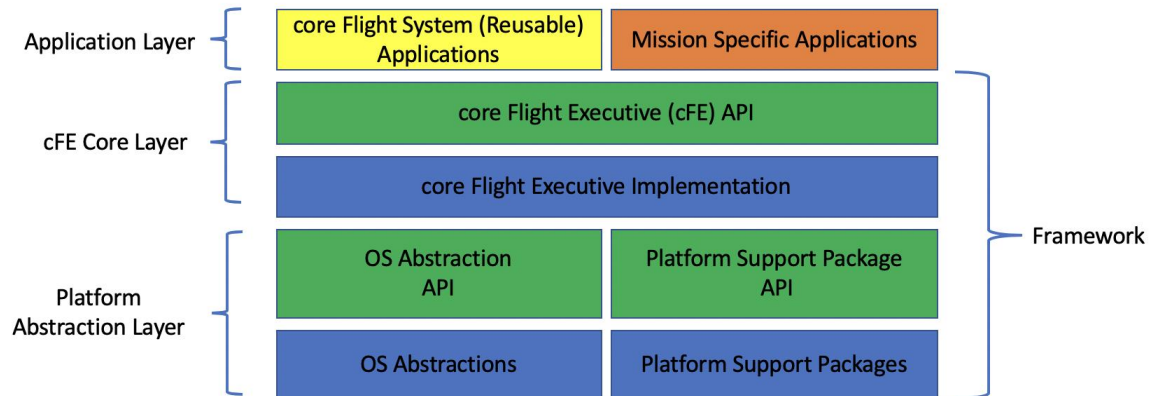
# 3 CSCI-WIDE DESIGN DECISIONS

## 3.1 Core Flight System

The Core Flight System (cFS) was developed by NASA Goddard Spaceflight Center (GSFC) as a reusable and extendible framework for developing flight software. The cFS framework has been developed over many years and was first used by NASA on the Lunar Reconnaissance Orbiter (LRO) spacecraft mission in 2009. Since then it has been successfully reused for other spacecraft missions, and its reuse has substantially increased across other NASA centers. A key feature of this framework is a layered software architecture proven to be robust and resilient in adapting to new hardware platforms with minimal changes. The cFS framework is composed of software abstraction layers from the underlying hardware and operating system as shown in Figure 3-1. Each layer provides a set of Application Programming Interfaces (APIs) that hides the underlying implementation for various platforms; and the implementation can be changed independently, without affecting the other layers.

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**Figure 3-1: Core Flight System Architectural Layers**

### 3.2 VxWorks6.9/SP0-S Platform Support Package

The Platform Support Package (PSP) is the abstraction layer of the processor's Board Support Package (BSP). A PSP provides a common set of Application Programming Interfaces (APIs) that can be used by the cFE, the OSAL and any cFS application/library.

The SP0-VxWorks6.9 PSP is implemented specifically for the AiTech SP0-S processor running VxWorks v6.9 operating system.

## 4 CSCI ARCHITECTURAL DESIGN

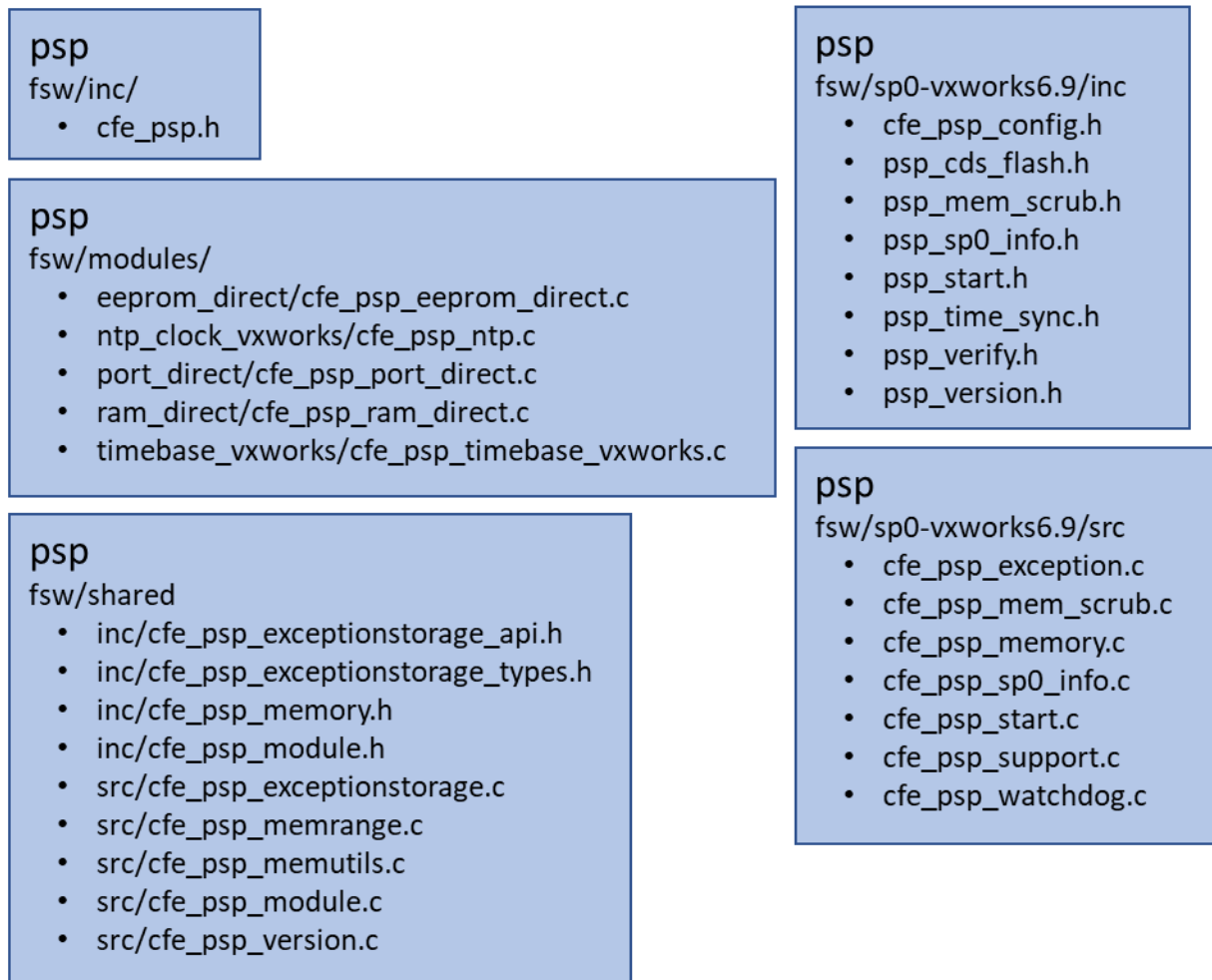
### 4.1 CSCI Components

The general design of the PSP is structured like a typical C library.

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**Figure 4-1. SP0-VxWorks6.9 PSP File Structure**

**Figure 4-1** depicts the file directory hierarchy of the PSP code base. The followings list the C source/header files and their purpose.

- psp/fsw/inc/cfe\_psp.h  
This header file contains the function declarations of the PSP’s public APIs.
- psp/fsw/modules/eeprom\_direct/cfe\_psp\_eeprom\_direct.c  
This source file defines the function definitions for the EEPROM-related APIs.
- psp/fsw/modules/ntp\_clock\_vxworks/cfe\_psp\_ntp.c  
This source file defines the function definitions for the NTP time-related APIs.
- psp/fsw/modules/port\_direct/cfe\_psp\_port\_direct.c  
This source file defines the function definitions for the port-related APIs for systems that can access I/O ports directly via memory-mapped addresses.
- psp/fsw/modules/ram\_direct/cfe\_psp\_ram\_direct.c

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This source file defines the function definitions for the RAM-related APIs for systems that can access physical memory directly.

- `psp/fsw/modules/timebase_vxworks/cfe_psp_timebase_vxworks.c`  
This source file defines the function definitions for the time-related APIs via the VxWorks `vxTimeBaseGet()` routine.
- `psp/fsw/shared/inc/cfe_psp_exceptionstorage_api.h`  
This header file defines the function declarations for the exception storage-related APIs. It provides a generic storage buffer ring for exceptions and functions to manipulate it.
- `psp/fsw/shared/inc/cfe_psp_exceptionstorage_types.h`  
This header file contains the definitions of data structures used by the exception storage functions.
- `psp/fsw/shared/inc/cfe_psp_memory.h`  
This header file contains the function declarations for the memory-related supporting functions for the local PSP routines.
- `psp/fsw/shared/inc/cfe_psp_module.h`  
This header file defines the data structures and function declarations for the module-related APIs.
- `psp/fsw/shared/src/cfe_psp_exceptionstorage.c`  
This source file contains the function definitions for the exception storage-related APIs.
- `psp/fsw/shared/src/cfe_psp_memrange.c`  
This source file contains the function definitions for the memory range-related APIs. The memory range is a table of valid memory address ranges maintained by the cFE.
- `psp/fsw/shared/src/cfe_psp_memutils.c`  
This source file contains the function definitions for the utility functions used by the memory-related APIs.
- `psp/fsw/shared/src/cfe_psp_module.c`  
This source file contains the function definitions for the module-related APIs.
- `psp/fsw/shared/src/cfe_psp_version.c`  
This source file contains the function definitions for routines that obtain the values of the various version identifiers.
- `psp/fsw/sp0-vxworks6.9/inc/cfe_psp_config.h`  
This header file defines the PSP configuration and data structure definitions for the SP0-VxWorks6.9 implementation.
- `psp/fsw/sp0-vxworks6.9/inc/psp_cds_flash.h`  
This header file contains the function declarations for the SP0-VxWorks6.9 PSP's CDS-related APIs. These functions save and restore CDS in FLASH memory.
- `psp/fsw/sp0-vxworks6.9/inc/psp_mem_scrub.h`  
This header file contains the function declarations for the SP0-VxWorks6.9 PSP's memory scrubbing-related APIs.
- `psp/fsw/sp0-vxworks6.9/inc/psp_sp0_info.h`

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This header file contains the data structure definitions and function declarations for obtaining statistical data on the SP0 processor such as Power-On Self Test (POST) results, processor temperatures, voltages, active boot EEPROM, etc.

- `psp/fsw/sp0-vxworks6.9/inc/psp_start.h`  
This header file contains the function declarations for the SP0-VxWorks6.9 PSP's startup/reset-related APIs.
- `psp/fsw/sp0-vxworks6.9/inc/psp_time_sync.h`  
This header file contains the function declarations for the SP0-VxWorks6.9 PSP's NTP time synchronization-related APIs.
- `psp/fsw/sp0-vxworks6.9/inc/psp_verify.h`  
This header file contains the static compile-time checks of the SP0-VxWorks6.9 PSP configurations.
- `psp/fsw/sp0-vxworks6.9/inc/psp_version.h`  
This header file defines the SP0-VxWorks6.9 PSP's version identifiers.
- `psp/fsw/sp0-vxworks6.9/src/cfe_psp_exception.c`  
This source file contains the function definitions for the SP0-VxWorks6.9 PSP's exception-related APIs.
- `psp/fsw/sp0-vxworks6.9/src/cfe_psp_mem_scrub.c`  
This source file contains the function definitions for the SP0-VxWorks6.9 PSP's memory scrubbing-related APIs.
- `psp/fsw/sp0-vxworks6.9/src/cfe_psp_memory.c`  
This source file contains the function definitions for the SP0-VxWorks6.9 PSP's memory-related APIs.
- `psp/fsw/sp0-vxworks6.9/src/cfe_psp_sp0_info.c`  
This source file contains the functions definitions for obtaining statistical data on the SP0 processor.
- `psp/fsw/sp0-vxworks6.9/src/cfe_psp_start.c`  
This source file contains the function definitions for the SP0-VxWorks6.9 PSP's startup/reset-related APIs.
- `psp/fsw/sp0-vxworks6.9/src/cfe_psp_support.c`  
This source file contains the function definitions for the SP0-VxWorks6.9 PSP's "glue" routines between the cFE and the SP0 Board Support Package (BSP).
- `psp/fsw/sp0-vxworks6.9/src/cfe_psp_watchdog.c`  
This source file contains the function definitions for the SP0-VxWorks6.9 PSP's watchdog-related APIs.

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## 4.2 Concept of Execution

As a library, PSP only provides the public functions that can be used by the cFE, OSAL and any cFS applications/libraries. It cannot be executed as a stand-alone task or application, and hence, has no concept of execution.

## 4.3 Interface Design

The SP0-VxWorks6.9 PSP's APIs are grouped into nine categories: common APIs, startup, CDS in FLASH, exception storage, memory, memory scrubbing, module, SP0 info, and NTP time synchronization.

### 4.3.1 Common APIs

Table 4.1 lists the SP0-VxWorks6.9 PSP APIs associated with common APIs for a cFE PSP.

**Table 4-1: [SP0-VxWorks6.9 PSP Common APIs](#)**

### 4.3.2 Startup APIs

Table 4.2 lists the SP0-VxWorks6.9 PSP APIs associated with PSP startup.

**Table 4-2: [SP0-VxWorks6.9 PSP Startup APIs](#)**

### 4.3.3 CDS in FLASH APIs

Table 4.3 lists the SP0-VxWorks6.9 PSP APIs associated with Critical Data Storage (CDS) in FLASH memory.

**Table 4-3: [SP0-VxWorks6.9 PSP CDS-in-FLASH APIs](#)**

### 4.3.4 Exception Storage APIs

Table 4.4 lists the SP0-VxWorks6.9 PSP's APIs associated with the exception storage.

**Table 4-4: [SP0-VxWorks6.9 PSP Exception Storage APIs](#)**

### 4.3.5 Memory APIs

Table 4.5 lists the SP0-VxWorks6.9 PSP's APIs associated with memory.

**Table 4-5: [SP0-VxWorks6.9 PSP Memory APIs](#)**

### 4.3.6 Memory Scrubbing APIs

Table 4.6 lists the SP0-VxWorks6.9 PSP's APIs associated with memory scrubbing.

**Table 4-6: [SP0-VxWorks6.9 PSP Memory Scrubbing APIs](#)**

### 4.3.7 Module APIs

Table 4.7 lists the SP0-VxWorks6.9 PSP's APIs associated with module.

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**Table 4-7: [SP0-VxWorks6.9 PSP Module APIs](#)**

#### 4.3.8 SP0 Info APIs

Table 4.8 lists the SP0-VxWorks6.9 PSP's APIs associated with SP0 statistical data.

**Table 4-8: [SP0-VxWorks6.9 PSP SP0 APIs](#)**

#### 4.3.9 NTP Time Synchronization APIs

Table 4.9 lists the SP0-VxWorks6.9 PSP's APIs associated with NTP time synchronization.

**Table 4-9: [SP0-VxWorks6.9 PSP NTP Time Synchronization APIs](#)**

## 5 CSCI DETAILED DESIGN

This section of the document is generated from Doxygen comments in the application's source code. The section contains the declarations of macros, variables and data structures, the function definitions, along with their inputs, outputs and limitations. The generated document also includes the application's configurable parameters and their values. For more details, see [Section 5](#).

### 5.1 Assumptions, Dependencies and Constraints

#### 5.1.1 Assumptions

- The SP0-VxWorks6.9 PSP contains the implementation of the common PSP APIs, as well as the additional custom APIs that are specific to the SP0 processor. The custom APIs are dictated by the software system's requirements, and hence, will vary from PSP to PSP.
- The SP0-VxWorks6.9 PSP's platform-specific configuration parameters are defined in the header file, *psp/fsw/sp0-vxworks6.9/inc/cfe\_psp\_config.h*.
- DeleteProcessorReservedMemory(), a common PSP API, is not implemented since it is not used for the SP0 processor running VxWorks6.9.
- Aitech Bootloader seems to delete the Reserved Memory after reboot. Since the Reserved Memory will get erased at each reboot, Critical Data Storage (CDS) is synchronized on FLASH memory.
  - The Reserved Memory on RAM is the Gold copy.
  - The Reserved Memory on FLASH is used for recovery after a soft reboot or a power cycle.
  - The CDS cannot be fully disabled on FLASH memory.

#### 5.1.2 Dependencies

- The SP0-VxWorks6.9 PSP is dependent on the Wind River development tools (cross compiler, loader, etc..) for the VxWorks v6.9 operating system for the PowerPC processor family.

#### 5.1.3 Constraints

- The SP0-VxWorks6.9 PSP is developed specifically for cFS, and hence, can only be used within the cFS development and run-time environments. For additional information on cFS, see documentation included with the cFE software release.

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## 5.2 LIMITATIONS AND WARNINGS

### 5.2.1 Limitations

- The SP0 exception handling is currently defaulted to the Kernel's default exception handling.
- Direct Memory Access (DMA) is not yet supported.
- When running the SP0-VxWorks6.9 PSP's unit tests on the SP0 platform, the SPE-based functions are currently stubbed out due to issues with the Wind River's code coverage tool.

### 5.2.2 Warnings

None.

## 6 BI-DIRECTIONAL TRACEABILITY MATRIX

This section documents the mapping of the software requirements to the design elements and from the design elements to the software requirements. The SP0-VxWorks6.9 PSP is a library, and therefore, does not have its own requirements. Hence, this section is not applicable to the SP0-VxWorks6.9 PSP.

### 6.1 From Requirement to Design Element

N/A.

### 6.2 From Design Element to Requirement

N/A.

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## 7 APPENDICES

### 7.1 Abbreviations and Acronyms

<i>Term</i>	<i>Definition</i>
AES	Advanced Exploration Systems
API	Application Programming Interface
CDR	Critical Design Review
cFE	Core Flight Executive
cFS	Core Flight System
CMD	Command
CR	Change Request
CSC	Computer Software Component
CSCI	Computer Software Configuration Item
CSU	Computer Software Unit
EA	Engineering Directorate Mail Code
FSW	Flight Software
GFE	Government Furnished Equipment
GSFC	Goddard Space Flight Center
GUI	Graphical User Interface
HK	Housekeeping cFS application
ICD	Interface Control Document
ISR	Interrupt Service Routine
JSC	Johnson Space Center
MD	Memory Dwell cFS Application
MDT	Message Definition Table (for SCH_TT application)
MID	Message Identifier
NASA	National Aeronautics and Space Administration
NPR	NASA Procedural Requirements
OS	Operating System
OSAL	Operating System Abstraction Layer
PDR	Preliminary Design Phase
PMP	Project Management Plan
PSP	Platform Support Package
PTRS	Project Technical Requirements Specification
SCH	Scheduler cFS Application
SCH_TT	Time-Triggered Ethernet Scheduler cFS Application
SB	cFE Software Bus
SBNG	Software Bus Network for Gateway cFS application
SDD	Software Design Document
SDP	Software Development Plan
SDT	Schedule Definition Table (for SCH_TT application)

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<i>Term</i>	<i>Definition</i>
SW, S/W	Software
TBD	To Be Determined
TBL	Table
TDM	Time-Division Multiplexing
TLM	Telemetry
TTE	Time-Triggered Ethernet
TTE_LIB	Time-Triggered Ethernet cFS library
TTE_MGR	Time-Triggered Manager cFS application
V&V	Verification and Validation
V&VD	Verification and Validation Document
VDD	Version Description Document
WI	Work Instruction

## 7.2 Definition of Terms

None.

## 8 NOTES

None.

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