

# Software Developer's Guide for the **Core Flight System SP0-VxWorks6.9 Platform Support Package – Version 1.5.1.0**

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Engineering Directorate  
Software, Robotics, and Simulation Division

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Space Administration  
**Lyndon B. Johnson Space Center**  
Houston, Texas

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# Software Developer's Guide for the **Core Flight System Time-Triggered Ethernet Library** **Version 1.5.1.0**

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## Change Record

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## 1 INTRODUCTION

### 1.1 Scope

This Software Developer's Guide is for the Core Flight System (cFS) SP0-VxWorks6.9 Platform Support Package (PSP). From here on, the software product will be referred to as the SP0-VxWorks6.9 PSP.

### 1.2 Purpose

This document describes how to install, configure, build, execute and troubleshoot the SP0-VxWorks6.9 PSP within the context of a cFS-based software system. The software was developed specifically as a software component of a cFS system, and hence, can only be built and executed within the cFS development and run-time environments. For additional information on cFE/cFS software framework, see documentation building and running included with the cFE software release. A copy can be obtained at <https://github.com/nasa/cfe>.

### 1.3 Audience

The intended audience of this document are the cFS software developers. It is assumed that the developers are familiar with the general infrastructure of the cFS and its ecosystem as well as the general build and run of cFS applications and libraries. New cFS developers can start with CFS-101 as the initial cFS training. A copy can be obtained at <https://github.com/nasa/cfs-101>.

Note that this is not the standard Software User's Guide for the Crew and Ground to command and control the target system. That would be a separate document to be produced by the project that uses this application.

### 1.4 Document Status and Schedule

This Software Developer's Guide is part of the documentation that comes with the software release of the SP0-VxWorks6.9 PSP.

## 2 RELATED DOCUMENTATION

### 2.1 Applicable Documents

The following documents, of the exact issue and revision shown, form a part of this Software Developer's Guide to the extent specified herein.

**Table 2-1: Applicable Documents**

<i>Document Number</i>	<i>Document Title</i>	<i>Revision / Release Date</i>
NPR 7150.2	NASA Software Engineering Procedural Requirements	Rev C / Aug 2019
EA-WI-025	GFE Flight Project Software and Firmware Development	Rev D / Sep 2013
GP-10021	Core Flight Software Certification Software Development Plan	Baseline / May 2020

### 2.2 Reference Documents

The following documents are reference documents utilized in the development of this Software Developer's Guide. These documents do not form a part of this document and are not controlled by their reference herein.

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**Table 2-2: Reference Documents**

<i>Document Number</i>	<i>Document Title</i>	<i>Revision / Release Date</i>
GSFC 582-2008-012	cFS Deployment Guide	Rel. 3.0 / Sep 2014
GSFC 582-2007-001	cFE Application Developer's Guide	Rel. 5.4 / Sep 2014
GSFC 582-2007-00	OSAL Configuration Guide	Rel. 4.2.1 / Aug 2016
TBD	SP0-VxWorks6.9 PSP Software Design Document	TBD

### 3 OVERVIEW

The SP0-VxWorks6.9 PSP is an abstraction layer of the processor's Board Support Package (BSP), similar to how the OSAL is the abstraction layer of the Operating System. A PSP provides a common set of Application Programming Interfaces (APIs) that can be used by the cFE, the OSAL and any cFS application/library.

The SP0-VxWorks6.9 PSP is implemented specifically for the AiTech SP0-S processor running VxWorks v6.9 operating system.

### 4 INSTALLATION

The SP0-VxWorks6.9 PSP requires no custom installation. It is packaged for distribution and installation just like any other PSP product, along with all the necessary documentation and artifacts. To install the SP0-VxWorks6.9 in a typical cFS workspace layout, the developer can add its source code to the “*psp*” directory. See <https://github.com/nasa/cfs> for a recommended cFS workspace layout.

Note that a project can opt to customize its own cFS workspace layout. When that is the case, the project's custom installation process supersedes the cFS default installation process.

### 5 BUILD

The SP0-VxWorks6.9 PSP requires no custom build. Adding the SP0-VxWorks6.9 PSP to the build is the same as adding any typical PSP implementation to an existing cFS build. See cFS Deployment Guide for information on cFS build process with CMake.

Note that if a project opts to use its own workspace layout, the cFS build steps will change to accommodate that custom workspace layout. When that is the case, the project's build process supersedes the cFS default build process.

The SP0-VxWorks6.9 PSP is developed to build, load and executed out-of-box with the defined default values of its configurable parameters.

### 6 CONFIGURATION

The SP0-VxWorks6.9 PSP can be configured for a project. To customize the configuration parameters, edit the C header file, “*psp/fsw/sp0-vxworks6.9/inc/cfe\_psp\_config.h*”.

### 7 APPLICATION PROGRAMMING INTERFACES

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This section includes the seven groups of SP0-VxWorks6.9 PSP APIs.

## 7.1 Common APIs

Table 7.1 lists the SP0-VxWorks6.9 PSP APIs associated with common APIs for a cFE PSP.

**Table 7-1: [SP0-VxWorks6.9 PSP Common APIs](#)**

## 7.2 Startup APIs

Table 7.2 lists the SP0-VxWorks6.9 PSP APIs associated with PSP startup.

**Table 7-2: [SP0-VxWorks6.9 PSP Startup APIs](#)**

## 7.3 CDS-in-FLASH APIs

Table 7.3 lists the SP0-VxWorks6.9 PSP APIs associated with Critical Data Storage (CDS) in FLASH memory.

**Table 7-3: [SP0-VxWorks6.9 PSP CDS-in-FLASH APIs](#)**

## 7.4 Exception Storage APIs

Table 7.2 lists the SP0-VxWorks6.9 PSP APIs associated with exception storage.

**Table 7-4: [SP0-VxWorks6.9 PSP Exception Storage APIs](#)**

## 7.5 Memory APIs

Table 7.3 lists the SP0-VxWorks6.9 PSP APIs associated with memory.

**Table 7-5: [SP0-VxWorks6.9 PSP Memory APIs](#)**

## 7.6 Memory Scrubbing APIs

Table 7.4 lists the SP0-VxWorks6.9 PSP APIs associated with memory scrubbing.

**Table 7-6: [SP0-VxWorks6.9 PSP Memory Scrubbing APIs](#)**

## 7.7 Module APIs

Table 7.5 lists the SP0-VxWorks6.9 PSP APIs associated with module.

**Table 7-7: [SP0-VxWorks6.9 PSP Module APIs](#)**

## 7.8 SP0 Info APIs

Table 7.6 lists the SP0-VxWorks6.9 PSP APIs associated with SP0 statistical data.

**Table 7-8: [SP0-VxWorks6.9 PSP SP0 APIs](#)**

## 7.9 NTP Time Synchronization APIs

Table 7.7 lists the SP0-VxWorks6.9 PSP APIs associated with NTP time synchronization.

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**Table 7-9: [SP0-VxWorks6.9 PSP NTP Time Synchronization APIs](#)**

## 8 ASSUMPTIONS, DEPENDENCIES AND CONSTRAINTS

### 8.1 Assumptions

- The SP0-VxWorks6.9 PSP contains the implementation of the common PSP APIs, as well as the additional custom APIs that are specific to the SP0 processor. The custom APIs are dictated by the software system's requirements, and hence, will vary from PSP to PSP.
- The SP0-VxWorks6.9 PSP's platform-specific configuration parameters are defined in the header file, *psp/fsw/sp0-vxworks6.9/inc/cfe\_psp\_config.h*.
- DeleteProcessorReservedMemory(), a common PSP API, is not implemented since it is not used for the SP0 processor running VxWorks6.9.
- Aitech Bootloader seems to delete the Reserved Memory after reboot. Since Reserved Memory will get erased at each reboot, Critical Data Storage (CDS) is synchronized on FLASH memory.
  - The Reserved Memory on RAM is the Gold copy.
  - The Reserved Memory on FLASH is used for recovery after a soft reboot or a power cycle.
  - The CDS cannot be fully disabled on FLASH memory.

### 8.2 Dependencies

- The SP0-VxWorks6.9 PSP is dependent on the Wind River development tools (cross compiler, loader, etc.) for the VxWorks v6.9 operating system for the PowerPC processor family.

### 8.3 Constraints

- The SP0-VxWorks6.9 PSP is developed specifically for cFS, and hence, can only be used within the cFS development and run-time environments. For additional information on cFS, see documentation included with the cFE software release.

## 9 LIMITATIONS AND WARNINGS

### 9.1 Limitations

- The SP0 exception handling is currently defaulted to the Kernel's default exception handling.
- Direct Memory Access (DMA) is not yet supported.
- When running the SP0-VxWorks6.9 PSP's unit tests on the SP0 platform, the SPE-based functions are currently stubbed out due to issues with the Wind River's code coverage tool.

### 9.2 Warnings

None.

## 10 KNOWN PROBLEMS

The SP0-VxWorks6.9 PSP's known problems and known changes are documented in the SP0-VxWorks6.9 PSP's Version Description Document (VDD).

## 11 TROUBLESHOOT

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## 11.1 Verifying successful startup

When the SP0-VxWorks6.9 PSP is successfully loaded and executed by the cFE Executive service, look for outputs similar to those below from the FSW execution output. Note that

- the expected outputs might not immediately follow one another; and
- the actual timestamps or will not be the same as the ones listed below; and
- certain values relating to kernel configurations, such as memory addresses could be different.

```
. . .
CFE_PSP_Main()
. . .
CFE_PSP: Set up VxWorks timebase, 50000000 ticks/sec, OS_time_t ratio=1/5
CFE_PSP: Using DIRECT memory mapped EEPROM implementation
CFE_PSP: Using DIRECT memory mapped RAM implementation
CFE_PSP: Using DIRECT memory mapped PORT implementation
PSP SP0: Collecting Data
CFE_PSP: Reset Memory Block at 0x3f000620, Total Size = 0x22de8
CFE_PSP: Volatile Disk Memory Block at 0x3f023420, Total Size = 0x200000
CFE_PSP: CDS Memory Block at 0x3f223420, Total Size = 0x20000
CFE_PSP: Reserved Memory Block at 0x3f000000 with size 0x343420, Total VxWorks
Reserved Size=0xffa000
PSP NTP SYNC: Task Initialized
PSP: Reset Register = 08
PSP: POWERON Reset: Power Switch ON.
CFE_PSP: Clearing Processor Reserved Memory.
CFE_PSP: Read 131072 bytes of CDS data from Flash.
PSP MEM SCRUB: Starting Active Memory Scrubbing
PSP: Setting system tasks' priorities for 10 tasks.
PSP: Setting tLogTask priority from 0 to 0
PSP: Setting tShell0 priority from 0 to 201
PSP: Setting tWdbTask priority from 0 to 203
PSP: Setting tVxdbgTask priority from 0 to 200
PSP: Setting tNet0 priority from 0 to 25
PSP: Setting ipftps priority from 0 to 202
PSP: Setting ipcom_syslogd priority from 0 to 205
PSP: Setting ipcom_telnetd priority from 0 to 204
PSP: Could not find task ipcom_egd
PSP: Setting FTCMP00 priority from 0 to 253
PSP: At least one vxWorks task priority set failed. System may have degraded
performance.
PSP: PROCESSOR rst Source = 0x8 = (RESET_SRC_POR) Safe mode = 0, sbc = LOCAL, reason =
0, cause = 0x00000000
PSP: POST Test - PASSED - Marching Address Test(L) .
PSP: POST Test - Not Run - Marching Address Test(W) .
PSP: POST Test - Not Run - Marching Address Test(B) .
PSP: POST Test - Not Run - Walk a Bit Test(L) .
PSP: POST Test - Not Run - Walk a Bit Test(W) .
PSP: POST Test - Not Run - Walk a Bit Test(B) .
PSP: POST Test - PASSED - Refresh Test(L) .
PSP: POST Test - Not Run - Refresh Test(W) .
PSP: POST Test - Not Run - Refresh Test(B) .
PSP: POST Test - PASSED - Random Data Test(L) .
PSP: POST Test - Not Run - Random Data Test(W) .
PSP: POST Test - Not Run - Random Data Test(B) .
```

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```

PSP: POST Test - PASSED - Clear Memory Test(L) .
PSP: POST Test - Not Run - Clear Memory Test(W) .
PSP: POST Test - Not Run - Clear Memory Test(B) .
PSP: POST Test - Not Run - N/D Marching Bit Test(L) .
PSP: POST Test - Not Run - N/D Marching Bit Test(W) .
PSP: POST Test - Not Run - N/D Marching Bit Test(B) .
PSP: POST Test - PASSED - ECC Read Test on SDRAM .
PSP: POST Test - Not Run - Boot Flash Fail Over.
PSP: POST Test - PASSED - EEPROM CRC Test .
PSP: POST Test - PASSED - User Flash CRC Test .
PSP: POST Test - Not Run - User Flash Retention Test.
PSP: POST Test - PASSED - CPU Test .
PSP: POST Test - Not Run - L1 Cache Test.
PSP: POST Test - Not Run - L2 Cache Test.
PSP: POST Test - PASSED - PCI Bridge Test .
PSP: POST Test - PASSED - cPCI Bridge Test .
PSP: POST Test - Not Run - Watchdog Reset Test.
PSP: POST Test - PASSED - Interrupt Test .
PSP: POST Test - PASSED - Timer Test .
PSP: POST Test - Not Run - Serial I/O External Loopback Test.
PSP: POST Test - PASSED - Memory Interface Test .
PSP: POST Test - Not Run - Combined Timer Test.
PSP: POST Test - PASSED - ECC Error Injection Test .
PSP: POST Test - PASSED - Serial I/O Internal Loopback Test - UART .
PSP: POST Test - Not Run - Watchdog Timer Test.
PSP: POST Test - Not Run - FPGA Watchdog Reset Test.
PSP: POST Test - PASSED - FPGA Watchdog Timer Test .
. . .
PSP: PSP Application Startup Complete
. . .
PSP EXC: Attached cFE Exception Handler.
PSP SetDefaultExceptionEnvironment not implemented
PSP NTP SYNC: CFE TIME Service is ready - Starting NTP Sync
CFE_PSP: Wrote 131072 bytes to FLASH CDS file
. . .

```

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## 12 APPENDICES

### 12.1 Abbreviations and Acronyms

Term	Definition
API	Application Programming Interface
BSP	Board Support Package
CCDD	CFS Command and Data Dictionary tool
CCSDS	Consultative Committee for Space Data Systems
cFE	Core Flight Executive
cFS	Core Flight System
CI	Command Ingest cFS application
COTS	Commercial Off-the-Shelf
CSC	Computer Software Component
CSCI	Computer Software Configuration Item
CSU	Computer Software Unit
EA	JSC Engineering Directorate Organization Code
ES	cFE Executive Services
EVS	cFE Event Services
GFE	Government Furnished Equipment
GSFC	Goddard Space Flight Center
HK	Housekeeping cFS application
JSC	Johnson Space Center
MDT	Message Definition Table (for SCH_TT application)
MID	Message Identifier
NASA	National Aeronautics and Space Administration
NPR	NASA Procedural Requirements
OS	Operating System
OSAL	Operating System Abstraction Layer
PSP	Platform Support Package
SB	cFE Software Bus
SBNg	Software Bus Network for Gateway cFS application

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Term	Definition
SCH	Scheduler cFS application
SCH_TT	Time-Triggered Ethernet Scheduler cFS application
SDD	Software Detailed Design
SDT	Schedule Definition Table (for SCH_TT application)
SRS	Software Requirements Specification
TBD	To Be Determined
TDM	Time-Division Multiplexer
TO	Telemetry Output cFS application
TTE	Time-Triggered Ethernet
TTE ES	Time-Triggered Ethernet End System
TTE_LIB	Time-Triggered Ethernet cFS Library
TTE_MGR	Time-Triggered Ethernet Manager cFS application
VDD	Version Description Document

## 12.2 Definition of Terms

None.

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## 13 NOTES

None.

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