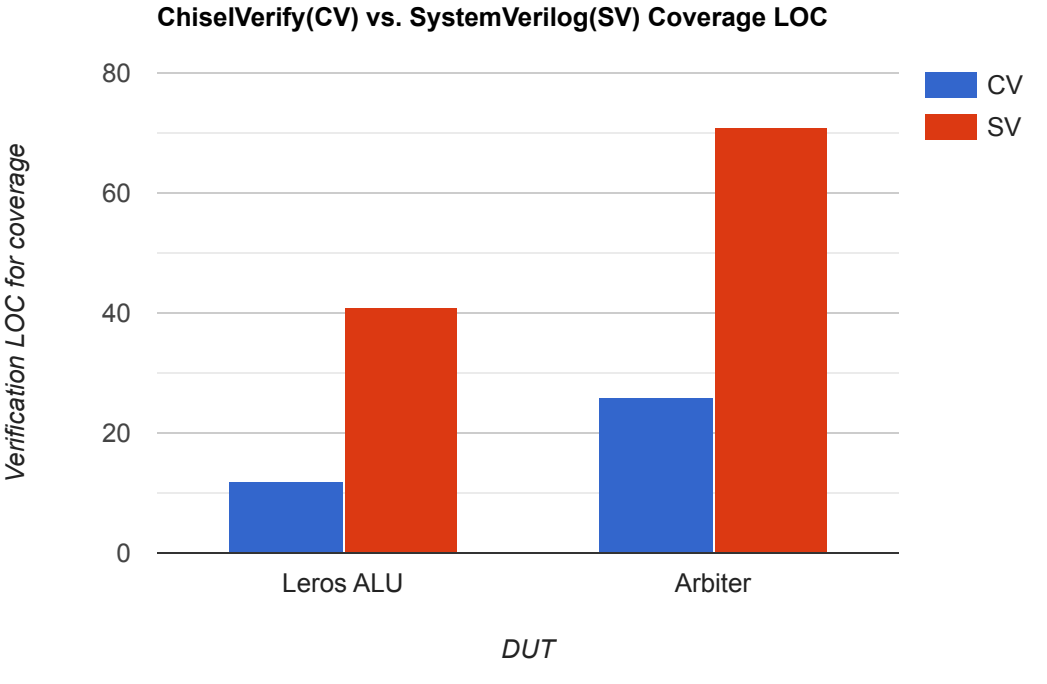
ChiselVerify(CV) vs. SystemVerilog(SV) Coverage LOC
80
60
40
20
0
Verification LOC for coverage
CV
SV
Leros ALU
Arbiter
DUT