

A COMPARISON OF SOFTWARE AND HARDWARE TECHNIQUES FOR X86 VIRTUALIZATION

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May 10th, Software Systems Seminar 2007

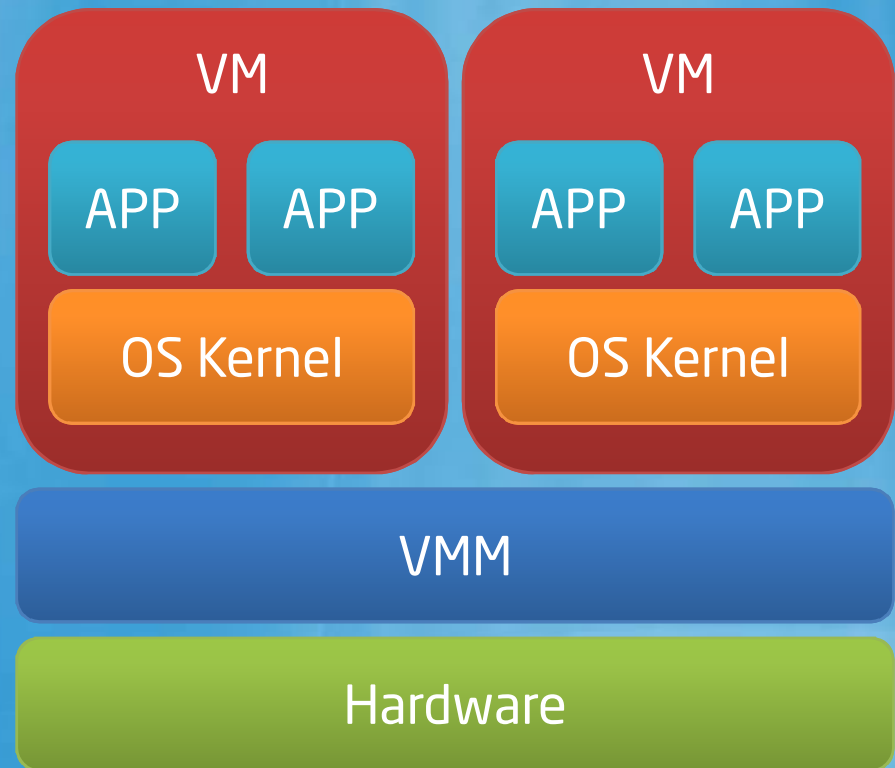
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Content

- Introduction
- Virtualization
 - Classical
 - Software
 - Hardware
- Comparison
- Opportunities
- Conclusion

Introduction and Terminology

- Virtualization
- Virtual Machine
 - Guest
- Virtual Machine Monitor
 - Host
- Motivation
 - Resource utilization
 - Development
 - ...



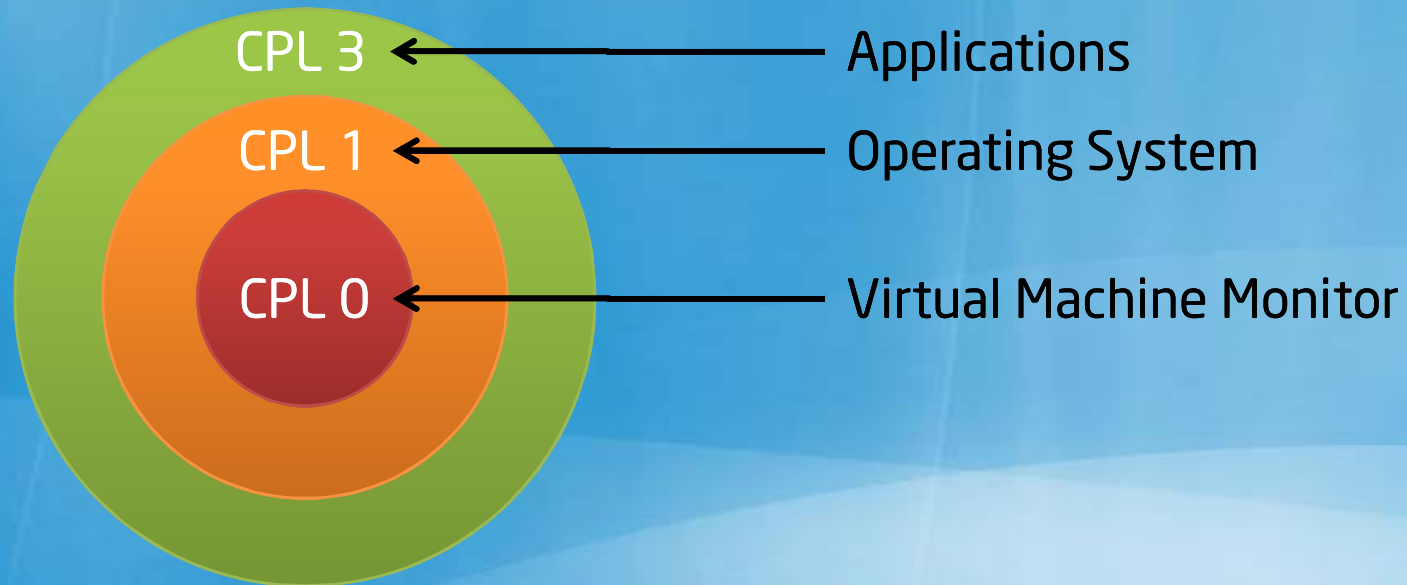
CLASSICAL VIRTUALIZATION

Classical Virtualization

- Three essential characteristics (Popek and Goldberg)
 - Fidelity - runs any software
 - Performance - fairly fast
 - Safety - VMM manages hardware
- Trap-and-Emulate
 - Only real solution until recently

De-Privileging

- Read/Write privileged state Instruction
- Direct Execution but reduced privileged level
- VMM intercepts traps and emulates



Shadow Structures

- Virtual state differs from physical state
- VMM provides basic Execution Environment
- Shadow Structures
- On-CPU privileged state
 - Maintained as Image
- Off-CPU privileged data
 - Resides in Memory

Memory Traces

- Use of hardware page protection mechanisms for coherency of shadow structures
- Protection for memory-mapped devices
- Handling a trace fault:
 - Decode guest instruction
 - Emulate its effect in the primary structure
 - Apply change to the shadow structure

Tracing Example

- Use of Shadow Page Tables to run guest
- Vmware manages SPTs as cache
- True Page Fault
 - Violation of the protection policy
 - Forwarded to guest
- Hidden Page Fault
 - Missing Page in SPT
 - No guest-visible effect

Refinements

- Flexibility in VMM/guest OS Interface
 - Modify guest OS
 - Performance Gains
 - Extended Features
- Flexibility in VMM/hardware Interface
 - Hardware Execution mode for guest OS
- “Paravirtualization”

SOFTWARE VIRTUALIZATION

x86 Obstacles

- Visibility of privileged state
- Lack of Traps at user-level
- Example: Unprivileged popf
 - Privileged level: ALU & system flags
 - De-privileged level: ALU changes
 - No trap in de-privileged level

Simple Binary Translation - Interpreter

- Use of an interpreter
- Prevent leakage of privileged state
- Correct implementation of non-trapping instructions
- Separation of virtual state from physical state
- Fails Performance Criteria

Simple Binary Translation

- Binary Translation combines Interpreter with Performance
- VMware's Translator offers this properties:
 - Binary
 - Dynamic
 - On Demand
 - System Level
 - Sub-Setting
 - Adaptive

Simple Binary Translation - Example

- Simple prime validation
- Invoke `isPrime(49)`

```
int isPrime(int a) {  
    for (int i = 2; i < a; i++) {  
        if (a % i == 0) return 0;  
    }  
    return 1;  
}
```

Simple Binary Translation - Example

isPrime:	mov %ecx, %edi	Translation Unit
	mov %esi, \$2 IR	
	cmp %esi, %ecx	
	jge prime	

nexti:	mov %eax, %ecx	Translation Unit
	cdq	
	idiv %esi	
	test %edx, %edx	
	jz notPrime	

	inc %esi
	cmp %esi, %ecx
	j1 nexti

prime:	mov %eax, \$1
	ret

notPrime:	xor %eax, %eax
	ret

isPrime':	mov %ecx, %edi	Compiled Code Fragment
	mov %esi, \$2	
	cmp %esi, %ecx	
	jge [takenAddr]	
	jmp [fallthrAddr]	

nexti':	mov %eax, %ecx	Compiled Code Fragment
	cdq	
	idiv %esi	
	test %edx, %edx	
	jz notPrime'	
	jmp [fallthrAddr]	

Simple Binary Translation - Example

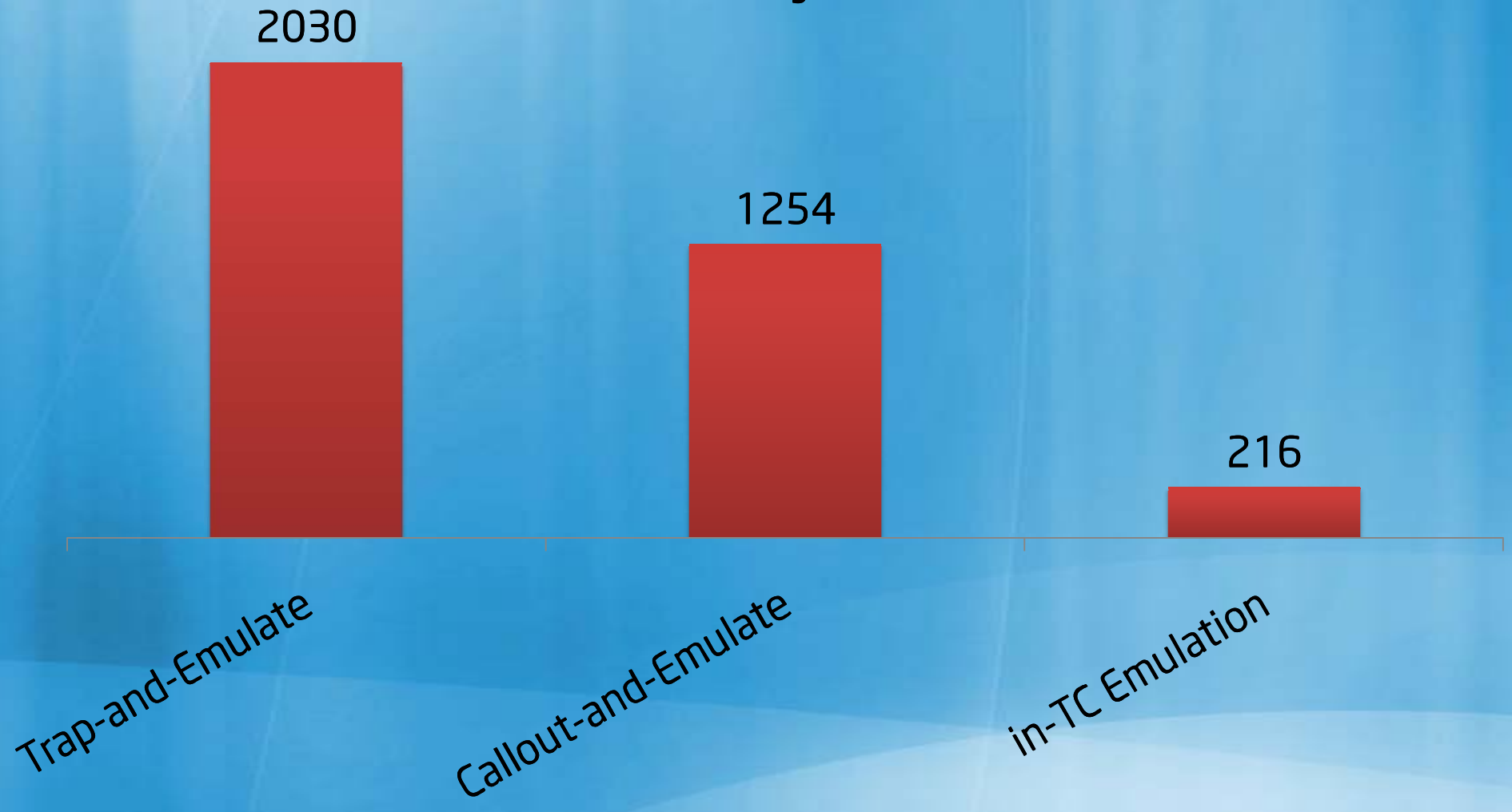
		<code>isPrime':</code>	<code>*mov %ecx, %edi</code>
<code>isPrime:</code>	<code>mov %ecx, %edi</code>		<code>mov %esi, \$2</code>
	<code>mov %esi, \$2</code>		<code>cmp %esi, %ecx</code>
	<code>cmp %esi, %ecx</code>		<code>jge [takenAddr]</code>
	<code>jge prime</code>	<code>nexti':</code>	<code>*mov %eax, %ecx</code>
<code>nexti:</code>	<code>mov %eax, %ecx</code>		<code>cdq</code>
	<code>cdq</code>		<code>idiv %esi</code>
	<code>idiv %esi</code>		<code>test %edx, %edx</code>
	<code>test %edx, %edx</code>		<code>jz notPrime'</code>
	<code>jz notPrime</code>		<code>*inc %esi</code>
	<code>inc %esi</code>		<code>cmp %esi, %ecx</code>
	<code>cmp %esi, %ecx</code>		<code>j1 nexti'</code>
	<code>j1 nexti</code>		<code>jmp [fallthrAddr3]</code>
<code>prime:</code>	<code>mov %eax, \$1</code>	<code>notPrime':</code>	<code>*xor %eax, %eax</code>
	<code>ret</code>		<code>pop %r11 ; RET</code>
<code>notPrime:</code>	<code>xor %eax, %eax</code>		<code>mov %gs:0xff39eb8(%rip), %rcx</code>
	<code>ret</code>		<code>movzx %ecx, %r11b</code>
			<code>jmp %gs:0xfc7dde0(8*%rcx)</code>

Simple Binary Translation - Exceptions

- PC-relative addressing
 - Translator output on different location
- Direct control flows
 - Code layout changes need reconnection
- Indirect control flows
 - Dynamically computed targets
- Privileged instructions

Comparison

rdtsc #Cycles



HARDWARE VIRTUALIZATION

x86 Architecture Extensions

- Allows classical Trap-and-Emulate
- Virtual Machine Control Block
 - Diagnostics Fields
- Guest Mode (VMX) vs. Host Mode
- `vmrun` Command

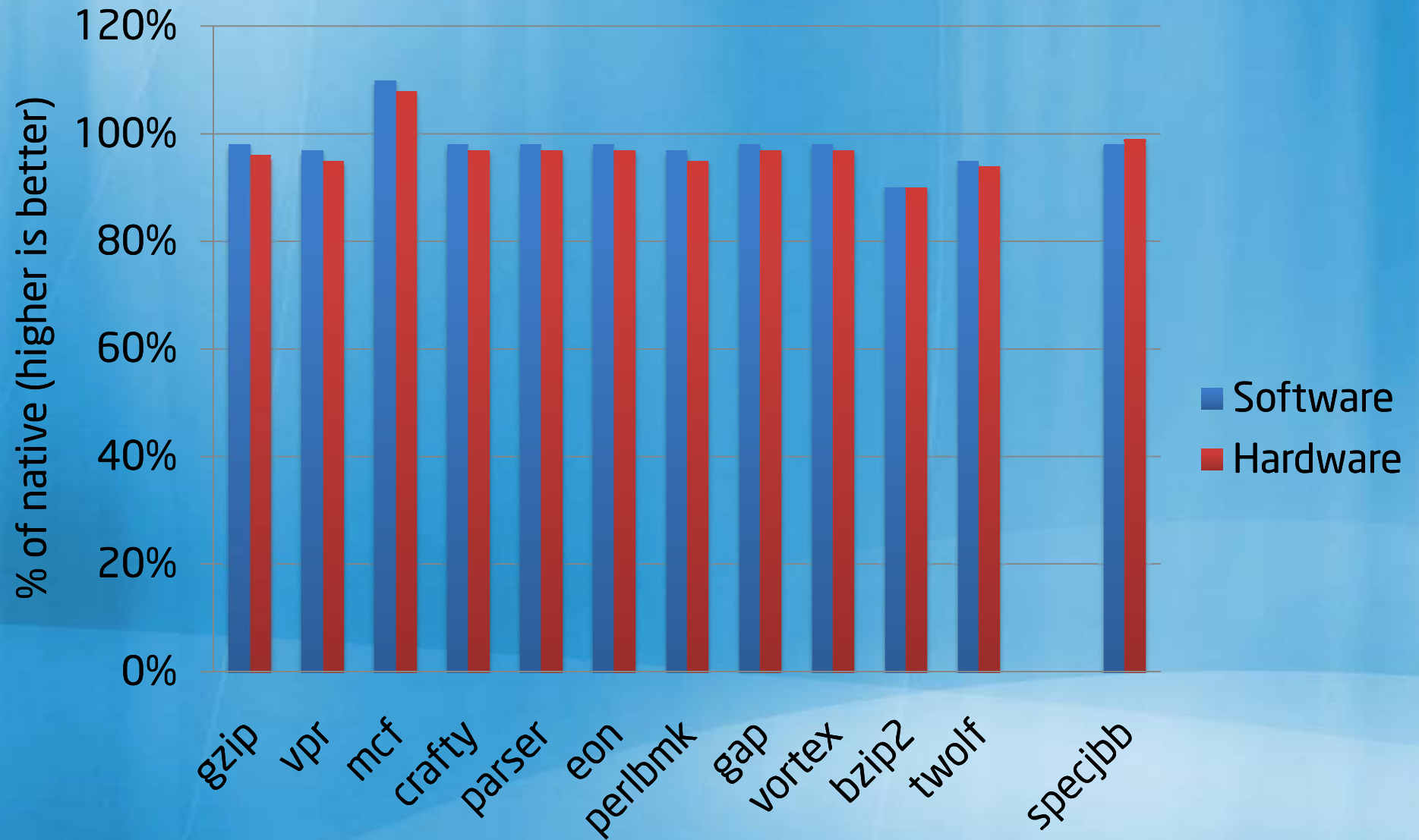
Qualitative Comparison

- Binary Translator
 - Trap Elimination
 - Emulation Speed
 - Callout avoidance
- Hardware-assisted VMM
 - Code density
 - Precise exceptions
 - System calls

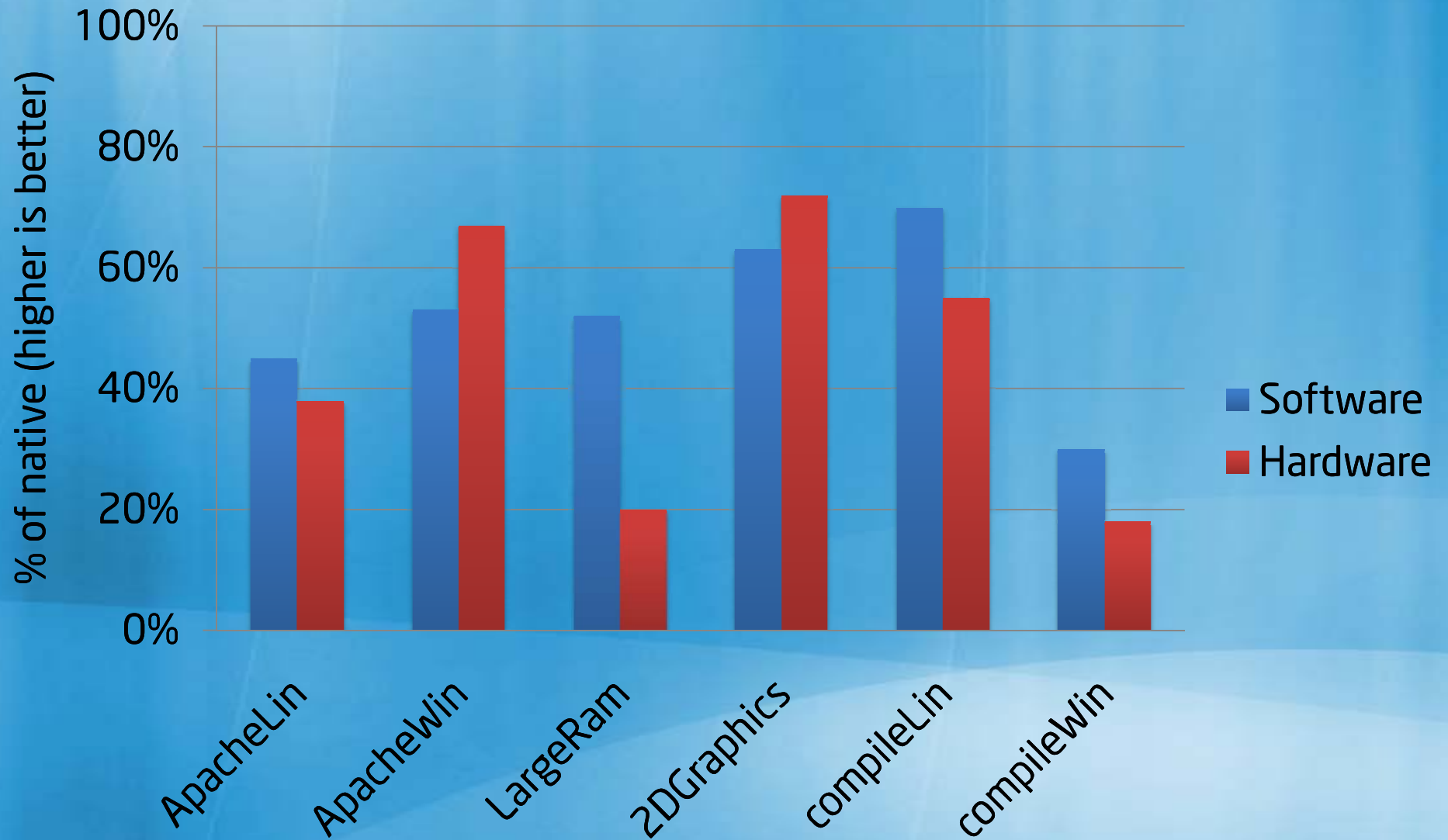
EXPERIMENTS AND RESULTS

Initial Measuring

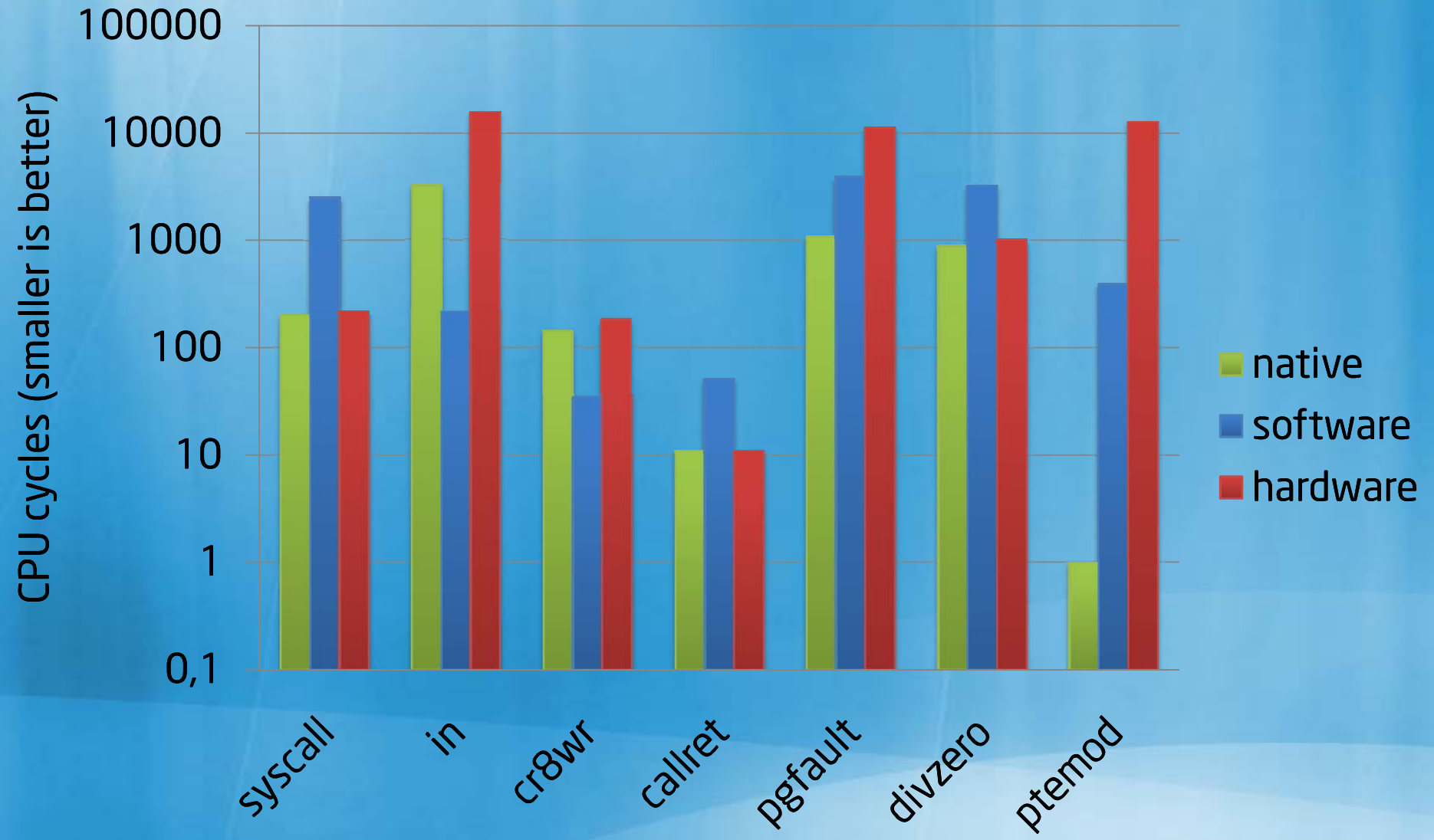
SPECint 2000 and SPECjbb 2005



Macrobenchmarks



Cost of Operations



Opportunities

- Faster MicroCoreArchitecture Implementations
- Hardware VMM Algorithms
- Hybrid VMM
- Hardware MMU

Conclusions

- First generation of hardware support
 - Permit tran-and-emulate
- No real performance decrease
 - Only at system calls
- New MMU algorithms could help

Michael Wallner

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