SIVI-NPLL1P25G65

TSMC 65nm (1P6M)

MAIN FEATURES

- Designed on TSMC 65nm
- Digital Supply 1V (+/-10%)
- Analog Supply 1.5V (+/-10%)
- Input frequency 25MHz
- Output clock frequency 1GHz
- Long term rms jitter 7ps
- Current consumption <5mA
- Integer Mode only
- Fully integrated solution
- Operational temperature range from -40°C to 125°C

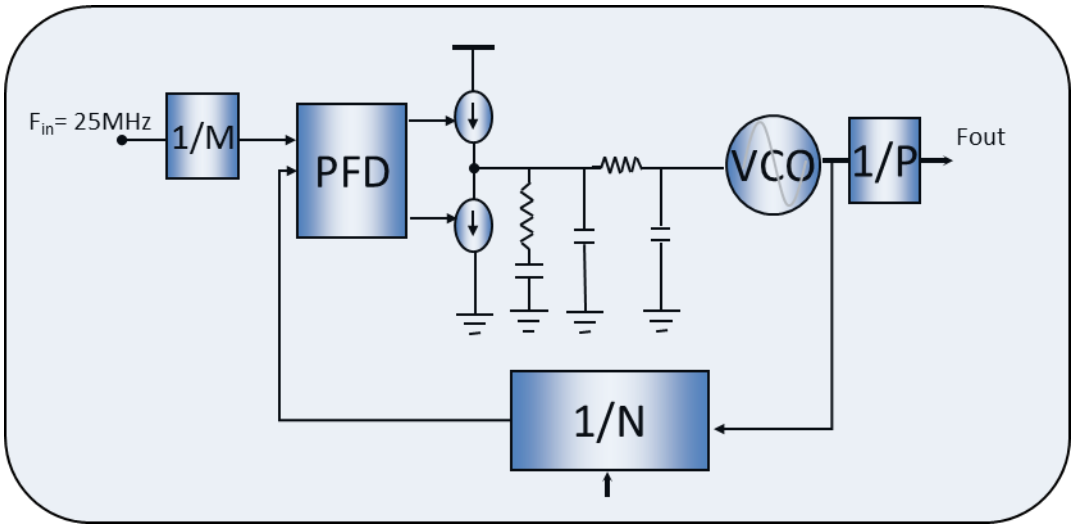
IP DESCRIPTION

Silicon Vision's SiVi-NPLL1P25G65 is an integer-N PLL that is used as the master clock generation in variety of state of the art wire-line SERDES applications as the EPON standard. It is a fully integrated, low power solution that uses a 25MHz crystal clock to generate a frequency of 1250MHz.

SiVi-NPLL1P25G65 is ready on 65nm TSMC

APPLICATIONS

- EPON SERDES
- General low jitter clock generation for wireline applications



Block Diagram for SiVi-NPLL1P25G65

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