SIVI-NPLL70M180

TSMC 180nm (1P4M)

MAIN FEATURES

- Designed on TSMC 180nm
- Voltage Supply 1.8V (+/-10%)
- Input Frequency 35MHz and 70MHz
- Output Frequency (640, 70, 35)MHz
- Long term rms Jitter < 30ps
- Startup time < 100us
- Current consumption < 3mA
- 8 output phases for the 640MHz
- Fully integrated solution
- Operational temperature range from -40°C to 125°C

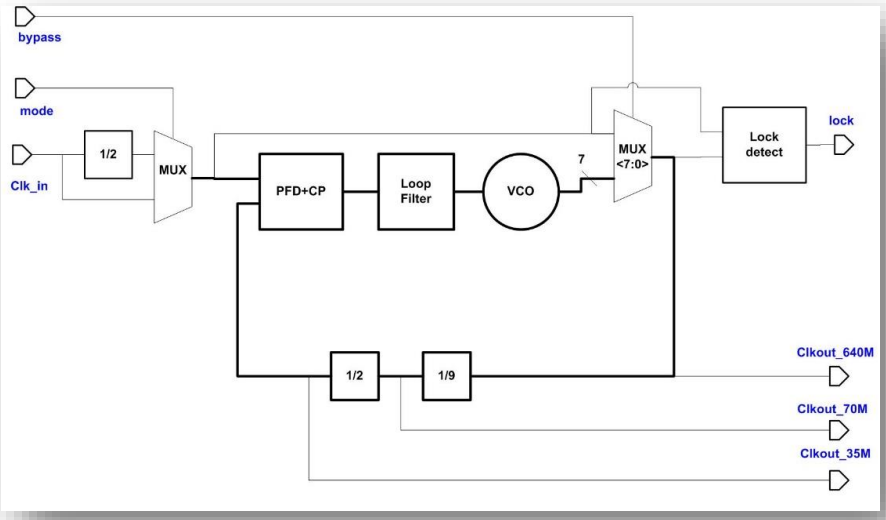
IP DESCRIPTION

Silicon Vision's SiVi-NPLL70M180 is an integer-N PLL that is used as the master clock generation in variety of state of the art wire-line applications as the ADSL-II AFEs. It is a fully integrated, low power solution that uses a 35MHz and 70MHz reference clocks to generate a set of frequencies, 640MHz, 70MHz and 35MHz.

SiVi-NPLL70M180 is ready on 180nm and 160nm TSMC processes

APPLICATIONS

- ADSL-II Analog Front End
- General low jitter clock generation for wire-line applications



Block Diagram for SiVi-NPLL70M180

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