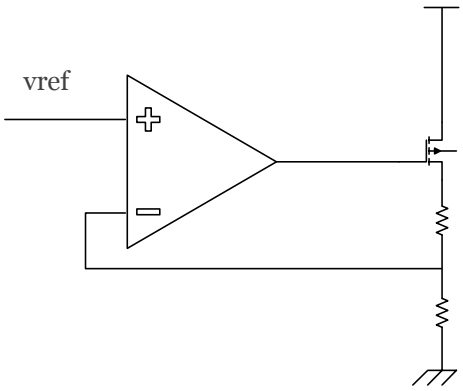
SIVI-LDO1060

TSMC 65nm-G (1P5M)

MAIN FEATURES

- Designed on TSMC 65nm Generic Process
- Supply a load current up to 60mA
- Input voltage ranges from 1.8V to 1.3V
- Output Voltage is 1.0V
- Low Quiescent current



SiVi-LDO1060 Block Diagram

IP DESCRIPTION

SiVi-LDO1060 is a voltage regulator with low quiescent current while supplying a load current up to 60mA. The regulator is fully integrated with no need of any external components. High supply rejection ratio is provided with super noise performance is provided which is required by clock generators, ADCs and other noise sensitive analog blocks.

SiVi-LDO1060 is silicon proven on TSMC – 60nm Generic technology.

ELECTRICAL SPECIFICATIONS

Spec / Result		Min	Typ	Max	Unit
Supply Voltage		1.3		1.8	V
Temperature Range		-40	27	125	°C
Output Voltage			1.0		V
Output Voltage Accuracy		-3		3	%
Load Current				60	mA
PSRR	@1kHz		-50		dB
	@32MHz		-7		
Quiescent Current				70	uA
Spot noise @100kHz				100	nV/√Hz

PIN DESCRIPTION

Pin Name	Direction	Description
vdd	Input	Analog supply rail
vss	Input	Analog ground rail
Iref_10uA	Input	10uA Bandgap current internally referred for reference generation
LDO_pd	Input	Power down signal for the LDO
vout	Output	Output voltage for the LDO

Silicon Vision Tech. Ltd.
14 Manchester Square, London
W1U 3PP, United Kingdom
info@si-vision.com