SIVI-PADC1004

TSMC 130nm-G (1P5M)

MAIN FEATURES

- Designed on TSMC 130nm-G
- 10-bit, 32 MS/S pipelined ADC
- Integrated S/H circuit and reference generator
- 1.0 Vp-p differential input range
- Low current consumption 16mA
- Architecture is based on opamp sharing for optimal power usage
- Power down mode and Automatic fast startup
- DNL = +/- 3 LSB , INL = +/- 3 LSB
- Operational temperature range from -40°C to 125°C

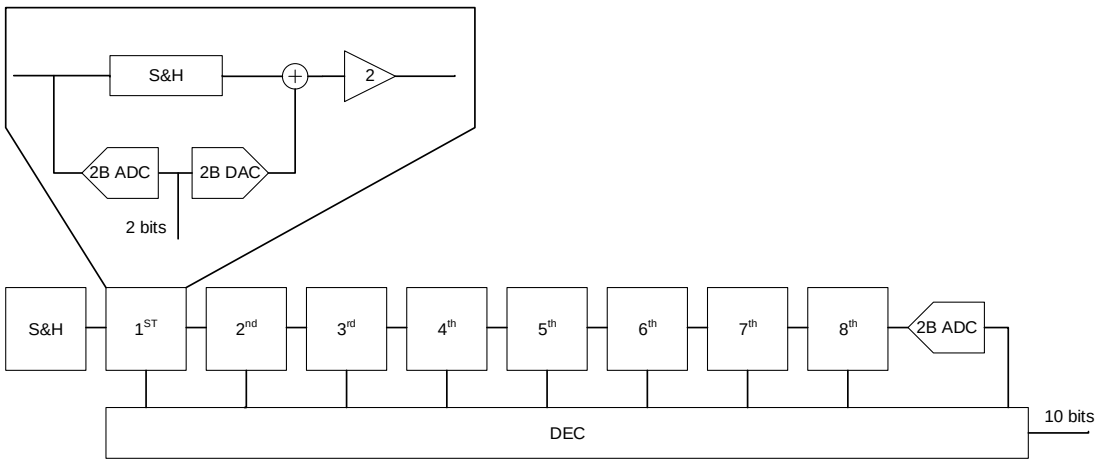
IP DESCRIPTION

Silicon Vision SiVi-PADC1004 is a high accuracy, high speed pipelined Analog to Digital Converter (ADC) IP core that offers 10-bit accuracy at a sampling rate of up to 32 MS/s with an input signal bandwidth of 8MHz. This IP is characterized by its low power consumption and small silicon area as it makes use of OPAMP sharing technique.

SiVi-PADC1004 is silicon proven in 130nm TSMC-G process technologies.

APPLICATIONS

- Video Analog Front Ends
- Analog front-end for wire bond communication
- Analog front-end for flat panel display and HDTV
- Base station receivers



Block Diagram for SIVI-PADC1004

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