SIVI-FPLL128M130

TSMC 130nm (1P5M)

MAIN FEATURES

- Designed on TSMC 130nm
- Supply Voltage 1.2V (+/-10%)
- Input Frequency 10MHz →20MHz
- Output Frequencies (8, 32, 64, 128)MHz
- Long Term rms Jitter (1MHz to 8MHz) 120ps
- Frequency resolution 5ppm
- Current Consumption 5mA
- High supply rejection and process tolerance
- Fully integrated solution
- Self-calibration mechanism using fully integrated calibrators and state machines
- Operational temperature range from -40°C to 125°C

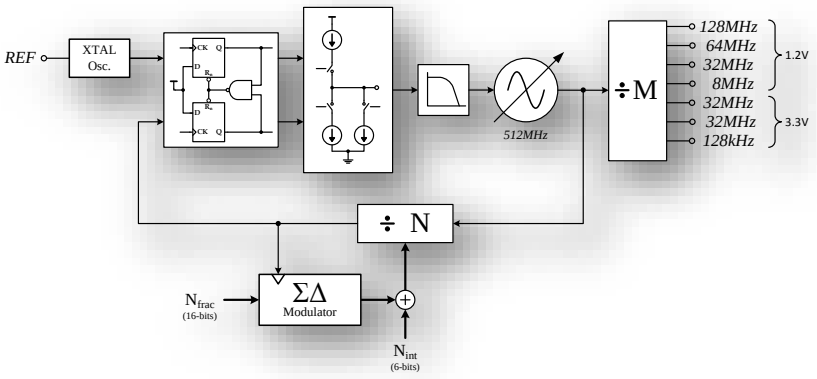
IP DESCRIPTION

Silicon Vision's SiVi-FPLL128M130 is a wide range low jitter fractional PLL that is suitable for providing a stable clock for low bit rate analog front ends. The IP is characterized by its high accuracy which is better than 5ppm and low power consumption. SiVi-FPLL128M130 has a fully integrated auto calibration state machine which operates on powering up the chip. It low power consumption, low noise performance and high accuracy makes this clock generator as perfect for low data rate powerline communication SOCs

SiVi-FPLL128M130 is ready on 130nm TSMC

APPLICATIONS

- Low Bit Rate DC Powerline Communications



Block Diagram for SiVi- FPLL128M130

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