# DIGITAL DESIGN

## SILICON VISION: ASIC/SOC/FPGA LEAD/SENIOR DESIGN ENGINEER (REFRENCE DSTL001)

### Job Description:

The ASIC/SoC/FPGA Lead/Senior Design Engineer position is part of a team responsible for all aspects of development of block and full chip RTL netlists, including design, audits, physical implementation and block level verification. In this role, there will be significant interaction with other design engineers.

- Design and verify digital RTL blocks that are implemented in standard cell ASIC and/or FPGA.
- Implement technical specification and/or design implementation documents. The RTL designs may be created in-house, obtained from a 3rd party IP vendor or from a customer.
- Implement design with VHDL and/or Verilog.
- Verify block design with Verilog or System Verilog testbenches. Knowledge of UVM or OVM a plus.
- Perform design audits, synthesis, static timing analysis, equivalence checking, SCAN insertion, ATPG.
- Support layout engineers by providing design constraints and assisting with floor-planning.
- Work with architect, marketing, and applications engineering to ensure finished product meets technical specifications and customers' needs.
- Work with project manager to ensure product is delivered on schedule.
- Support application and software teams with functional models and SW/HW co-verification issues.
- Support test and validation teams with ATE and board-level test issues.
- Support technical development of junior engineers.

### Required Skills:

- BS or MS in Electrical Engineering or Computer Engineering.
- 8+ years of ASIC design and verification experience.
- Experienced in ASIC design flow (RTL design, simulation, synthesis, clock tree insertion, static timing analysis and timing closure, equivalence checking, DFT, ATPG). Key tools include Modelsim, Cadence RC, Synopsys
- Design Compiler, Formality, Primetime, Galaxy Constraint Audits, and Subversion/Synchronicity. Knowledge of
- Place and Route tools such as Synopsys ICC is a plus.
- Proficient in Verilog HDL and System Verilog. UVM or OVM knowledge preferred.
- Experience in deep-submicron ASIC design at 90 nm or less preferred. Experience with high speed RTL block design in excess of 300 MHz is also preferred. Experience in techniques for low power implementation is also preferred.
- Proficient in Perl, Tcl and Unix/Linux shell scripting. Object-oriented programming skill is a plus.
- Knowledge of standards (Ethernet, PCIe, JTAG, SPI, I2C, DDRx memory interfaces) preferred.
- Experience in projects planning and projects managing is required.
- Good teamwork and able to collaborate with multi-site teams.


**Silicon Vision**
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## Company Offers:

- A stimulating, exciting and dynamic work environment, where your personal contributions to our business success will be optimally rewarded
- Room for career growth and external training.
- A competitive packages including excellent salaries, health insurance for employees and their families, and bonus system

**Interested candidates should send their resumes to careers@si-vision.com.**
**Please include "DSTL001 "in the e-mail subject.**


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