SIVI-FPLL4G65

TSMC 65nm (1P4M)

MAIN FEATURES

- Designed on TSMC 65nm
- Wide input range of frequencies up to 1.6GHz
- Wide output range of frequencies up to 3.2GHz
- Ability to operate in Frac-N and Integer-N modes
- Very high frequency resolution
- Low long term jitter down to 5ps rms
- High supply rejection and process tolerance
- Fully integrated solution
- Self-calibration mechanism using fully integrated calibrators and state machines
- Low current operation
- Operational temperature range from -40°C to 125°C

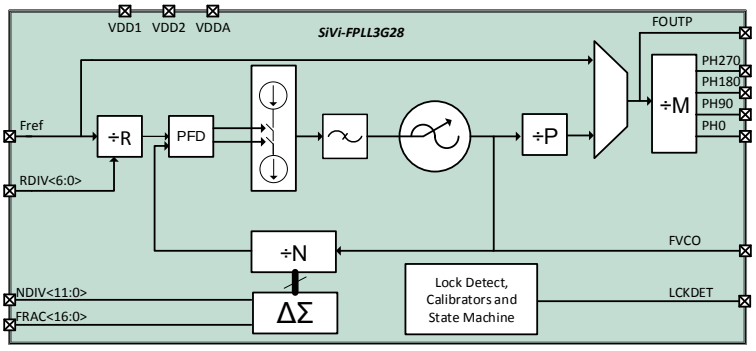
IP DESCRIPTION

Silicon Vision's SiVi-FPLL4G65 is a wide range low jitter fractional PLL that is suitable for DDR3 and DDR4 clock generation. It includes a low-power, low noise supply independent VCO's, self-calibrators, high resolution sigma-delta modulator and availability of multiphase output

SiVi-FPLL4G65 is silicon proven in 65nm TSMC

APPLICATIONS

- DDR3 and DDR4 PHYs
- Multi-Purpose high speed SerDes Clocking
- Generic low jitter clocking systems
- High definition video analog front ends



Block Diagram for SiVi- FPLL4G65

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