SIVI-SDADC1201

TSMC 180nm (1P4M)

MAIN FEATURES

- Designed on TSMC 180nm
- 12 bit low power sigma delta ADC
- Operates from a 3.3V and 1.8V supply voltages
- 0 to 4.0V input differential dynamic range
- Sampling frequency up to 36MHz
- Signal Bandwidth up to 1.1MHz
- SNR> 74dB at 1.1MHz bandwidth
- THD> 80dB at 100kHz full swing
- Low current consumption<7mA
- Operational temperature range from -40°C to 125°C

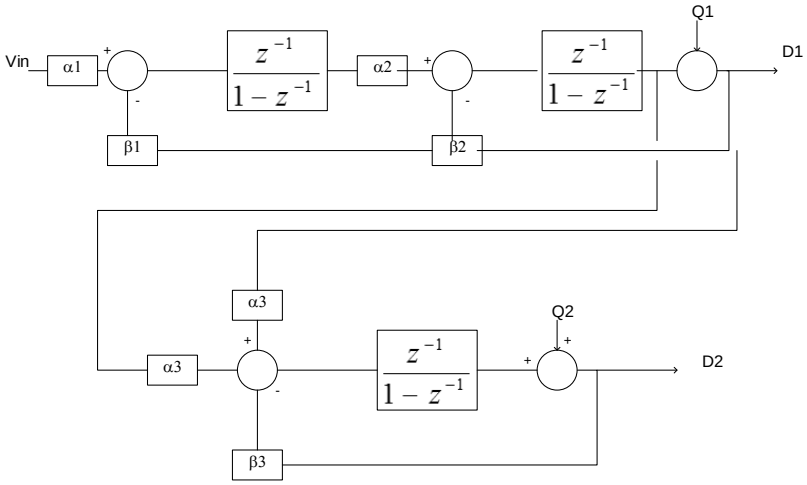
IP DESCRIPTION

Silicon Vision SiVi-SDADC1201 offers a high performance and cost-effective solution for ADCs that can be used for high end analog signal reception. The IP uses a sampling clock of 36MHz to receive signals with frequencies up to 1.1MHz with 12 bit resolution. Silicon Vision SiVi-SDADC1201 consumes less than 7mA at maximum input signal frequency and dynamic range that can go up to 4.0Vpp differential

The IP was implemented and silicon verified on TSMC 180nm LP

APPLICATIONS

- Analog Front End Signal reception
- Monitoring Analogue Voltages or Currents from External Sensing Devices



Block Diagram for SiVi-SDADC1201

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