NAS-GEM-80 FDC CARD

Instruction Manual & Functional Description

Contents

1 Introduction

This card has been designed to be a form, fit and function replacement for the Nascom Floppy Disk Controller, which is proving to be a very difficult item to source for the Nascom / Gemini retro community.

The card has been tested against original Teac FD-50E/F drives without observed issues under NAS-DOS 1.4

Further testing with CP/M and PolyDos is planned

Note: The card is designed to handle 5.25-inch drives. Support for 8-inch drives has been removed ***(Did anyone ever use this?)***

2 Components

Reference	Value	Qty
C1	1uF	1
C2	33pF	1
C3	150pF	1
C4	4n7	1
C5	1nF	1
C6	100uF	1
C7	22uF	1
C8, C9, C101, C102, C103, C104, C105, C106	10uF	8
D1	LED	1
DC1, DC2, DC3, DC4, DC5, DC6, DC7, DC8, DC9, DC10, DC11, DC12, DC13, DC14, DC14_12, DC15, DC16, DC17, DC18, DC19, DC20, DC21, DC22, DC23, DC24	10nF	25
LK1	READY	1
LK2	SW_SPDT	1
LK3	SPARE 1	1
LK4	SPARE 2	1
LKB2	Conn_02x10_Counter_Clockwise	1
P4, P5, P8, P9, TP1, TP2, TP3, TP5, TP6, TP8, TP9, TP10, TP12	Test Point	13
PL1	Conn_02x17_Odd_Even	1
R1	100K	1
R2	5K6	1
R3, R10, R26, R27	4K7	4
R4, R16, R17, R18, R19, R20, R22, R23, R24, R25	10K	10
R5	22K	1
R6, R7	1M	2
R8	15K	1
R9	1K	1
R11, R12, R13, R14, R15	150	5
R21	10k	1
R28	220K	1
R29	150K	1
R30	1K0	1
R31	470	1
RV1	50K	1
SW1	SW_DIP_x08	1
U1	74LS245	1
U2	74LS138	1
U3	74LS10	1
U4, U17	74LS04	2

Reference	Value	Qty
U5	74LS365	1
U6	74LS163	1
U7, U8	74LS257	2
U9, U10	74LS32	2
U11	74LS02	1
U12	74LS195	1
U13	74LS273	1
U14	WD1793	1
U15	4013B	1
U16	7407	1
U18, U24	74LS123	2
U19	7438	1
U20	4046B	1
U21	4016	1
U22	74LS14	1
U23	7406	1

3 Construction

3.1 Before you start construction

Inspect the PCB for any visible signs of damage

Plug the board into an 80-BUS and power it up.

- Verify no latent shorts exist
- Verify correct voltages on power rails

Select your components:

- Turned pin sockets are recommended due to robustness and reliability
- Tantalum capacitors can be temperamental. Make sure they are inserted with the correct polarity, are of good quality and are overrated voltage wise.

U15, U20 & U21 are static sensitive. Handling precautions need to be observed.

3.2 Order of construction

The recommended order of construction is:

- Resistors
- Sockets
- Decoupling capacitors
- Tantalum capacitors
- Switches
- LED
- Wire header
- Insert IC’s

4 Functionality

4.1 Links

The board contains 4 links, which can be implemented as switches or hard wired with links depending on the user's preference.

Link (Default) Usage	Link (Default) Usage
LK1 Open Ready	LK1 Open Ready
LK2 A -> C	Side Select. Set A -> C for 1793 Side Select
LK3 Open	Spare – Port x4 Bit 5
LK4 Open	Spare – Port x4 Bit 7

4.2 SW1 – Base Port Select

This allows the board to be mapped to ports 0x20, 0x40, 0x60, 0x80, 0xA0, 0xC0, 0xE0. The default is 0xE0. User options are to either hard wire a link, use a link block or use an 8-way DIL switch

Connect Pins Port Base Address	Connect Pins Port Base Address
1 to 16	N/A
2 to 15	0x20
3 to 14	0x40
4 to 13	0x60
5 to 12	0x80
6 to 11	0xA0
7 to 10	0xC0
8 to 9 (Default)	0xE0

4.3 LKB2 – Configuration Switch

This is implemented as a 10-way DIL switch. The switch settings are as follows:

Switch	Usage	2MHz Default	4MHz Default
SW1	Set write pre-compensation	Off	Off
SW2	Set write pre-compensation	Off	On
SW3	Set write pre-compensation	Off	Off
SW4	Clock divide by 2 (For 2MHz systems)	On	Off
SW5	Clock divide by 4 (For 4MHz systems)	Off	On
SW6	SW6 Clock divide by 4 (For 2MHz systems),	On	Off
SW7	Clock divide by 8 (For 4MHz systems), VCO=500KHz	Off	On
SW8	Select single /. double density	On	On
SW9	Disable / enable track 43 pre-compensation	On	On
SW0	Disable write pre-compensation	On	Off

Notes on write pre-compensation:

For 2MHz systems, SW1 is set to on, giving 500ns pre-compensation

For 4MHz systems, SW2 is set to one giving 250ns pre-compensation OR SW3 is set to on giving 500ns pre-compensation

Only one of SW1, SW2 or SW3 should be selected at any time. If all are deselected then SW0 must be selected (disables write pre-compensation)

4.4 Ports

The board uses six ports, selected from the base port (Default 0xE0). These are:

Port	Read	Write
0xE0	1793 Status	1793 Command register
0xE1	1793 Track	1793 Track register
0xE2	1793 Sector	1793 Sector Register
0xE3	1793 Data	1793 Data register
0xE4	Drive	Drive select control
0xE5	INTRQ / DRQ status	N/A

4.4.1 For Port 0xE4

Bit	Read	Write
0	Drive select 0	Drive select 0
1	Drive select 1	Drive select 1
2	Drive select 2	Drive select 2
3	Drive select 3	Drive select 3
4	Side select	Side select (When LK2 A->C)
5	LK3	Motor 0=off, 1=on
6	Density (0=low, 1 = high)	Density (0=low, 1 = high)
7	LK4	N/A

4.4.2 For Port 0xE5

Bit	Read	Write
0	1793 INTRQ	N/A
1	0=Ready, 1=Not Ready	N/A
2	N/A	N/A
3	N/A	N/A
4	N/A	N/A
5	N/A	N/A
6	N/A	N/A
7	1793 DRQ	N/A

5 Configuration

Once the board has been built and configured via links options and switches, the VCO center frequency needs to be set. This can be done in two ways:

5.1 Without A Scope

The following steps are required to perform the configuration:

1. Ensure the board is disconnected from any drives (Disconnect PL1)
2. Turn the potentiometer at VR1 anti-clockwise until the LED illuminates
3. Turn the potentiometer at VR1 a quarter turn clockwise

5.2 With A Scope

The following steps are required to perform the configuration:

1. Ensure the board is disconnected from any drives (Disconnect PL1)
2. Observe the signal at U20 Pin 3
3. Turn the potentiometer until a 500KHz square wave is observed

6 Notes on Components

All the components used have been selected at time of design to be readily available via eBay and other sources.

6.1 LKB2 Configuration Switch

It is recommended to fit a 20-pin socket and use a 10-way DIL switch

6.2 SW1 Decode Header

The socket at SW1 is recommended to be of the turned pin variety so as to allow easier insertion of the header. The default header is a 16-way DIL header.
An alternative is to use Single-In-Line (SIL) Turned Pin Socket 0.1 Inch Pitch strips which are readily available instead of a header. These are then snipped down to the required number of pins before being inserted into the socket and the desired wire links being made. An 8-way DIL switch may also be used if one is available.
A second alternative is to insert and solder a wire link between the required PCB pads if the ability to change the base address is not required.

6.3 C4

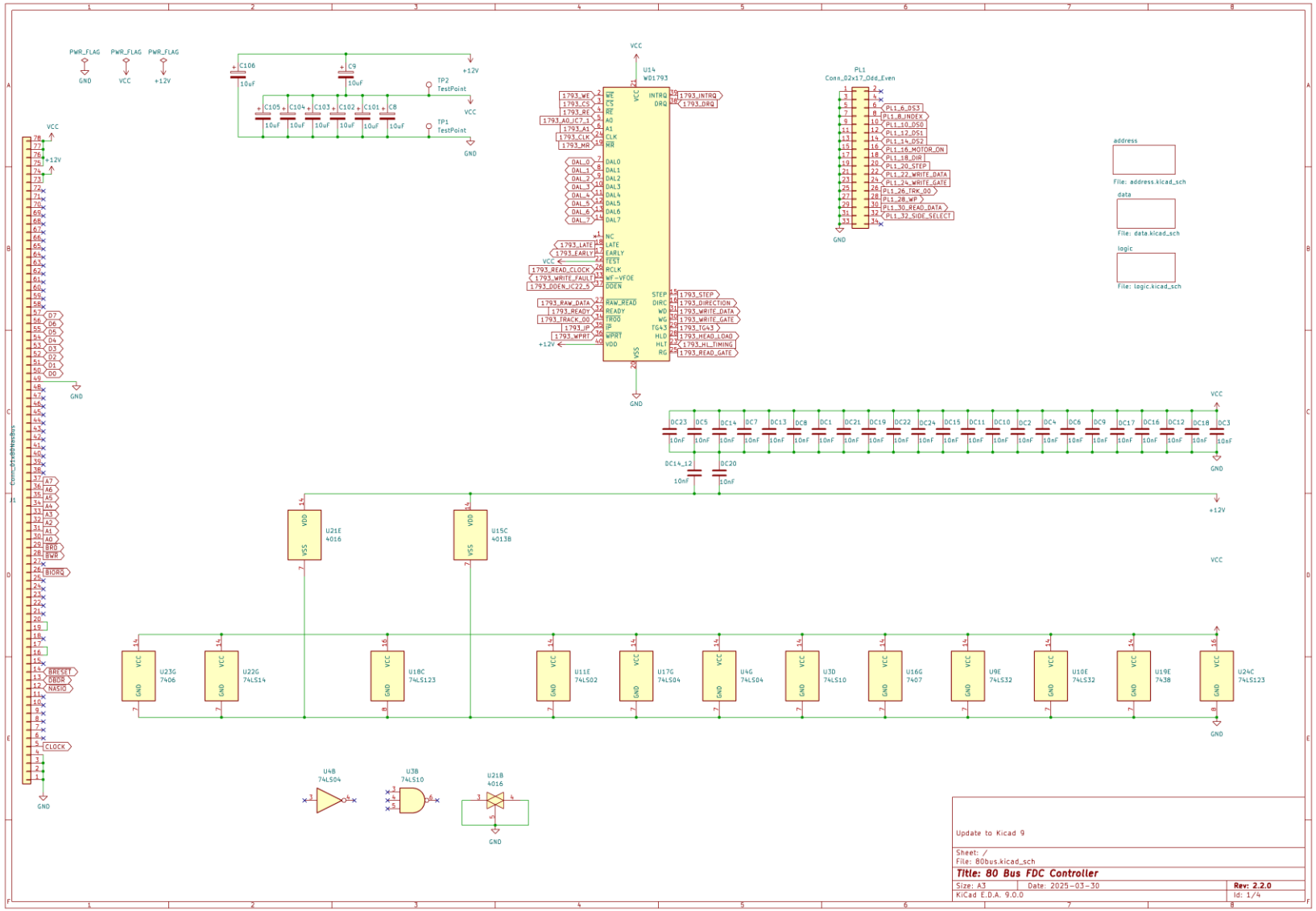
This capacitor is of the film type in the original design. I have used an Axial Polypropylene Film Capacitor here without issue. Other types (e.g. ceramic) may work but that configuration is untested.

6.4 IC's U15, U20, U21

These parts are static sensitive. Handling precautions need to be observed.

6.5 1793 FDC Controller

A 1797 controller, in theory, may be substituted, but this configuration is untested. To use the 1797 Side-Select feature, set LK3 to B -> C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WD1793
PL1
Conn_02x17_Odd_Even
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data
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logic
File: logic.kicad_sch
Update to Kicad 9
Sheet: /
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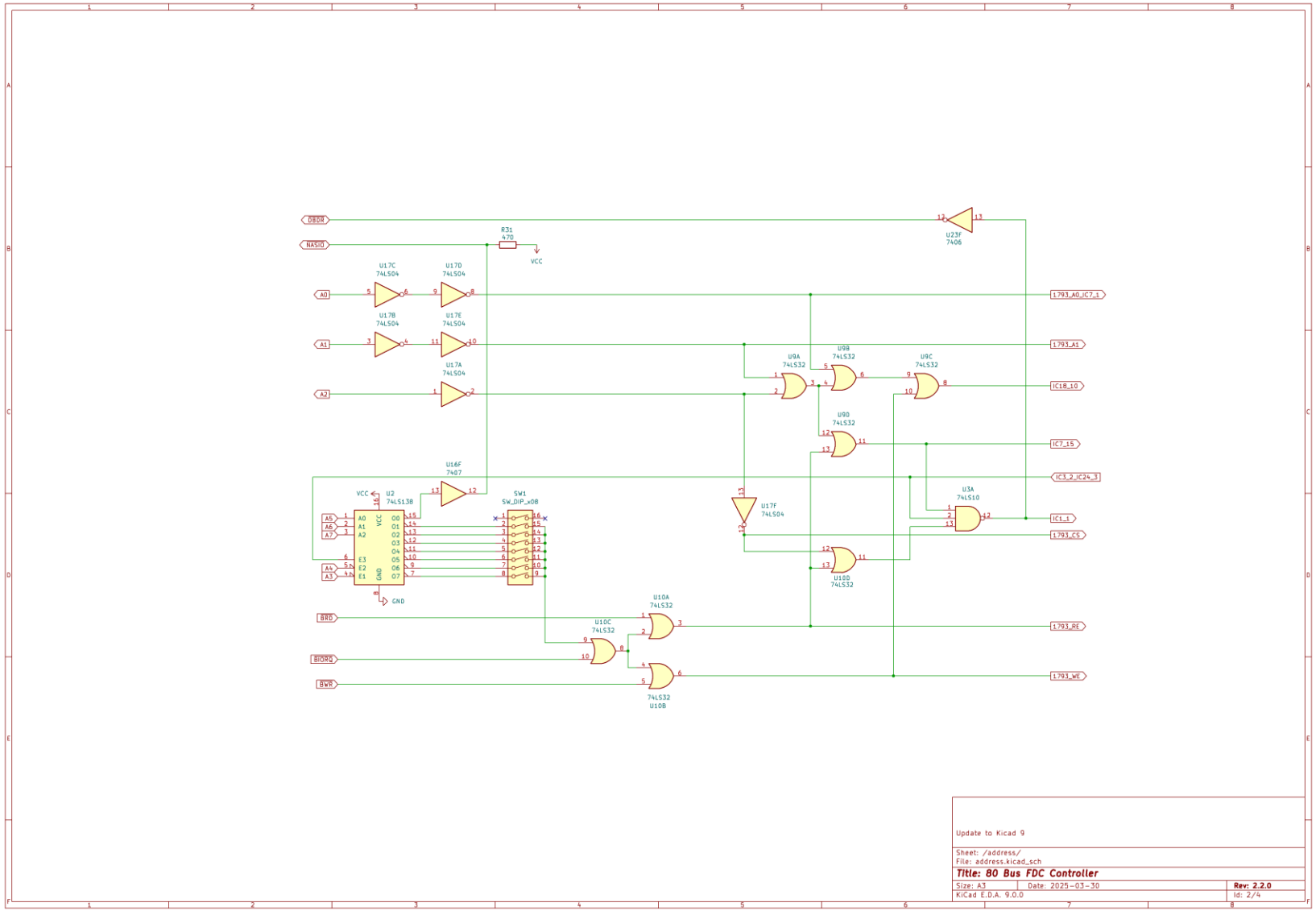
Title: 80 Bus FDC Controller
Size: A3
Date: 2025-03-30
Rev: 2.2.0
KiCad E.D.A. 9.0.0
Id: 1/4


DIRIN
NASIO
R31
470
VCC
U17C
74LS04
U17D
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A0
U17B
74LS04
U17E
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A1
U17A
74LS04
A2
U16F
7407
U2
74LS138
SW1
SW_DIP_x08
A5
A6
A7
A4
A3
GND
U23F
7406
1793_A0_IC7_1
1793_A1
IC18_10
IC7_15
IC3_2_IC24_3
IC1_1
1793_CS
U9A
74LS32
U9B
74LS32
U9C
74LS32
U9D
74LS32
U17F
74LS04
U3A
74LS10
U10D
74LS32
U10A
74LS32
U10C
74LS32
U10B
74LS32
BRD
BIORQ
BWR
1793_RE
1793_WE
Update to Kicad 9
Sheet: /address/
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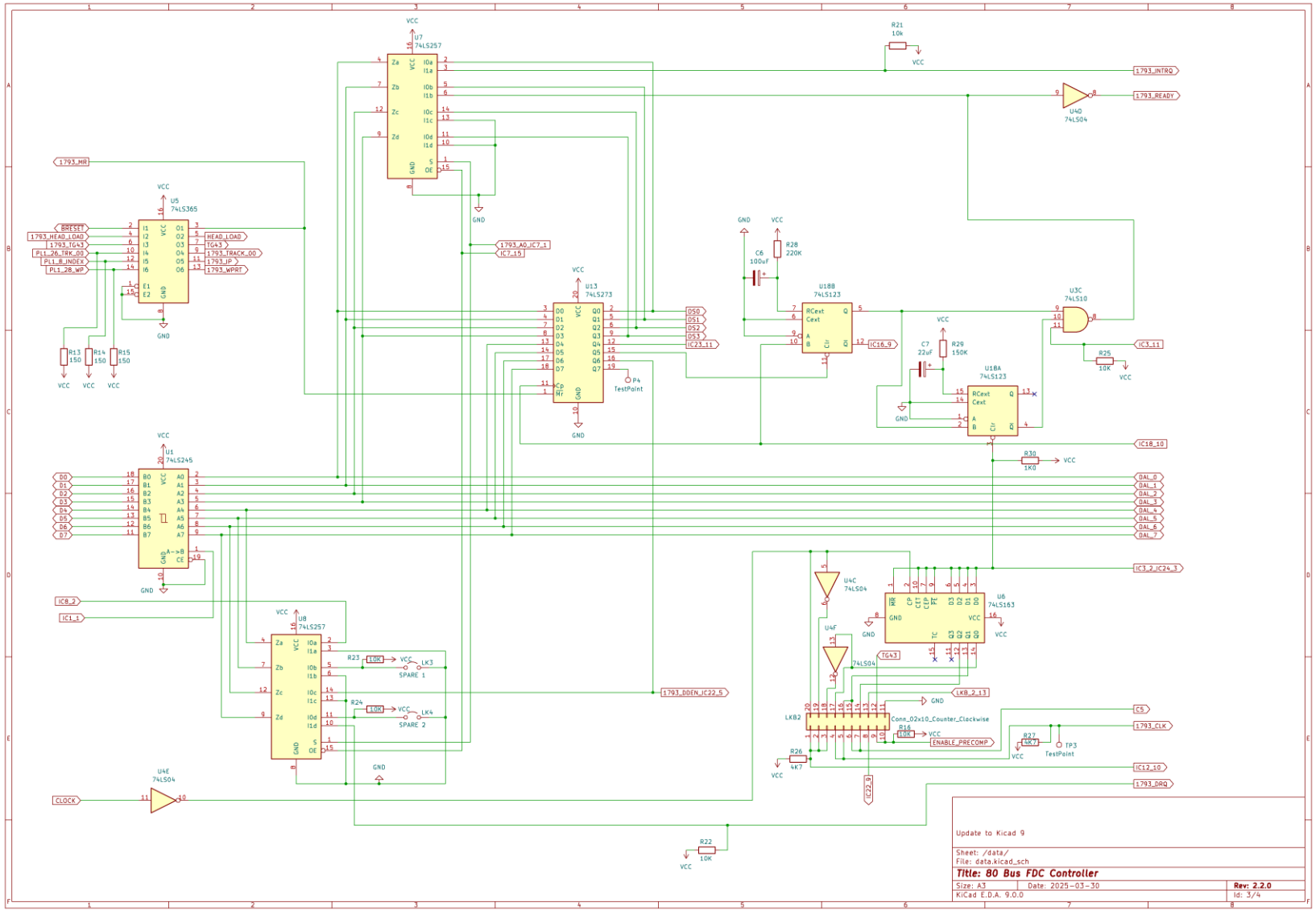
Size: A3
Date: 2025-03-30
Rev: 2.2.0
KiCad E.D.A. 9.0.0
Id: 2/4


Update to Kicad 9
Sheet: /data/
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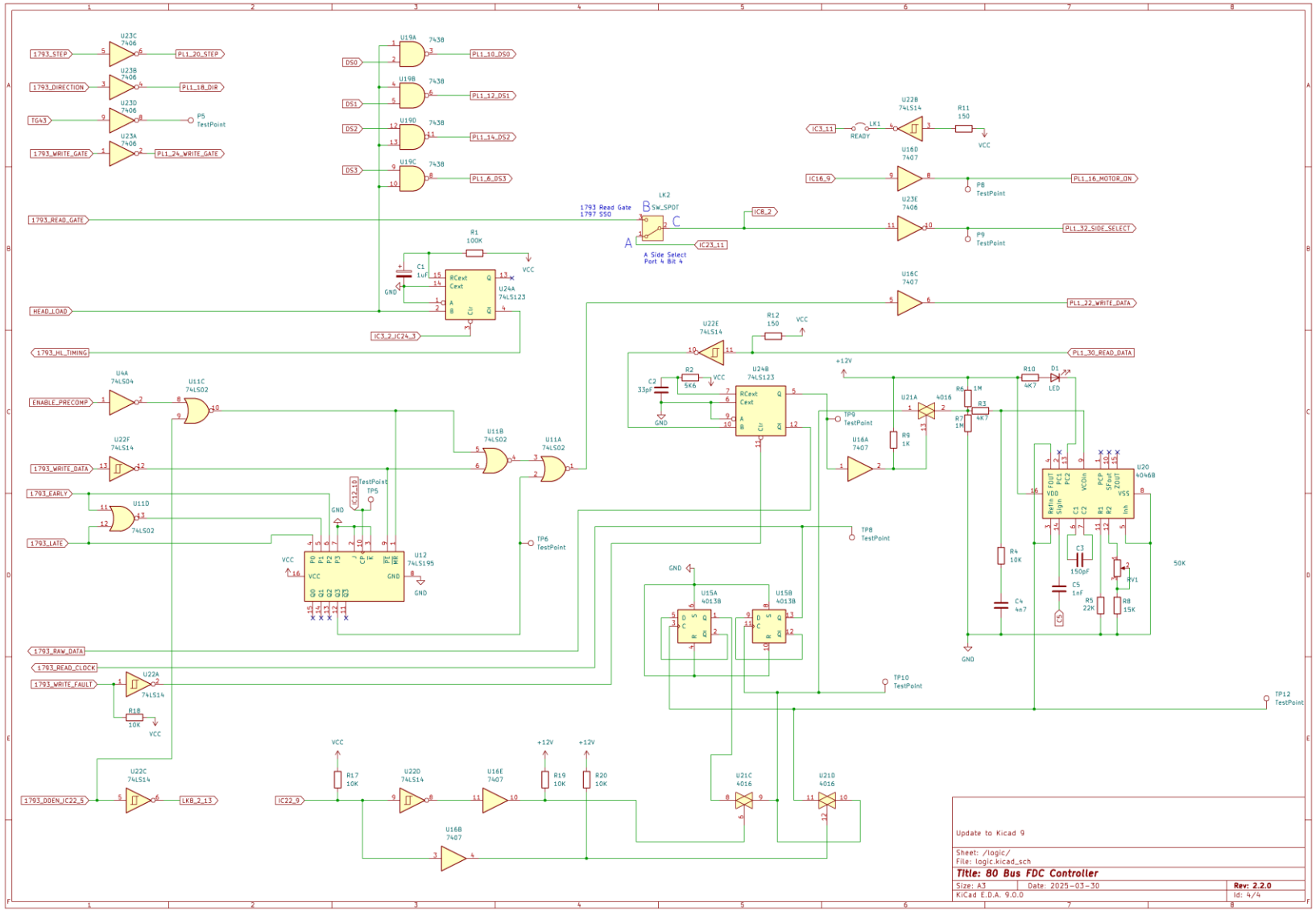
Rev: 2.2.0
KiCad E.D.A. 9.0.0
Id: 3/4


1793_STEP
1793_DIRECTION
TG43
1793_WRITE_GATE
PL1_20_STEP
PL1_18_DIR
P5
PL1_24_WRITE_GATE
DS0
DS1
DS2
DS3
PL1_10_DS0
PL1_12_DS1
PL1_14_DS2
PL1_8_DS3
1793_READ_GATE
1793 Read Gate
1797 SSO
LK2
SW_SPDT
A Side Select
Port 4 Bit 4
IC8_2
IC23_11
IC3_11
READY
LK1
IC16_9
P8
PL1_16_MOTOR_ON
P9
PL1_32_SIDE_SELECT
HEAD_LOAD
1793_HL_TIMING
IC3_2_IC24_3
PL1_22_WRITE_DATA
PL1_30_READ_DATA
ENABLE_PRECOMP
1793_WRITE_DATA
1793_EARLY
1793_LATE
TP5
TP6
TP8
TP9
TP10
TP12
1793_RAW_DATA
1793_READ_CLOCK
1793_WRITE_FAULT
1793_DDEN_IC22_5
LKB_2_13
IC22_9
IC12_10
VCC
GND
+12V
50K
Update to Kicad 9
Sheet: /logic/
File: logic.kicad_sch
Title: 80 Bus FDC Controller
Size: A3
Date: 2025-03-30
Rev: 2.2.0
KiCad E.D.A. 9.0.0
Id: 4/4

7 Errata

Initial release boards (1.2.0) have an incorrect ground line for C1.

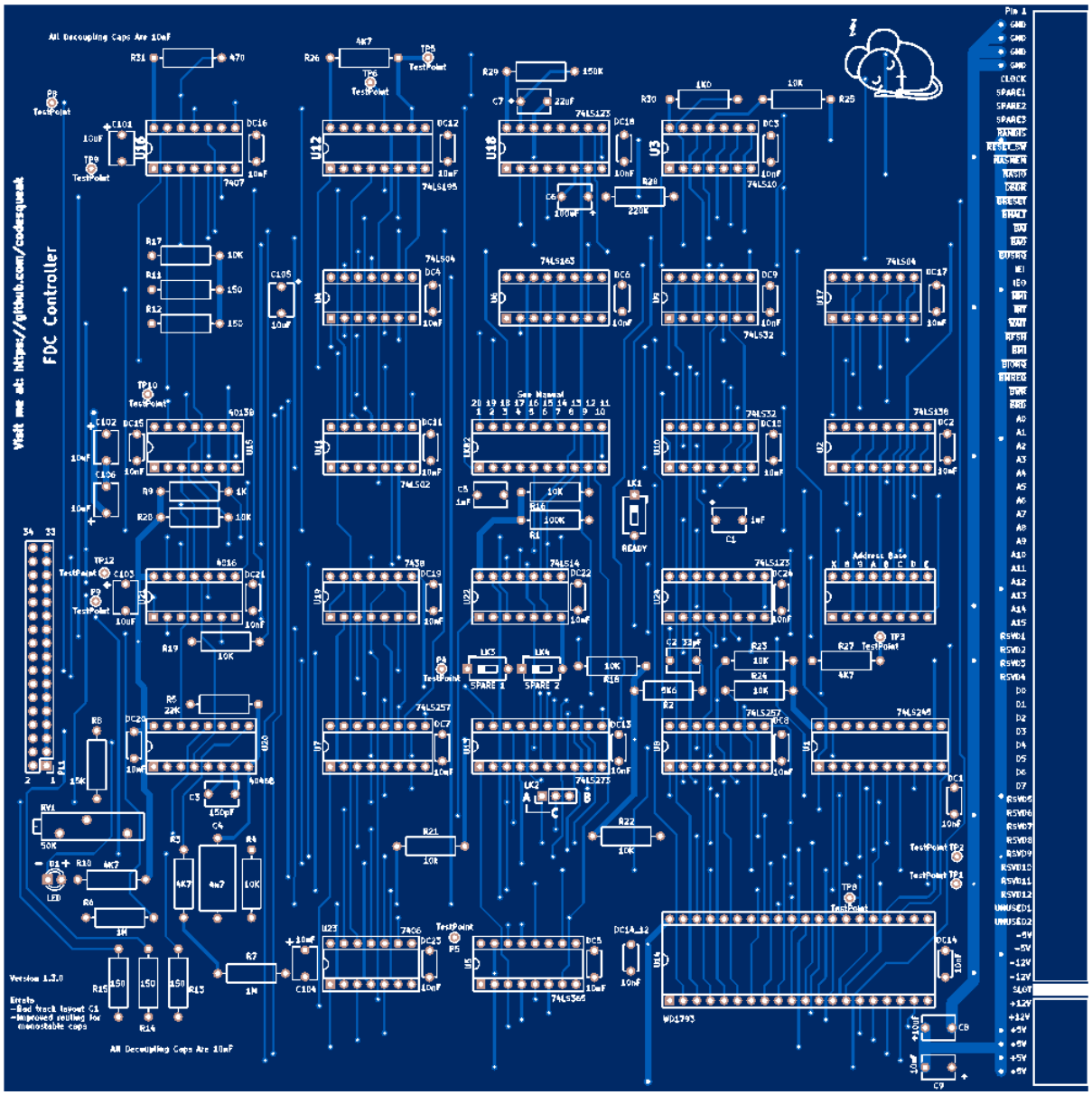
The capacitor at location C1 should be:

1. Mounted on the back of the board
2. The positive leg should go through the existing positive through plated hole for the component
3. The negative leg should go to pin 14 of U24

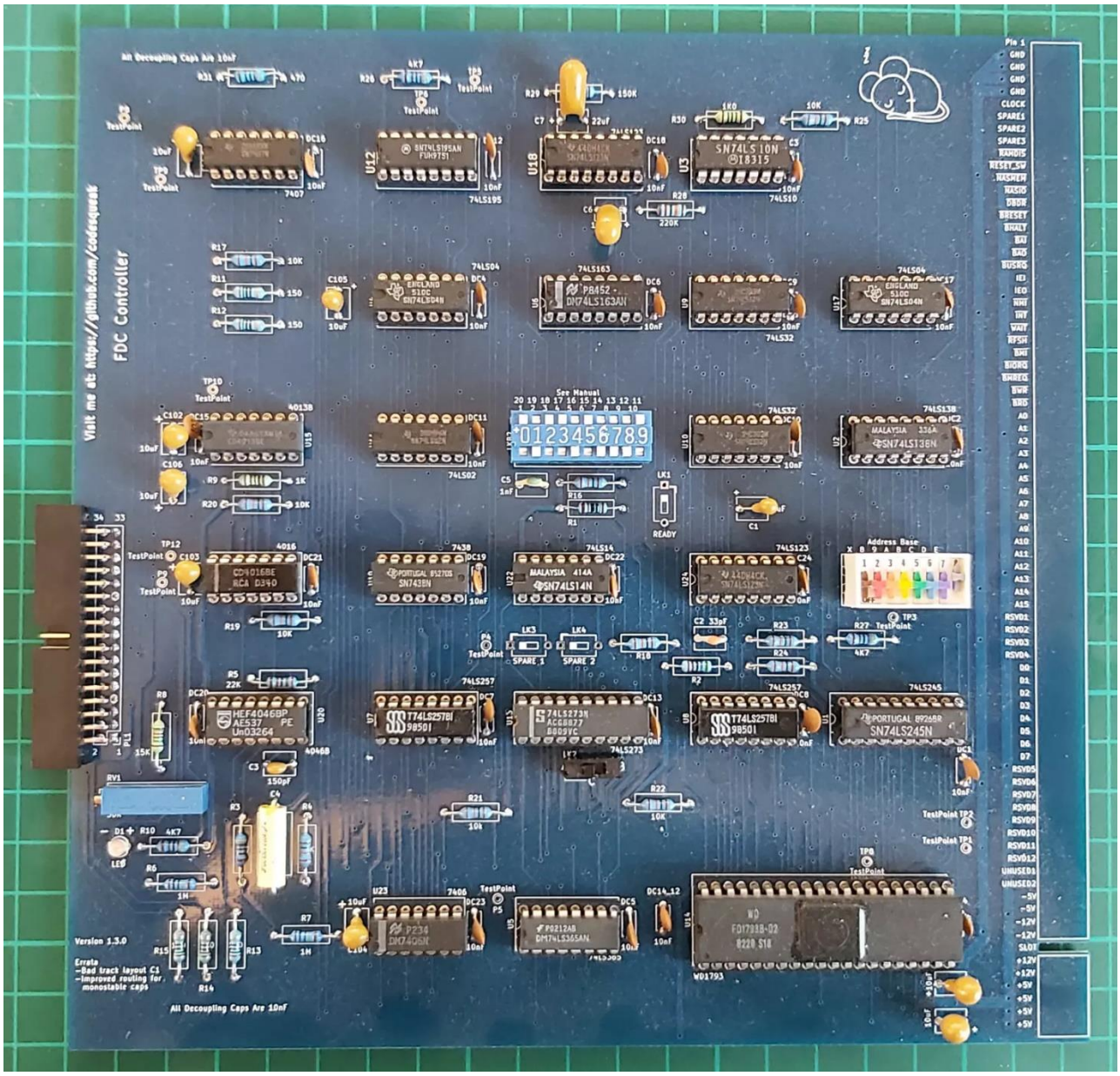
This modification fixes an issue with the unstable operation of the Head Load monostable

8 Reference Images

8.1 PCB



8.2 Built


FDC Controller
Visit me at: https://github.com/codesqueek
Version 1.3.0
Errata
-Bad track layout C1
-improved routing for monostable caps
All Decoupling Caps Are 10nF
WD1793