NAS-GEM-80 FDC CARD

Instruction Manual & Functional Description

Contents

1 Introduction

This card has been designed to be a form, fit and function replacement for the Nascom Floppy Disk Controller, which is proving to be a very difficult item to source for the Nascom / Gemini retro community.

The card has been tested against original Teac FD-50E/F drives without observed issues under NAS-DOS 1.4

Further testing with CP/M and PolyDos is planned

Note: The card is designed to handle 5.25-inch drives. Support for 8-inch drives has been removed (***Did anyone ever use this?***)

2 Components

Reference	Quantity	Value
Capacitors		
C1 (Tantalum)	1	1uF
C2	1	33pF
C3	1	150pF
C4 (Polyester Film)	1	4n7
C5	1	1nF
C6 (Tantalum)	1	100uF
C7 (Tantalum)	1	22uF
C8, C9, C101 - C106 (Tantalum)	8	10uF
DC1 - DC24 – Decoupling caps	25	10nF
Resistors	**Quantity**	**Value**
R1	1	100K
R2	1	5K6
R3	1	4K7
R4	1	10K
R5	1	22K
R6	1	1M
R7	1	1M
R8	1	15K
R9	1	1K
R10	1	4K7
R11	1	150
R12	1	150
R13	1	150
R14	1	150
R15	1	150
R16	1	10K
R17	1	10K
R18	1	10K
R19	1	10K
R20	1	10K
R21	1	10k
R22	1	10K
R23	1	10K
R24	1	10K
R25	1	10K
R26	1	4K7

R27	1	4K7
R28	1	220K
R29	1	150K
R30	1	1K0
R31	1	470
IC's	**Quantity**	**Value**
U1 – DIP 20	1	74LS245
U2 – DIP 16	1	74LS138
U3 – DIP 14	1	74LS10
U4 – DIP 14	1	74LS04
U5 – DIP 16	1	74LS365
U6 – DIP 16	1	74LS163
U7 – DIP 16	1	74LS257
U8 – DIP 16	1	74LS257
U9 – DIP 14	1	74LS32
U10 – DIP 14	1	74LS32
U11 – DIP 14	1	74LS02
U12 – DIP 16	1	74LS195
U13 – DIP 20	1	74LS273
U14 – DIP 40	1	WD1793
U15 – DIP 14 (Static sensitive)	1	4013B
U16 – DIP 14	1	7407
U17 – DIP 14	1	74LS04
U18 – DIP 16	1	74LS123
U19 – DIP 14	1	7438
U20 – DIP 16 (Static sensitive)	1	4046B
U21 – DIP 14 (Static sensitive)	1	4016
U22 – DIP 14	1	74LS14
U23 – DIP 14	1	7406
U24 – DIP 16	1	74LS123
Other Items	**Quantity**	**Value**
D1 – LED	1	LED 3mm
LK1, LK3, LK4 (optional)	3	Switch SPST Slide, 6.7x4.1mm, W7.62mm, P2.54mm
LK2	1	Switch DPDT, 3 pins, P2.54mm
RV1	1	50K, Cermet type potentiometer
SW1	1	Switch or header, x8, W7.62mm_Socket
LKB2	1	Switch SW_DIP_x10, W7.62mm_Socket
PL1	1	Connector, Header 2x17, P2.54mm

3 Construction

3.1 Before you start construction

Inspect the PCB for any visible signs of damage

Plug the board into an 80-BUS and power it up.

- Verify no latent shorts exist
- Verify correct voltages on power rails

Select your components:

- Turned pin sockets are recommended due to robustness and reliability
- Tantalum capacitors can be temperamental. Make sure they are inserted with the correct polarity, are of good quality and are overrated voltage wise.

U15, U20 & U21 are static sensitive. Handling precautions need to be observed.

3.2 Order of construction

The recommended order of construction is:

- Resistors
- Sockets
- Decoupling capacitors
- Tantalum capacitors
- Switches
- LED
- Wire header
- Insert IC’s

4 Functionality

4.1 Links

The board contains 4 links, which can be implemented as switches or hard wired with links depending on the user's preference.

Link (Default)	**Usage**
LK1 Open	Ready
LK2 A -> C	Side Select. Set A -> C for 1793 Side Select
LK3 Open	Spare – Port x4 Bit 5
LK4 Open	Spate – Port x4 Bit 7

4.2 SW1 – Base Port Select

This allows the board to be mapped to ports 0x20, 0x40, 0x60, 0x80, 0xA0, 0xC0, 0xE0. The default is 0xE0. User options are to either hard wire a link, use a link block or use an 8-way DIL switch.

Connect Pins	**Port Base Address**
1 to 16	N/A
2 to 15	0x20
3 to 14	0x40
4 to 13	0x60
5 to 12	0x80
6 to 11	0xA0
7 to 10	0xC0
8 to 9 (Default)	0xE0

4.3 LKB2 – Configuration Switch

This is implemented as a 10-way DIL switch. The switch settings are as follows:

Switch	Usage	2MHz Default	4MHz Default
1	Set write pre-compensation	Off	Off
2	Only one of SW1, SW2 or SW3 should be selected	Off	On
3	…	Off	Off
4	Clock divide by 2 (For 2MHz systems)	On	Off
5	Clock divide by 4 (For 4MHz systems)	Off	On
6	Clock divide by 4 (For 2MHz systems), VCO=500KHz	On	Off
7	Clock divide by 8 (For 4MHz systems), VCO=500KHz	Off	On
8	Select single /. double density	On	On
9	Disable / enable track 43 pre-compensation	On	On
0	Disable write pre-compensation	On	Off

4.4 Ports

The board uses six ports, selected from the base port (Default 0xE0). These are:

Port	Read	Write
0xE0	1793 Status register	1793 Command register
0xE1	1793 Track register	1793 Track register
0xE2	1793 Sector register	1793 Sector Register
0xE3	1793 Data register	1793 Data register
0xE4	Drive selection	Drive select control
0xE5	INTRQ / DRQ status	N/A

4.4.1 For port 0xE4

Bit	Read	Write
0	Drive select 0	Drive select 0
1	Drive select 1	Drive select 1
2	Drive select 2	Drive select 2
3	Drive select 3	Drive select 3
4	Side select	Side select (When LK2 A->C)
5	LK3	Motor 0=off, 1=on
6	Density (0=low, 1 = high)	Density (0=low, 1 = high)
7	LK4	N/A

4.4.2 For port 0xE5

Bit	Read	Write
0	1793 INTRQ	N/A
1	0=Ready, 1=Not Ready	N/A
2	N/A	N/A
3	N/A	N/A
4	N/A	N/A
5	N/A	N/A
6	N/A	N/A
7	1793 DRQ	N/A

5 Configuration

Once the board has been built and configured via links options and switches, the VCO center frequency needs to be set. This can be done in two ways:

5.1 Without A Scope

The following steps are required to perform the configuration:

1. Ensure the board is disconnected from any drives (Disconnect PL1)
2. Turn the potentiometer at VR1 anti-clockwise until the LED illuminates
3. Turn the potentiometer at VR1 a quarter turn clockwise

5.2 With A Scope

The following steps are required to perform the configuration:

1. Ensure the board is disconnected from any drives (Disconnect PL1)
2. Observe the signal at U20 Pin 3
3. Turn the potentiometer until a 500KHz square wave is observed

6 Notes on Components

All the components used have been selected at time of design to be readily available via eBay and other sources.

6.1 LKB2 Configuration Switch

It is recommended to fit a 20-pin socket and use a 10-way DIL switch

6.2 SW1 Decode Header

The socket at SW1 is recommended to be of the turned pin variety so as to allow easier insertion of the header. The default header is a 16-way DIL header.

An alternative is to use Single-In-Line (SIL) Turned Pin Socket 0.1 Inch Pitch strips which are readily available instead of a header. These are then snipped down to the desired length before being inserted into the socket and the desired wire links being made.

An 8-way DIL switch may also be used if one is available.

6.3 C4

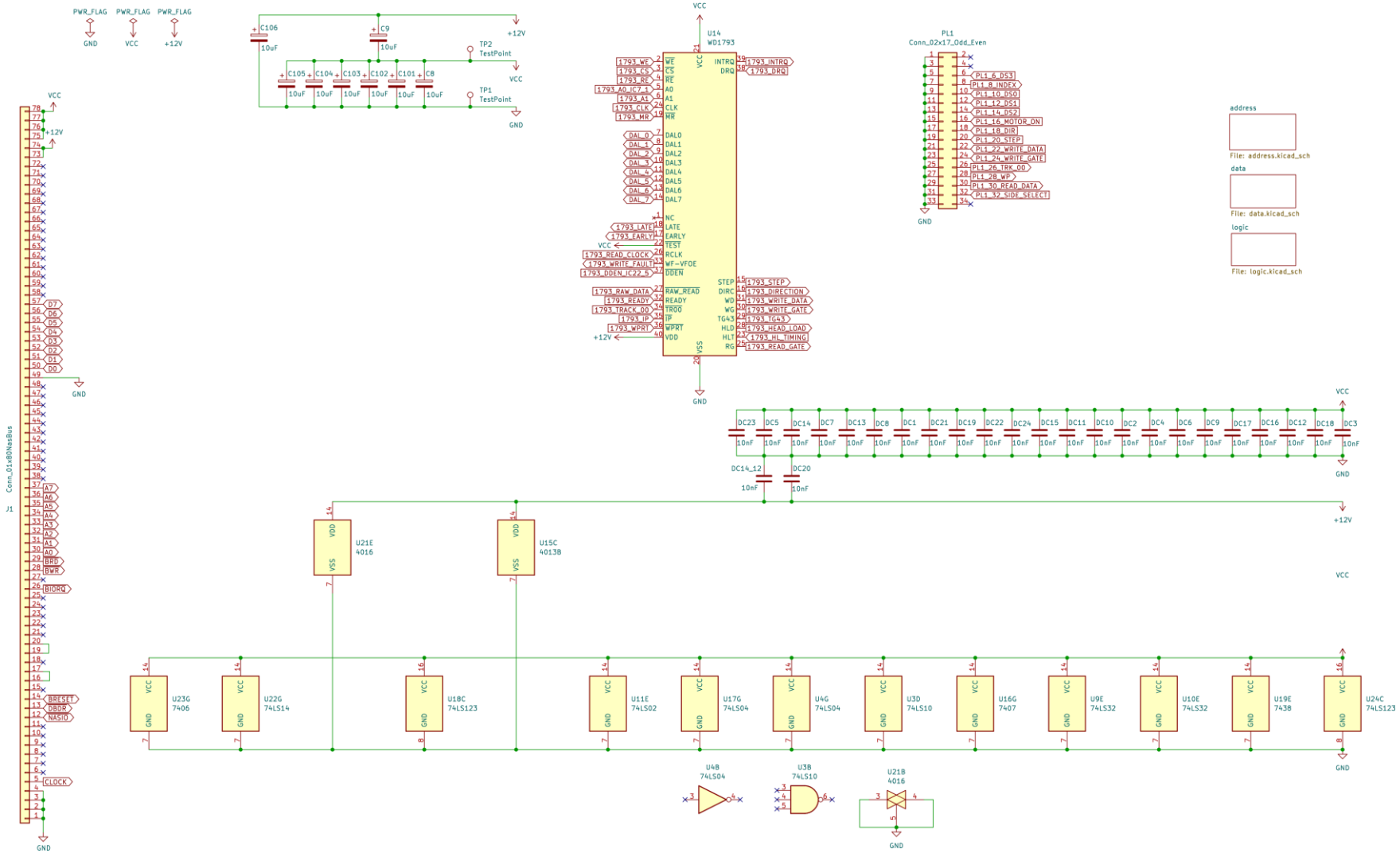
This capacitor is of the film type in the original design. I have used an ***Axial Polypropylene Film Capacitor*** here without issue. Other types (e.g. ceramic) may work but that configuration is untested.

6.4 IC's U15, U20, U21

These parts are static sensitive. Handling precautions need to be observed.

6.5 1793 FDC Controller

A 1797 controller, in theory, may be substituted, but that configuration is untested. To use the 1797 Side-Select feature, set LK3 to B -> C


PWR_FLAG
GND
VCC
+12V
C106
10uF
C9
TP2
TestPoint
TP1
C105
C104
C103
C102
C101
C8
U14
WD1793
PL1
Conn_02x17_Odd_Even
address
File: address.kicad_sch
data
File: data.kicad_sch
logic
File: logic.kicad_sch
J1
Conn_01x80NasBus
U21E
4016
U15C
4013B
U23G
7406
U22G
74LS14
U18C
74LS123
U11E
74LS02
U17G
74LS04
U4G
74LS04
U3D
74LS10
U16G
7407
U9E
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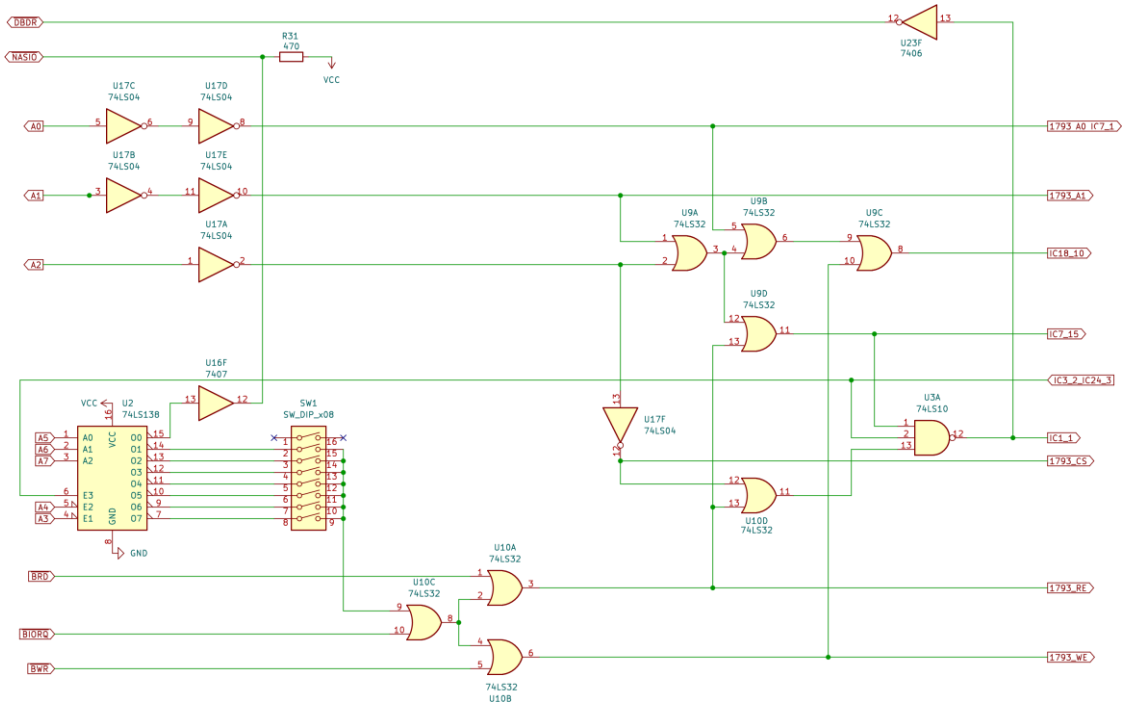
74LS04
U3B
74LS10
U21B
4016


DBDR
NASIO
R31
470
VCC
U17C
74LS04
U17D
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A0
U17B
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U17E
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A1
U17A
74LS04
A2
U16F
7407
U23F
7406
1793_A0_IC7_1
1793_A1
IC18_10
IC7_15
IC3_2_IC24_3
IC1_1
1793_CS
U9A
74LS32
U9B
74LS32
U9C
74LS32
U9D
74LS32
U17F
74LS04
U3A
74LS10
U10D
74LS32
U2
74LS138
SW1
SW_DIP_x08
A5
A6
A7
A4
A3
GND
BRD
BIORQ
BWR
U10A
74LS32
U10C
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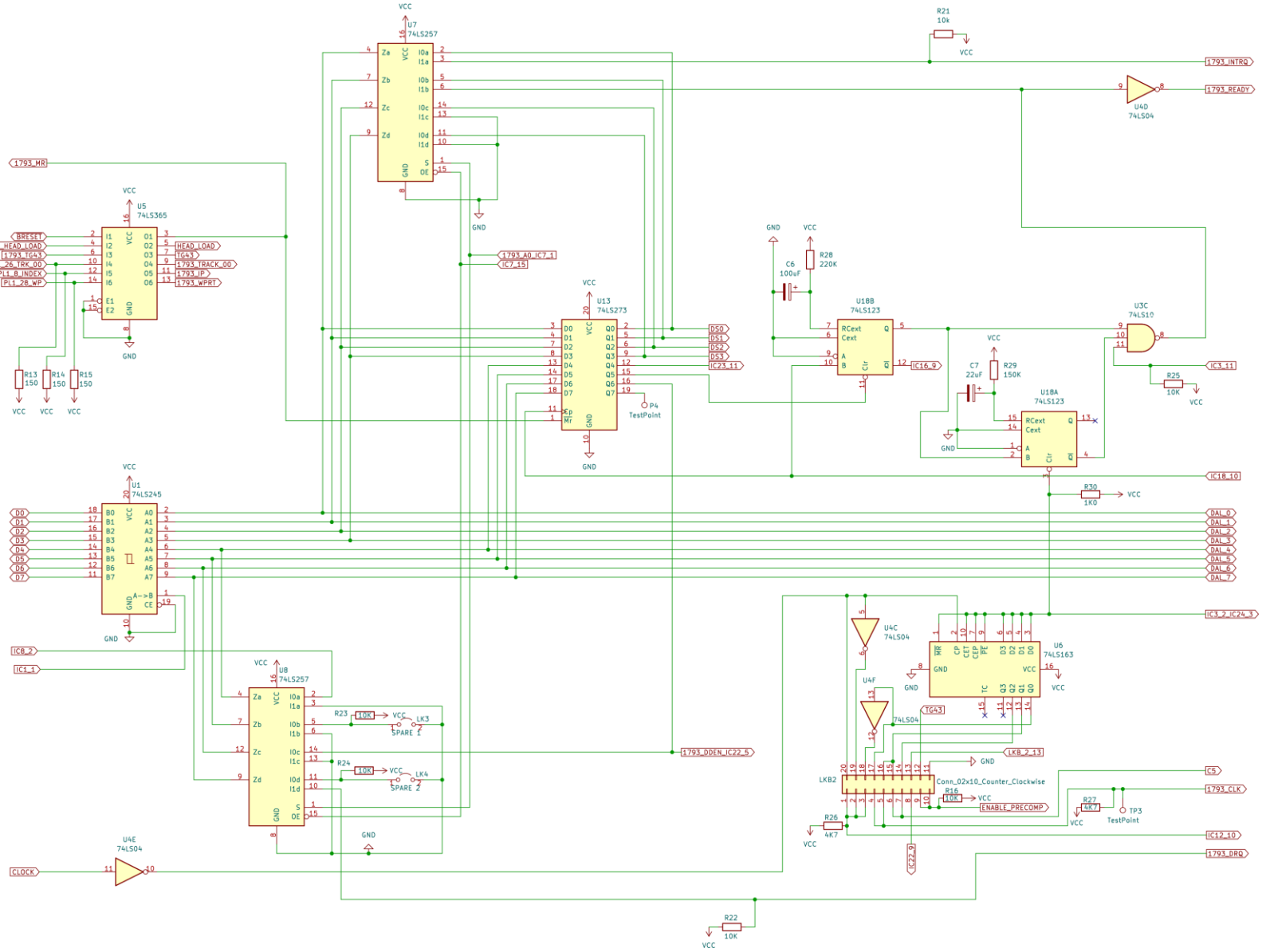
U10B
74LS32
1793_RE
1793_WE


U7
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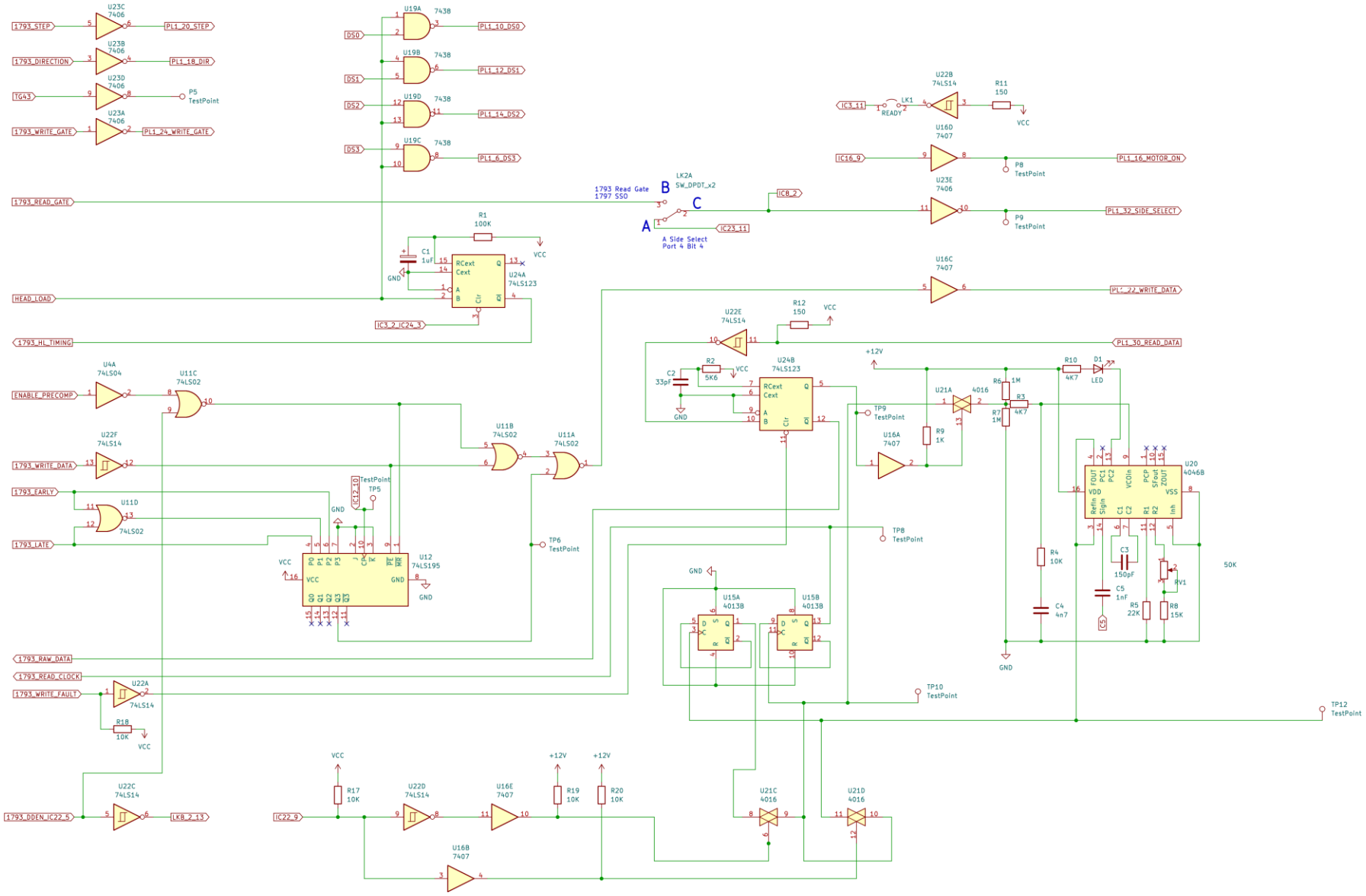
U5
74LS365
U13
74LS273
U1
74LS245
U8
74LS257
U18B
74LS123
U18A
74LS123
U3C
74LS10
U4D
74LS04
U4C
74LS04
U4F
74LS04
U4E
74LS04
U6
74LS163
R21
10k
R28
220K
C6
100uF
C7
22uF
R29
150K
R30
1K0
R25
10K
R13
150
R14
150
R15
150
R23
10K
R24
10K
R16
10K
R26
4K7
R27
4K7
R22
10K
LK3
SPARE 1
LK4
SPARE 2
LKB2
Conn_02x10_Counter_Clockwise
P4
TestPoint
TP3
TestPoint
1793_MR
1793_INTRQ
1793_READY
1793_A0_IC7_1
IC7_15
DS0
DS1
DS2
DS3
IC23_11
IC16_9
IC3_11
IC18_10
IC3_2_IC24_3
D0
D1
D2
D3
D4
D5
D6
D7
DAL_0
DAL_1
DAL_2
DAL_3
DAL_4
DAL_5
DAL_6
DAL_7
BRESET
1793_HEAD_LOAD
1793_TG43
PL1_26_TRK_00
PL1_8_INDEX
PL1_28_WP
HEAD_LOAD
TG43
1793_TRACK_00
1793_IP
1793_WPRT
IC8_7
IC1_1
1793_DDEN_IC22_5
TG43
LKB_2_13
ENABLE_PRECOMP
C5
1793_CLK
IC12_10
1793_DRQ
IC22_9
CLOCK
VCC
GND


1793_STEP
PL1_20_STEP
1793_DIRECTION
PL1_18_DIR
TG43
P5
TestPoint
1793_WRITE_GATE
PL1_24_WRITE_GATE
DS0
PL1_10_DS0
DS1
PL1_12_DS1
DS2
PL1_14_DS2
DS3
PL1_6_DS3
1793_READ_GATE
1793 Read Gate
1797 SSO
LK2A
SW_DPDT_x2
A Side Select
Port 4 Bit 4
IC23_11
IC8_2
PL1_32_SIDE_SELECT
P9
IC3_11
LK1
READY
VCC
IC16_9
PL1_16_MOTOR_ON
P8
HEAD_LOAD
IC3_2_IC24_3
1793_HL_TIMING
PL1_22_WRITE_DATA
PL1_30_READ_DATA
ENABLE_PRECOMP
1793_WRITE_DATA
1793_EARLY
1793_LATE
IC12_10
TP5
TP6
TP8
TP9
TP10
TP12
1793_RAW_DATA
1793_READ_CLOCK
1793_WRITE_FAULT
1793_DDEN_IC22_5
LKB_2_13
IC22_9
GND
+12V
50K
U4A
74LS04
U11C
74LS02
U22F
74LS14
U11D
U11B
U11A
U12
74LS195
U22A
U22C
U22D
U16E
7407
U16B
U16C
U16D
U16A
U22B
U22E
U19A
U19B
U19D
U19C
7438
U23C
U23B
U23D
U23A
7406
U24A
U24B
74LS123
U15A
U15B
4013B
U21A
U21C
U21D
4016
U20
4046B
R1
100K
C1
1uF
R2
5K6
C2
33pF
R3
4K7
R4
10K
R5
22K
R6
1M
R7
1M
R8
15K
R9
1K
R10
4K7
R11
150
R12
150
R17
10K
R18
10K
R19
10K
R20
10K
C3
150pF
C4
4n7
C5
1nF
RV1
D1
LED

7 Errata

Initial release boards (1.2.0) have an incorrect ground line for C1.

The capacitor at location C1 should be:

1. Mounted on the back of the board
2. The positive leg should go through the existing positive through plated hole for the component
3. The negative leg should go to pin 14 of U24

This modification fixes an issue with the unstable operation of the Head Load monostable

8 Reference Images

<Insert photo’s here>