Lecture-17
SSK

Simple parity check } - Addition
2D " "

Cycle redundancy check (CRC) - modulo-2 division

Remainder of division → CRC

Dividend → data stream
Divisor → pre-defined

- ≃98% error detection

CRC generator (at source)

← n bits

1 because this bit is 1 (MSB)

```
         11001
1101 ) 101101010[000]   → n-1 0's
       1101
        1100
        1101
         0011
         0000
          0110
          0000
           1101
           1101
           [000]  → co-incidentally it came 000.
```

ignore borrow

this with the remainder

∴ 101101010[001] ← the remainder

total msg ready for transmission

If it were 001, we exchange

How to choose this predefined divisor

- Receiver has CRC checker

chose using a polynomial

$x^3 + x + 1$ → divisor polynomial

$\underline{1} \cdot x^3 + \underline{0} \cdot x^2 + \underline{1} \cdot x + \underline{1}$

1011

[Restrictions] The divisor polynomial ~~exact~~ :-
1) Must not be divisible by x
2) Must be divisible by $(x+1)$.

Some divisor polynomials accepted worldwide :

CRC-12

CRC-16

CRC-CCITT

Checksum

Error detection method based on 1's arithmetic complement

n bits, n=16

11000011 0011 0011 $\boxed{\text{CHECKSUM}}$

11001100

11000011

11110110 → SUM

ignore carry from MSB

1 → $\boxed{00001001}$ → CHECKSUM

→ bitwise complement

11000011

11001100

00001001

11111111

if we add the message parts & checksum, we should get all 1's

- Better than simple and 2D parity check.
- But CRC provides the best performance.

Error correction

It would be better if reciever could correct erroneous messages after recieving.

Forward error correction (FEC) → Hamming code → for detecting single bit errors.

Burst error correction → not in syllabus

message bits ← m, r → redundancy bit

~~Total length = (m+r)~~

∴ total no of states = m+r+1

2^r ~~word~~ states must ~~have~~ enough to contain all of m+r+1 states.

∴ $2^r \geq m+r+1$

Scanned by CamScanner

~~$7+4+1 \leq 2^r$~~

For ex,

if $m = 7$

$r = 4$

so that

$m+r+1 = 12 \leq 2^4 = 16$

Redundancy bits are inserted at positions that are power of 2. (1, 2, 4, 8..)

r bits : r_1, r_2, r_4, r_8

$\therefore$ d d d r_8 d d d r_4 d r_2 r_1

$r_1 \rightarrow$ 1, 3, 5, 7, 9, 11

$r_2 \rightarrow$ 2, 3, 6, 7, 10, 11

$r_4 \rightarrow$ 4, 5, 6, 7

$r_8 \rightarrow$ 8, 9, 10, 11

$r_1 \rightarrow$ 1, 3, 5, 7, 9, 11

1+2, 1+4, 1+2+4, 1+8, 1+2+8 — no repetition

$r_2 \rightarrow$ 2, 3, 6, 7, 10, 11

2+1, 2+4, 2+4+1, 2+8, 2+8+1

- If the message is error-free, then all the redundancy bits will be 0s.

Generation

Ex- 1000101 $\rightarrow m = 7$, $\therefore r = 4$ so that $2^r \geq m+r+1$

1 0 0 r_8 0 1 0 r_4 1 r_2 r_1 $\Rightarrow$ 10010101110

($r_8 = 1$, $r_4 = 1$, $r_2 = 1$, $r_1 = 0$)

(1) not considering 1, 2, 4, 8 bits as we don't know them

$r_1 \rightarrow$ 3, 5, 7, 9, 11 $\Rightarrow$ 0 $\rightarrow$ Even nos. of 1s at positions 3, 5, 7, 9, 11 (total 2 1's) $\therefore$ even parity

$r_2 \rightarrow$ 3, 6, 7, 10, 11 $\Rightarrow$ 1

$r_4 \rightarrow$ 5, 6, 7 $\Rightarrow$ 1

$r_8 \rightarrow$ 9, 10, 11 $\Rightarrow$ 1

$\rightarrow$ odd ones are corresponding pos's.

erroneous bit → at posn 5

Detection

1 0 0 1 0 1 0 1 1 1 1 0 → actual msg

1 0 0 1 0 1 1 1 1 1 1 0 → erroneous msg

(I)

Here we will consider bits 1,2,4,8

$r_1 \rightarrow 1, 3, 5, 7, 9, 11 \Rightarrow 1 \rightarrow$ odd no. of 1s

$r_2 \rightarrow 0$

$r_4 \rightarrow 1$

$r_8 \rightarrow 0$

$$\underbrace{\begin{matrix} r_8 & r_4 & r_2 & r_1 \\ 0 & 1 & 0 & 1 \end{matrix}}_{5}$$

5 → Location of the erroneous bit