

Simple Parity check } - Addition
2D " " }

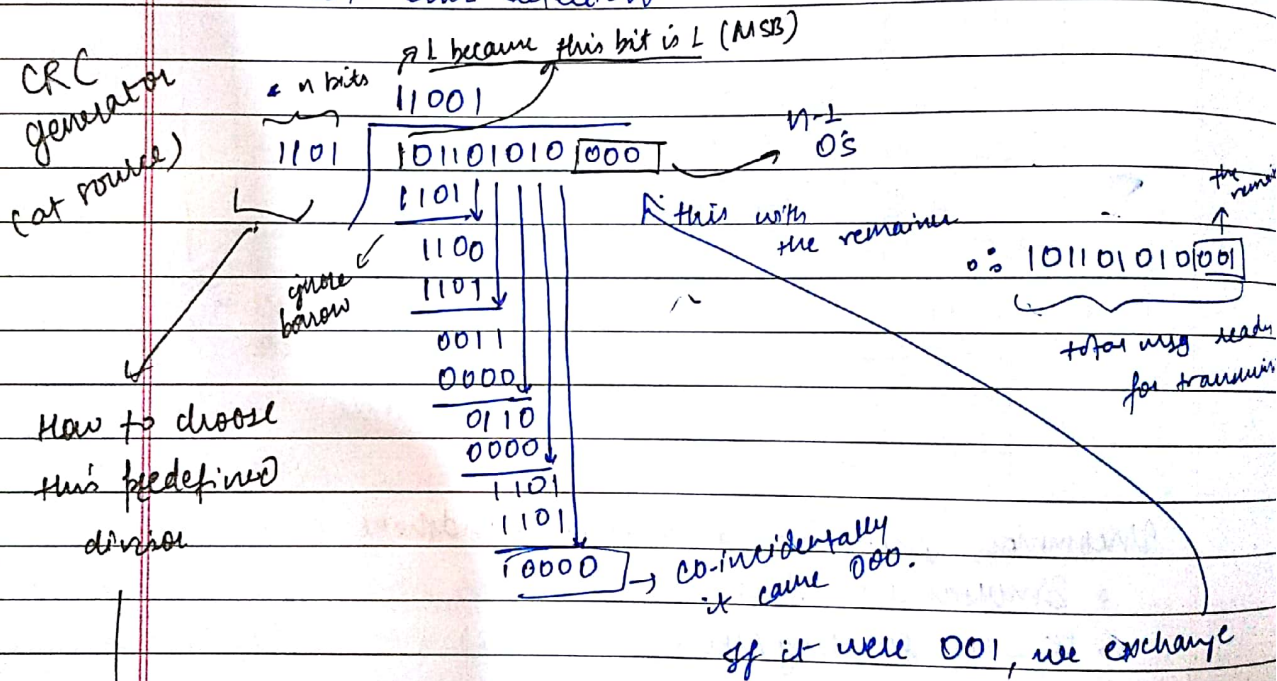
Cycle redundancy check (CRC) - modulo-2 division

Remainder of division \rightarrow CRC

Dividend \rightarrow data stream

Divisor \rightarrow pre-defined

- $\approx 98\%$ error detection



- Receiver has CRC checker

chose using a polynomial

$x^3 + x + 1 \rightarrow$ divisor polynomial

$1 \cdot x^3 + 0 \cdot x^2 + 1 \cdot x + 1$

(1011)

[Restrictions] The divisor polynomial must be :-

- 1) Must not be divisible by x
- 2) Must be divisible by $(x+1)$.

Some division polynomials accepted world-wide:

CRC-12

CRC-16

CRC-CCITT

Checksum

Error detection method based on 1's arithmetic complement

$\leftarrow n \text{ bits}$
 $n=16$
 $\underbrace{11000011}_{\text{data}} \quad \underbrace{00110011}_{\text{checksum}} \quad \boxed{\text{CHECKSUM}}$

$$\begin{array}{r} 11001100 \\ 11000011 \\ \hline 11110110 \rightarrow \text{SUM} \end{array}$$

 \leftarrow ignore carry from MSB
 \rightarrow bit-wise complement
 \rightarrow $\boxed{00001001} \rightarrow \text{CHECKSUM}$

$$\begin{array}{r} 11000011 \\ 11001100 \\ 00001001 \\ \hline 11111111 \end{array}$$

 if we add the message parts & checksum, we should get all 1's

- Better than simple and 2D parity check.
- But CRC provides the best performance.

Error correction

It would be better if receiver could correct erroneous messages after receiving.

Forward Error Correction (FEC) \rightarrow Hamming code
 message bits $\leftarrow m$ \rightarrow redundancy bits

\rightarrow for detecting single bit errors.

Bit error correction \rightarrow not in syllabus

$$\text{Total length} = (m+r)$$

$$\therefore \text{total no of states} = m+r+1$$

2^r states must be enough to contain all of $m+r+1$ states.

$$\therefore 2^r \geq m+r+1$$

For ex,

if $m = 7$

$r = 4$

so that

$m+r+1 = 12 < 2^4 = 16$

Redundancy bits are inserted at positions that are power of 2. (1, 2, 4, 8, ...)

bits: r_1, r_2, r_3, r_4

$\therefore d d d r_3 d d d r_2 d r_1 r_4$

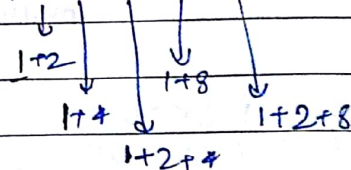
$r_1 \rightarrow 1, 3, 5, 7, 9, 11$

$r_2 \rightarrow 2, 3, 6, 7, 10, 11$

$r_4 \rightarrow 4, 5, 6, 7$

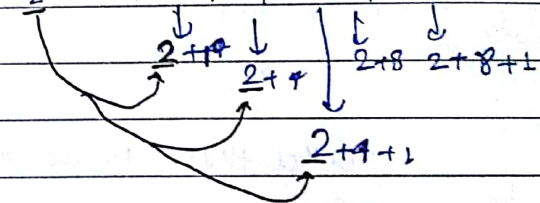
$r_3 \rightarrow 8, 9, 10, 11$

$r_1 \rightarrow 1, 3, 5, 7, 9, 11$



no repetition

$r_2 \rightarrow 2, 3, 6, 7, 10, 11$



If the message is error-free, then all the redundancy bits will be 0s.

Generation

Ex-

1000101

$\rightarrow m=7, r=4$ so that $2^4 \geq m+r+1$

100 r_1 0 10 r_4 1 r_2 1 r_3 \Rightarrow 10010101110

①

not considering 1, 2, 4, 8 bits as we don't know their

$r_1 \rightarrow 3, 5, 7, 9, 11 \Rightarrow 0$

$r_2 \rightarrow 3, 6, 7, 10, 11 \Rightarrow 1$

$r_3 \rightarrow 5, 6, 7 \Rightarrow 1$

$r_4 \rightarrow 9, 10, 11 \Rightarrow 1$

Even nos. of 1s at positions 3, 5, 7, 9, 11 (Total 2 1's) \therefore even parity

odd ones are corresponding posns.

Defect on

erroneous bit \rightarrow at posⁿ 51 0 0 1 0 1 0 1 1 1 0 \rightarrow actual msg1 0 0 1 0 1 1 1 1 1 0 \rightarrow erroneous msg

(1)

Here we will consider bits 1, 2, 4, 8

 $s_1 \rightarrow 1, 3, 5, 7, 9, 11 \Rightarrow 1 \rightarrow$ odd no. of 1s $s_2 \rightarrow 0$ $s_4 \rightarrow 1$ $s_8 \rightarrow 0$ $s_8 s_4 s_2 s_1$

0 1 0 1

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5

 $\rightarrow$  Location of the erroneous bit