

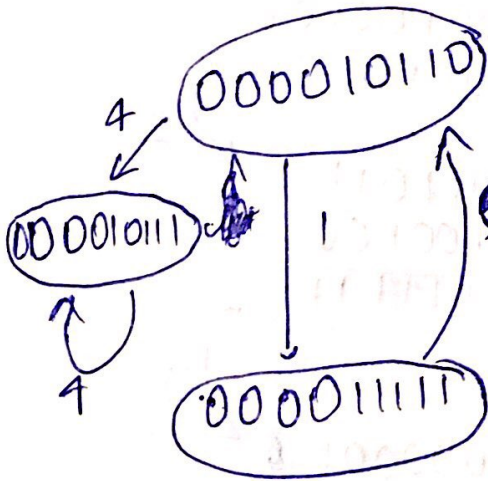
	1	2	3	4	5	6	7	8	9
$S_1$	X					X			
$S_2$		X			X		X		
$S_3$			X					X	
$S_4$				X					X

$\sum C$

$$\tau = \max_i \{ \tau z_i^k \} + \tau_e$$

Forbidden latency =  $(6-1), (5-2), (7-5), (7-2), (8-3), (9-4)$   
 $= 5, 3, 2, 5, 5, 5$

collision vector (C) = 0100 0000.10110



Permissible latency cycle

$\alpha(1, b), 4, 3$

Average latency cycle

$$= \sqrt{\left\{ \frac{1+6}{2}, \frac{4}{1} \right\}}$$

$$= \{3.5, 4\}$$

Handwritten binary addition examples showing carry propagation:

- Example 1:
 
$$\begin{array}{r} 000010110 \\ 000101100 \\ \hline 000111110 \end{array}$$
- Example 2:
 
$$\begin{array}{r} 00111100 \\ 00101100 \\ \hline 00111100 \end{array}$$
- Example 3:
 
$$\begin{array}{r} 0111000 \\ 101100 \\ \hline 101100 \end{array}$$

$$\begin{array}{r} 0000 \\ 10110 \\ \hline 10111 \end{array}$$

$$\begin{array}{r} 000001011 \\ \text{OR } 000010110 \\ \hline 000011111 \end{array}$$

OK

0	0	0	0	0	1	1	1
0	0	0	0	1	0	1	0
0	0	0	0	1	1	1	1

	1	2	3	4	5	6	7	8	9	10
$S_1$	X			X			X			X
$S_2$			X			X			X	
$S_3$		X			X			X		

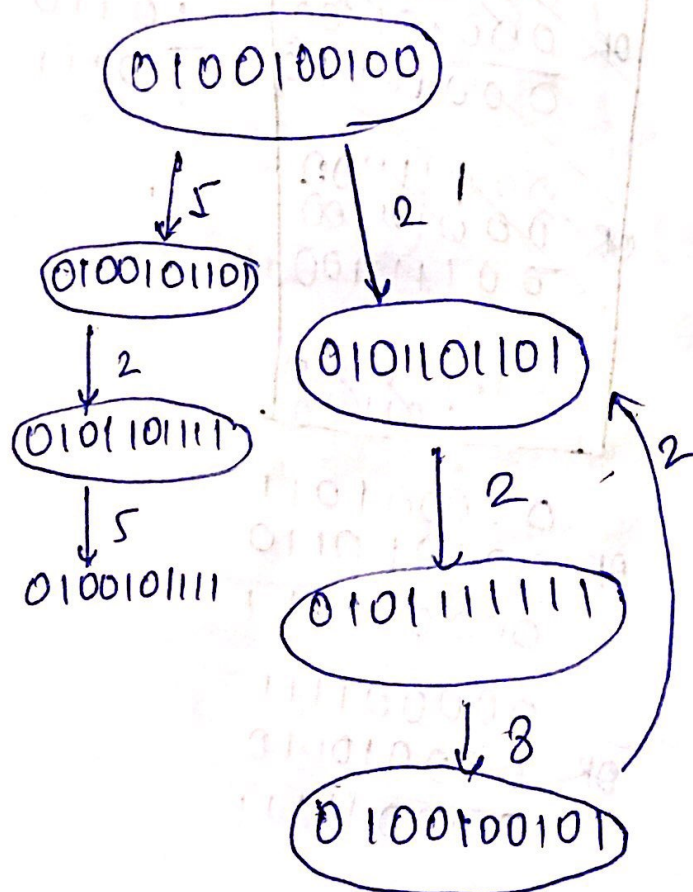
Forbidden latency = (4-1), (7-4), (7-1), (10-7), (10-4), (10-1),

(6-3), (9-6), (9-3), (5-2), (8-5), (8-2)

= 3, 3, 6, 3, 6, 9, 3, 3, 6, 3, 3, 6

= (3, 6, 9)

Collision vector = 0100100100



$$\begin{array}{r}
 0001001001 \quad \swarrow 2 \\
 \text{OR } 0100100100 \\
 \hline
 0101101101 \quad \swarrow 2 \\
 \\
 0001011101 \\
 \text{OR } 0100100100 \\
 \hline
 0101111111 \quad \swarrow 8 \\
 \\
 0000000001 \\
 \text{OR } 0100100100 \\
 \hline
 0100100101 \quad \swarrow 2 \\
 0001001001 \quad \swarrow 2
 \end{array}$$



$$\begin{array}{r} 0000001001 \\ 0100100100 \\ \hline 0100101101 \end{array}$$

$$\begin{array}{r} 0100100100 \\ \downarrow 3 \\ 0000000000 \\ 0100100100 \\ \hline 0100100101 \end{array}$$

$$\begin{array}{r} 0100100100 \\ \downarrow 5 \\ 0000001001 \\ 0100100100 \\ \hline 0100101101 \end{array}$$

$$\begin{array}{r} 0001001001 \\ 01000000100 \\ \hline 0101101101 \end{array}$$

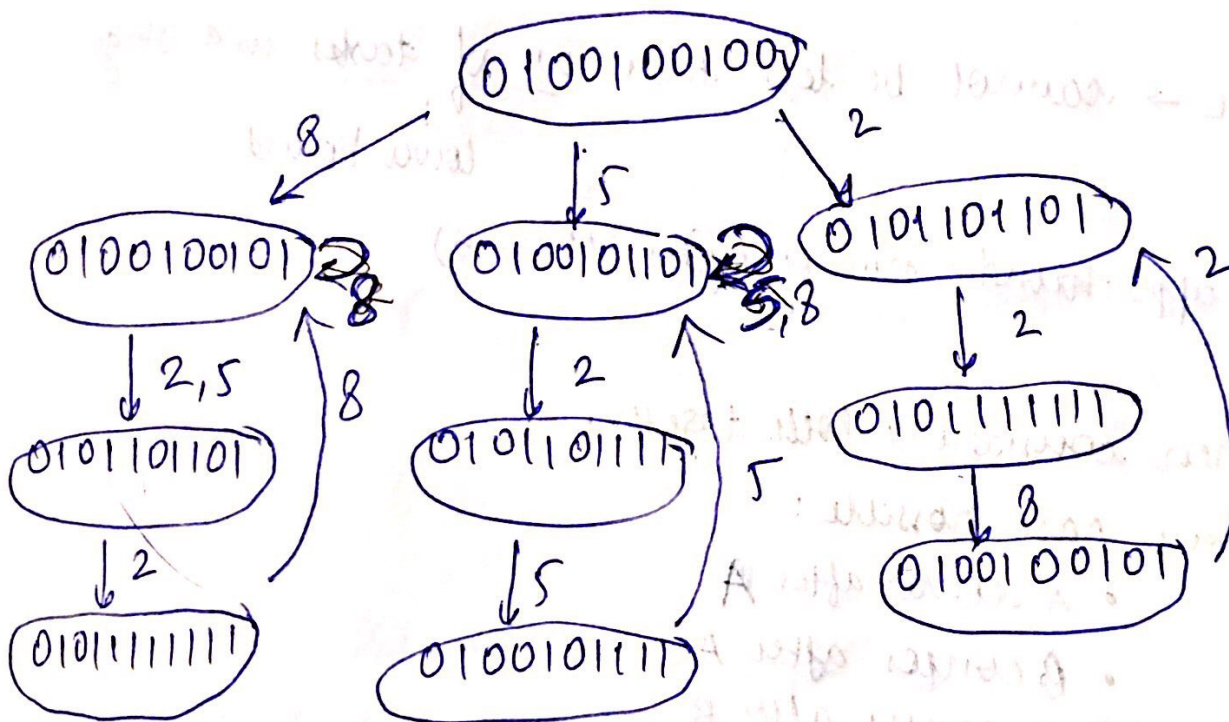
$$\begin{array}{r} 0001001011 \\ 0100100100 \\ \hline 0101101111 \end{array}$$

$$\begin{array}{r} 0001011011 \\ 0100100100 \\ \hline 0101111111 \end{array}$$

$$\begin{array}{r} 0000001011 \\ 0100100100 \\ \hline 0100101111 \end{array}$$

$$\begin{array}{r} 0000000001 \\ 0100100100 \\ \hline 0100100101 \end{array}$$

$$\begin{array}{r} 0000001001 \\ 0100100100 \\ \hline 0100101101 \end{array}$$



Permissible latency cycle

$$\text{Avg LC} = \{ (8, 2, 2, 8), (8, 5, 2, 8), (8), (5), (5, 2, 5, 5), (2, 2, 8, 2) \}$$

$$= \{ 5, \frac{23}{4}, 8, 5, \frac{17}{4}, \frac{14}{4} \} = \{ 5, 5.75, 8.5, 4.25, 3.5 \}$$

Minimum avg. latency (MAL) = 3.5