Lecture-2 (AP)
29/01/2019

Classification of pipeline

By level of processing (defined by Handler 1977)

- Arithmetic pipeline - 4 stage & 8 stage (TI ASC)
- Instruction pipeline - multiple inst. stages interwind
- Processor pipeline - multiprocessor

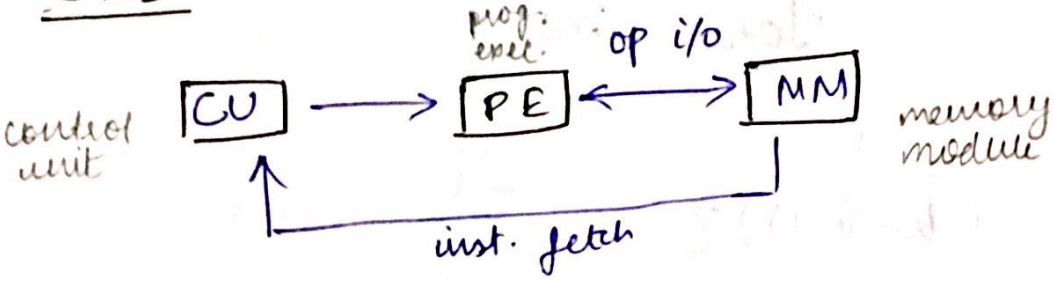
Classification by configuration & control strategy

- Static pipeline - single conf.
- Dynamic pipeline - changed based on feedback
- Unifunctional
- Multifunctional

Classification by architecture (Flynn's classificatio

- SISD single instruction, single data stream
- SIMD
- MISD
- MIMD

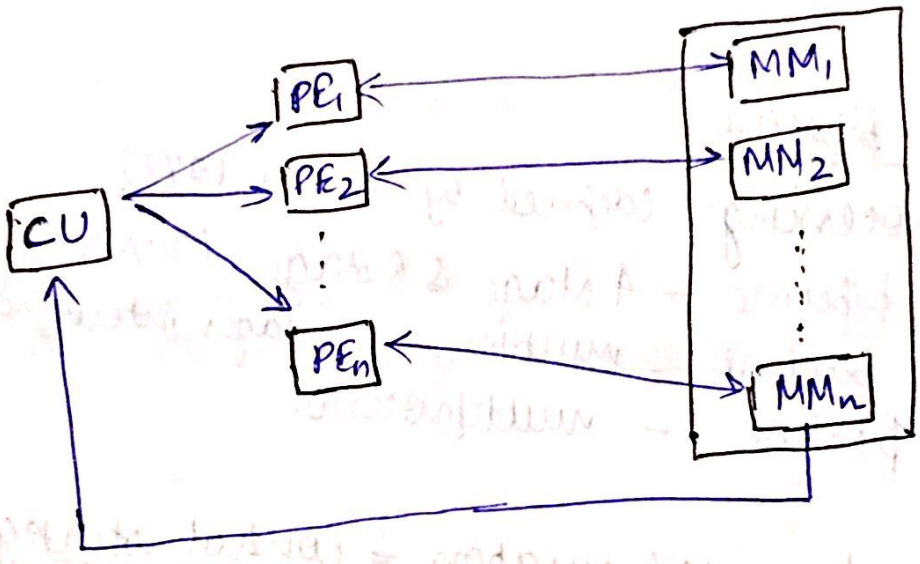
SISD



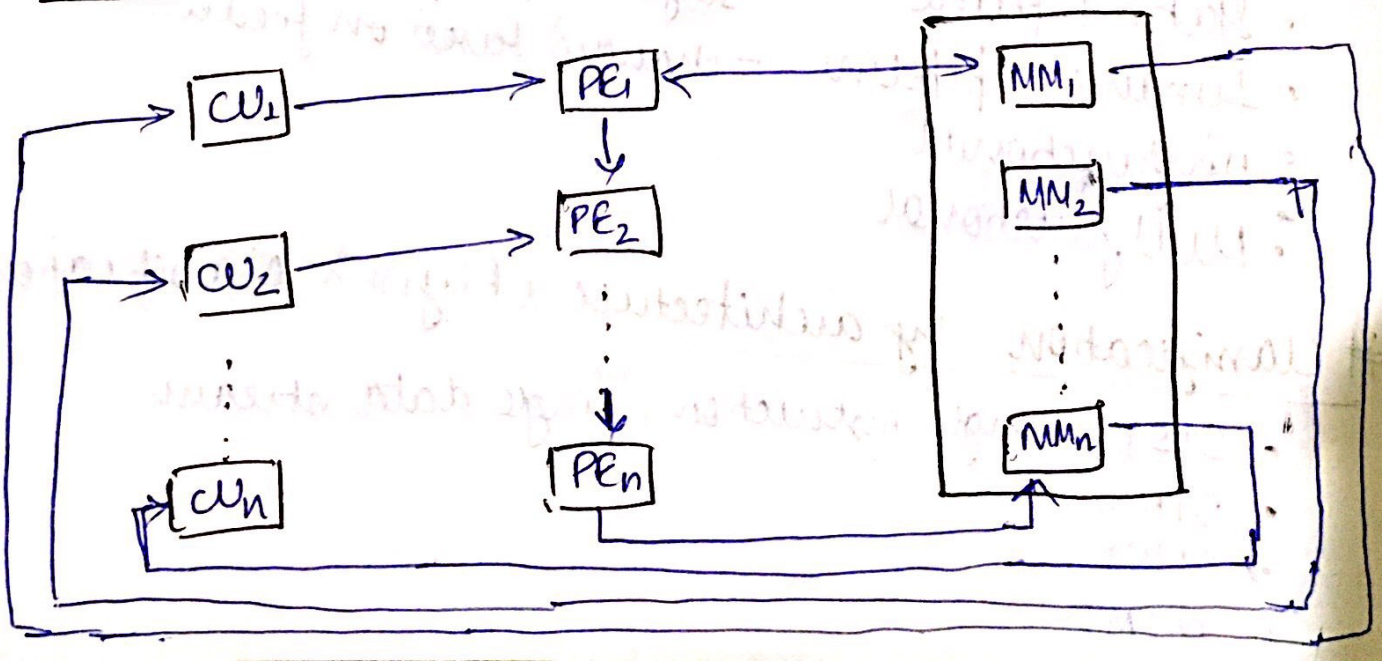
SIMD (Vectored. Ex- GPU)

for ex.

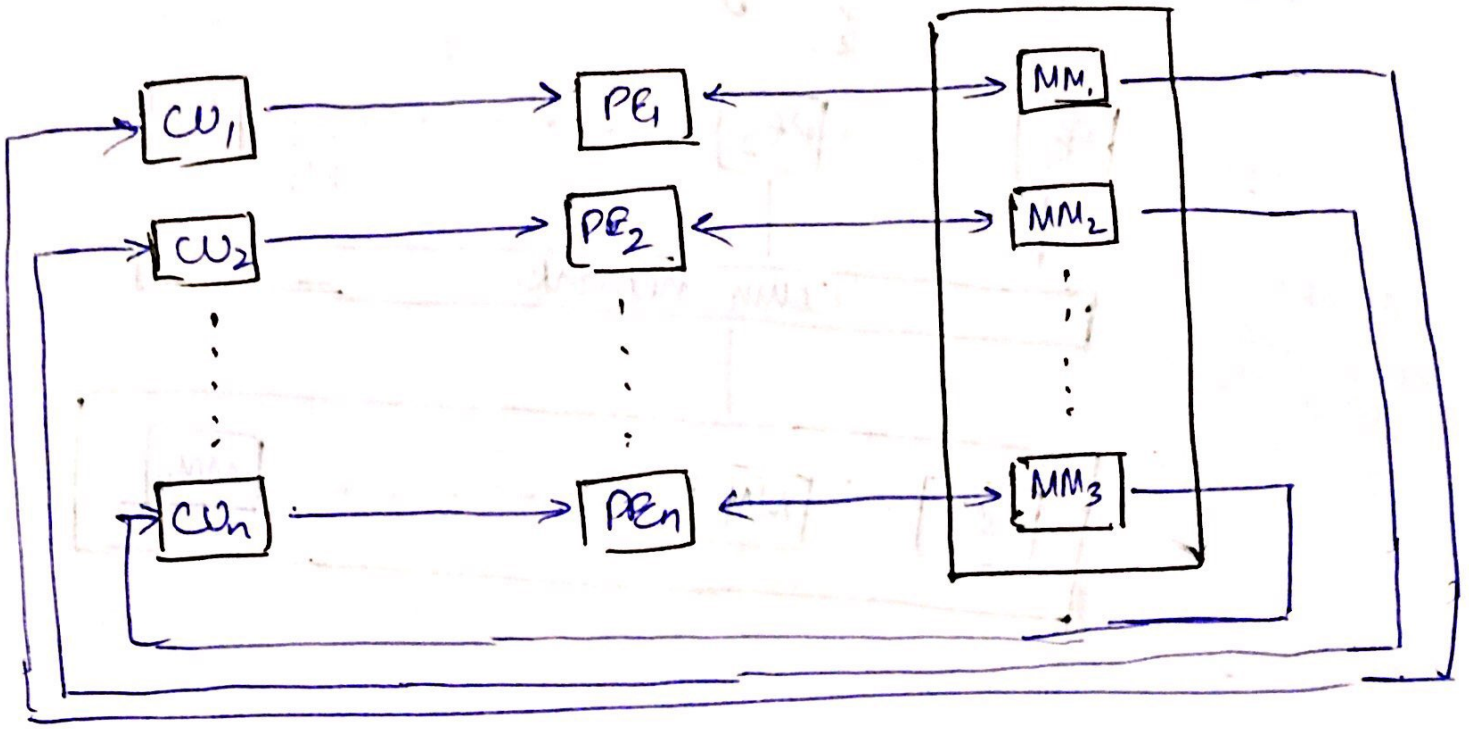
ADD A[][], B[][]



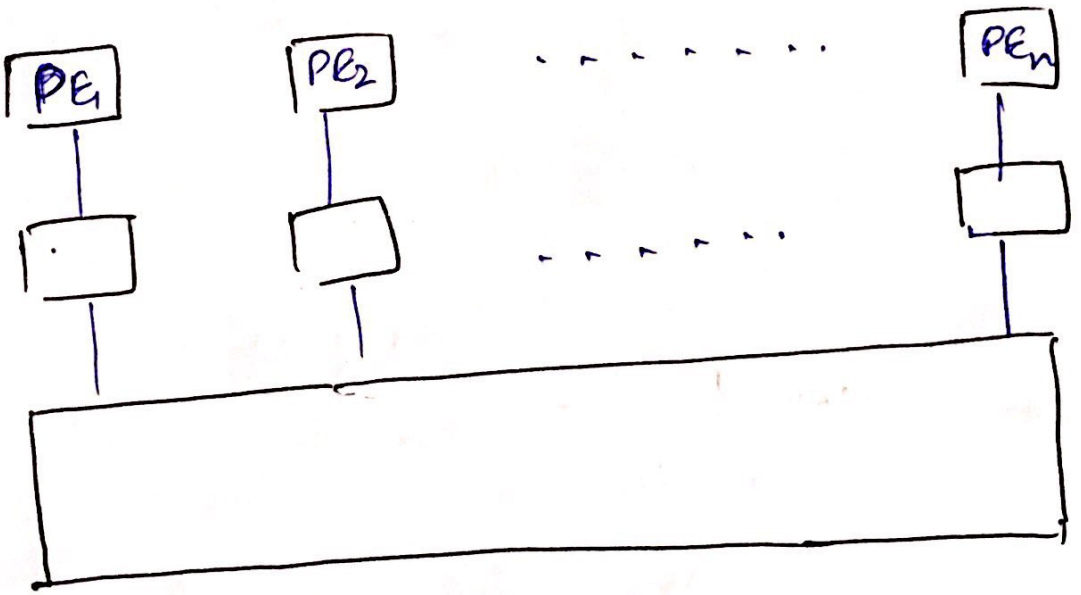
MISD (Not feasible)



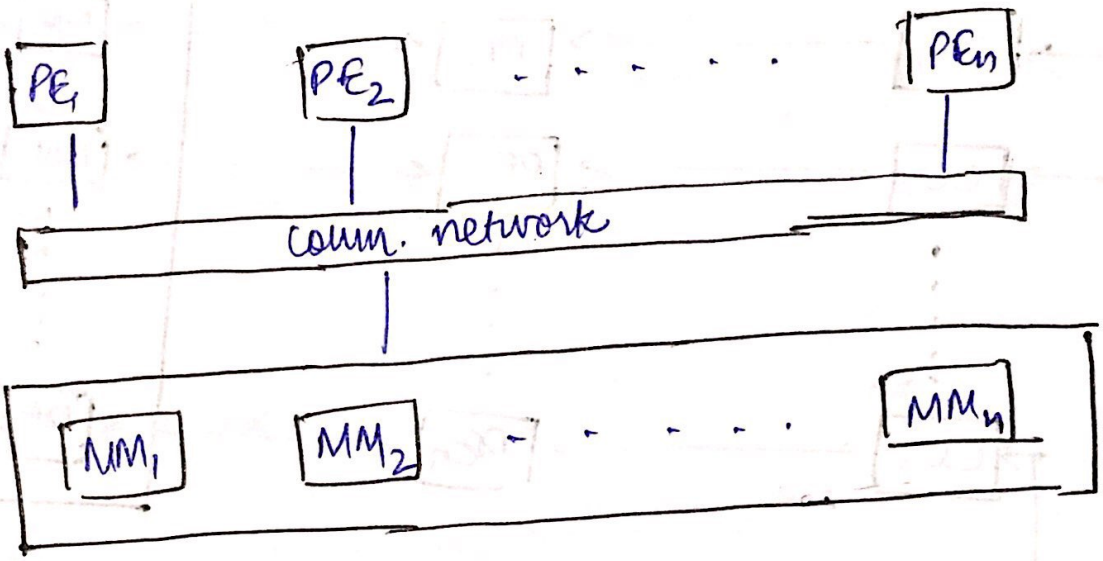
MIMD (Multiple cores)



Uniform memory access (UMA)



Non-uniform memory access (NUMA)



Blocks conflicting accesses