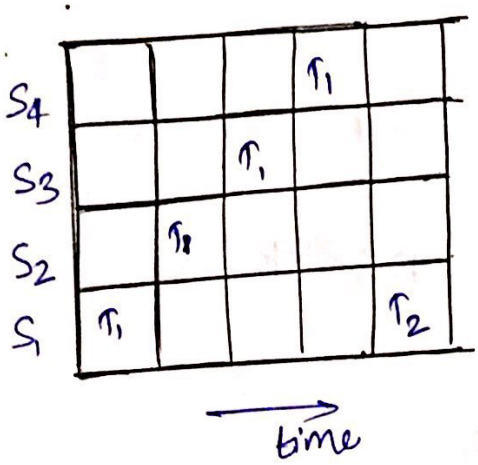
Lecture-1 (AP)

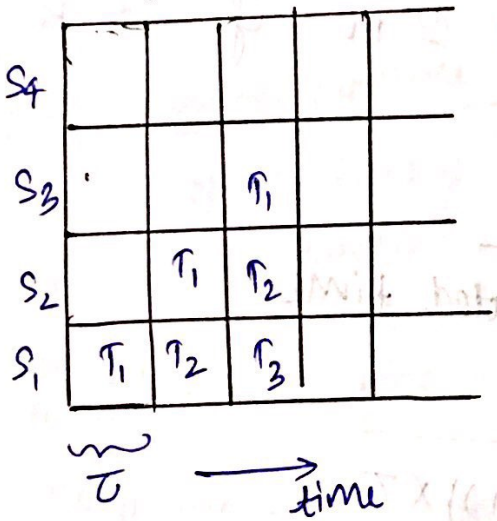
28/01/2019

Books
- Hwang, Briggs
- Naresh Jatwani

• Time-space diagram of a non-pipelined processor




• Time-space diagram of a pipelined processor




k : no. of stages
n : no. of task
τ : time taken for each task

Time taken for n process in k stages :

By non-pipelined processor : $nk\tau$

By pipelined processor : $k\tau + (n-1)\tau$

$\therefore$ Speed up ($S_k$) = $\frac{\text{time taken by non-pipelined processor}}{\text{time taken by pipelined processor}}$

$$\Rightarrow S_k = \frac{nk\tau}{k\tau + (n-1)\tau}$$

For maximum speed up, $n >> k$

Then,

$$S_k = \frac{nk}{n} = k$$

as $k + (n-1) \simeq n$ if $n >> k$

Efficiency ($\eta$) = $\frac{\text{Busy time}}{\text{Total allocated time}}$

$$\Rightarrow \eta = \frac{nk\tau}{k \times (k + (n-1)) \times \tau}$$

→ area of complete square in T-S diag

→ area of all allocated tasks

$$= \frac{n}{k + (n-1)}$$

$$= \frac{S_k}{k}$$

Throughput ($T$) = $\frac{\text{Total output}}{\text{Total time}}$

$$T = \frac{n}{(k + (n-1))\tau} = \frac{n}{\tau}$$

when $n \to \infty$

$T = \frac{1}{\tau}$ → frequency of processor