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DIGITAL ELECTRONICS DESIGN GROUP

DBHI: towards decoupled functional hardware-software co-design on SoCs

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A system-level co-simulation and verification workflow to ease the transition from a software-only procedure to the integration of a custom hardware accelerator developed in a Hardware Description Language (HDL).

- It provides support for rapid iterative exploration and functional verification of hardware designs.
- DBMs could be able to instrument an application and inject compiled hardware.
- Foreign architecture emulation overhead during development is avoided, and early integration with peripherals in the target System-on-Chip would be possible.
- Allows migration from application source code, progressively, to non-synthesizable HDL, and to synthesizable HDL.
- It keeps the software application unmodified, as a reference.
- It preserves cycle-accurate/bit-accurate results, and provides run-time visibility of the internal data buffers for debugging purposes.
- The design flow can be evaluated on executions of hardware simulations on x86-64 and Arm architectures.
- The technique is not tied to any specific architecture.

The design flow was developed using existing off-the-shelf tools.

GHDL

FOSS analyser, compiler, simulator and experimental synthesiser for VHDL (1987, 1993, 2002 or 2008). GHDL allows to analyse and elaborate sources to generate machine code paired with a runtime library. At runtime, it can generate waveforms in multiple formats, for inspection with tools such as GtkWave. It has partial support of Property Specification Language (PSL).

ghdl.rtfd.io, gh:ghdl/ghdl

VUnit

FOSS unit testing framework for VHDL or SystemVerilog. It features the functionality needed to realize continuous and automated testing of HDL designs.

- Avalon: Memory-Mapped (master, slave), Stream (sink, source)
- AXI: Lite master, slave (read, write), stream (master, slave, monitor, protocol checker)
- Wishbone (master, slave)
- UART (master, slave)
- RAM master

vunit.github.io, gh:VUnit/vunit

MAMBO

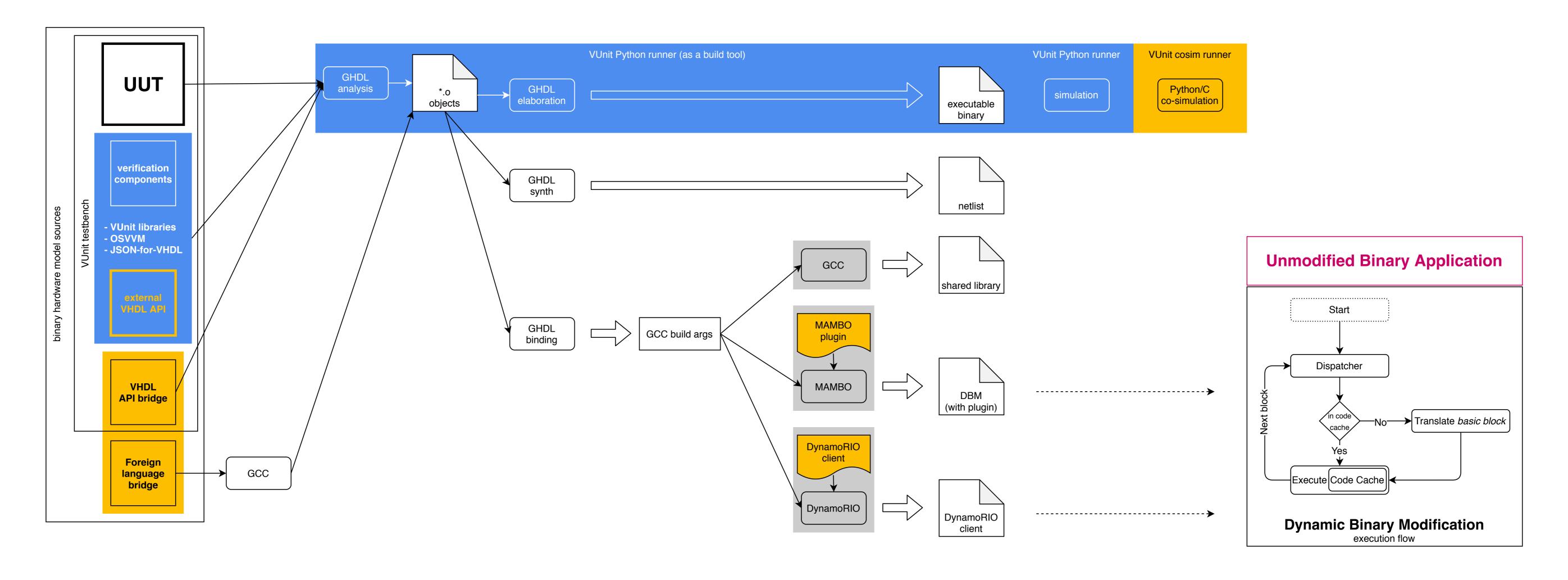
FOSS low-overhead dynamic binary instrumentation and modification tool for ARM. Both AArch32 and AArch64 are supported. It provides a Plugin API that allows to replace functions in existing binaries with user-defined alternative implementations.

gh:beehive-lab/mambo

DynamoRIO

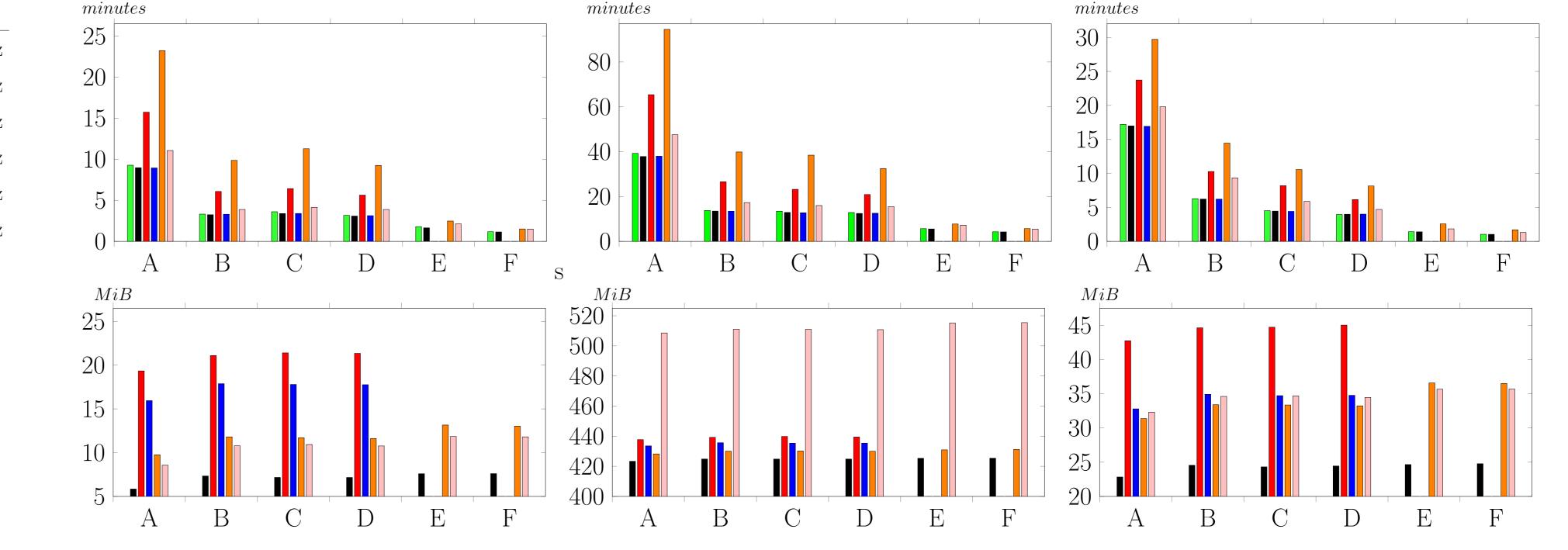
FOSS runtime code manipulation system that supports code transformations on any part of a program. It exports an interface for building dynamic tools for a wide variety of uses: program analysis and understanding, profiling, instrumentation, optimization, etc. DynamoRIO allows arbitrary modifications to application via instruction manipulation library. It provides efficient, transparent, and comprehensive manipulation of unmodified applications running on stock operating systems (Windows, GNU/Linux, or Android, with experimental macOS support) and commodity IA-32, AMD64, Arm, and AArch64 hardware.

dynamorio.org, gh:DynamoRIO/dynamorio



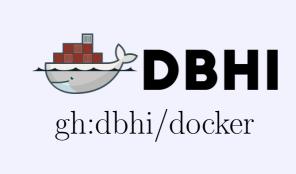
	Device			$\mathbf{R}\mathbf{A}\mathbf{M}$		
A	Pine A64+ (RK3328)	4x A53	1.2GHz	2GB	DDR3	1600MHz
В	Rock960 (RK3399)	2x A72 + 4x A53	1.8GHz	4GB	LPDDR3	1866MHz
С	Jetson TX1	4x A57	1.73GHz	4GB	LPDDR4	1600MHz
D	APM883408-X2	8x X-Gene 2	$2.4\mathrm{GHz}$	32GB	DDR3	1866MHz
E	F555LD-XX110H	i7-4510U	2-3.1GHz	8GB	DDR3	1600MHz
F	ThinkCentre-M910-SFF	i7-6700	3.40GHz	16GB	DDR4	2400MHz

- testbench with VUnit's Python runner
- native execution by building VHDL in the application
- native binary on top of MAMBO
- software-only application with VHDL built in the plugin (MAMBO)
- native binary on top of DynamoRIO
- software-only application with VHDL built in the client (DynamoRIO)











binhook gh:dbhi/binhook

