Microprocessor - 8085 Branching Instructions

Previous Page Next Page

The following table shows the list of Branching instructions with their meanings.

<table>
<tr><th colspan="2">Opcode</th><th>Operand</th><th>Meaning</th><th>Explanation</th></tr>
<tr><td colspan="2">JMP</td><td>16-bit address</td><td>Jump unconditionally</td><td>The program sequence is transferred to the memory address given in the operand.</td></tr>
<tr><td colspan="2"><table><tr><th>Opcode</th><th>Description</th><th>Flag Status</th></tr><tr><td>JC</td><td>Jump on Carry</td><td>CY=1</td></tr><tr><td>JNC</td><td>Jump on no Carry</td><td>CY=0</td></tr><tr><td>JP</td><td>Jump on positive</td><td>S=0</td></tr><tr><td>JM</td><td>Jump on minus</td><td>S=1</td></tr><tr><td>JZ</td><td>Jump on zero</td><td>Z=1</td></tr><tr><td>JNZ</td><td>Jump on no zero</td><td>Z=0</td></tr><tr><td>JPE</td><td>Jump on parity even</td><td>P=1</td></tr><tr><td>JPO</td><td>Jump on parity odd</td><td>P=0</td></tr></table></td><td>16-bit address</td><td>Jump conditionally</td><td>The program sequence is transferred to the memory address given in the operand based on the specified flag of the PSW.</td></tr>
<tr><td colspan="2"><table><tr><th>Opcode</th><th>Description</th><th>Flag Status</th></tr><tr><td>CC</td><td>Call on Carry</td><td>CY=1</td></tr><tr><td>CNC</td><td>Call on no Carry</td><td>CY=0</td></tr><tr><td>CP</td><td>Call on positive</td><td>S=0</td></tr><tr><td>CM</td><td>Call on minus</td><td>S=1</td></tr><tr><td>CZ</td><td>Call on zero</td><td>Z=1</td></tr><tr><td>CNZ</td><td>Call on no zero</td><td>Z=0</td></tr><tr><td>CPE</td><td>Call on parity even</td><td>P=1</td></tr><tr><td>CPO</td><td>Call on parity odd</td><td>P=0</td></tr></table></td><td>16-bit address</td><td>Unconditional subroutine call</td><td>The program sequence is transferred to the memory address given in the operand. Before transferring, the address of the next instruction after CALL is pushed onto the stack.</td></tr>
<tr><td colspan="2">RET</td><td>None</td><td>Return from subroutine unconditionally</td><td>The program sequence is transferred from the subroutine to the calling program.</td></tr>
<tr><td colspan="2"><table><tr><th>Opcode</th><th>Description</th><th>Flag Status</th></tr><tr><td>RC</td><td>Return on</td><td>CY=1</td></tr></table></td><td>None</td><td>Return from subroutine conditionally</td><td>The program sequence is transferred from the subroutine to the calling program based on the specified flag of the PSW and the program execution begins at the new address.</td></tr>
</table>

	Carry	
RNC	Return on no Carry	CY=0
RP	Return on positive	S=0
RM	Return on minus	S=1
RZ	Return on zero	Z=1
RNZ	Return on no zero	Z=0
RPE	Return on parity even	P=1
RPO	Return on parity odd	P=0

PCHL	**None**	Load the program counter with HL contents	The contents of registers H & L are copied into the program counter. The contents of H are placed as the high-order byte and the contents of L as the loworder byte.
RST	**0-7**	Restart	The RST instruction is used as software instructions in a program to transfer the program execution to one of the following eight locations. Instruction – Restart Address RST 0 – 0000H RST 1 – 0008H RST 2 – 0010H RST 3 – 0018H RST 4 – 0020H RST 5 – 0028H RST 6 – 0030H RST 7 – 0038H The 8085 has additionally 4 interrupts, which can generate RST instructions internally and doesn't require any external hardware. Following are those instructions and their Restart addresses – Interrupt – Restart Address TRAP – 0024H RST 5.5 – 002CH RST 6.5 – 0034H RST 7.5 – 003CH

Previous Page Next Page