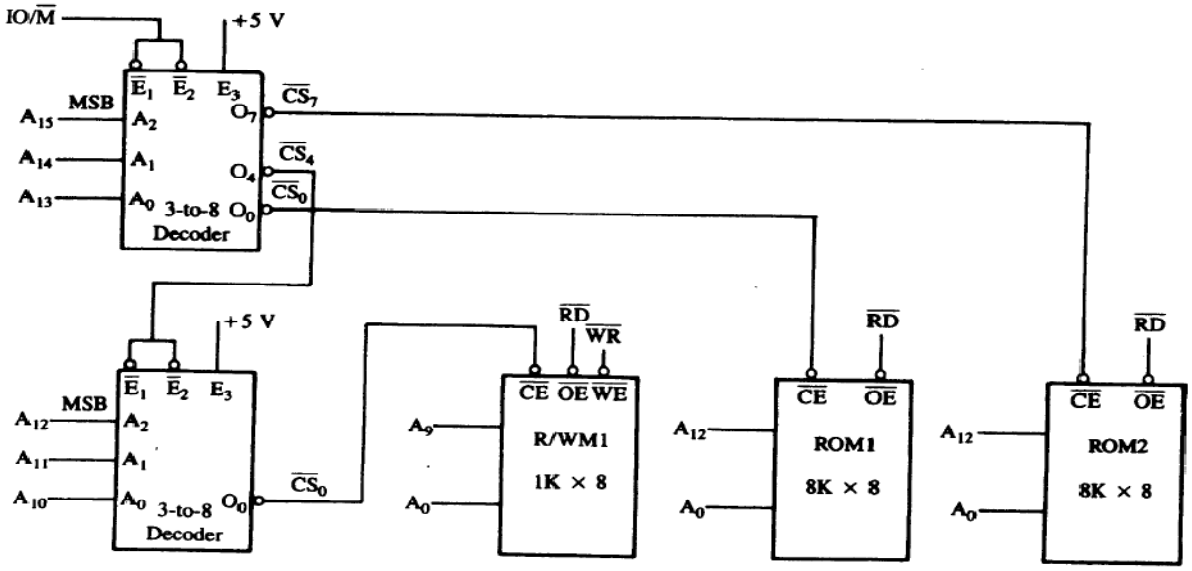
Suggestion related to Paper-V, Computer Science (Hons).

Group-A

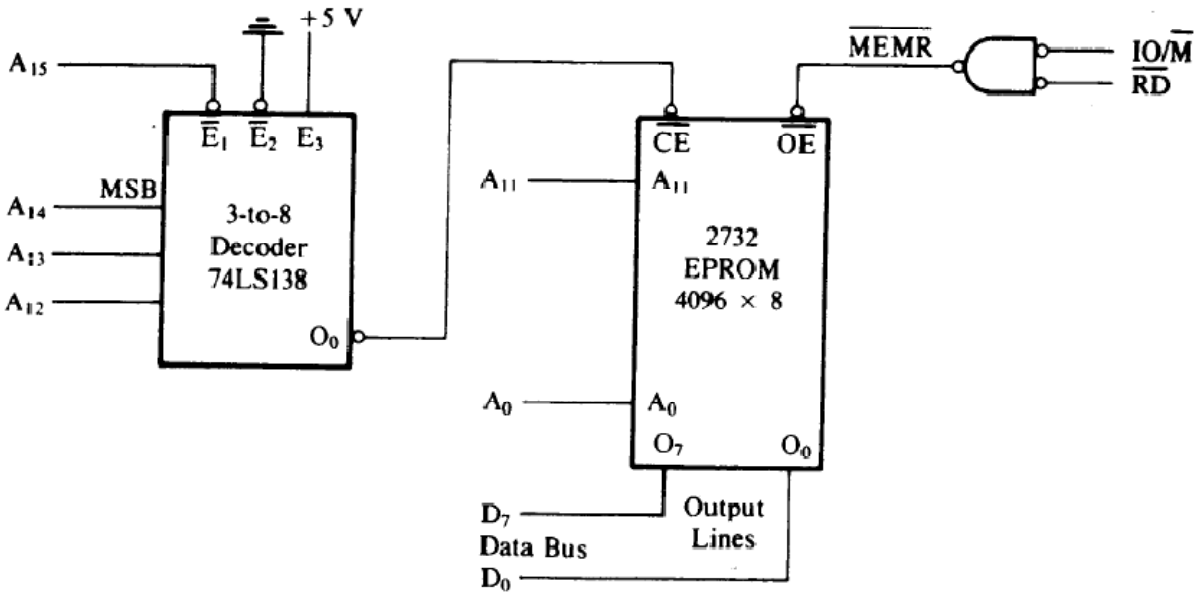
Microprocessor Intel 8085

1. What are the different programmable registers of Intel 8085? Explain with suitable example.
2. Write a program to reset all the flags of Intel 8085.
3. Cascade two 1Kbyte memories to form 2Kbyte memory in the memory address range starting from 0000_H to $07FF_H$.
4. An instruction code $7E_H$ is loaded into a memory module at a location corresponding to the location 8000_H. Draw the data flow diagram along with proper explanation of each and every step involved during the instruction fetch operation.
5. What are the advantages of multiplexed data/Address bus? How can we achieve de-multiplexing of Address/data bus?
6. Discuss the different status and control signals relate d to Intel 8085 microprocessor? Generate four control signals which can separately control memory and Input output device.
7. Draw the timing diagram for the following instructions STAX B, LHLD $F000_H$, CALL $FF00_H$, LXI $F000_H$, PCHL and XTHL.
8. Discuss the different flags of Intel 8085. Discuss each with suitable example.
9. Differentiate between machine cycle and T states. Number of machine cycles and number of bytes of an instruction may be or may not be the same. Justify your answer with suitable supporting example.
10. Differentiate between partial and absolute decoding with suitable example. Show that partial decoding has multiple addresses pointing to a single location of memory.
11. Discuss the general architecture of Intel 8085 microprocessor explaining each and every block in brief.
12. A memory is to be connected in the memory address range starting from $E000_H$ to $EFFF_H$. Draw the necessary circuit diagram along with absolute decoding circuit, control signals along with a suitable memory and interface it with Intel 8085 microprocessor.
13. Differentiate between memory mapped IO and IO mapped IO. Construct an input port having $9E_H$ and an output port $9F_H$ using IO mapped IO.

14. Identify the memory address range of the ROM1, ROM2, R/W M1 for the figure given below. Remove the second decoder and connect the CS_4 connection to the CE terminal of the first memory module (R/W M1) and find the memory address range along with foldback memory space.



15. Identify the memory range for the following circuit.



Connect the A_{15} to enable inputs E_1 and E_2 and connect A_{14} to the E_3 enable terminal along with the MSB input of the decoder. Now find the memory address range. What is alternate logic gate that can be used to generate the control signal MEMR.

16. When an input and output port is interfaced with the Intel microprocessor in IO mapped IO method then what are the three important steps that needs to be considered when designing the circuit diagram.
17. What are the different addressing modes? Explain each with suitable example.
18. What do you mean by Restart instruction? Can the microprocessor be interrupted before the completion of the first interrupt service routine (ISR), justify your answer with suitable example.
19. Differentiate between hardware and software interrupt. Let us assume that the INTR terminal is used to interrupt the microprocessor. When INTR is activated RST 5 is inserted. Implement a circuit which can insert RST 5 when the microprocessor is interrupted and write software program which will take the control of the microprocessor to a memory location $F000_H$ where the interrupt service routine has been stored and also assuming that the monitor program gives the jump location 2700_H corresponding to RST 5.
20. Discuss different vector hardware interrupt related to microprocessor Intel 8085. Write an assembly language program to enable all the hardware interrupts of Intel 8085 microprocessor.
21. Describe the control word pattern of 8255A. Describe the control word with respect to IO mode operation and BSR mode operation. Interface the PPI 8255 with ports having addresses as given below;

    Port A 10_H, Port B – 11_H, Port C – 12_H, Port D-13_H.
22. Generate a square wave pulse coming out of the MSB of the port C of 8255 having a time period of ten milliseconds, assuming that the delay subroutine of 10msecs is available to you.
23. What is DMA? Discuss the all the steps involved during DMA operation. Discuss all the relevant control signals involved during DMA operation.
24. Interface a 4X4 key board matrix with the PPI 8255 and microprocessor Intel 8085.
25. Compare the basic features or differences in the architecture part of 8085 and 8086.

Note: Study all the short notes, the question above are only indicative try to study the entire syllabus giving stress on the above questions.