



Vietnam National University HCMC
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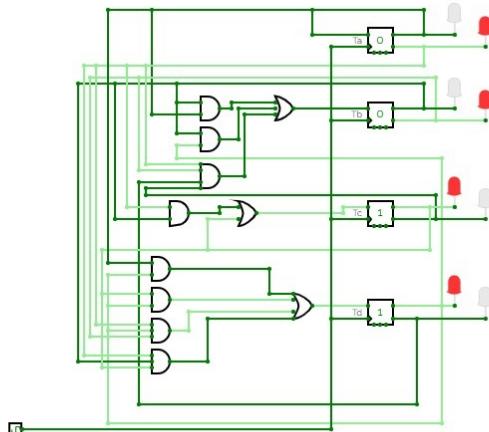


School of
Electrical Engineering

EE053IU

Digital Logic Design

Lecture 7: Latches, Flip-Flops, and Timers

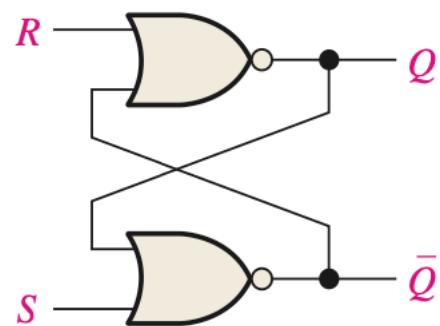


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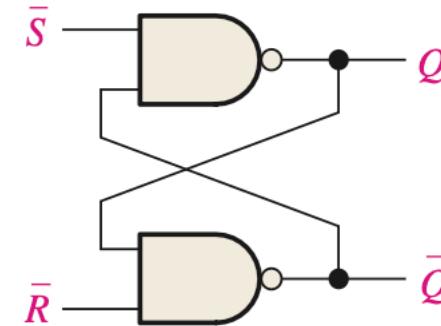
1. Latches

The S-R (SET-RESET) Latch

- A latch is a type of bistable logic device or multivibrator.
- An active-HIGH input S-R (SET-RESET) latch is formed with two cross-coupled NOR gates.
- An active-LOW input \bar{S} - \bar{R} latch is formed with two cross-coupled NAND gates



(a) Active-HIGH input S-R latch



(b) Active-LOW input \bar{S} - \bar{R} latch

FIGURE 7-1 Two versions of SET-RESET (S-R) latches.

- A latch can reside in either of its two states, SET or RESET.
- When the Q output is HIGH, the latch is in the SET state.
- When the Q output is LOW, the latch is in the RESET state.

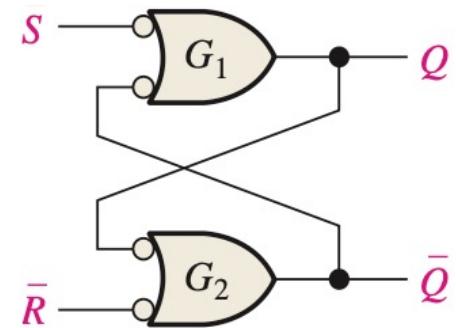
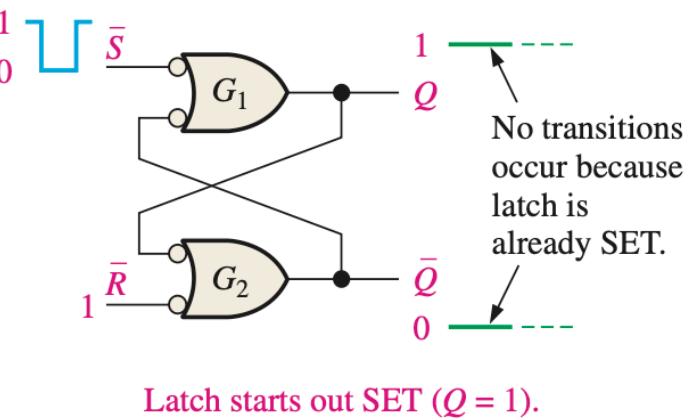
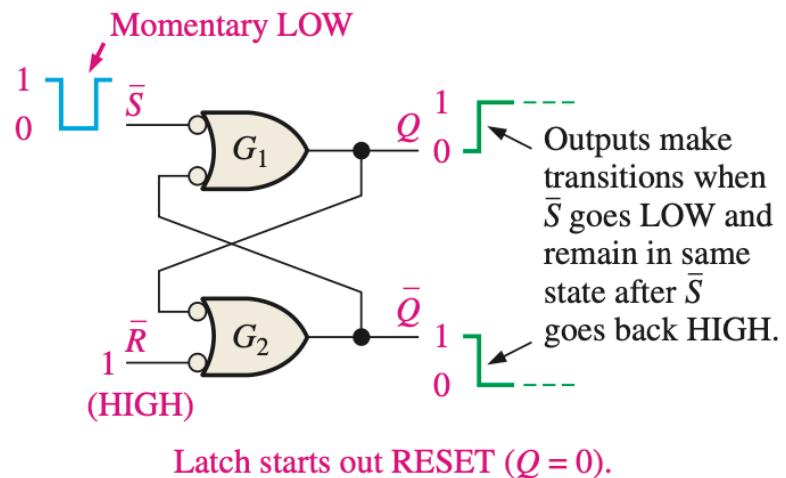
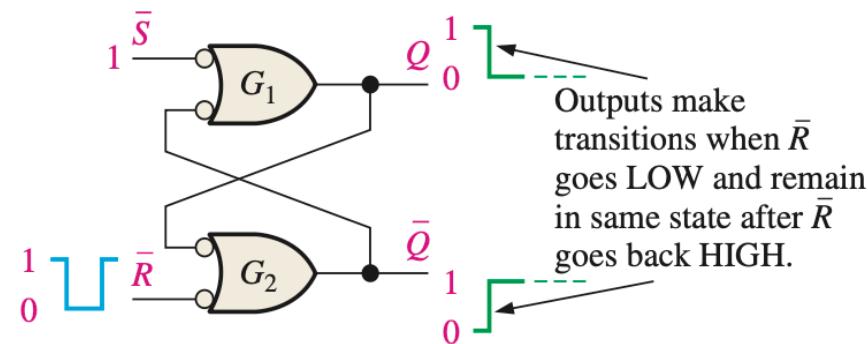


FIGURE 7-2 Negative-OR equivalent of the NAND gate S-R latch in Figure 7-1(b).

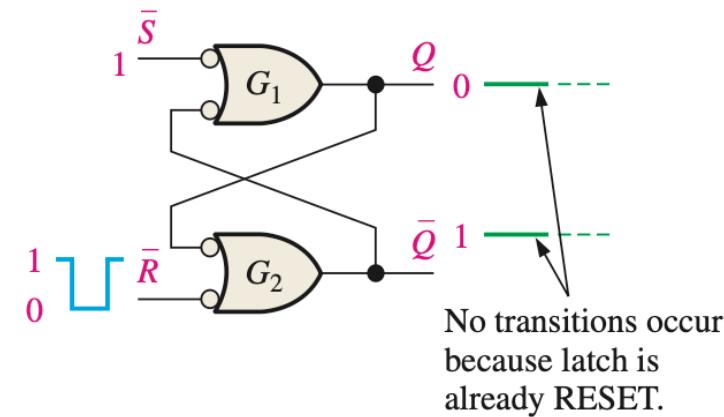


(a) Two possibilities for the SET operation

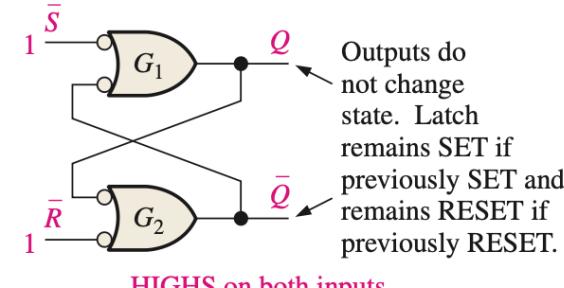


Latch starts out SET ($Q = 1$).

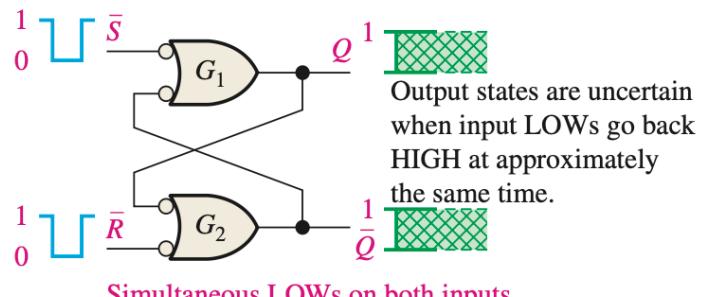
(b) Two possibilities for the RESET operation



Latch starts out RESET ($Q = 0$).



(c) No-change condition



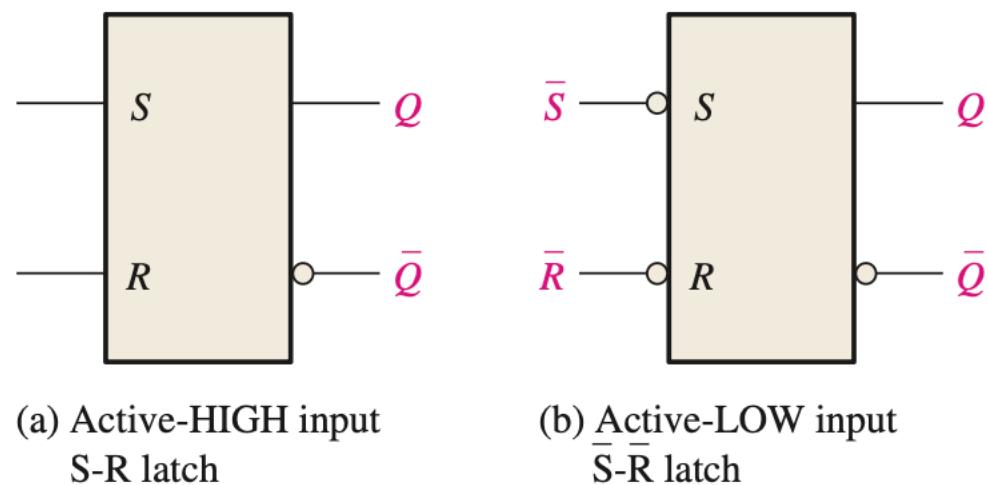
(d) Invalid condition

FIGURE 7-3 The three modes of basic \bar{S} - \bar{R} latch operation (SET, RESET, no-change) and the invalid condition.

TABLE 7-1

Truth table for an active-LOW input \bar{S} - \bar{R} latch.

Inputs		Outputs		Comments
\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

**FIGURE 7-4** Logic symbols for the S-R and \bar{S} - \bar{R} latch.

EXAMPLE 7-1

If the \bar{S} and \bar{R} waveforms in Figure 7-5(a) are applied to the inputs of the latch in Figure 7-4(b), determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.

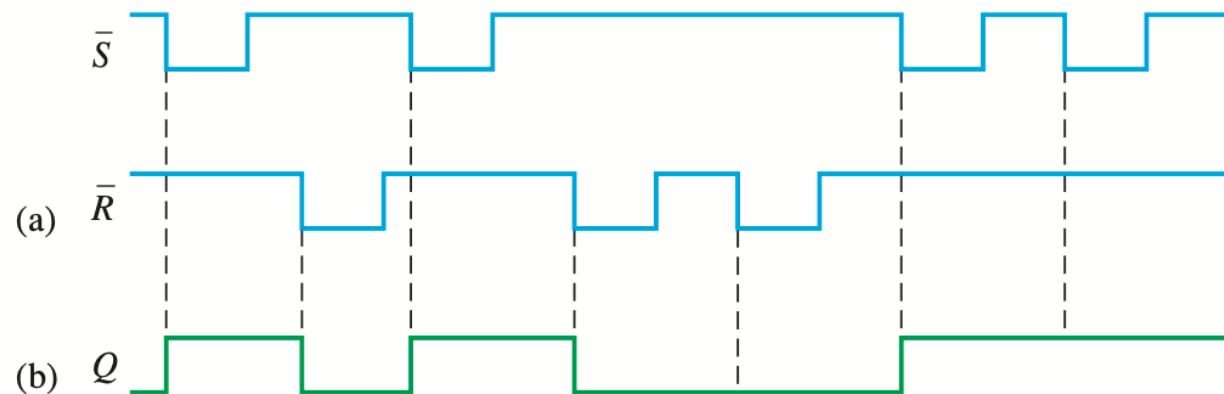
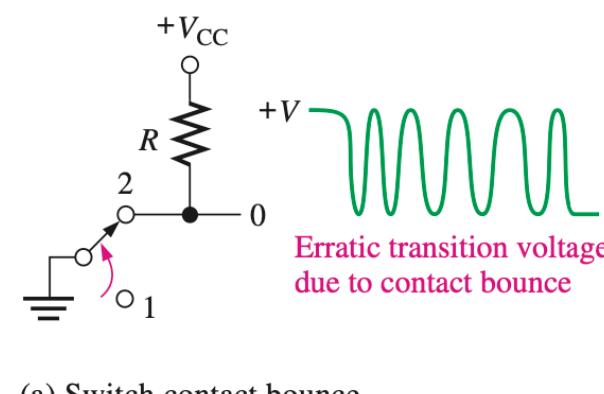


FIGURE 7-5

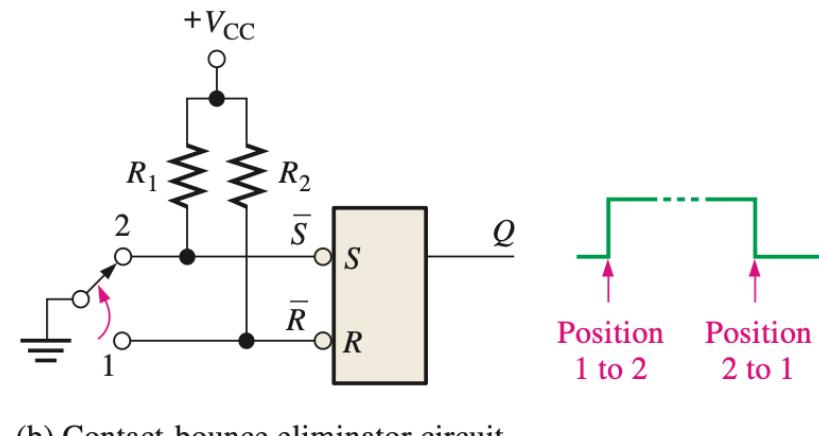
An Application

Solution

See Figure 7-5(b).



(a) Switch contact bounce

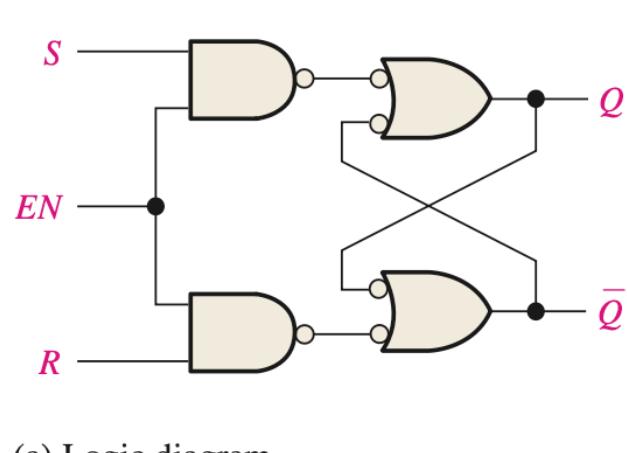


(b) Contact-bounce eliminator circuit

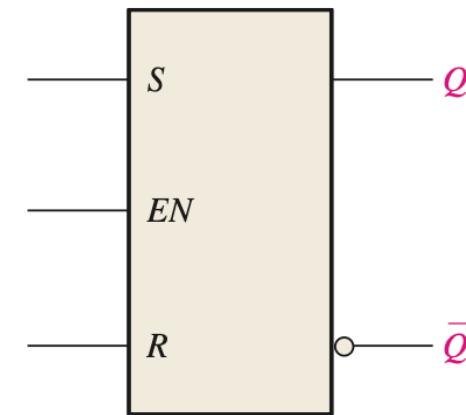
FIGURE 7-6 The $\bar{S}-\bar{R}$ latch used to eliminate switch contact bounce.

The Gated S-R Latch

- A gated latch requires an enable input, EN (G is also used to designate an enable input).
- The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input. The latch will not change until EN is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs.
- The gated latch is a level-sensitive device. In this circuit, the invalid state occurs when both S and R are simultaneously HIGH and EN is also HIGH.



(a) Logic diagram



(b) Logic symbol

FIGURE 7-8 A gated S-R latch.

EXAMPLE 7-2

Determine the Q output waveform if the inputs shown in Figure 7-9(a) are applied to a gated S-R latch that is initially RESET.

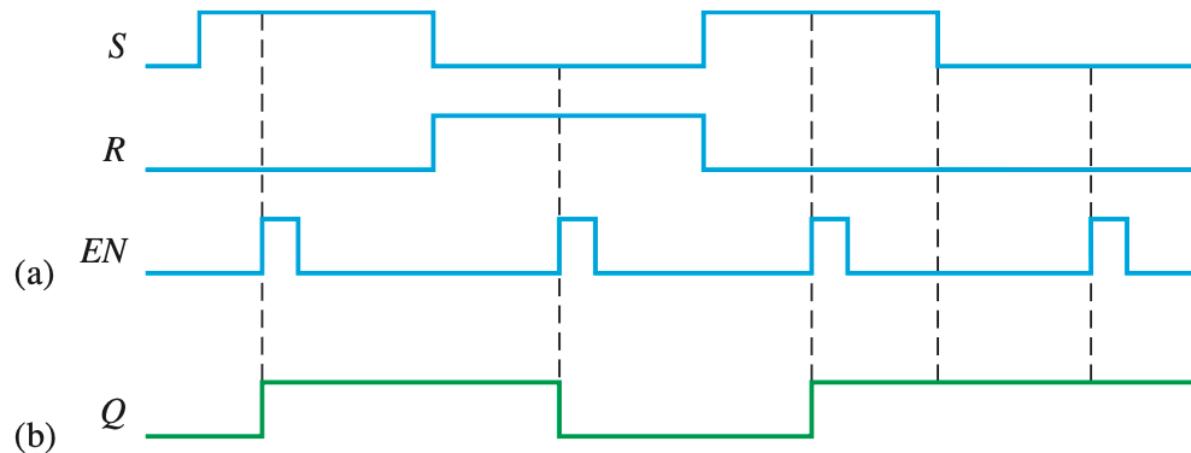


FIGURE 7-9

Solution

The Q waveform is shown in Figure 7-9(b). When S is HIGH and R is LOW, a HIGH on the EN input sets the latch. When S is LOW and R is HIGH, a HIGH on the EN input resets the latch. When both S and R are LOW, the Q output does not change from its present state.

The Gated D Latch

- Another type of gated latch is called the D latch. It differs from the S-R latch because it has only one input in addition to EN. This input is called the D (data) input.
- When the D input is HIGH and the EN input is HIGH, the latch will set. When the D input is LOW and EN is HIGH, the latch will reset. Stated another way, the output Q follows the input D when EN is HIGH.

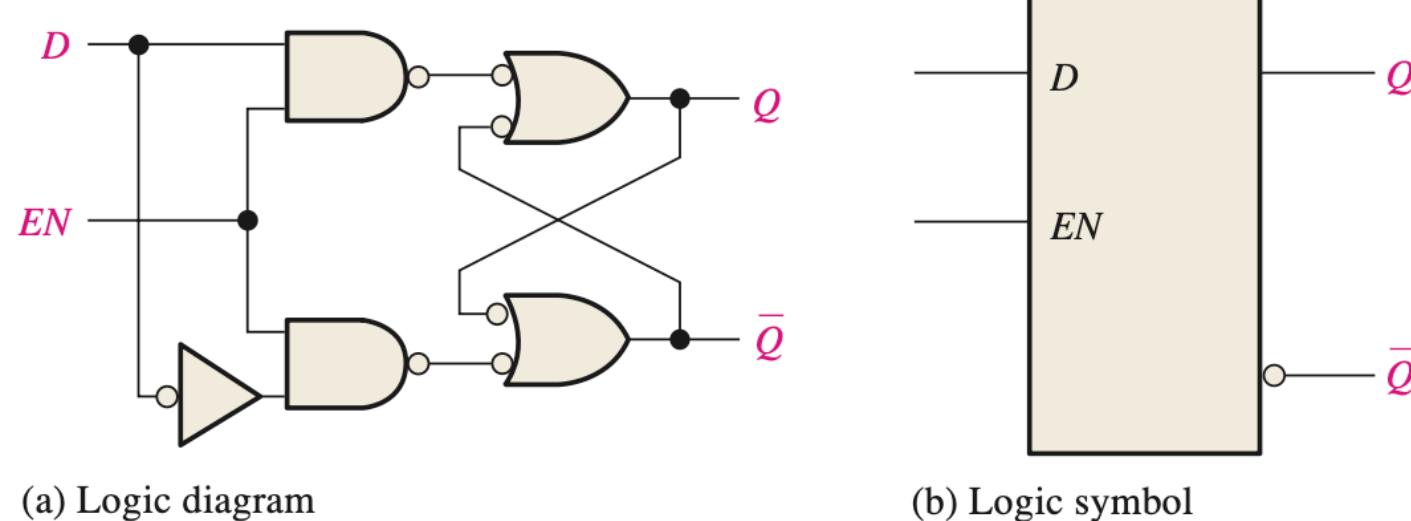


FIGURE 7-10 A gated D latch. Open file F07-10 and verify the operation.

EXAMPLE 7-3

Determine the Q output waveform if the inputs shown in Figure 7-11(a) are applied to a gated D latch, which is initially RESET.

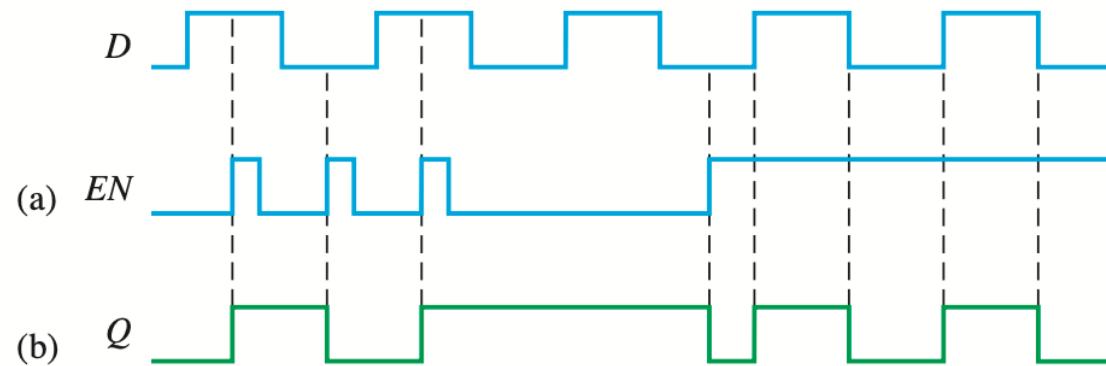


FIGURE 7-11

Solution

The Q waveform is shown in Figure 7-11(b). When D is HIGH and EN is HIGH, Q goes HIGH. When D is LOW and EN is HIGH, Q goes LOW. When EN is LOW, the state of the latch is not affected by the D input.

2. Flip-Flops

- Flip-flops are synchronous bistable devices, also known as bistable multivibrators.
- An edge-triggered flip-flop changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.

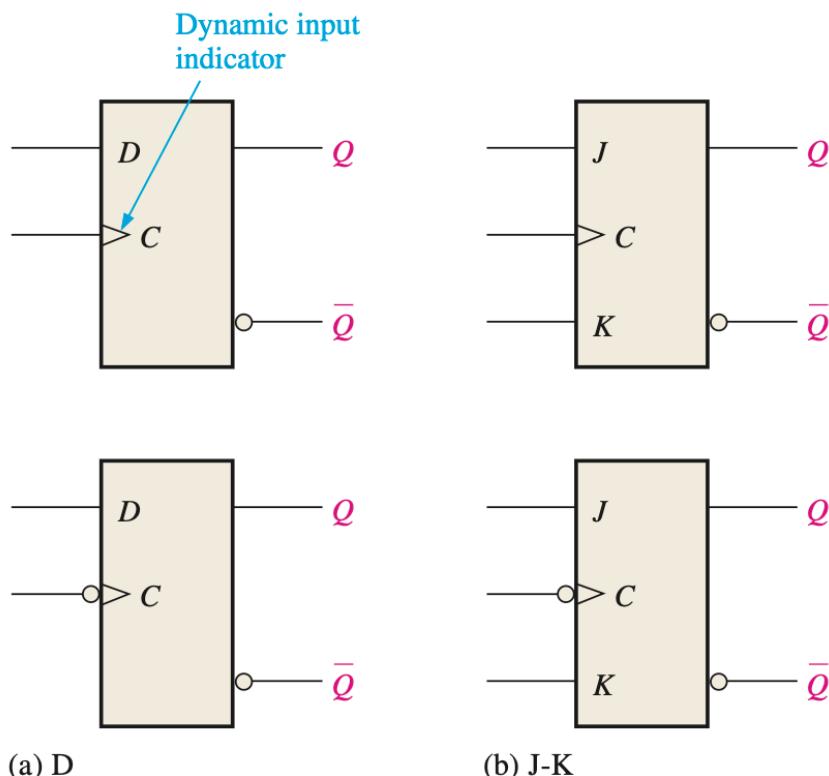


FIGURE 7-13 Edge-triggered flip-flop logic symbols (top: positive edge-triggered; bottom: negative edge-triggered).

The D Flip-Flop

- The D input of the D flip-flop is a synchronous input because data on the input are transferred to the flip-flop's output only on the triggering edge of the clock pulse.
- When D is HIGH, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.
- When D is LOW, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.

TABLE 7-2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		Comments
D	CLK	Q	\bar{Q}	
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

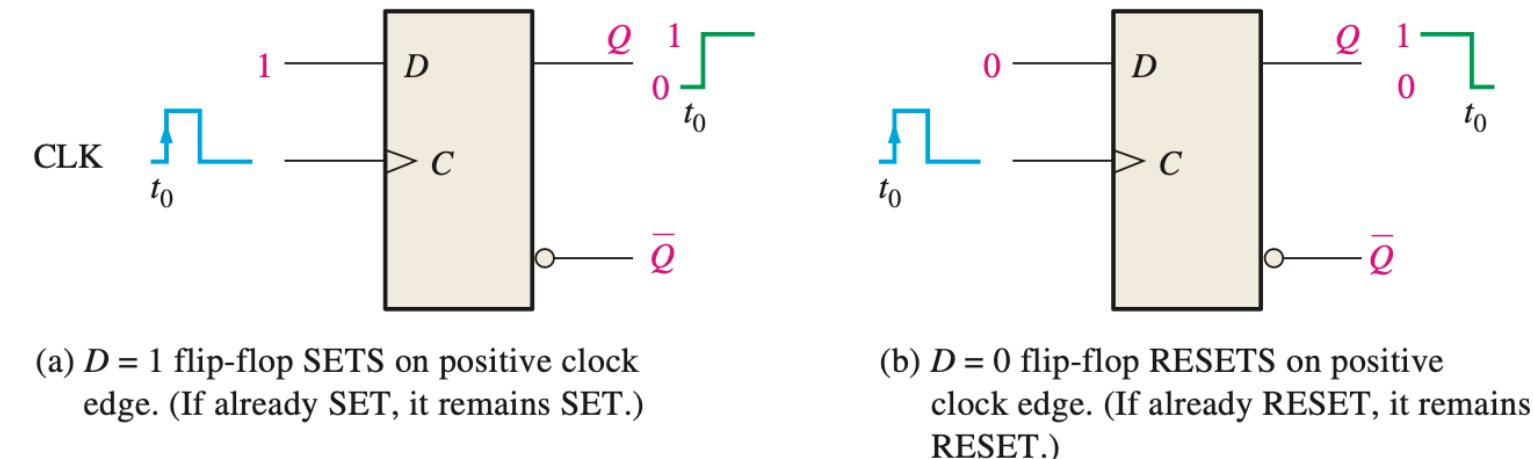


FIGURE 7-14 Operation of a positive edge-triggered D flip-flop.

Determine the Q and \bar{Q} output waveforms of the flip-flop in Figure 7-15 for the D and CLK inputs in Figure 7-16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

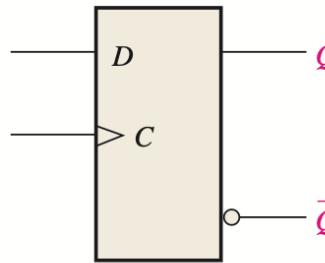


FIGURE 7-15

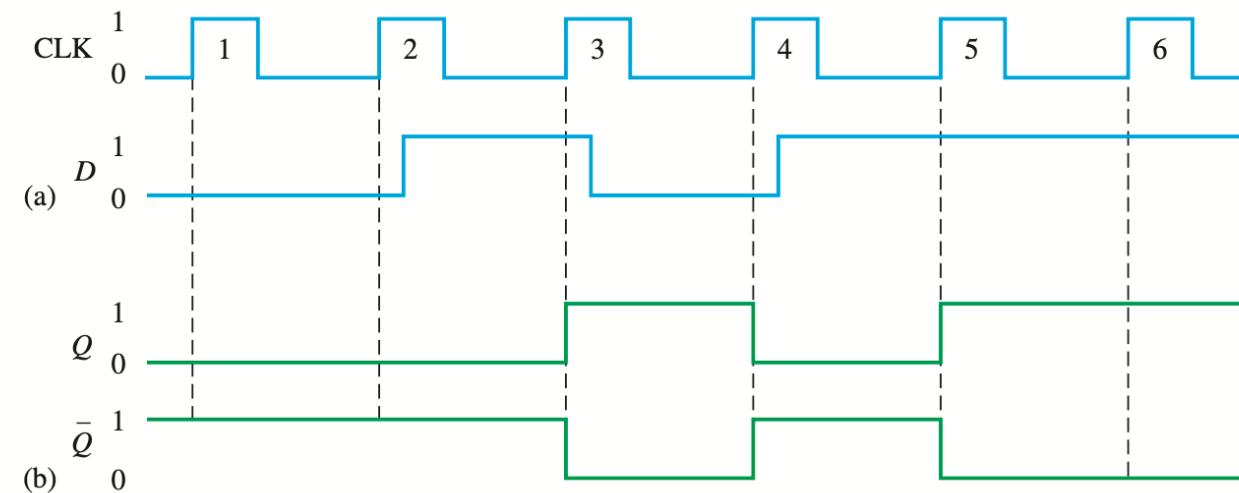


FIGURE 7-16

Solution

1. At clock pulse 1, D is LOW, so Q remains LOW (RESET).
2. At clock pulse 2, D is LOW, so Q remains LOW (RESET).
3. At clock pulse 3, D is HIGH, so Q goes HIGH (SET).
4. At clock pulse 4, D is LOW, so Q goes LOW (RESET).
5. At clock pulse 5, D is HIGH, so Q goes HIGH (SET).
6. At clock pulse 6, D is HIGH, so Q remains HIGH (SET).

Once Q is determined, \bar{Q} is easily found since it is simply the complement of Q . The resulting waveforms for Q and \bar{Q} are shown in Figure 7-16(b) for the input waveforms in part (a).

The J-K Flip-Flop

- The J and K inputs of the J-K flip-flop are synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse.
- When J is HIGH and K is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.
- When J is LOW and K is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.
- When both J and K are LOW, the output does not change from its prior state.
- When J and K are both HIGH, the flip-flop changes state. This called the toggle mode.

The J-K Flip-Flop

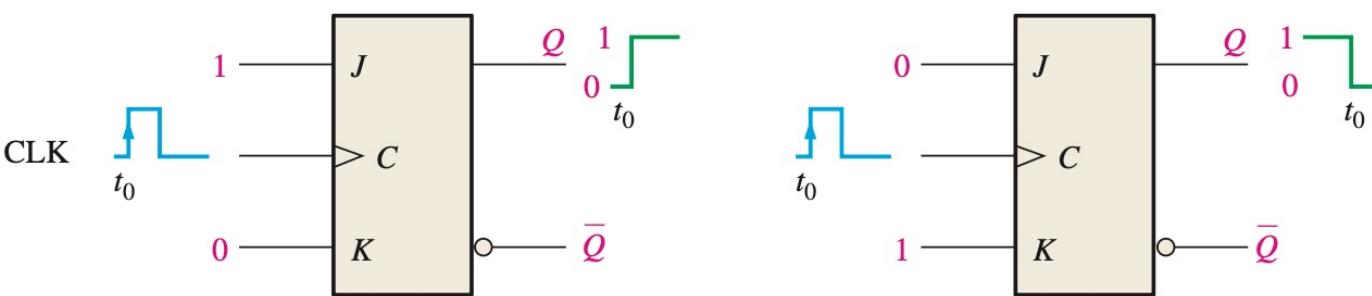
TABLE 7-3

Truth table for a positive edge-triggered J-K flip-flop.

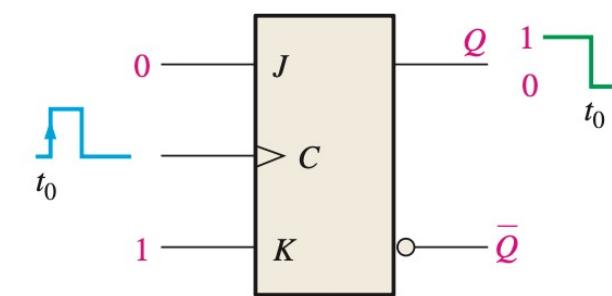
Inputs			Outputs		Comments
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	\bar{Q}_0	Q_0	Toggle

↑ = clock transition LOW to HIGH

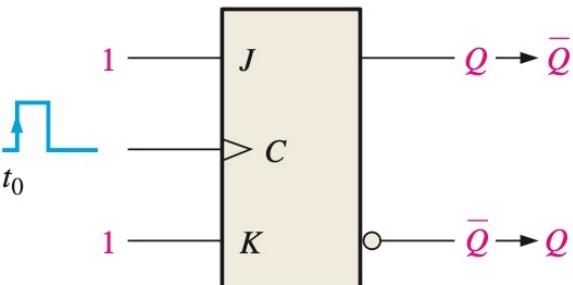
Q_0 = output level prior to clock transition



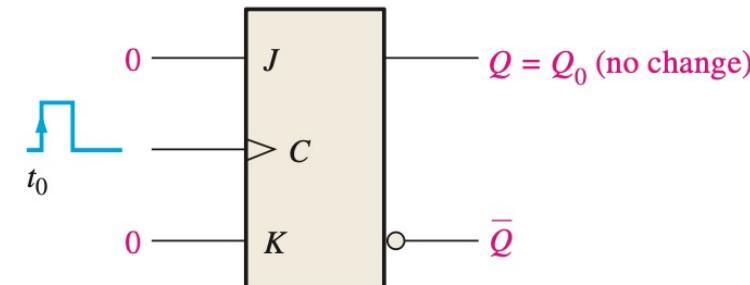
(a) $J = 1, K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0, K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1, K = 1$ flip-flop changes state (toggle).



(d) $J = 0, K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

FIGURE 7-17 Operation of a positive edge-triggered J-K flip-flop.

EXAMPLE 7-5

The waveforms in Figure 7–18(a) are applied to the J , K , and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.

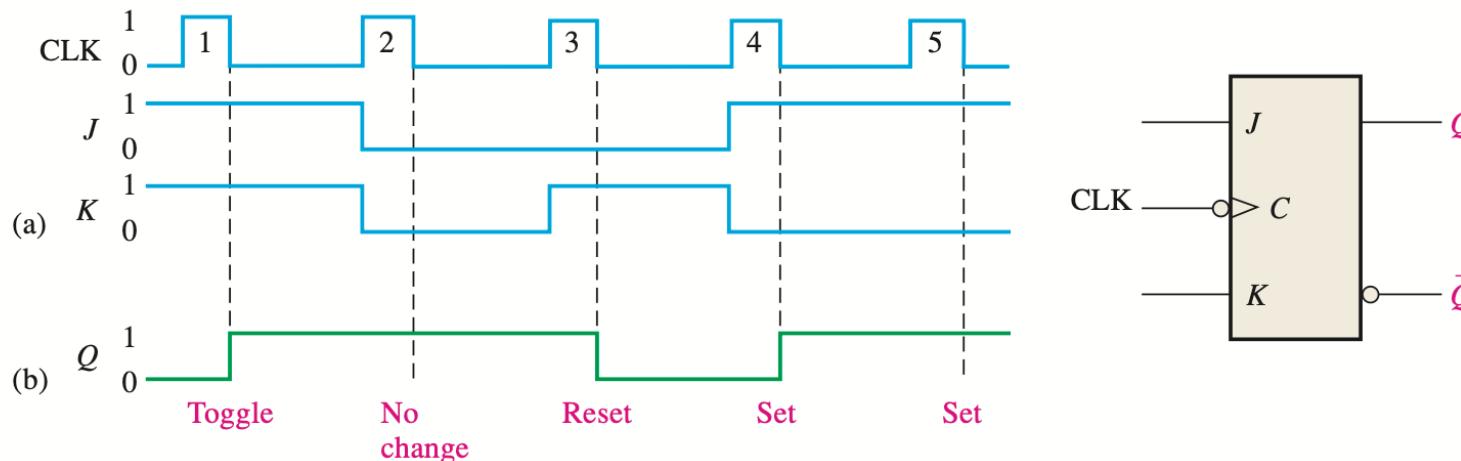


FIGURE 7-18

Solution

Since this is a negative edge-triggered flip-flop, as indicated by the “bubble” at the clock input, the Q output will change only on the negative-going edge of the clock pulse.

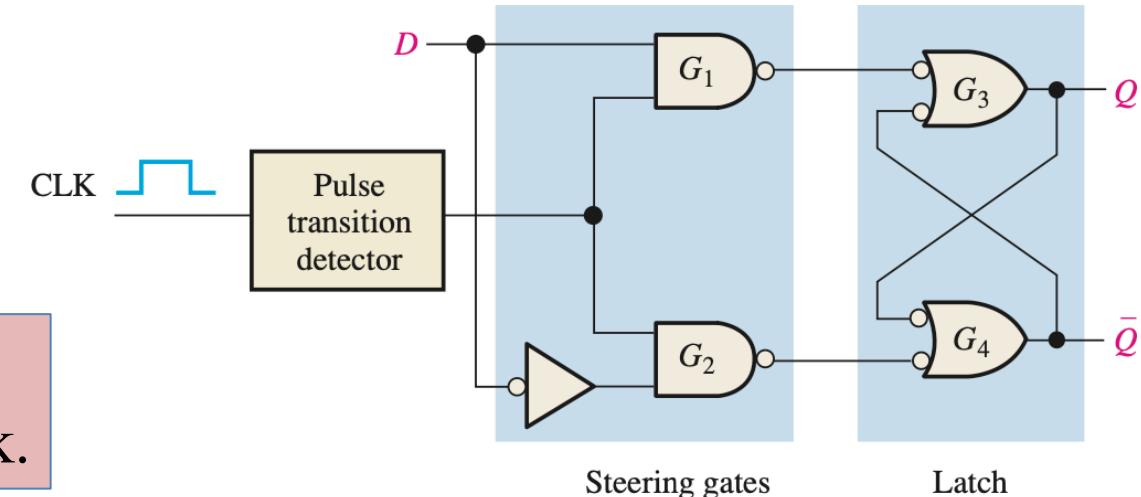
1. At the first clock pulse, both J and K are HIGH; and because this is a toggle condition, Q goes HIGH.
2. At clock pulse 2, a no-change condition exists on the inputs, keeping Q at a HIGH level.
3. When clock pulse 3 occurs, J is LOW and K is HIGH, resulting in a RESET condition; Q goes LOW.
4. At clock pulse 4, J is HIGH and K is LOW, resulting in a SET condition; Q goes HIGH.
5. A SET condition still exists on J and K when clock pulse 5 occurs, so Q will remain HIGH.

The resulting Q waveform is indicated in Figure 7–18(b).

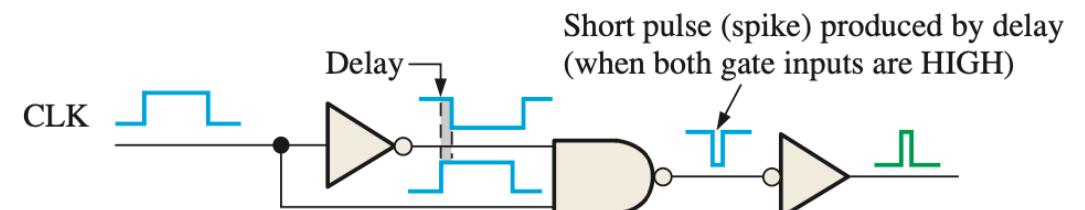
Edge-Triggered Operation

D Flip-Flop

The Q output of a D flip-flop assumes the state of the D input on the triggering edge of the clock.



(a) A simplified logic diagram for a positive edge-triggered D flip-flop



(b) A type of pulse transition detector

FIGURE 7-19 Edge triggering.

D Flip-Flop

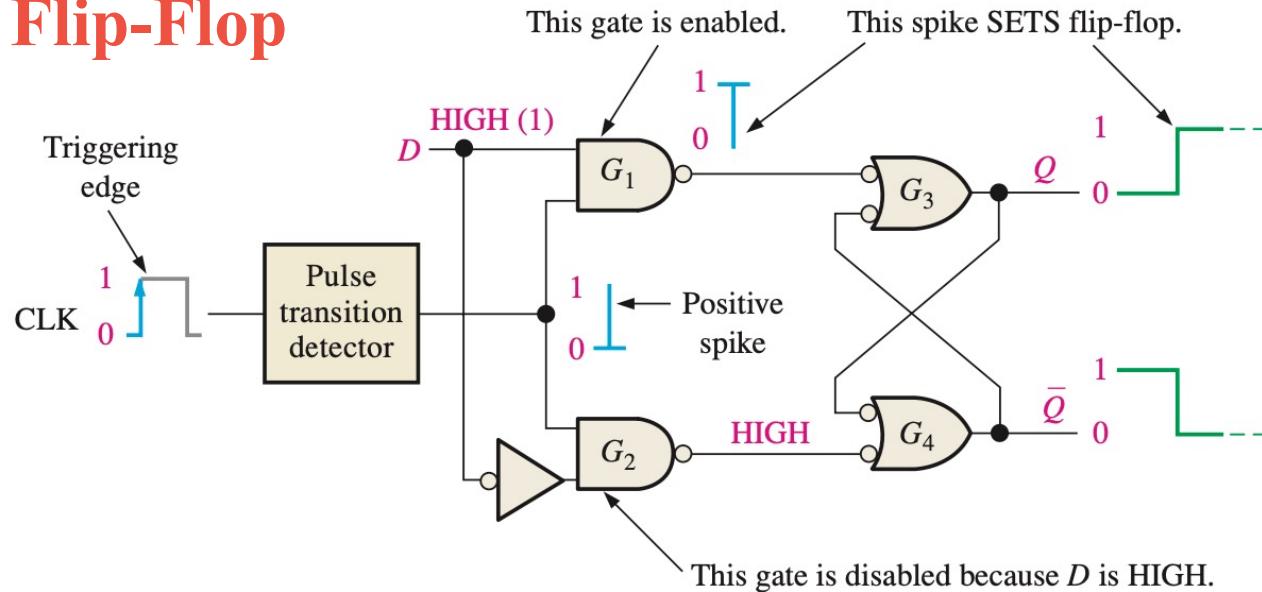


FIGURE 7-20 Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

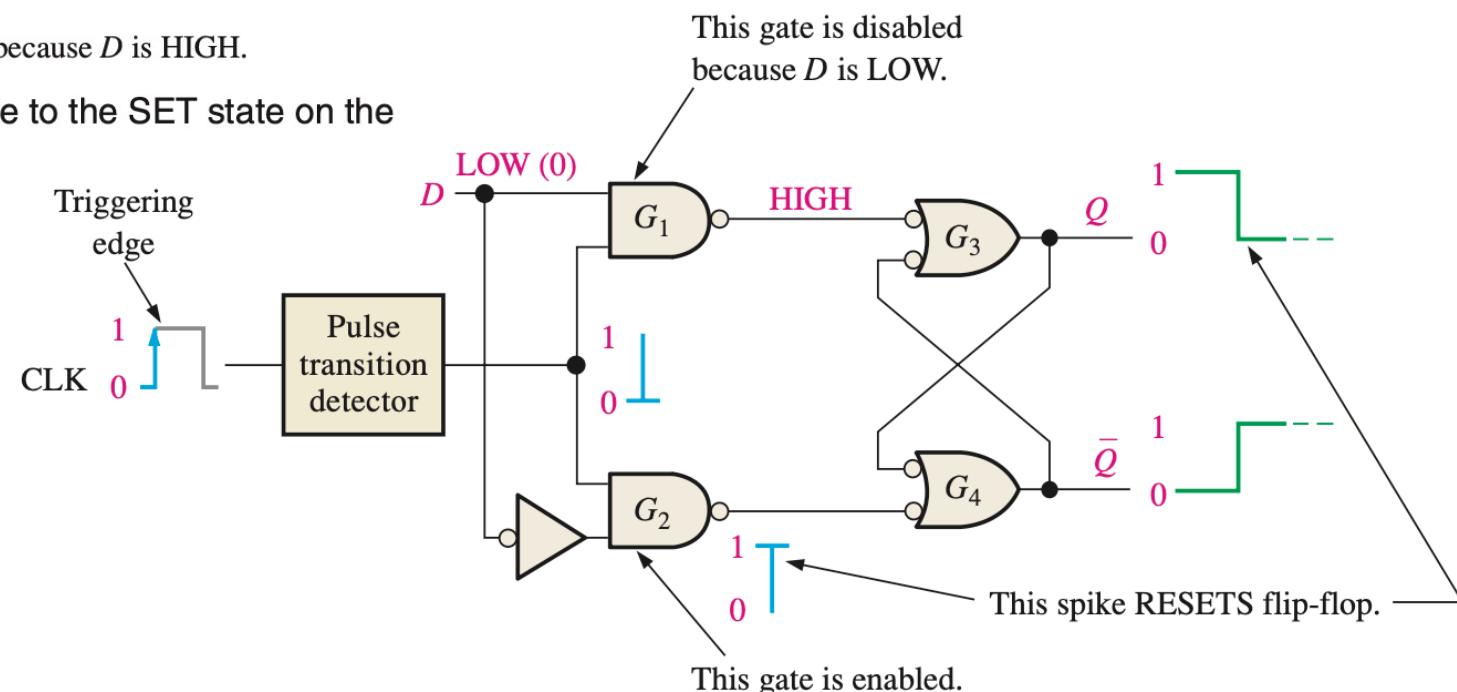


FIGURE 7-21 Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.

EXAMPLE 7-6

Given the waveforms in Figure 7–22(a) for the D input and the clock, determine the Q output waveform if the flip-flop starts out RESET.

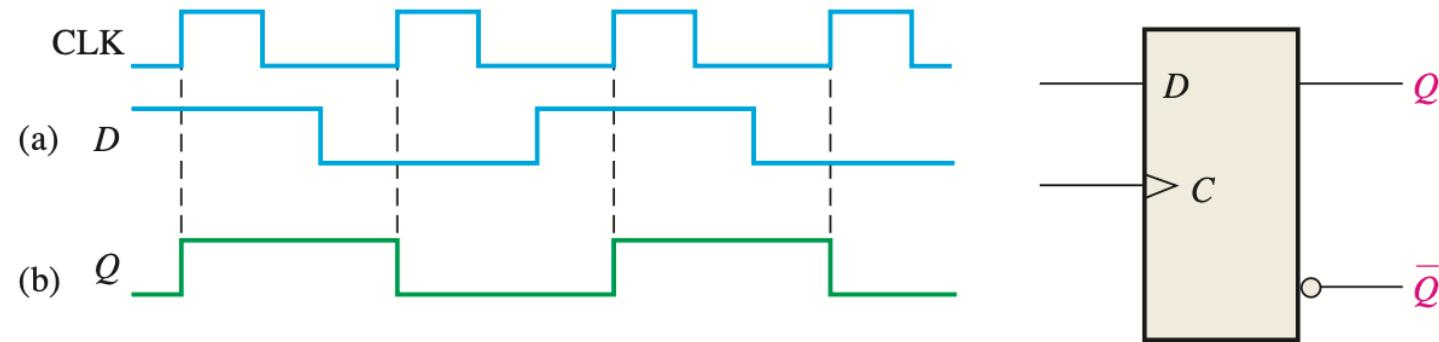


FIGURE 7-22

Solution

The Q output goes to the state of the D input at the time of the positive-going clock edge. The resulting output is shown in Figure 7–22(b).

J-K Flip-Flop

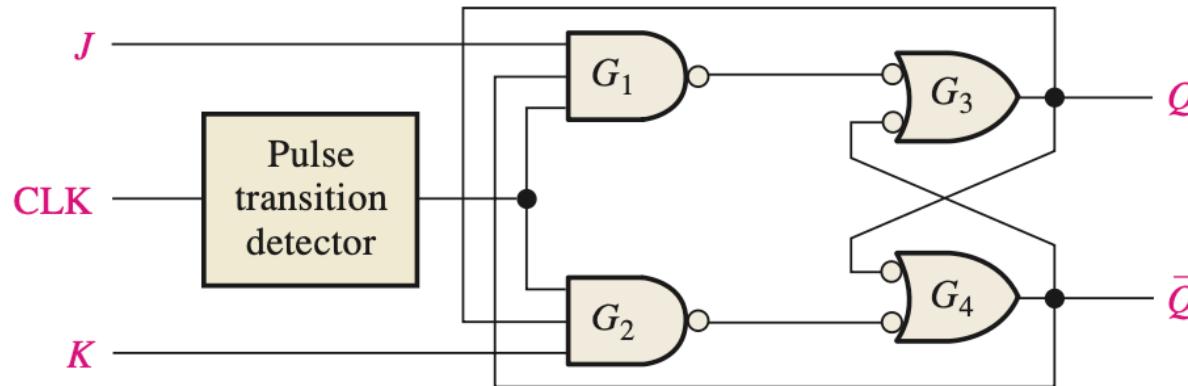


FIGURE 7-23 A simplified logic diagram for a positive edge-triggered J-K flip-flop.

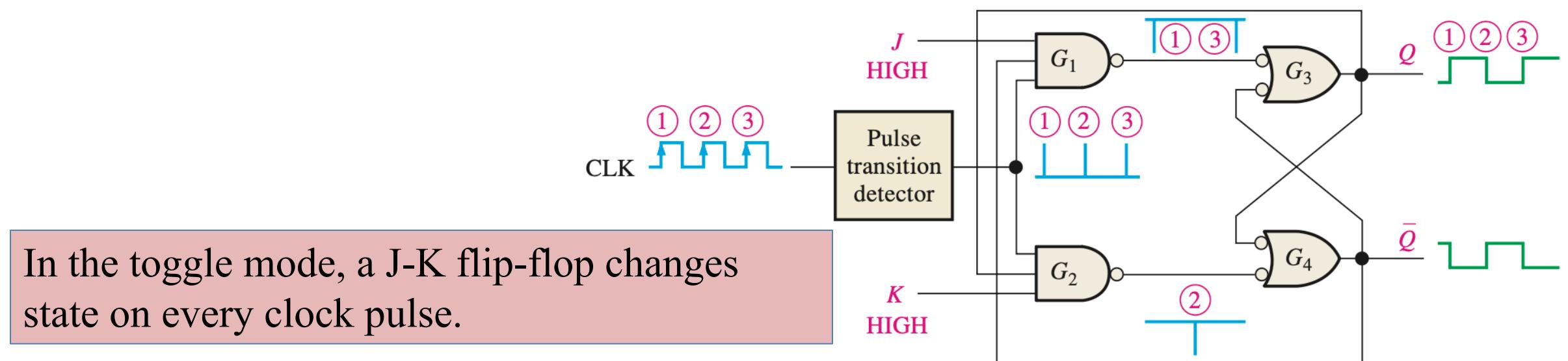


FIGURE 7-24 Transitions illustrating flip-flop operation.

Asynchronous Preset and Clear Inputs

- Most integrated circuit flip-flops also have asynchronous inputs. These are inputs that affect the state of the flip-flop independent of the clock. They are normally labeled **preset** (PRE) and **clear** (CLR), or direct set (S_D) and direct reset (R_D) by some manufacturers. An active level on the preset input will set the flip-flop, and an active level on the clear input will reset it.

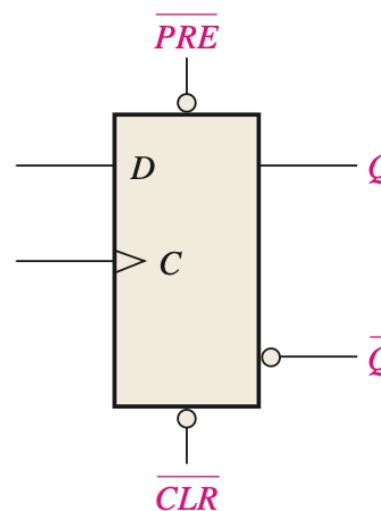


FIGURE 7-25 Logic symbol for a D flip-flop with active-LOW preset and clear inputs.

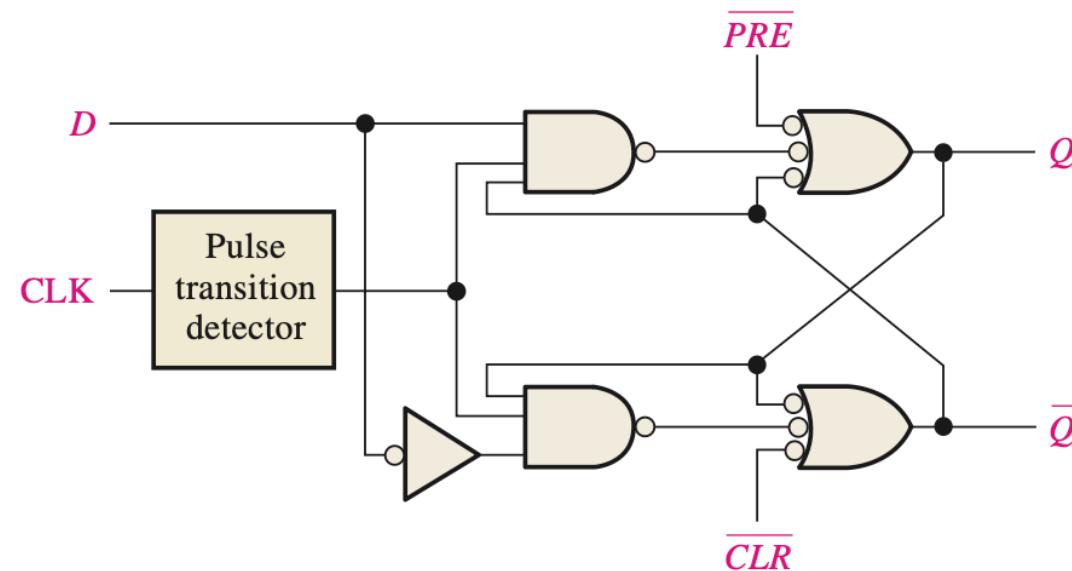


FIGURE 7-26 Logic diagram for a basic D flip-flop with active-LOW preset and clear inputs.

EXAMPLE 7-7

For the positive edge-triggered D flip-flop with preset and clear inputs in Figure 7-27, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially LOW.

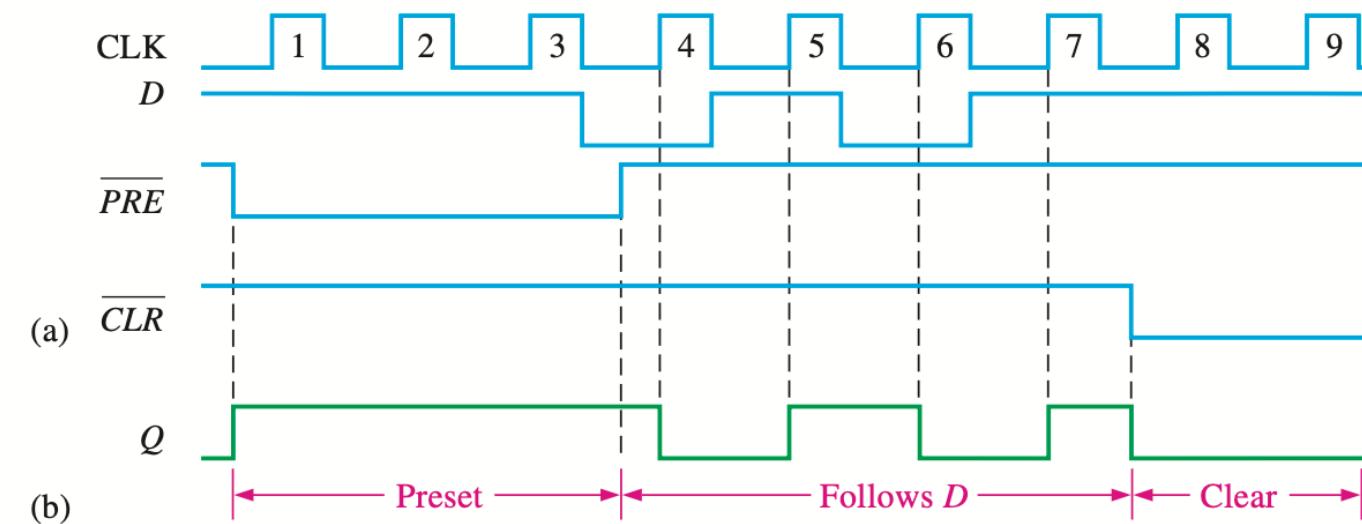
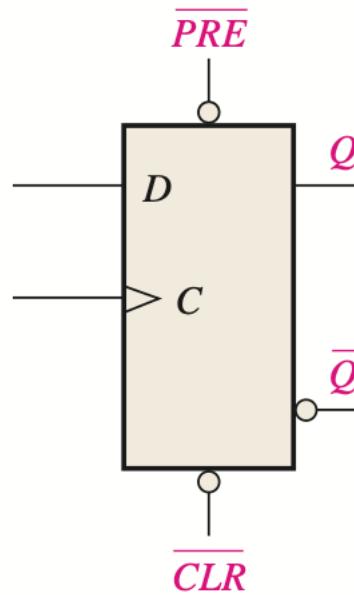


FIGURE 7-27 Open file F07-27 to verify the operation.

Solution

1. During clock pulses 1, 2, and 3, the preset (\overline{PRE}) is LOW, keeping the flip-flop SET regardless of the synchronous D input.
2. For clock pulses 4, 5, 6, and 7, the output follows the input on the clock pulse because both \overline{PRE} and \overline{CLR} are HIGH.
3. For clock pulses 8 and 9, the clear (\overline{CLR}) input is LOW, keeping the flip-flop RESET regardless of the synchronous inputs.

The resulting Q output is shown in Figure 7-27(b).

3. Flip-Flop Operating Characteristics

Propagation Delay Times

A propagation delay time is the interval of time required after an input signal has been applied for the resulting output change to occur. Four categories of propagation delay times are important in the operation of a flip-flop:

1. Propagation delay t_{PLH} as measured from the triggering edge of the clock pulse to the LOW-to-HIGH transition of the output.
2. Propagation delay t_{PHL} as measured from the triggering edge of the clock pulse to the HIGH-to-LOW transition of the output.
3. Propagation delay t_{PLH} as measured from the leading edge of the preset input to the LOW-to-HIGH transition of the output.
4. Propagation delay t_{PHL} as measured from the leading edge of the clear input to the HIGH-to-LOW transition of the output.

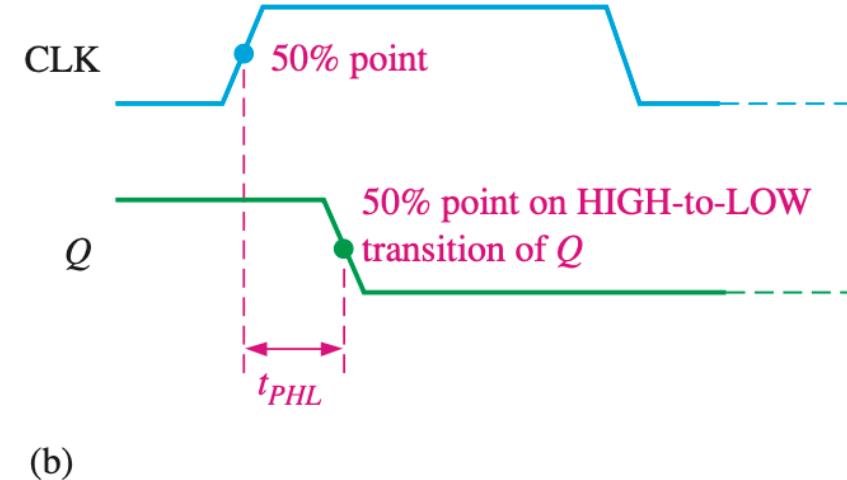
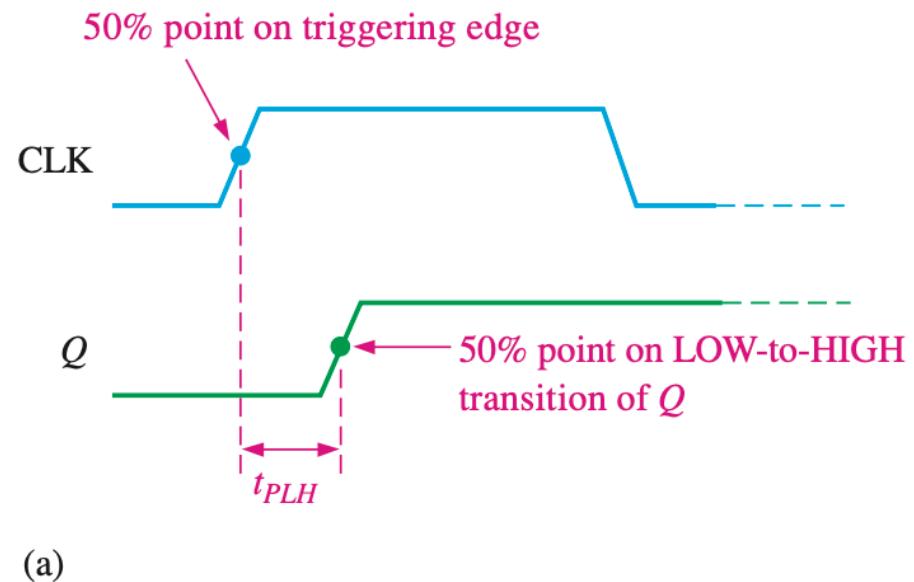


FIGURE 7–31 Propagation delays, clock to output.

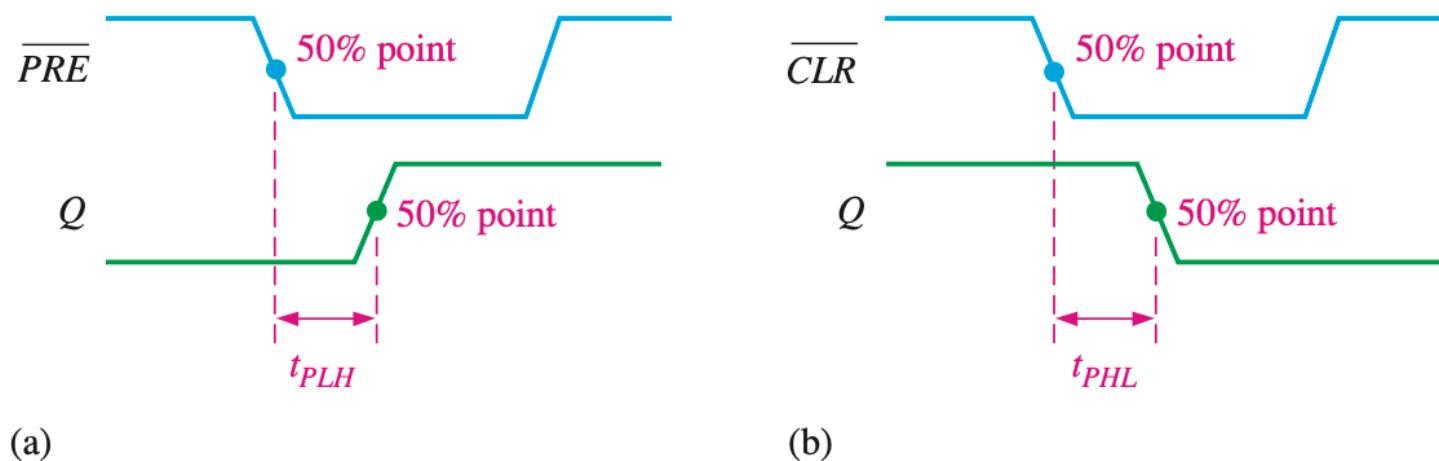


FIGURE 7–32 Propagation delays, preset input to output and clear input to output.

Set-up Time

The **set-up time** (t_s) is the minimum interval required for the logic levels to be maintained constantly on the inputs (J and K, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.

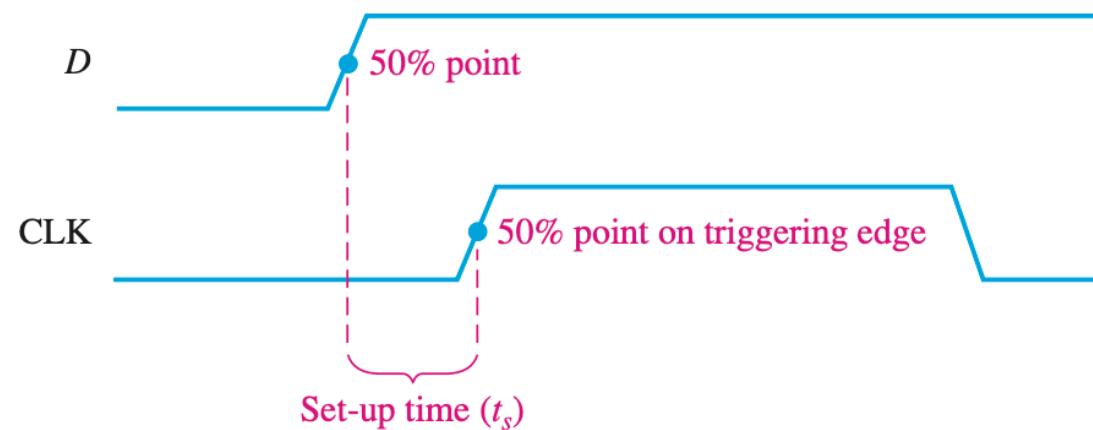


FIGURE 7-33 Set-up time (t_s). The logic level must be present on the D input for a time equal to or greater than t_s before the triggering edge of the clock pulse for reliable data entry.

Hold Time

The **hold time** (t_h) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.

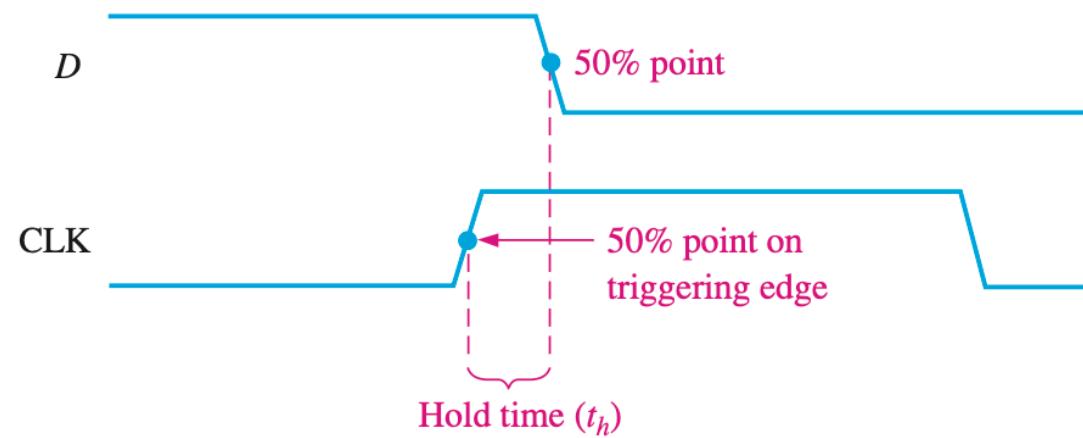


FIGURE 7–34 Hold time (t_h). The logic level must remain on the *D* input for a time equal to or greater than t_h after the triggering edge of the clock pulse for reliable data entry.

Maximum Clock Frequency

The maximum clock frequency (f_{\max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths

Minimum pulse widths (t_w) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The power dissipation of any digital circuit is the total power consumption of the device.

$$P = V_{CC} \times I_{CC}$$

Comparison of Specific Flip-Flops

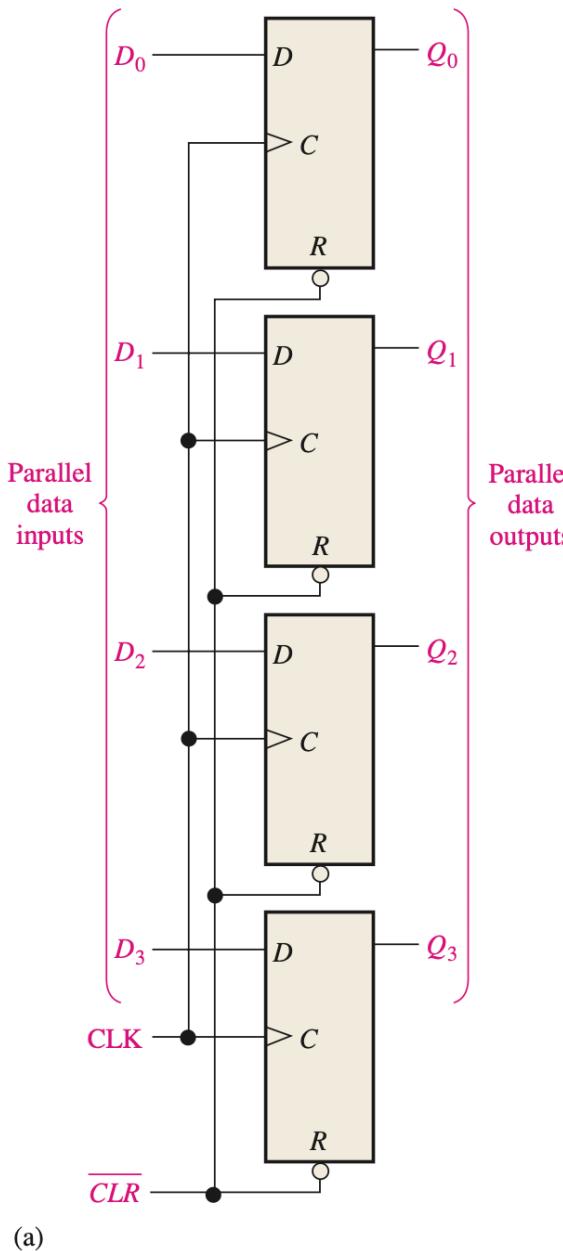
TABLE 7-4

Comparison of operating parameters for four IC families of flip-flops of the same type at 25°C.

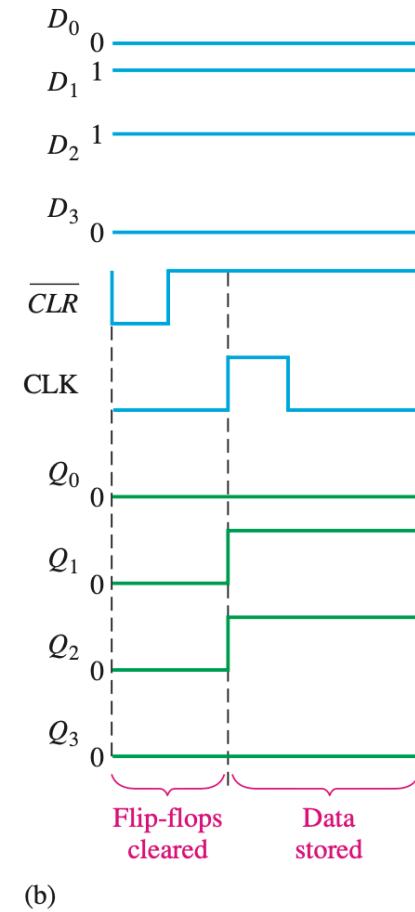
Parameter	CMOS		Bipolar (TTL)	
	74HC74A	74AHC74	74LS74A	74F74
t_{PHL} (CLK to Q)	17 ns	4.6 ns	40 ns	6.8 ns
t_{PLH} (CLK to Q)	17 ns	4.6 ns	25 ns	8.0 ns
$t_{PHL}(\overline{CLR}$ to Q)	18 ns	4.8 ns	40 ns	9.0 ns
$t_{PLH}(\overline{PRE}$ to Q)	18 ns	4.8 ns	25 ns	6.1 ns
t_s (set-up time)	14 ns	5.0 ns	20 ns	2.0 ns
t_h (hold time)	3.0 ns	0.5 ns	5 ns	1.0 ns
t_W (CLK HIGH)	10 ns	5.0 ns	25 ns	4.0 ns
t_W (CLK LOW)	10 ns	5.0 ns	25 ns	5.0 ns
$t_W(\overline{CLR}/\overline{PRE})$	10 ns	5.0 ns	25 ns	4.0 ns
f_{max}	35 MHz	170 MHz	25 MHz	100 MHz
Power, quiescent	0.012 mW	1.1 mW		
Power, 50% duty cycle			44 mW	88 mW

4. Flip-Flop Applications

Parallel Data Storage



(a)



(b)

FIGURE 7-35 Example of flip-flops used in a basic register for parallel data storage.

Frequency Division

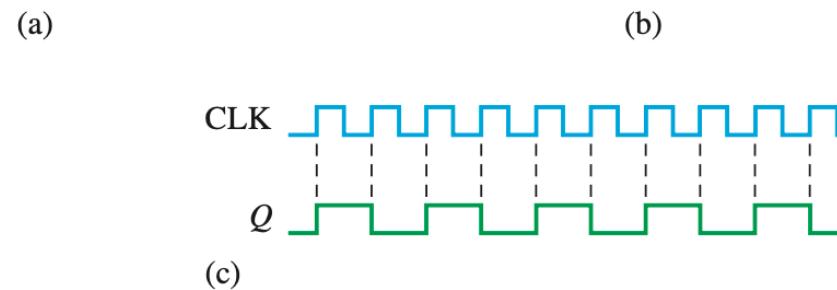
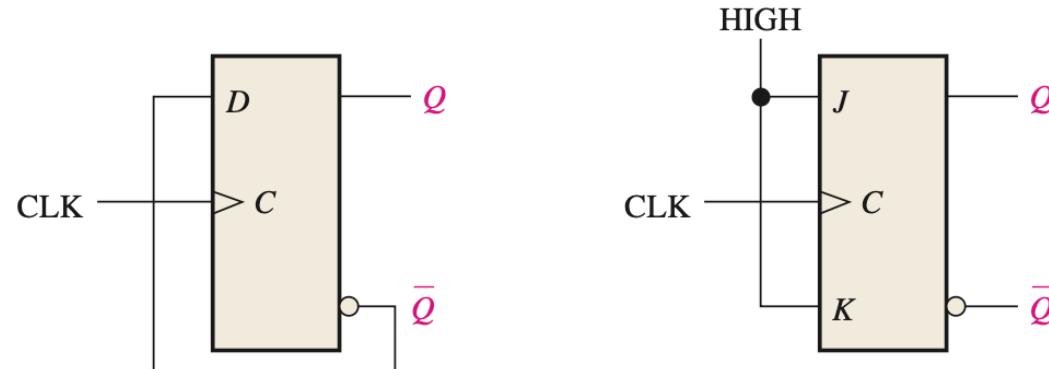


FIGURE 7-36 The D flip-flop and J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK. Open file F07-36 and verify the operation.

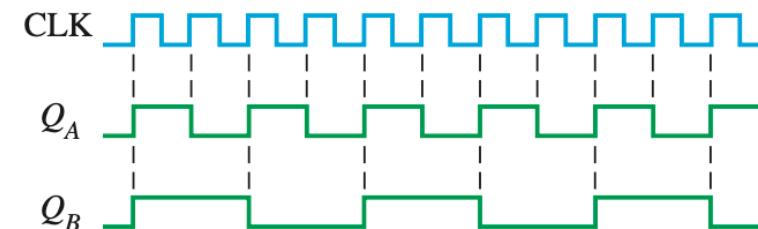
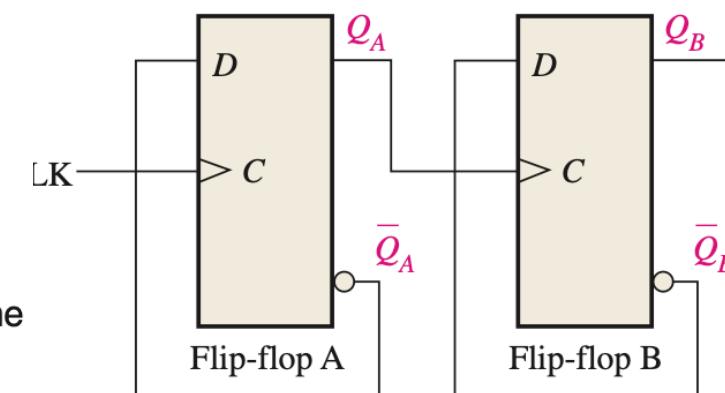
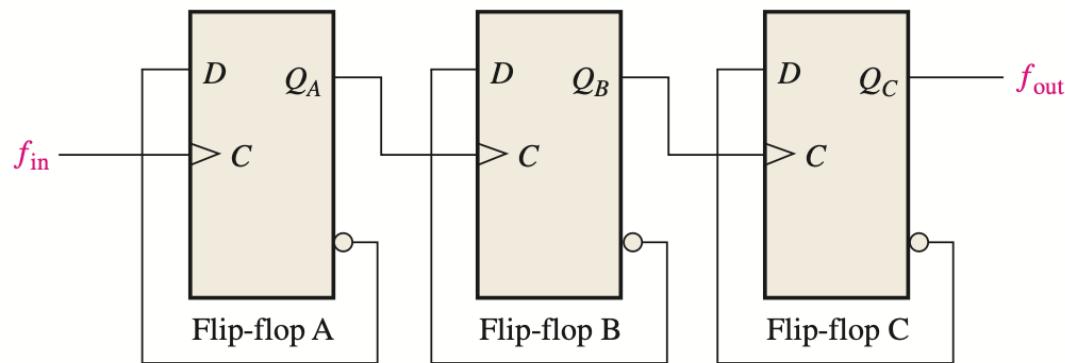
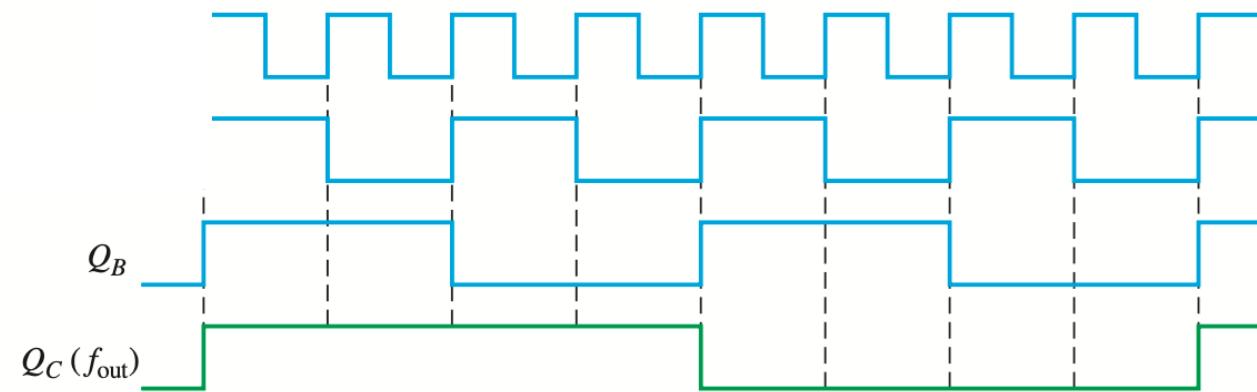


FIGURE 7-37 Example of two D flip-flops used to divide the clock frequency by 4. Q_A is one-half and Q_B is one-fourth the frequency of CLK. Open file F07-37 and verify the operation.

EXAMPLE 7-9

Develop the f_{out} waveform for the circuit in Figure 7-38 when an 8 kHz square wave input is applied to the clock input of flip-flop A.

**FIGURE 7-38****FIGURE 7-39****Solution**

The three flip-flops are connected to divide the input frequency by eight ($2^3 = 8$) and the $Q_C(f_{\text{out}})$ waveform is shown in Figure 7-39. Since these are positive edge-triggered flip-flops, the outputs change on the positive-going clock edge. There is one output pulse for every eight input pulses, so the output frequency is 1 kHz. Waveforms of Q_A and Q_B are also shown.

Counting

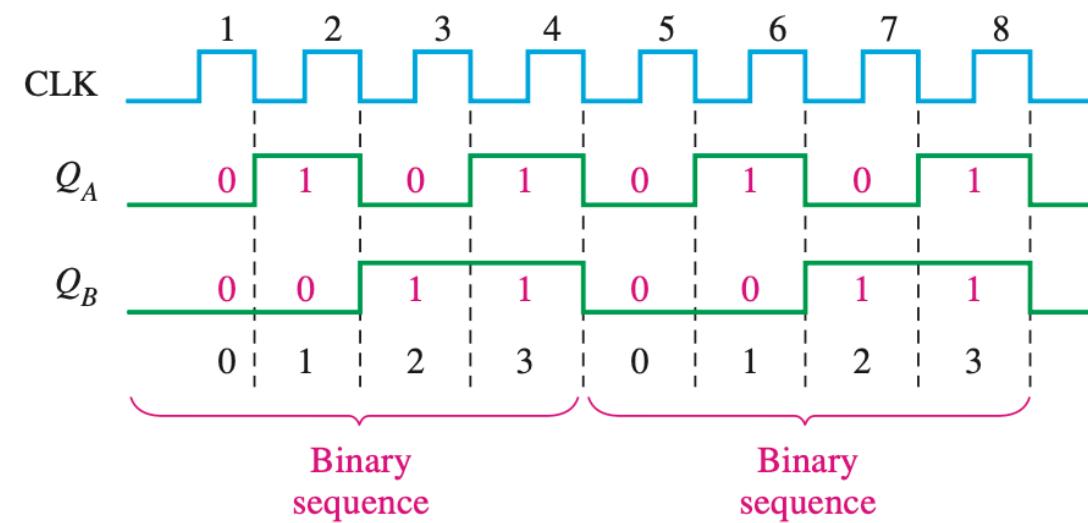
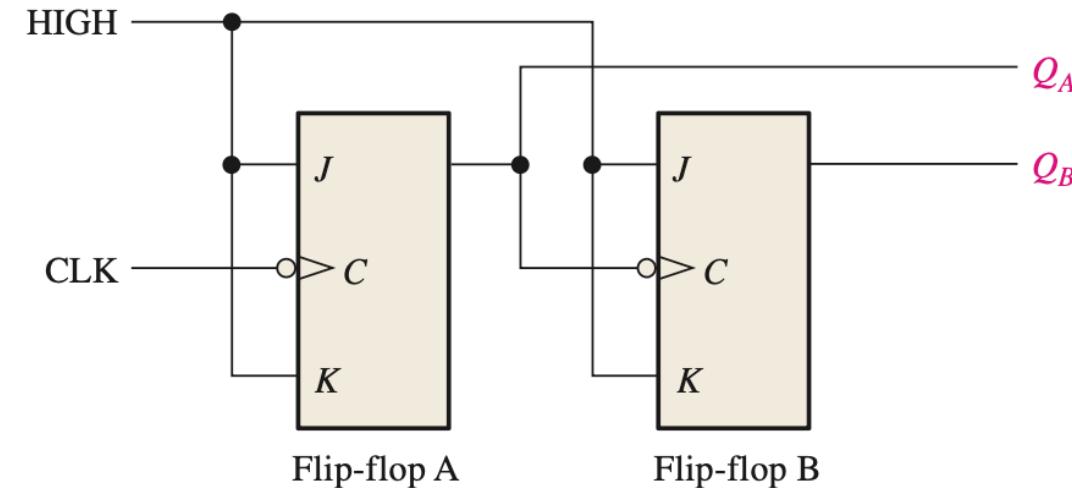
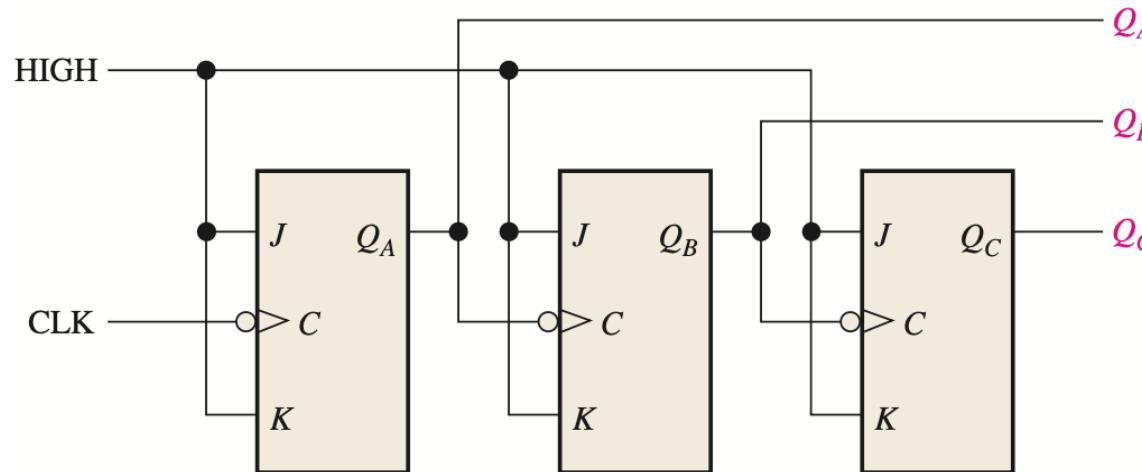


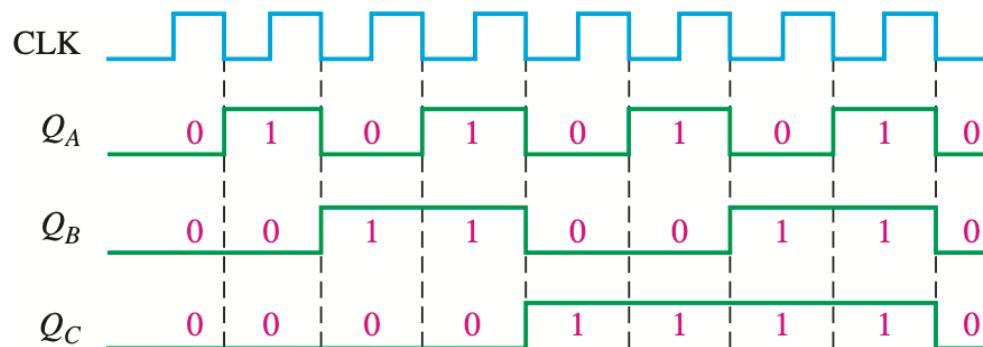
FIGURE 7-40 J-K flip-flops used to generate a binary count sequence (00, 01, 10, 11). Two repetitions are shown.

EXAMPLE 7-10

Determine the output waveforms in relation to the clock for Q_A , Q_B , and Q_C in the circuit of Figure 7-41 and show the binary sequence represented by these waveforms.

**FIGURE 7-41****Solution**

The output timing diagram is shown in Figure 7-42. Notice that the outputs change on the negative-going edge of the clock pulses. The outputs go through the binary sequence 000, 001, 010, 011, 100, 101, 110, and 111 as indicated.

**FIGURE 7-42**

5. One-Shots

- The one-shot, also known as a monostable multivibrator, is a device with only one stable state.
- A one-shot is normally in its stable state and will change to its unstable state only when triggered.
- Once it is triggered, the one-shot remains in its unstable state for a predetermined length of time and then automatically returns to its stable state.
- The time that the device stays in its unstable state determines the pulse width of its output.

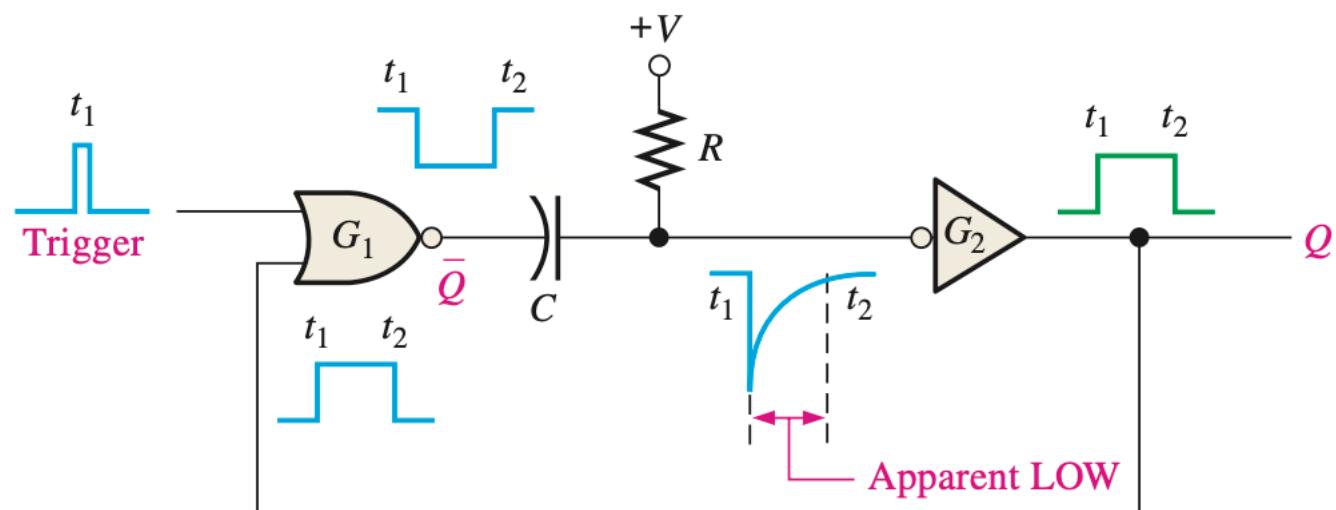


FIGURE 7–43 A simple one-shot circuit.

5. One-Shots

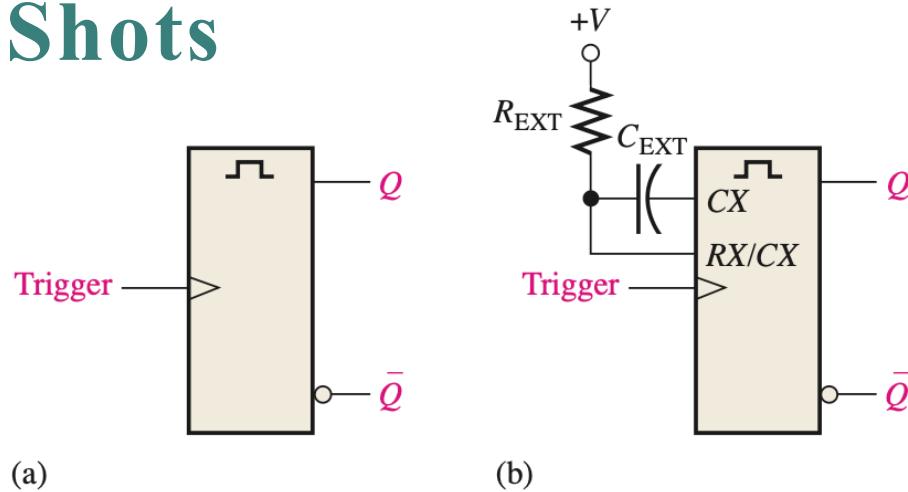


FIGURE 7-44 Basic one-shot logic symbols. CX and RX stand for external components.

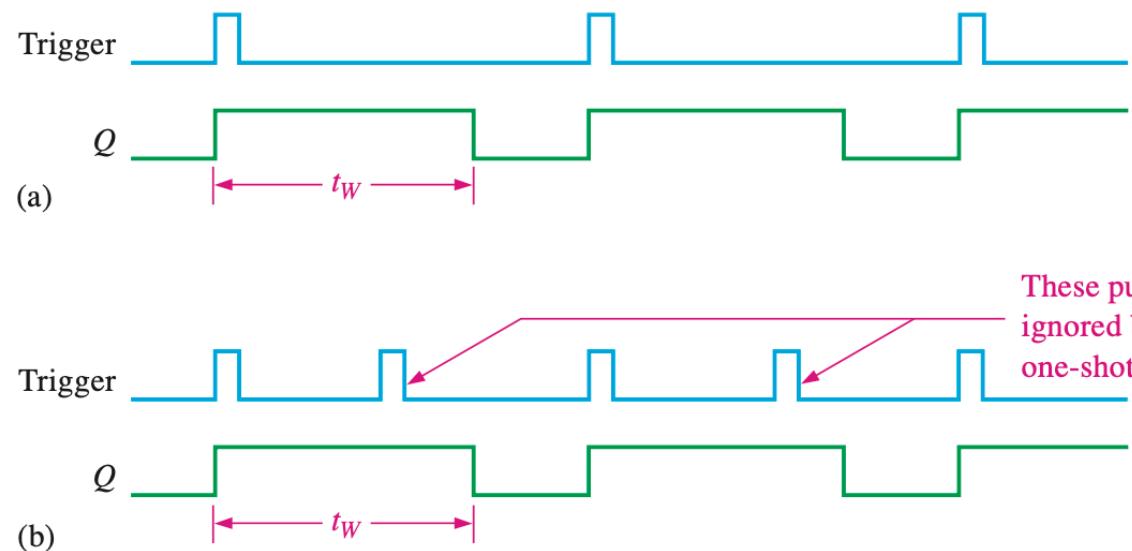


FIGURE 7-45 Nonretriggerable one-shot action.

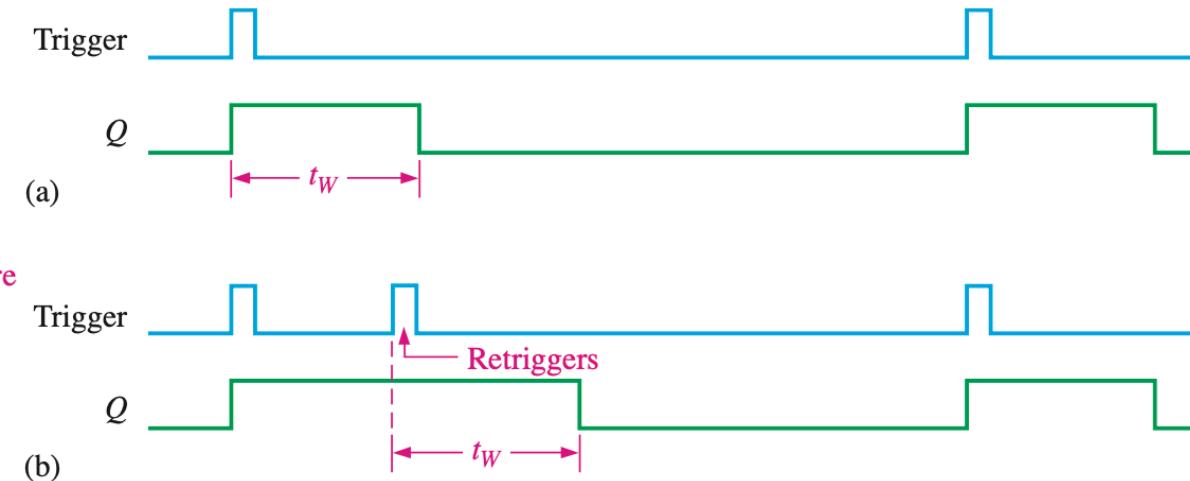


FIGURE 7-46 Retriggerable one-shot action.

6. The Astable Multivibrator

- An astable multivibrator is a device that has no stable states; it changes back and forth (oscillates) between two unstable states without any external triggering.
- The resulting output is typically a square wave that is used as a clock signal in many types of sequential logic circuits.
- Astable multivibrators are also known as pulse oscillators.

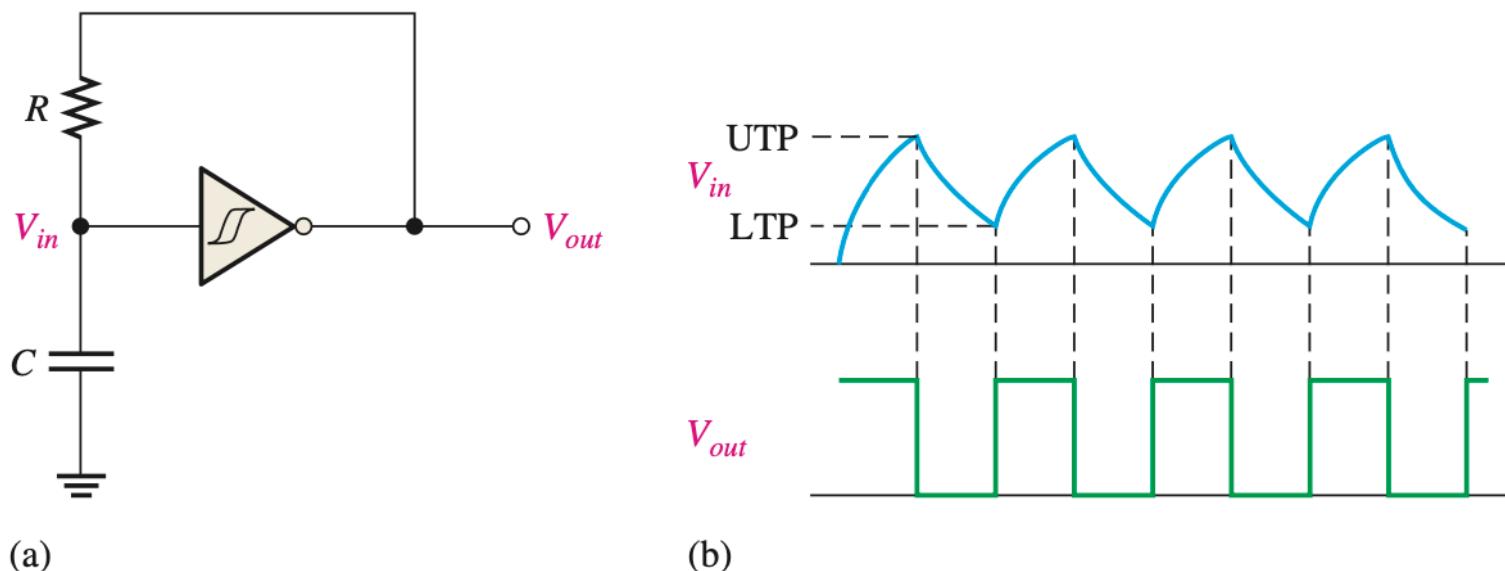


FIGURE 7-55 Basic astable multivibrator using a Schmitt trigger.

The 555 Timer as an Astable Multivibrator

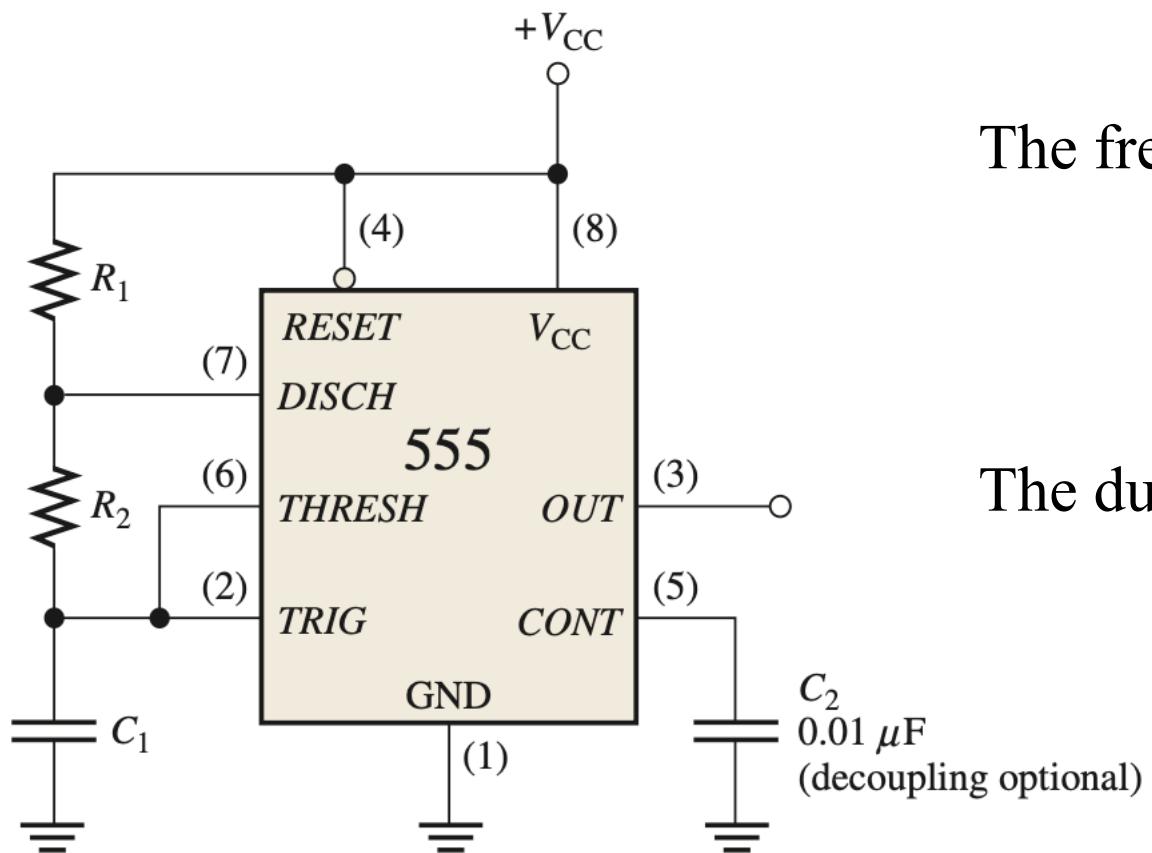


FIGURE 7–56 The 555 timer connected as an astable multivibrator (oscillator).

The frequency of oscillation is given by

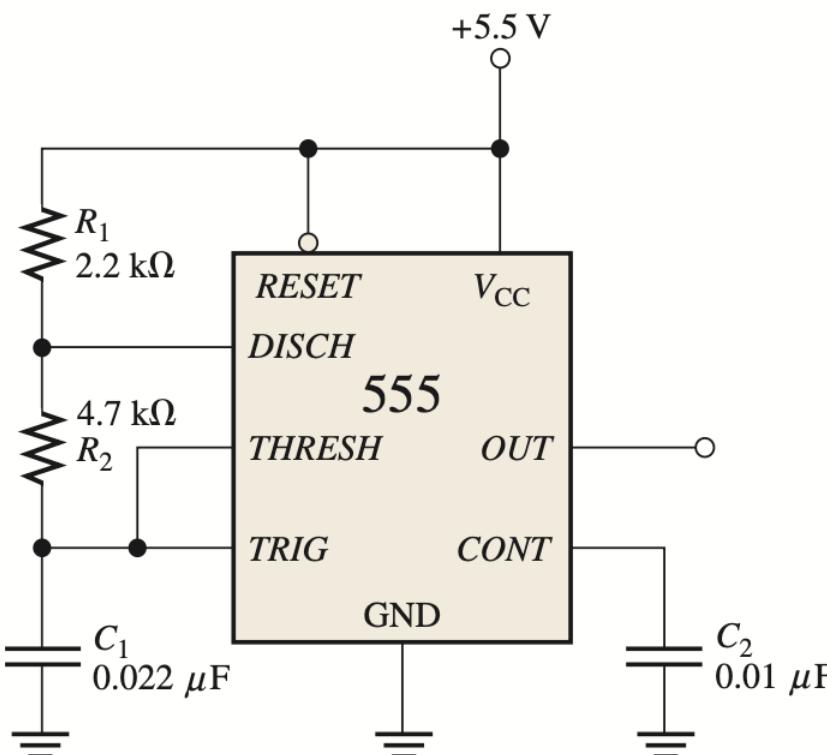
$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

The duty cycle is

$$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2} \right) 100\%$$

EXAMPLE 7-14

A 555 timer configured to run in the astable mode (pulse oscillator) is shown in Figure 7-60. Determine the frequency of the output and the duty cycle.

**FIGURE 7-60**

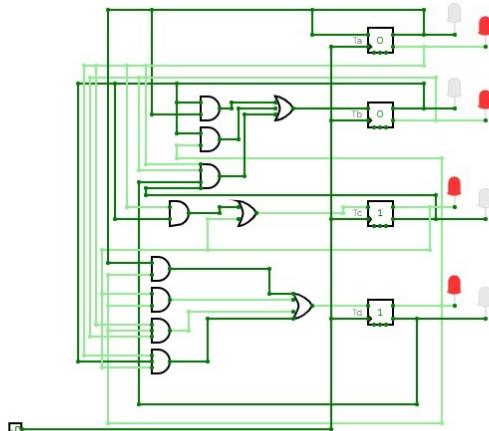
$$f = \frac{1.44}{(R_1 + 2R_2)C_1} = \frac{1.44}{(2.2 \text{ k}\Omega + 9.4 \text{ k}\Omega)0.022 \mu\text{F}} = 5.64 \text{ kHz}$$

$$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2} \right) 100\% = \left(\frac{2.2 \text{ k}\Omega + 4.7 \text{ k}\Omega}{2.2 \text{ k}\Omega + 9.4 \text{ k}\Omega} \right) 100\% = 59.5\%$$



THE END

Lecture 7: Latches, Flip-Flops, and Timers



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