



Vietnam National University HCMC
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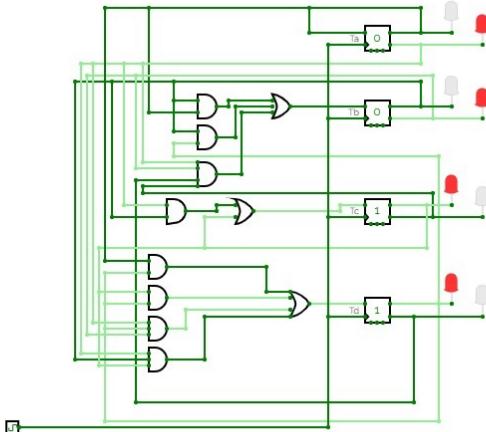


School of
Electrical Engineering

EE053IU

Digital Logic Design

Lecture 15: Integrated Circuit Technologies

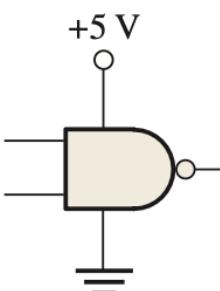


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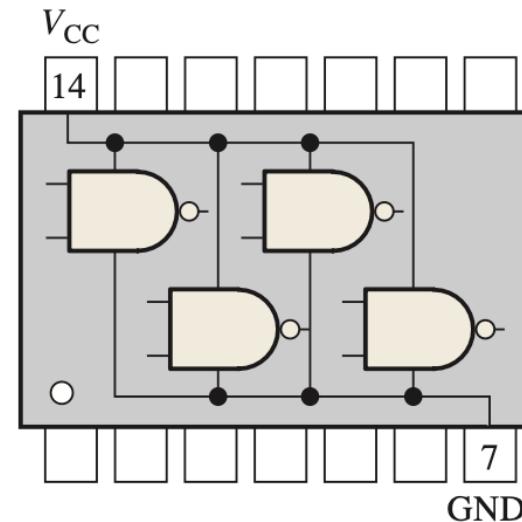
1. Basic Operational Characteristics and Parameters

DC Supply Voltage

- The nominal value of the dc supply voltage for TTL (transistor-transistor logic) devices is +5 V. TTL is also designated T²L.
- CMOS (complementary metal-oxide semiconductor) devices are available in different supply voltage categories: +5 V, +3.3 V, 2.5 V, and 1.8 V.



(a) Single gate



(b) IC dual in-line package

FIGURE 15-1 Example of V_{CC} and ground connection and distribution in an IC package. Other pin connections are omitted for simplicity.

CMOS Logic Levels

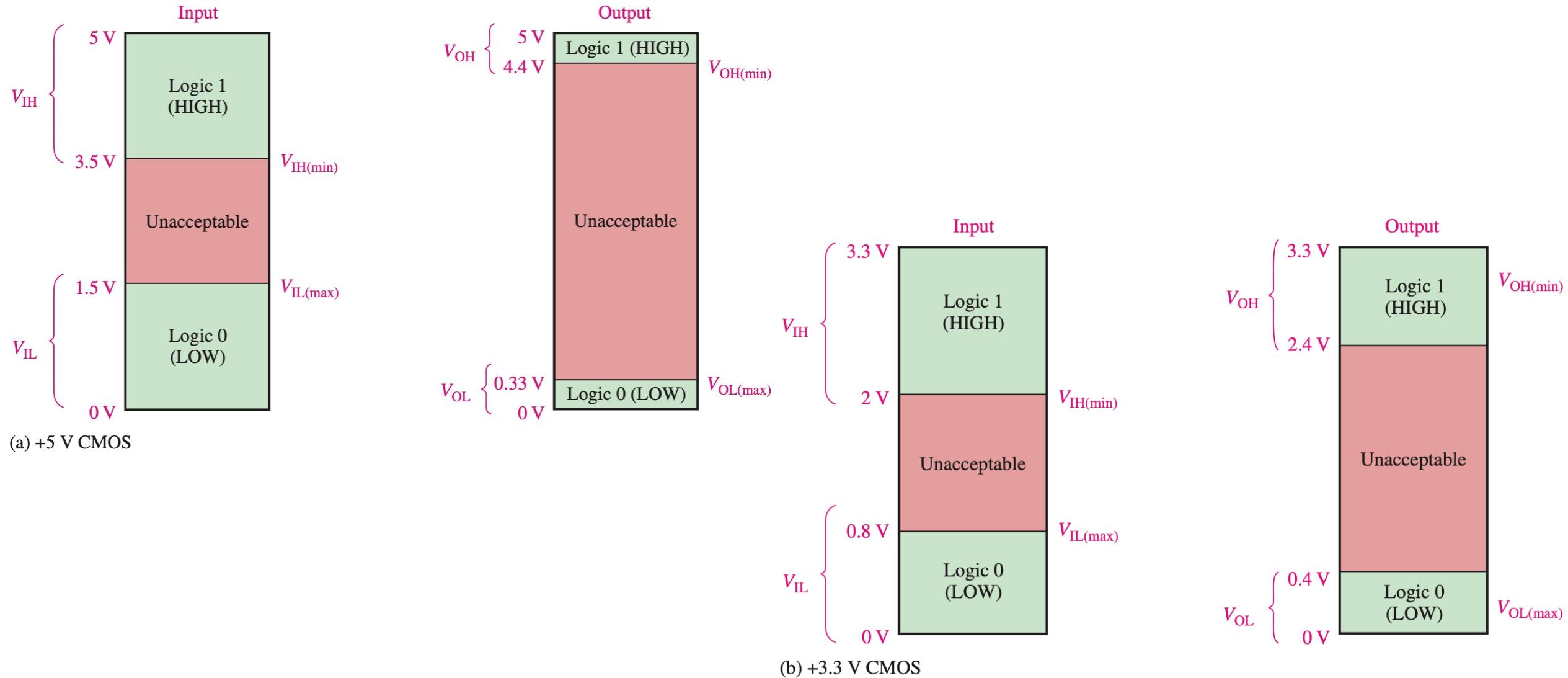


FIGURE 15-2 Input and output logic levels for CMOS.

TTL Logic Levels

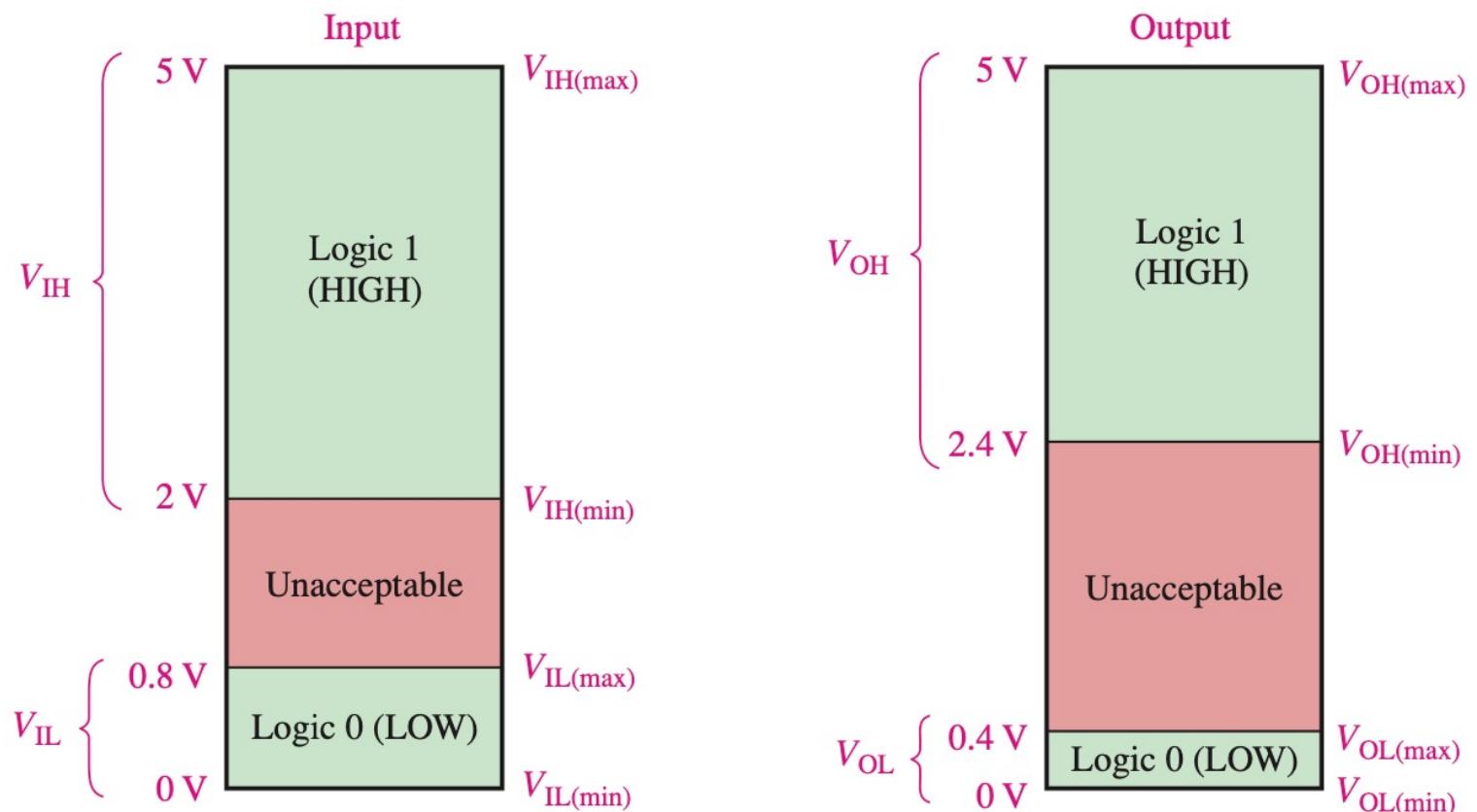


FIGURE 15–3 Input and output logic levels for TTL.

Noise Immunity

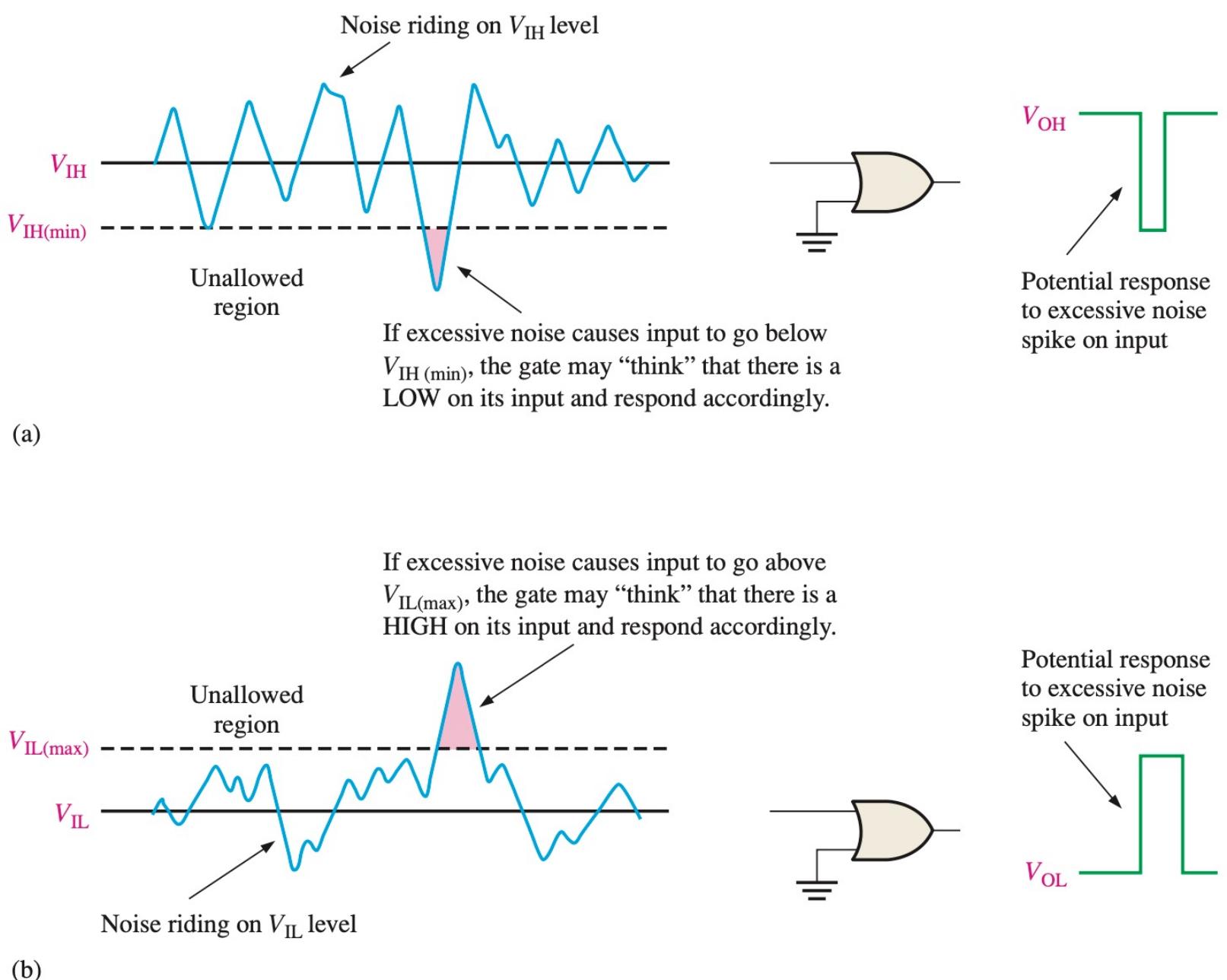


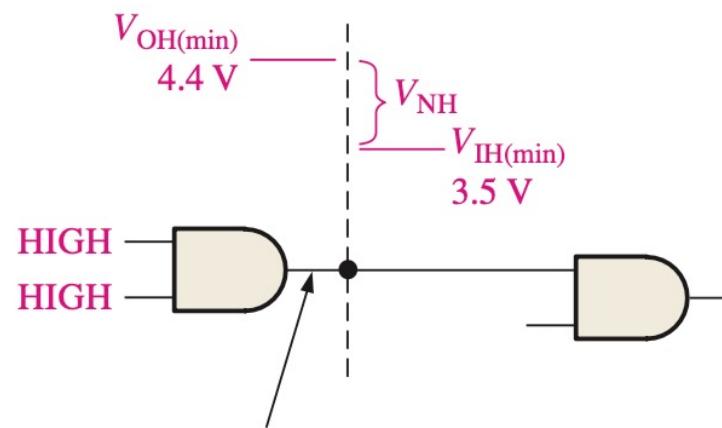
FIGURE 15-4 Illustration of the effects of input noise on gate operation.

Noise Margin

A measure of a circuit's noise immunity is called the **noise margin**, which is expressed in volts.

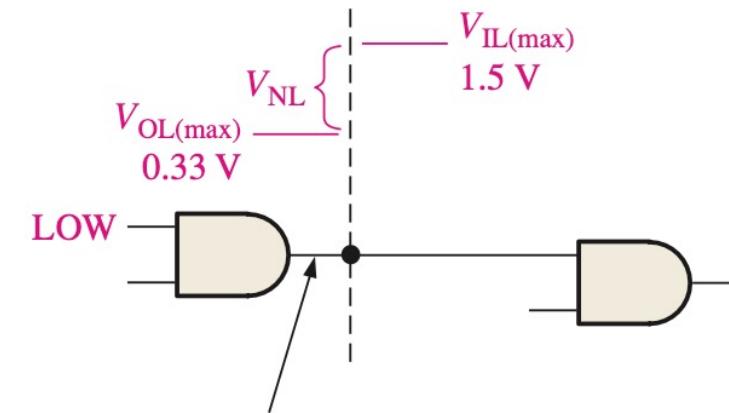
$$V_{NH} = V_{OH(\min)} = V_{IH(\min)}$$

$$V_{NL} = V_{IL(\max)} = V_{OL(\max)}$$



The voltage on this line will never be less than 4.4 V unless noise or improper operation is introduced.

(a) HIGH-level noise margin



The voltage on this line will never exceed 0.33 V unless noise or improper operation is introduced.

(b) LOW-level noise margin

FIGURE 15-5 Illustration of noise margins. Values are for 5 V CMOS, but the principle applies to any logic family.

EXAMPLE 15-1

Determine the HIGH-level and LOW-level noise margins for CMOS and for TTL by using the information in Figures 15–2 and 15–3.

Solution

For 5 V CMOS,

$$V_{IH(min)} = 3.5 \text{ V}$$

$$V_{IL(max)} = 1.5 \text{ V}$$

$$V_{OH(min)} = 4.4 \text{ V}$$

$$V_{OL(max)} = 0.33 \text{ V}$$

$$V_{NH} = V_{OH(min)} - V_{IH(min)} = 4.4 \text{ V} - 3.5 \text{ V} = \mathbf{0.9 \text{ V}}$$

$$V_{NL} = V_{IL(max)} - V_{OL(max)} = 1.5 \text{ V} - 0.33 \text{ V} = \mathbf{1.17 \text{ V}}$$

For TTL,

$$V_{IH(min)} = 2 \text{ V}$$

$$V_{IL(max)} = 0.8 \text{ V}$$

$$V_{OH(min)} = 2.4 \text{ V}$$

$$V_{OL(max)} = 0.4 \text{ V}$$

$$V_{NH} = V_{OH(min)} - V_{IH(min)} = 2.4 \text{ V} - 2 \text{ V} = \mathbf{0.4 \text{ V}}$$

$$V_{NL} = V_{IL(max)} - V_{OL(max)} = 0.8 \text{ V} - 0.4 \text{ V} = \mathbf{0.4 \text{ V}}$$

A TTL gate is immune to up to 0.4 V of noise for both the HIGH and LOW input states.

Power Dissipation

The **power dissipation** (P_D) of the gate is $P_D = V_{CC}I_{CC}$

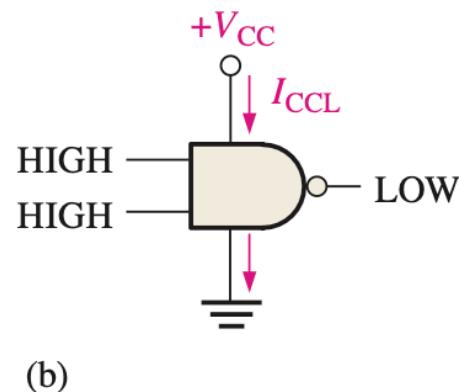
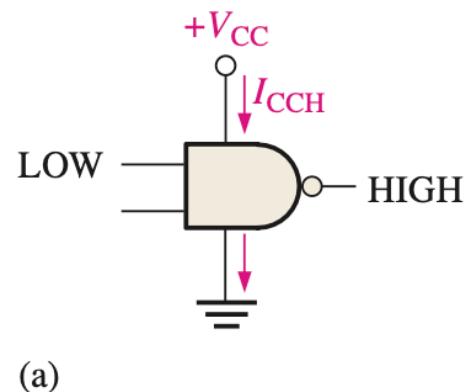


FIGURE 15-6 Currents from the dc supply. Conventional current direction is shown. Electron flow notation is opposite.

The average supply current is:

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2}$$

The average power dissipation is $P_D = V_{CC}I_{CC}$

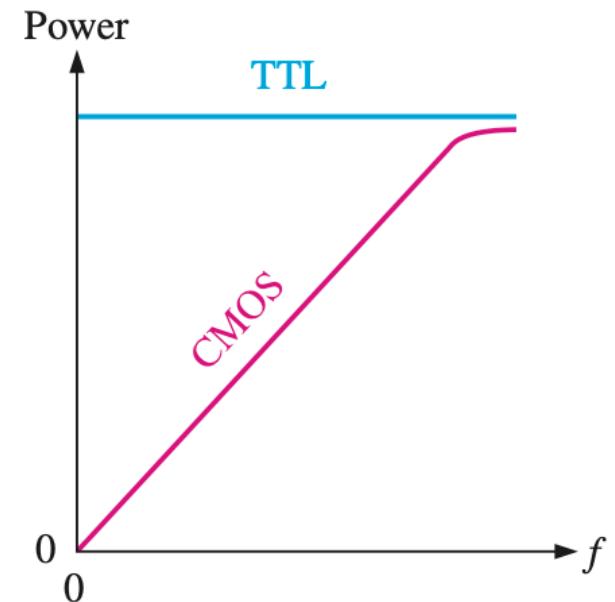


FIGURE 15-7 Power-versus-frequency curves for TTL and CMOS.

EXAMPLE 15-2

A certain gate draws $2 \mu\text{A}$ when its output is HIGH and $3.6 \mu\text{A}$ when its output is LOW. What is its average power dissipation if V_{CC} is 5 V and the gate is operated on a 50% duty cycle?

Solution

The average I_{CC} is

$$I_{\text{CC}} = \frac{I_{\text{CCH}} + I_{\text{CCL}}}{2} = \frac{2.0 \mu\text{A} + 3.6 \mu\text{A}}{2} = 2.8 \mu\text{A}$$

The average power dissipation is

$$P_{\text{D}} = V_{\text{CC}}I_{\text{CC}} = (5 \text{ V})(2.8 \mu\text{A}) = 14 \mu\text{W}$$

Related Problem

A certain IC gate has an $I_{\text{CCH}} = 1.5 \mu\text{A}$ and $I_{\text{CCL}} = 2.8 \mu\text{A}$. Determine the average power dissipation for 50% duty cycle operation if V_{CC} is 5 V.

Propagation Delay Time

A change in the output level always occurs a short time, called the propagation delay time, later than the change in the input level that caused it.

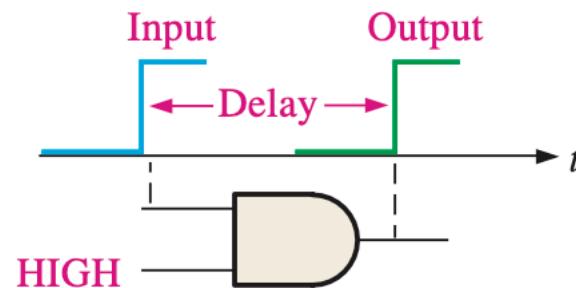


FIGURE 15–8 A basic illustration of propagation delay time.

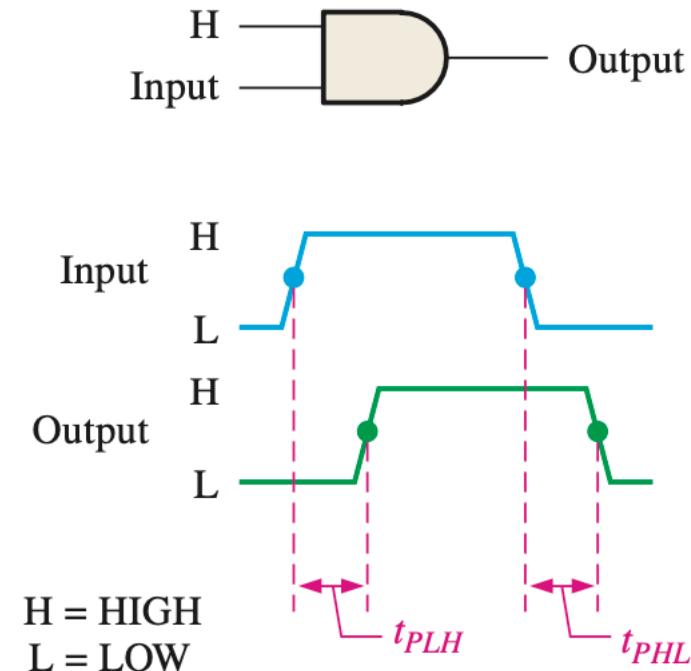


FIGURE 15–9 Propagation delay times.

Loading and Fan-Out

There is a limit to the number of load gate inputs that a given gate can drive. This limit is called the fan-out of the gate. Fan-out is expressed as unit loads.

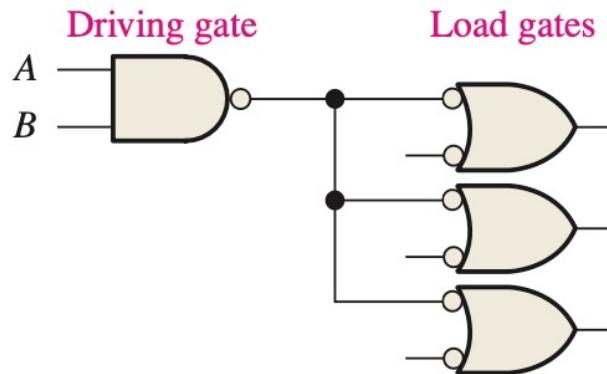


FIGURE 15-10 Loading a gate output with gate inputs.

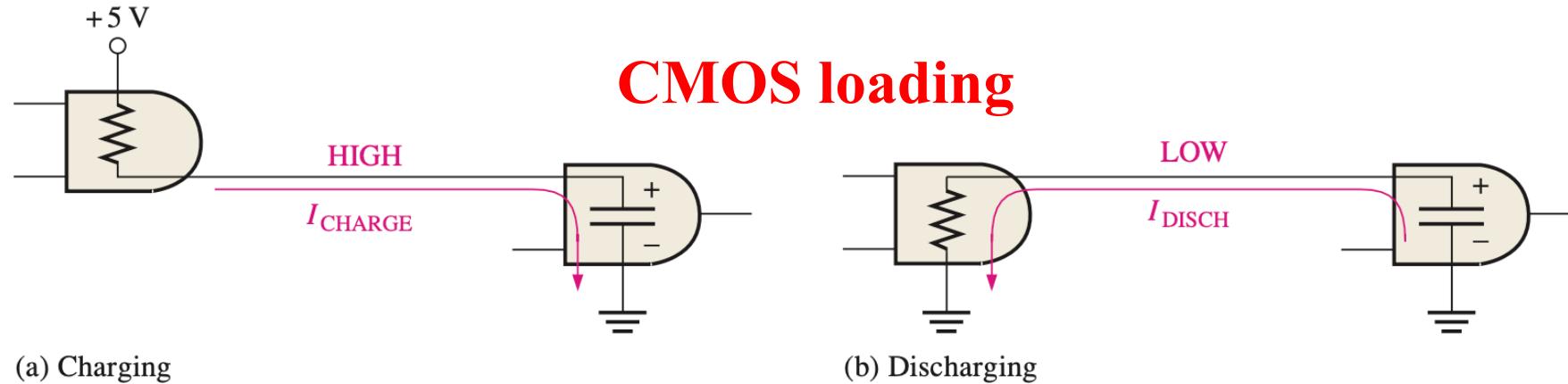
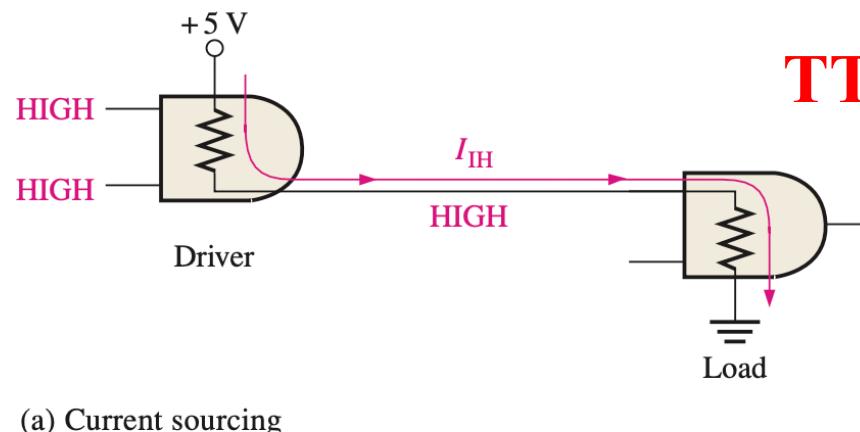


FIGURE 15-11 Capacitive loading of a CMOS gate.



TTL loading

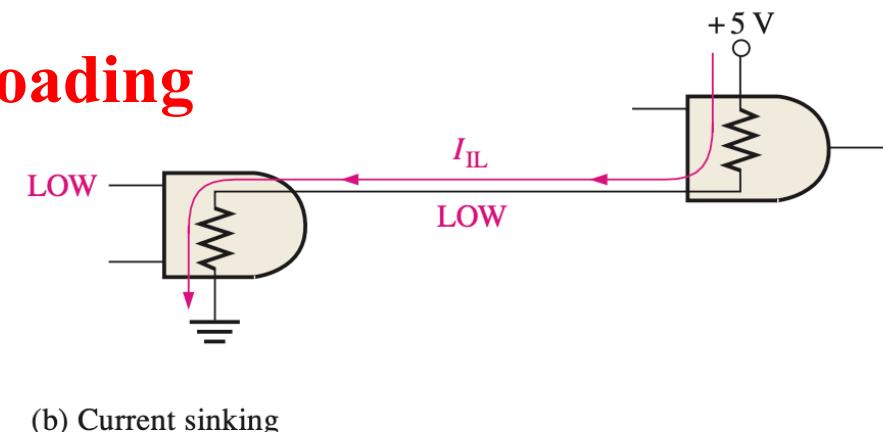


FIGURE 15-12 Basic illustration of current sourcing and current sinking in logic gates.

TTL loading

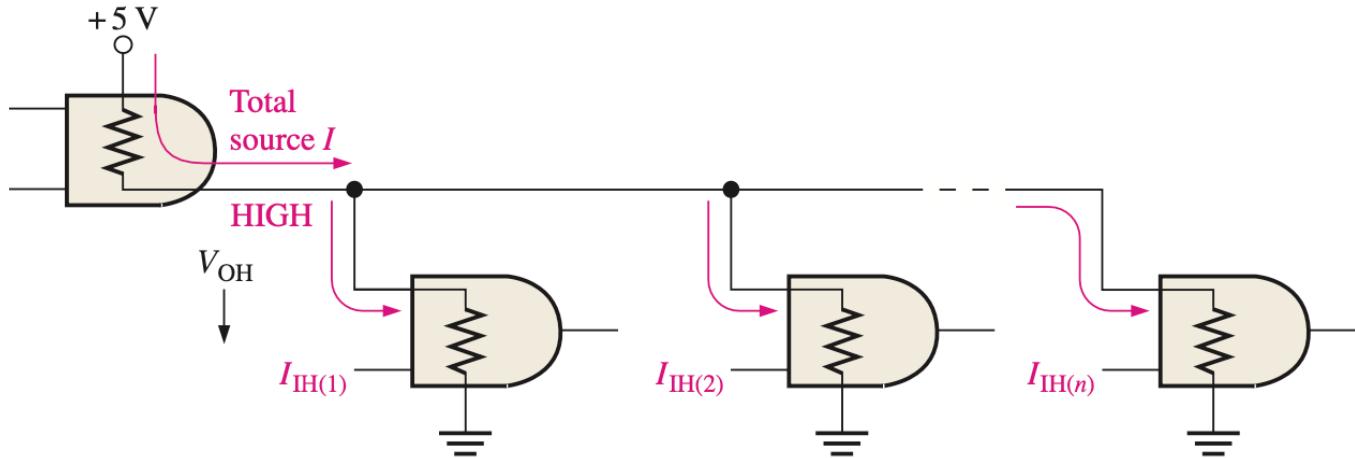


FIGURE 15–13 HIGH-state TTL loading.

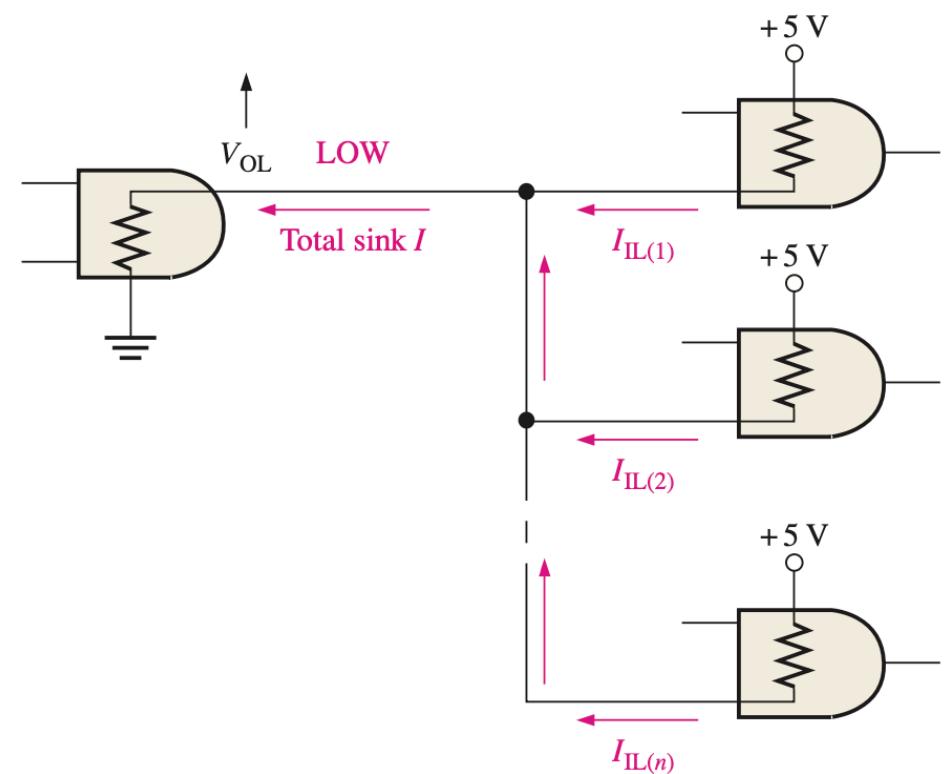


FIGURE 15–14 LOW-stage TTL loading.

2. CMOS Circuits

Metal-oxide semiconductor field-effect transistors (MOSFETs)

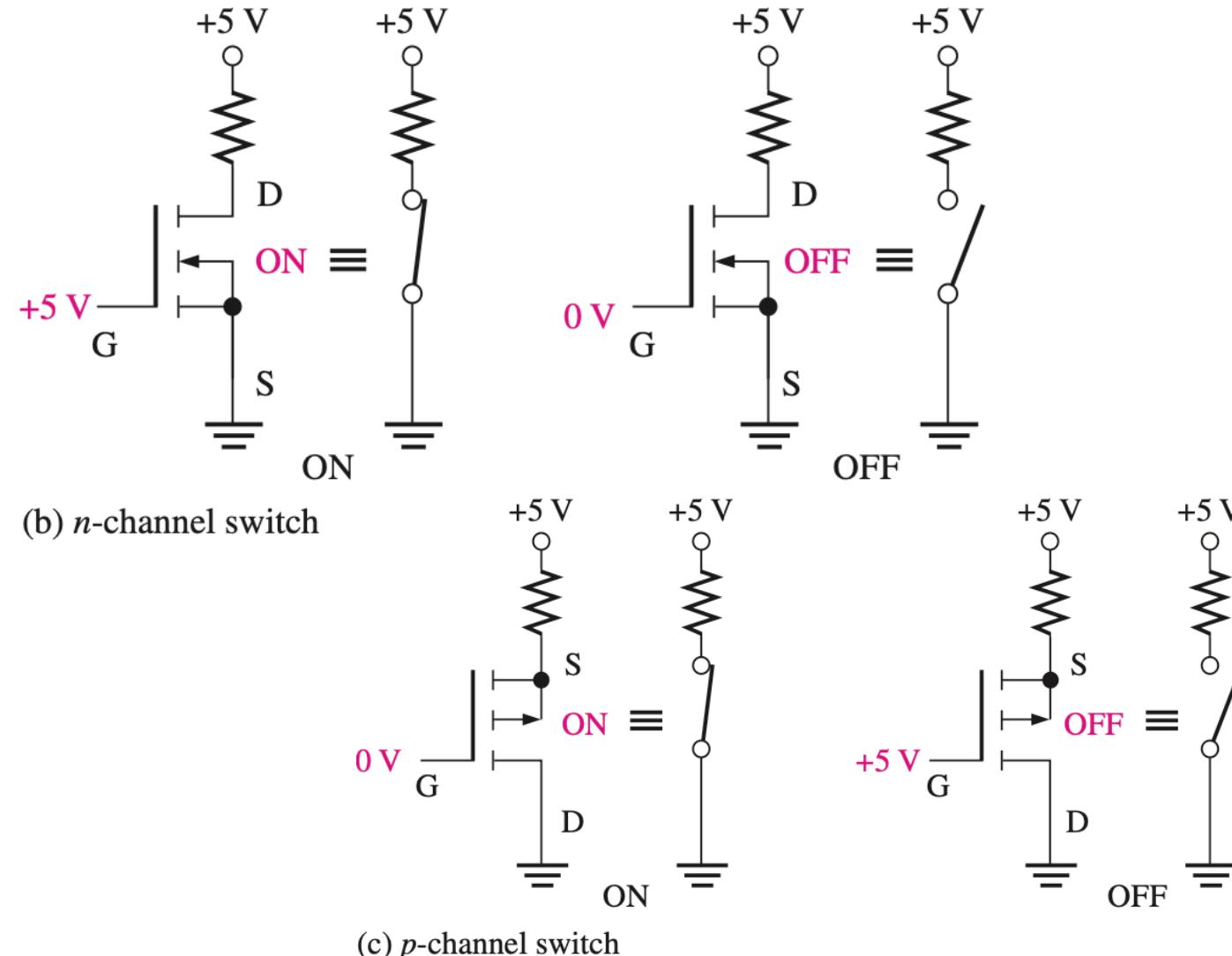
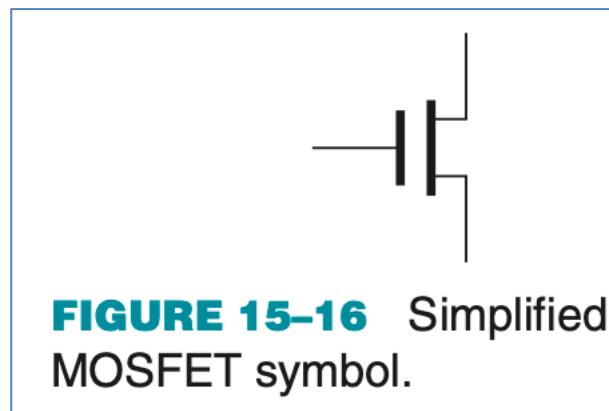
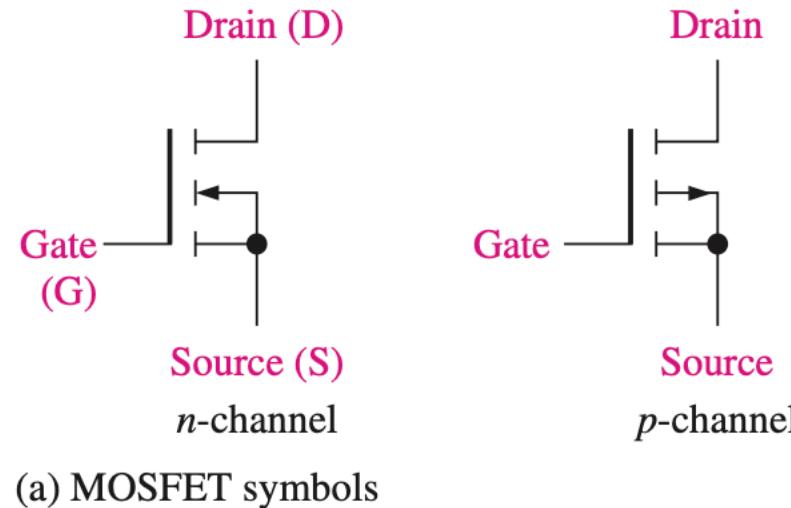


FIGURE 15-15 Basic symbols and switching action of MOSFETs.

CMOS Inverter

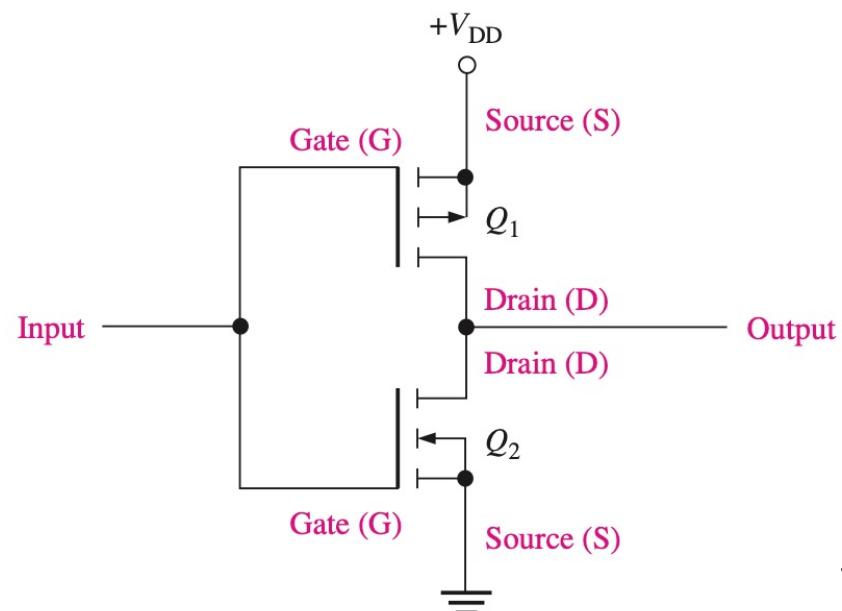


FIGURE 15-17 A CMOS inverter circuit.

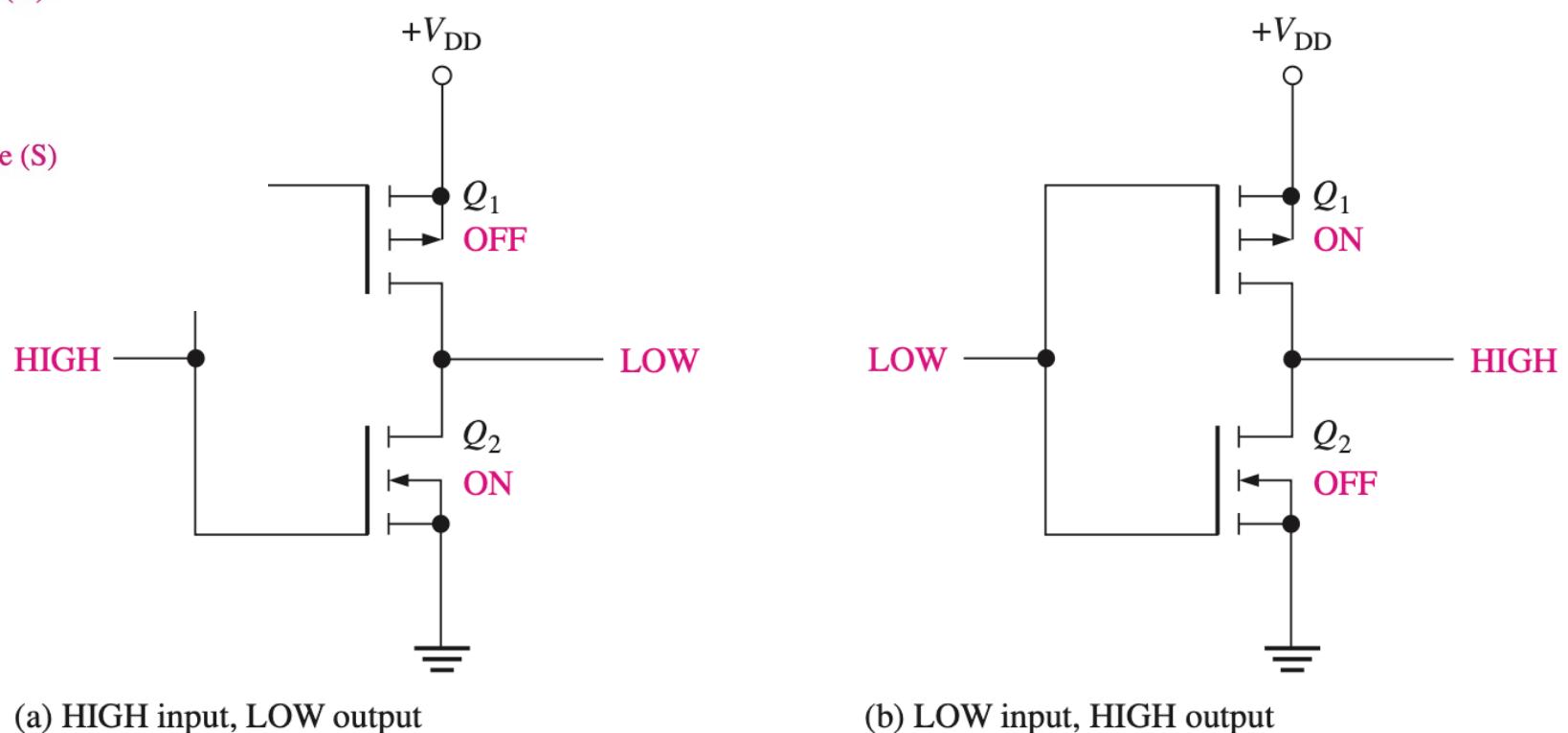


FIGURE 15-18 Operation of a CMOS inverter.

CMOS NAND Gate

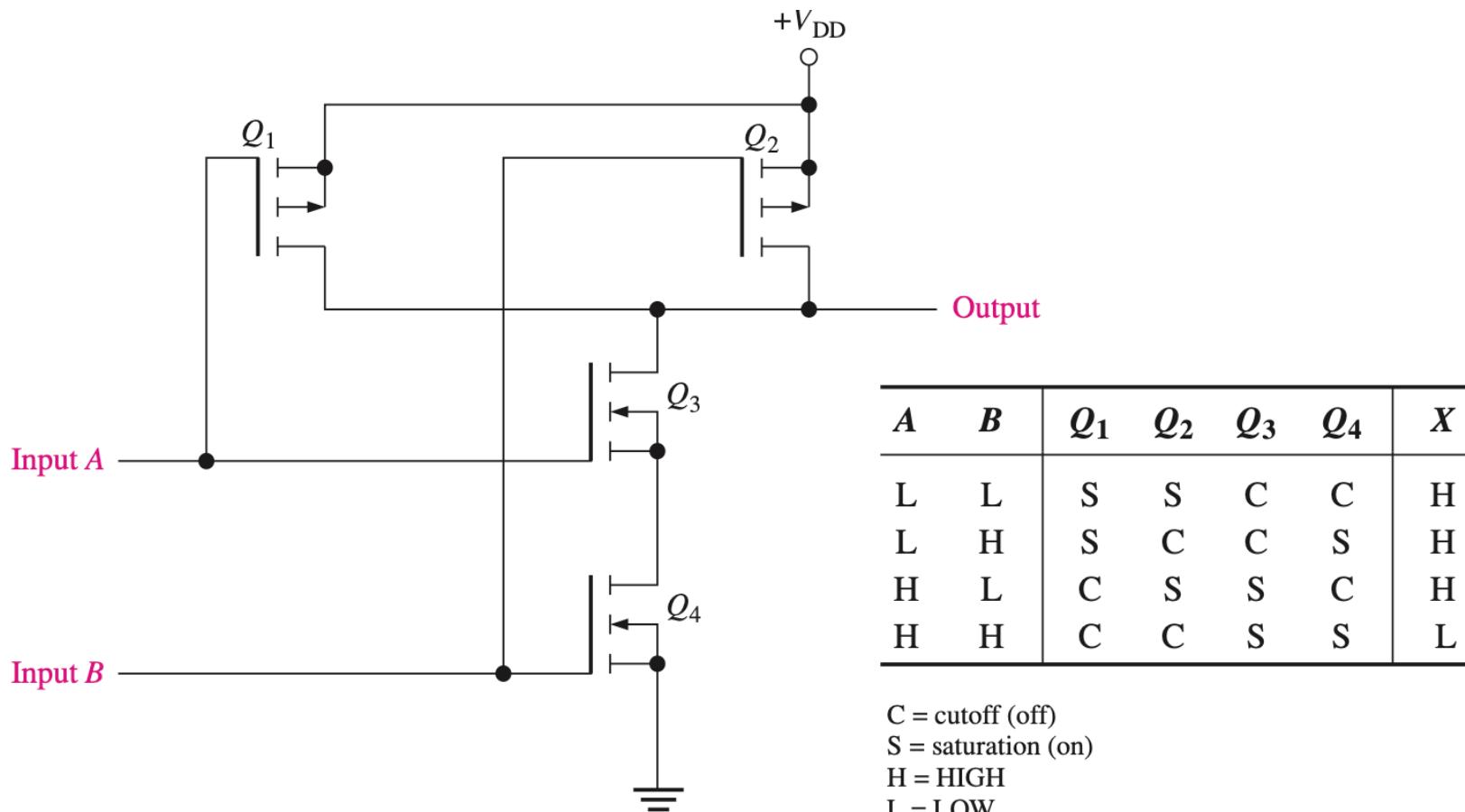


FIGURE 15–19 A CMOS NAND gate circuit.

CMOS NOR Gate

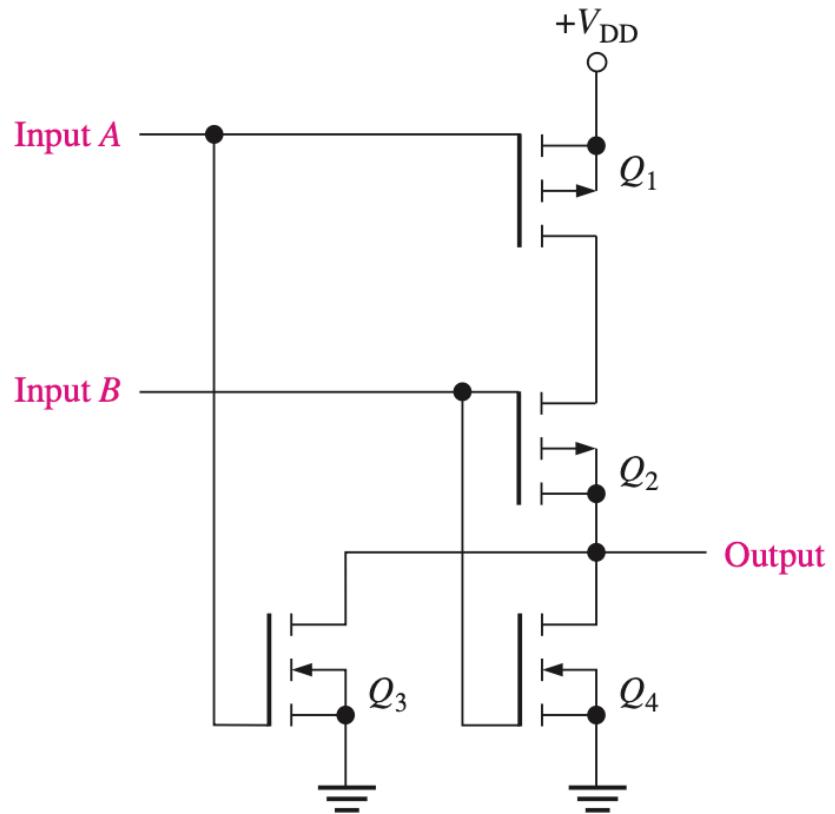


FIGURE 15–20 A CMOS NOR gate circuit.

A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	L
H	L	C	S	S	C	L
H	H	C	C	S	S	L

C = cutoff (off)

S = saturation (on)

H = HIGH

L = LOW

Open-Drain Gates

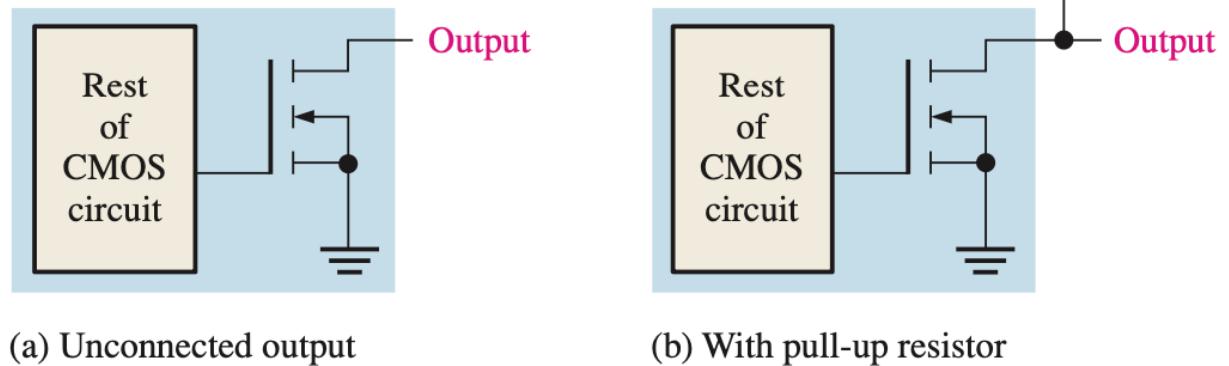


FIGURE 15-21 Open-drain CMOS gates.

Tri-state CMOS Gates

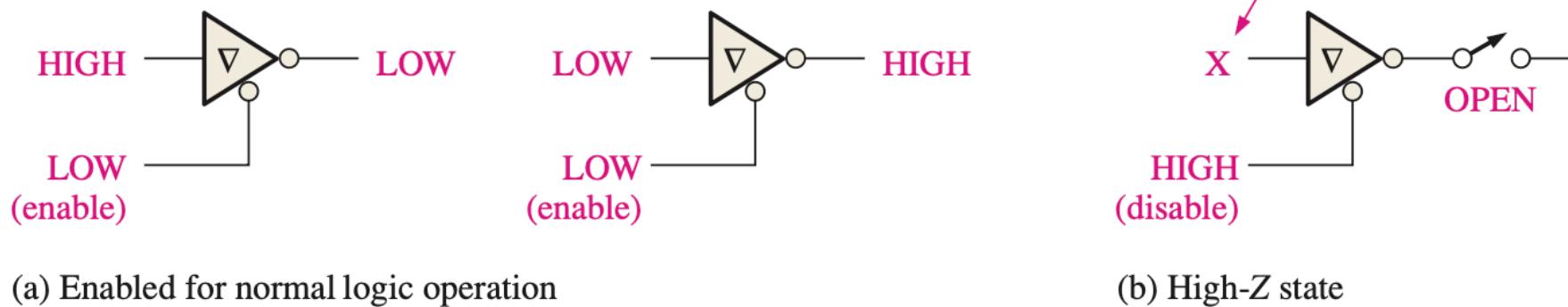
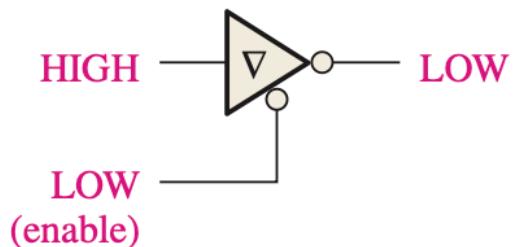
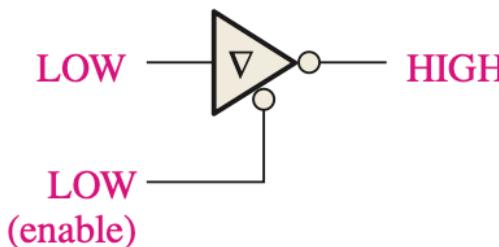


FIGURE 15-22 The three states of a tri-state circuit.

Tri-state CMOS Gates



(a) Enabled for normal logic operation



(b) High-Z state

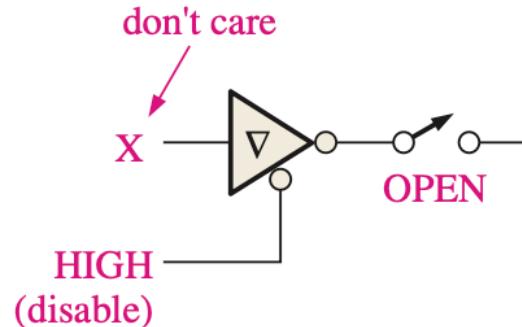


FIGURE 15-22 The three states of a tri-state circuit.

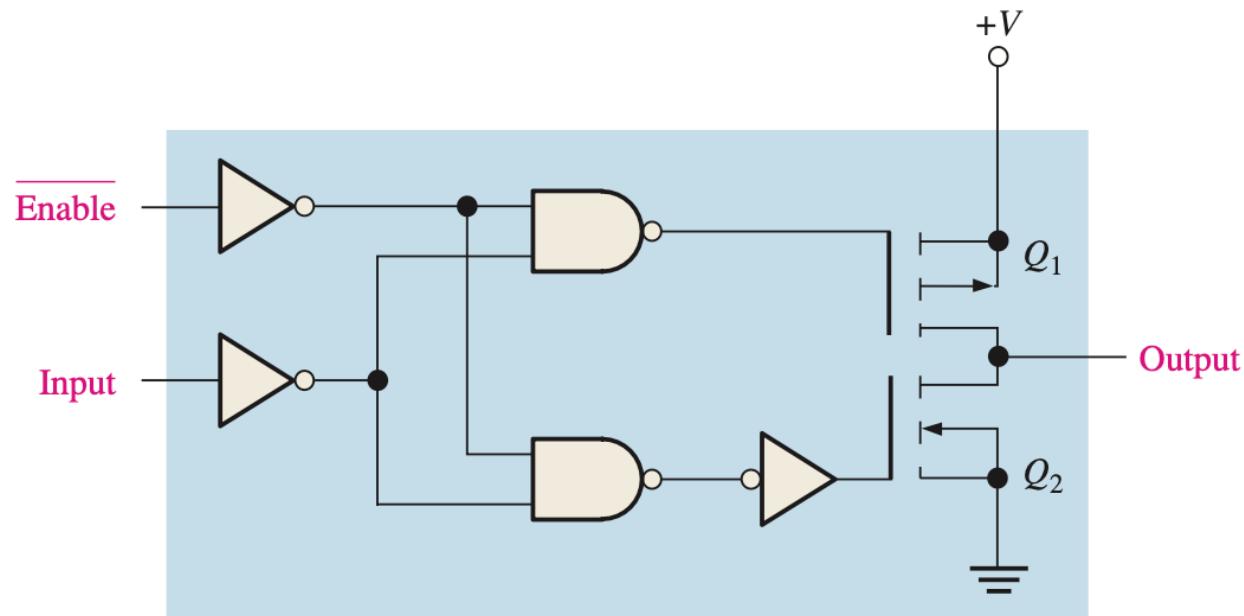


FIGURE 15-23 A tri-state CMOS inverter.

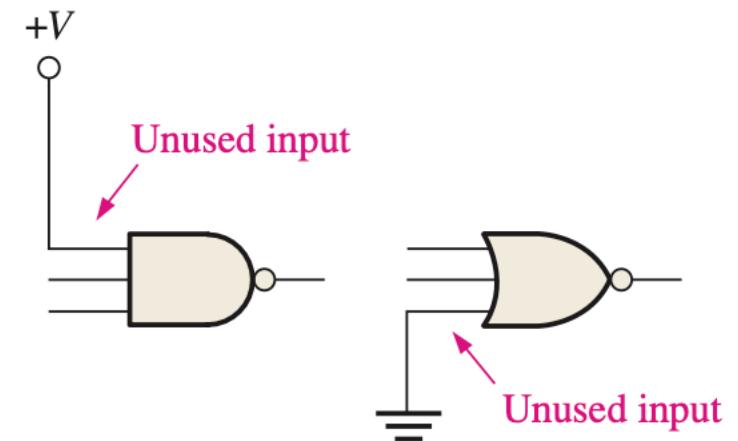


FIGURE 15-24 Handling unused CMOS inputs.

3. TTL (Bipolar) Circuits

The Fetch/Execute Cycle

The bipolar junction transistor (BJT) is the active switching element used in all TTL circuits.

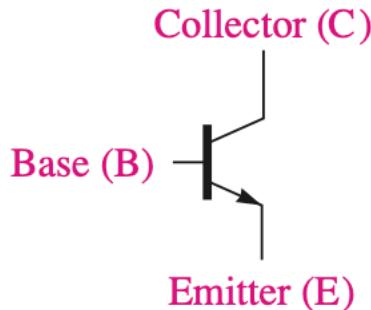


FIGURE 15–25 The symbol for a BJT.

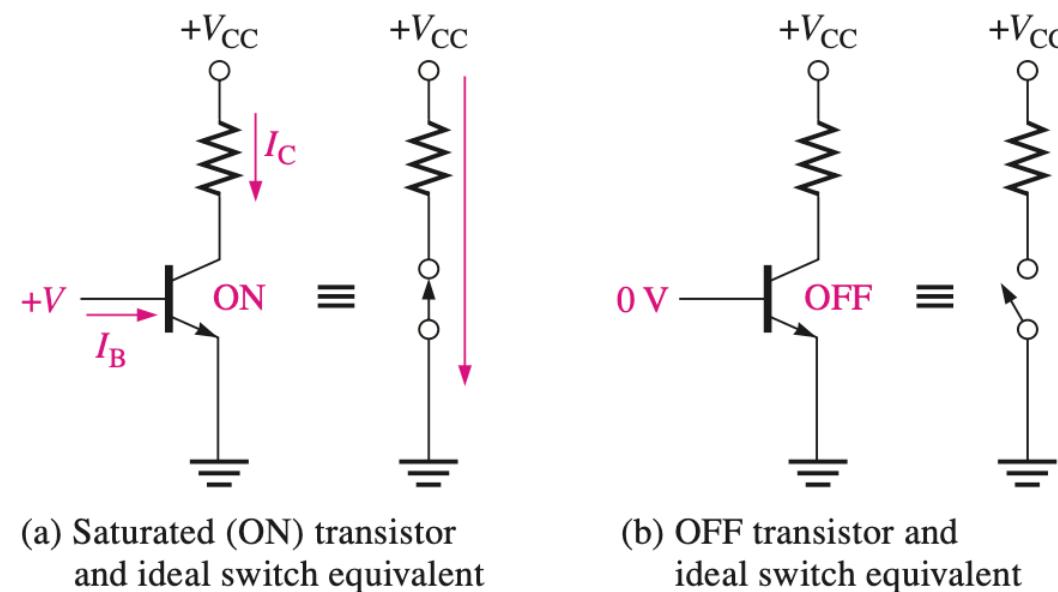


FIGURE 15–26 The ideal switching action of the BJT. Conventional current direction is shown. Electron flow notation is opposite.

TTL Inverter

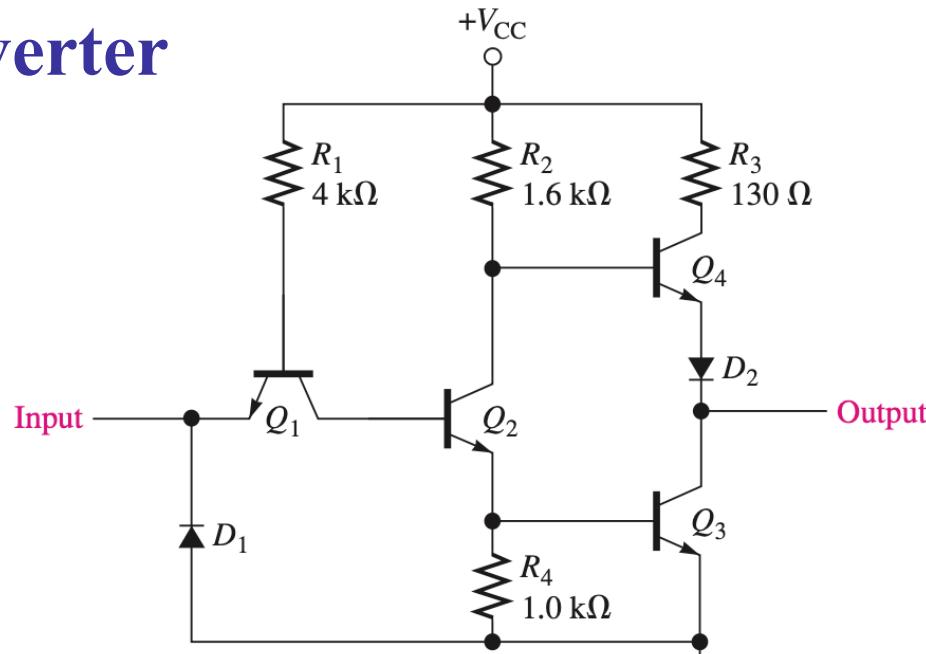
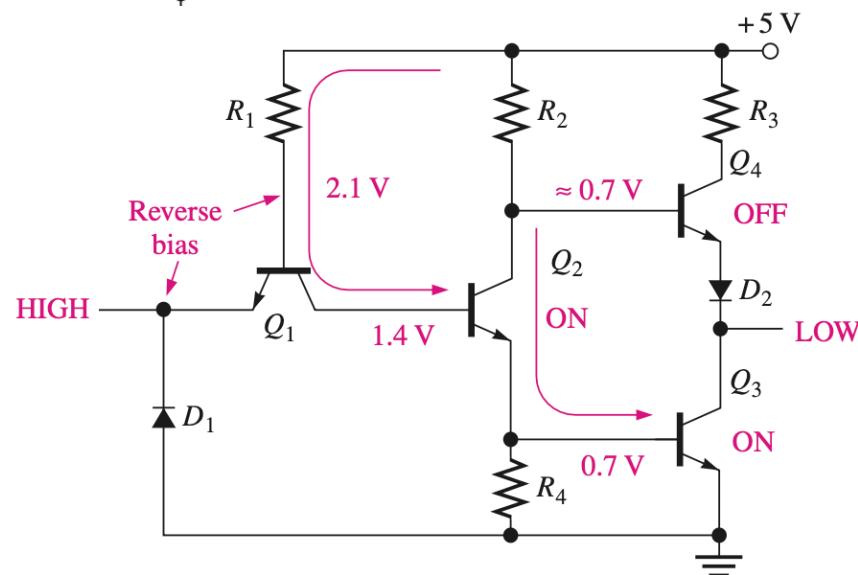
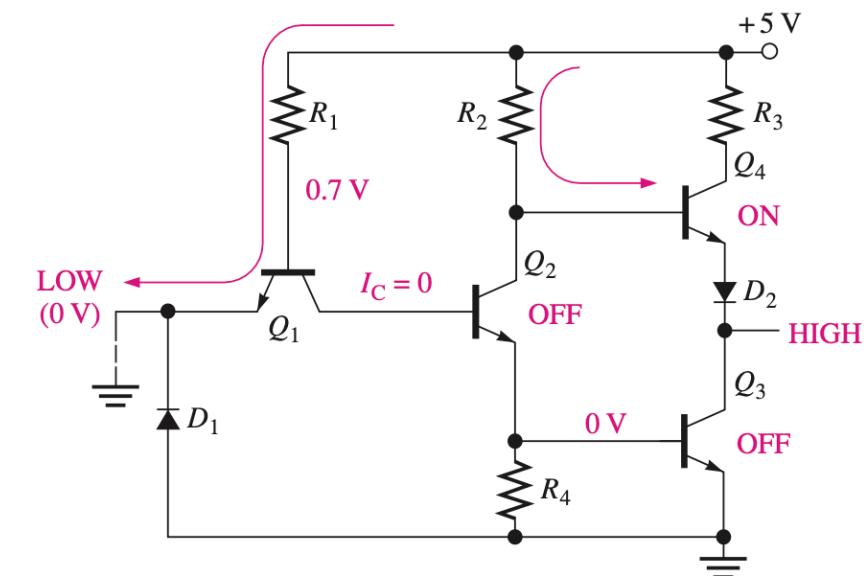


FIGURE 15-27 A standard TTL inverter circuit.



(a)



(b)

FIGURE 15-28 Operation of a TTL inverter.

TTL NAND Gate

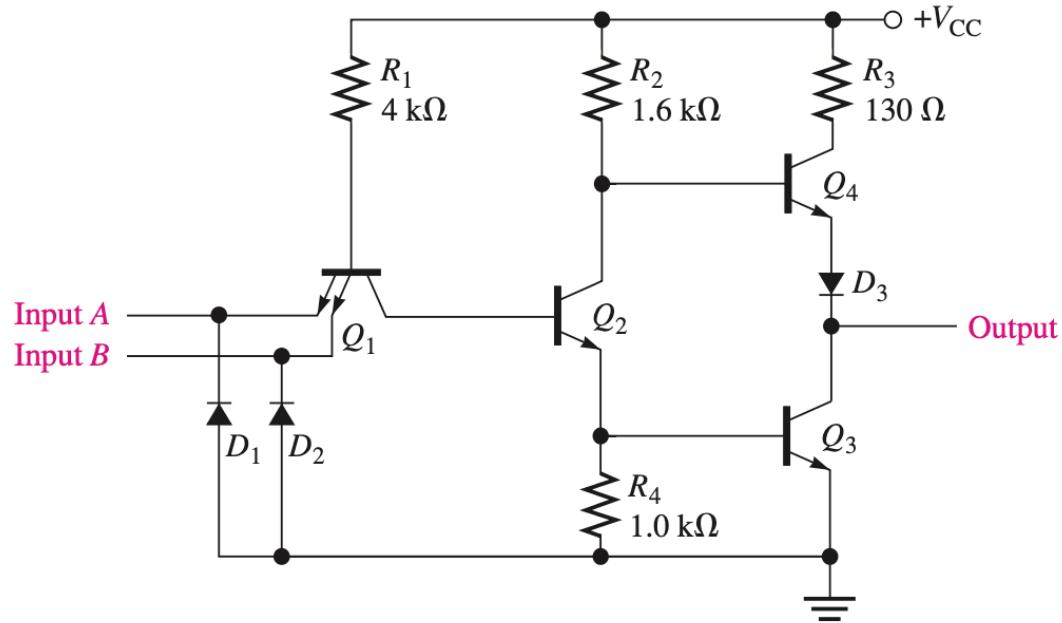


FIGURE 15–29 A TTL NAND gate circuit.

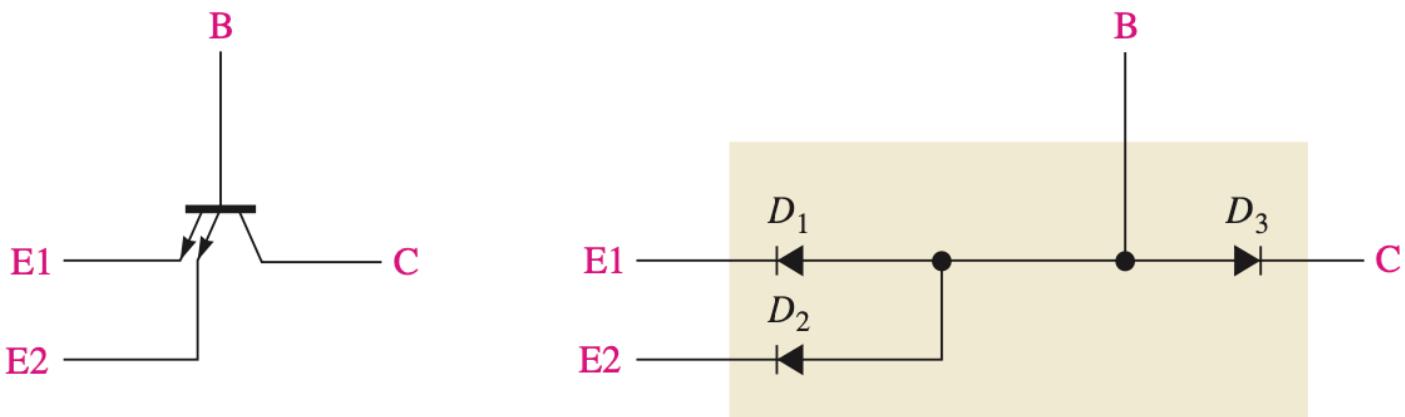
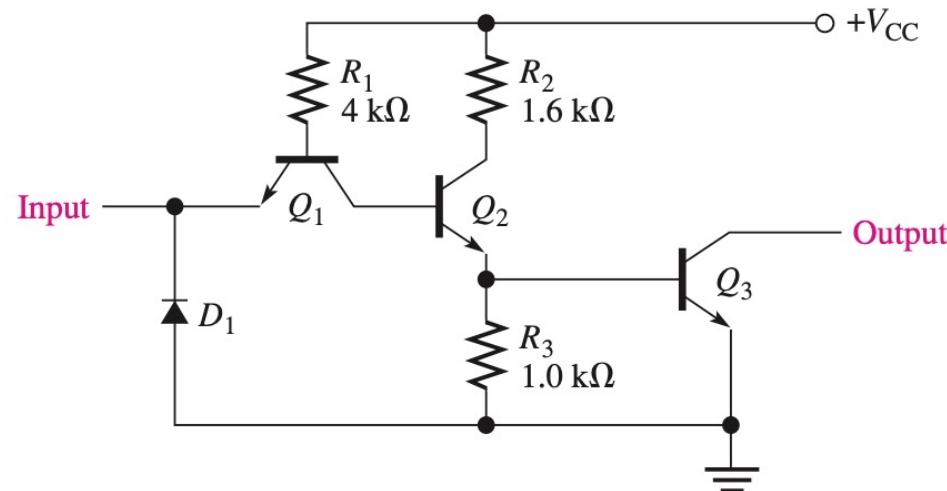
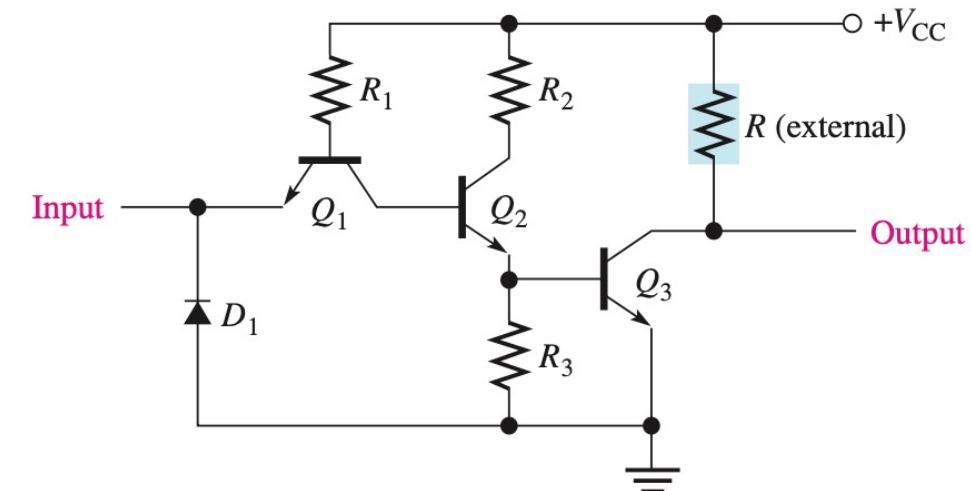


FIGURE 15–30 Diode equivalent of a TTL multiple-emitter transistor.

Open-Collector Gates



(a) Open-collector inverter circuit



(b) With external pull-up resistor

FIGURE 15-31 TTL inverter with open-collector output.

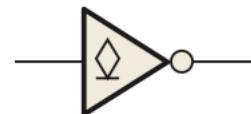


FIGURE 15-32 Open-collector symbol in an inverter.

Tri-state TTL Gates

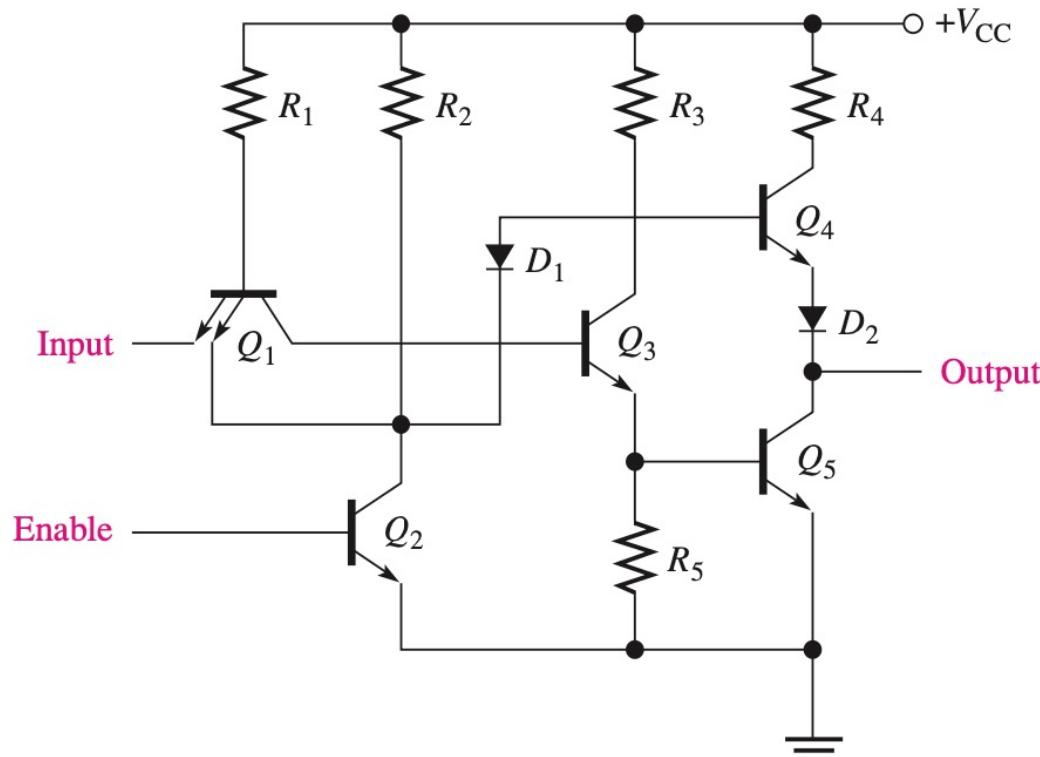


FIGURE 15–33 Basic tri-state inverter circuit.

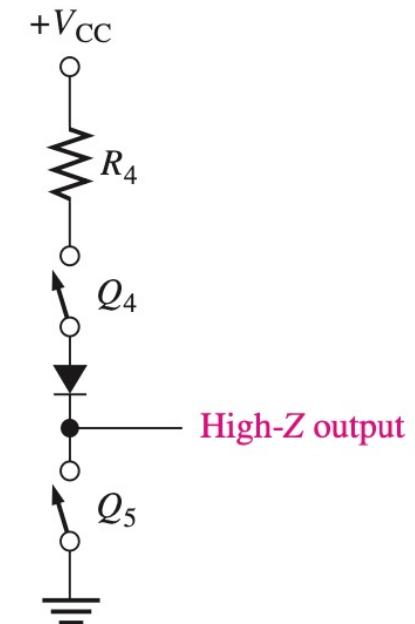


FIGURE 15–34 An equivalent circuit for the tri-state output in the high-Z state.

Schottky TTL

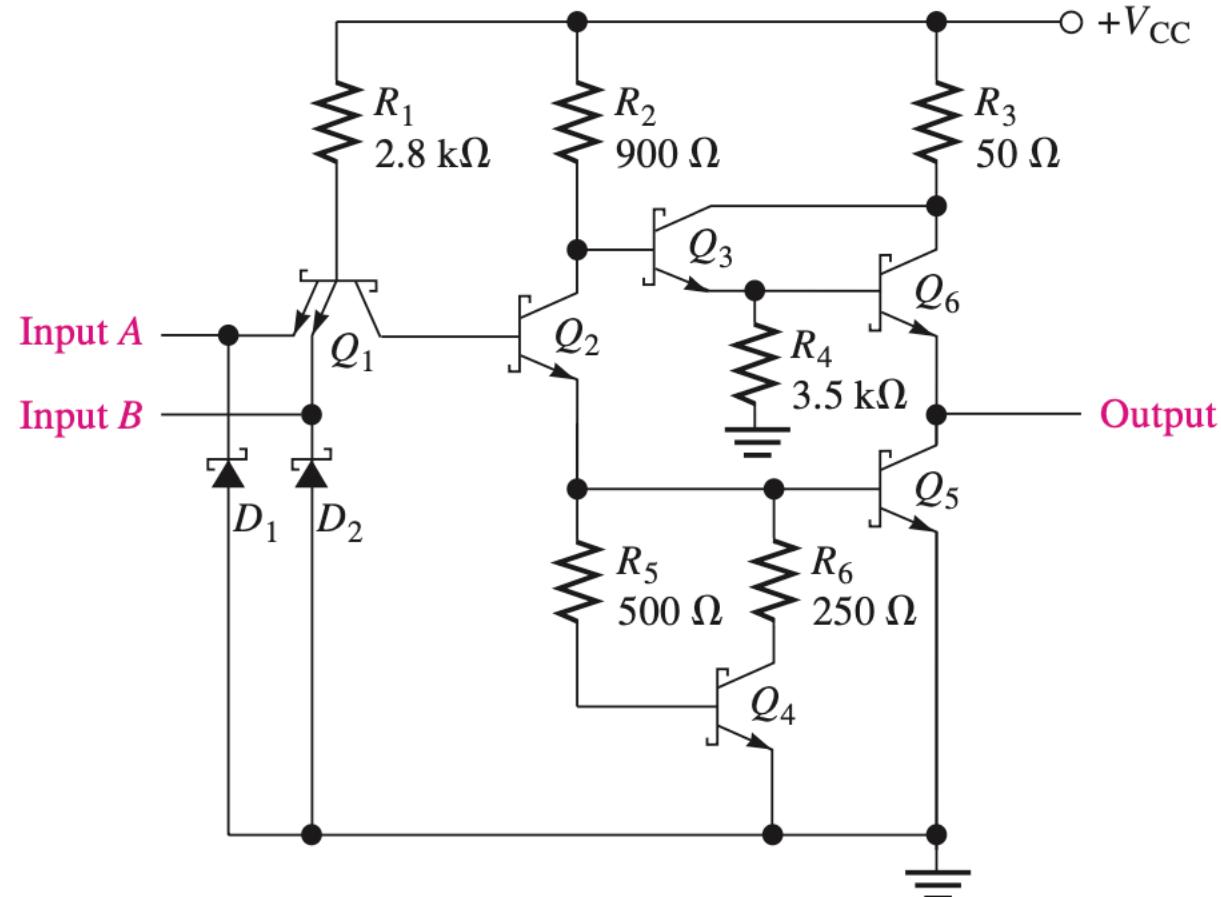


FIGURE 15–35 Schottky TTL NAND gate.

4. Practical Considerations in the Use of TTL

Current Sinking and Current Sourcing

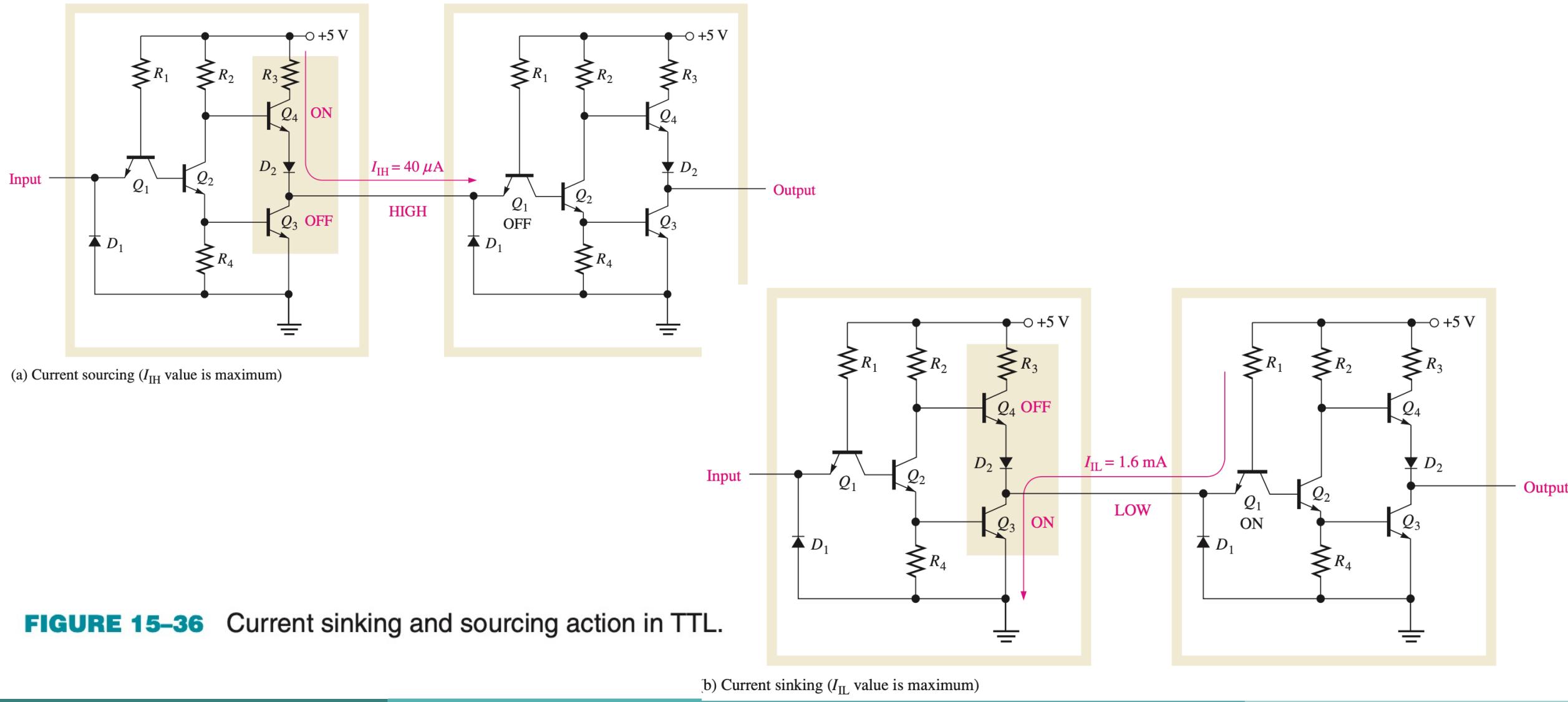


FIGURE 15-36 Current sinking and sourcing action in TTL.

EXAMPLE 15–3

When a standard TTL NAND gate drives five TTL inputs, how much current does the driver output source, and how much does it sink? (Refer to Figure 15–36.)

Solution

Total source current (in HIGH output state):

$$I_{IH(\max)} = 40 \mu\text{A} \text{ per input}$$

$$I_{T(\text{source})} = (5 \text{ inputs})(40 \mu\text{A}/\text{input}) = 5(40 \mu\text{A}) = 200 \mu\text{A}$$

Total sink current (in LOW output state):

$$I_{IL(\max)} = -1.6 \text{ mA per input}$$

$$I_{T(\text{sink})} = (5 \text{ inputs})(-1.6 \text{ mA}/\text{input}) = 5(-1.6 \text{ mA}) = -8.0 \text{ mA}$$

EXAMPLE 15-4

Refer to the data sheet available at www.ti.com, and determine the fan-out of the 7400 NAND gate.

Solution

According to the data sheet, the current parameters are as follows:

$$I_{IH(max)} = 40 \mu A \quad I_{OH(max)} = -400 \mu A$$

$$I_{IL(max)} = -1.6 mA \quad I_{OL(max)} = 16 mA$$

Fan-out for the HIGH output state is calculated as follows: Current $I_{OH(max)}$ is the maximum current that the gate can source to a load. Each load input requires an $I_{IH(max)}$ of $40 \mu A$. The HIGH-state fan-out is

$$\left| \frac{I_{OH(max)}}{I_{IH(max)}} \right| = \frac{400 \mu A}{40 \mu A} = \mathbf{10 \text{ unit loads}}$$

For the LOW output state, fan-out is calculated as follows: $I_{OL(max)}$ is the maximum current that the gate can sink. Each load input produces an $I_{IL(max)}$ of $-1.6 mA$. The LOW-state fan-out is

$$\left| \frac{I_{OL(max)}}{I_{IL(max)}} \right| = \frac{16 mA}{1.6 mA} = \mathbf{10 \text{ unit loads}}$$

In this case both the HIGH-state fan-out and the LOW-state fan-out are the same.

Using Open-Collector Gates for Wired-AND Operation

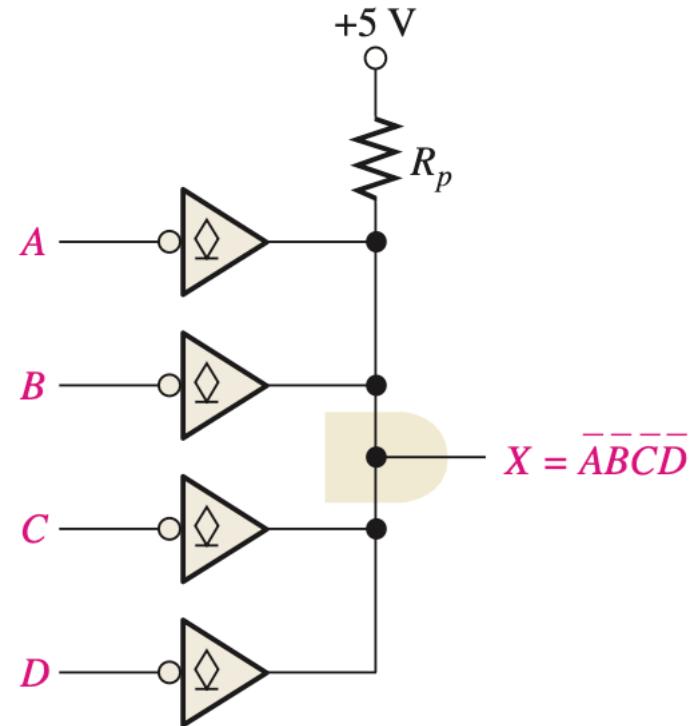


FIGURE 15-37 A wired-AND configuration of four inverters.

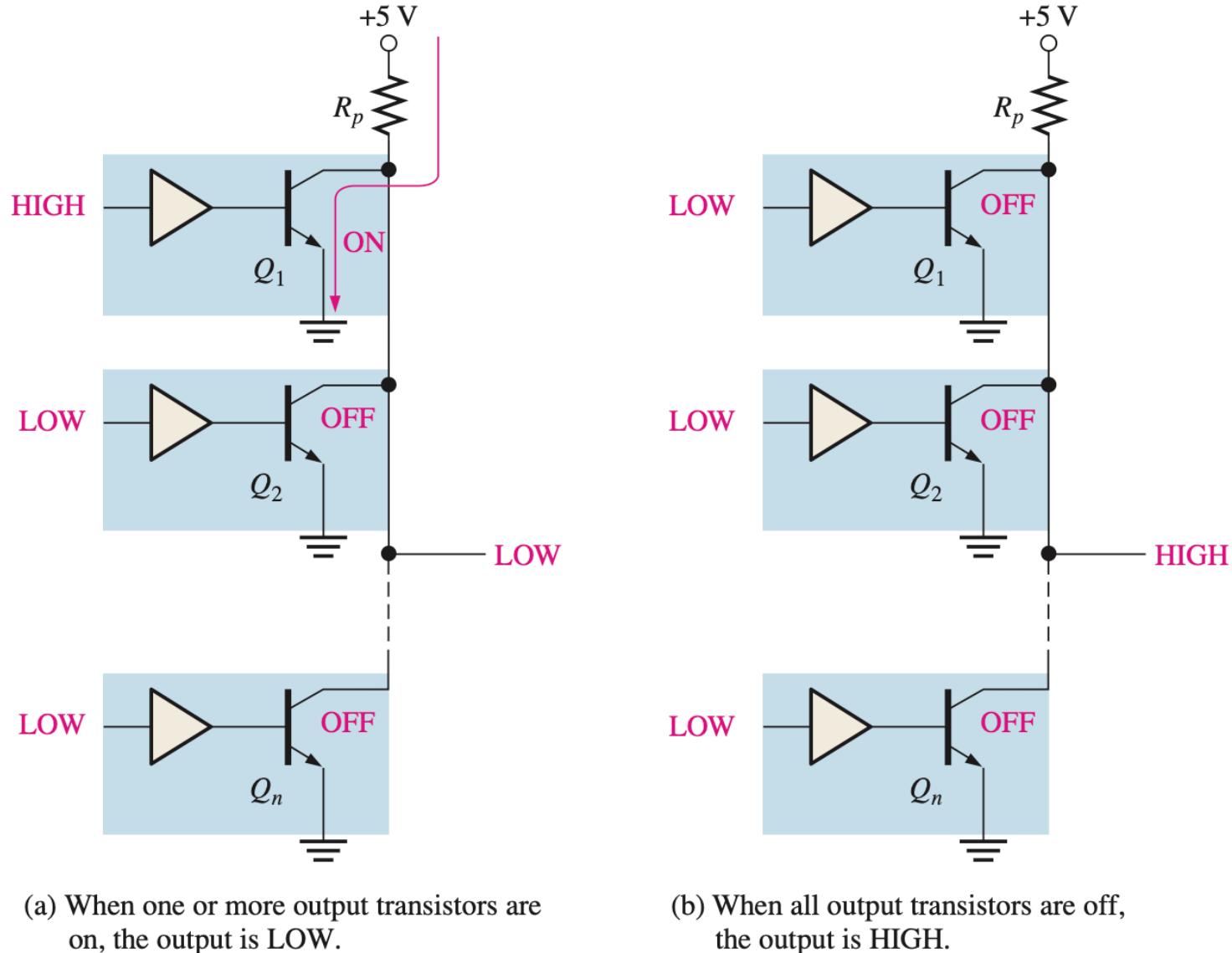
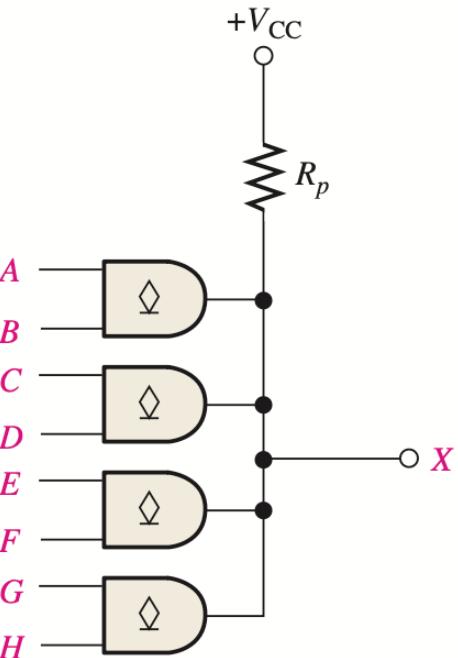


FIGURE 15-38 Open-collector wired negative-AND operation with inverters.

EXAMPLE 15–5

Write the output expression for the wired-AND configuration of open-collector AND gates in Figure 15–39.

**FIGURE 15–39****Solution**

The output expression is

$$X = ABCDEFGH$$

The wired-AND connection of the four 2-input AND gates creates an 8-input AND gate.

EXAMPLE 15–6

Three open-collector AND gates are connected in a wired-AND configuration as shown in Figure 15–40. Assume that the wired-AND circuit is driving four standard TTL inputs (-1.6 mA each).

- Write the logic expression for X .
- Determine the minimum value of R_p if $I_{OL(\max)}$ for each gate is 30 mA and $V_{OL(\max)}$ is 0.4 V .

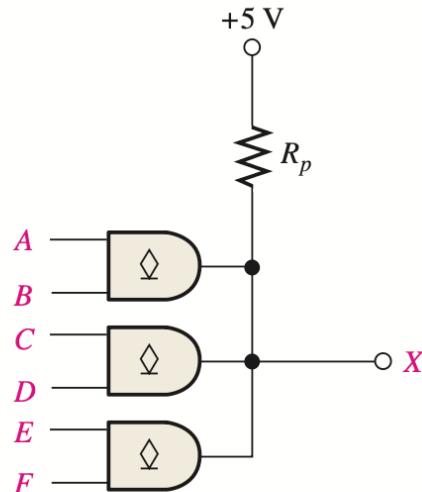


FIGURE 15–40

Solution

- $X = ABCDEF$
- $4(1.6\text{ mA}) = 6.4\text{ mA}$

$$I_{R_p} = I_{OL(\max)} - 6.4\text{ mA} = 30\text{ mA} - 6.4\text{ mA} = 23.6\text{ mA}$$

$$R_P = \frac{V_{CC} - V_{OL(\max)}}{I_{R_p}} = \frac{5\text{ V} - 0.4\text{ V}}{23.6\text{ mA}} = 195\text{ }\Omega$$

Connection of Totem-Pole Outputs

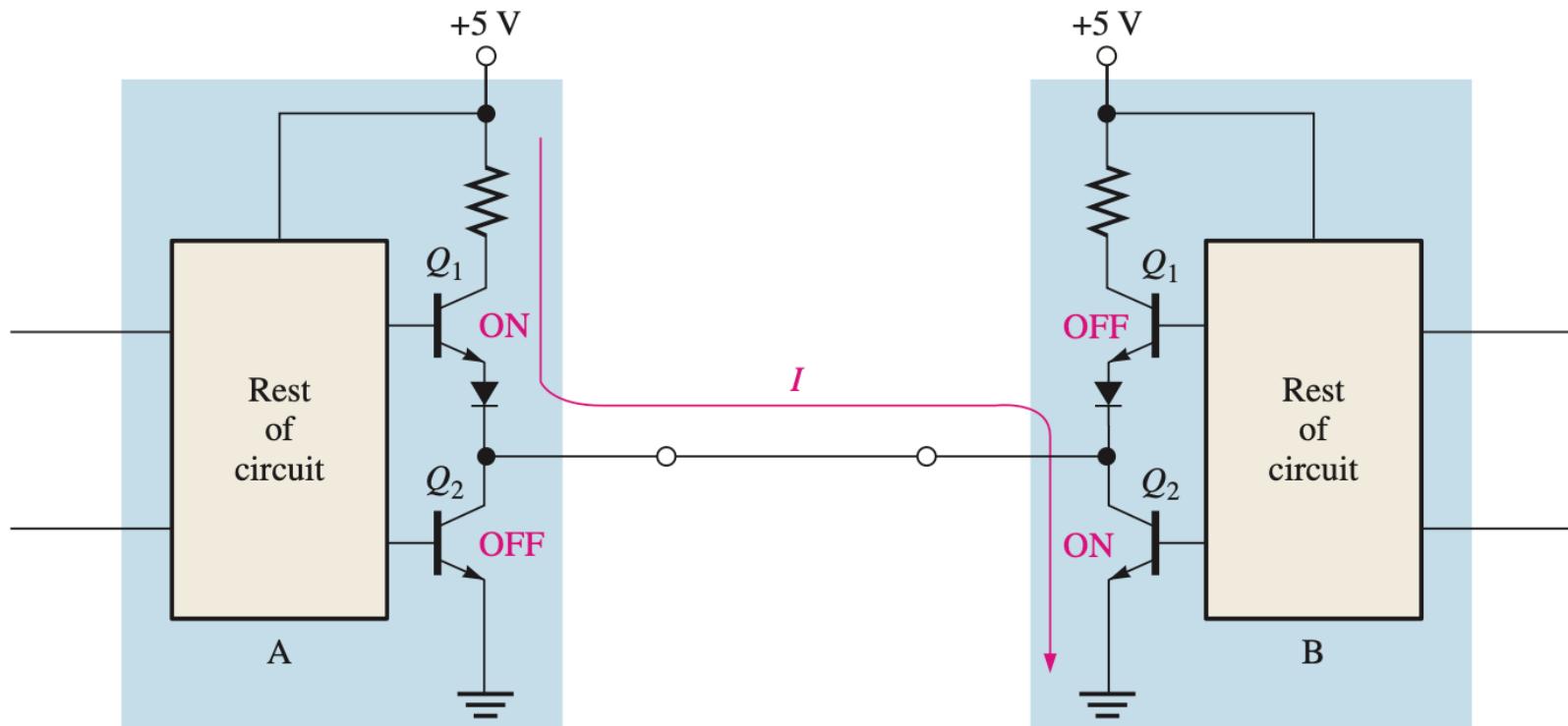
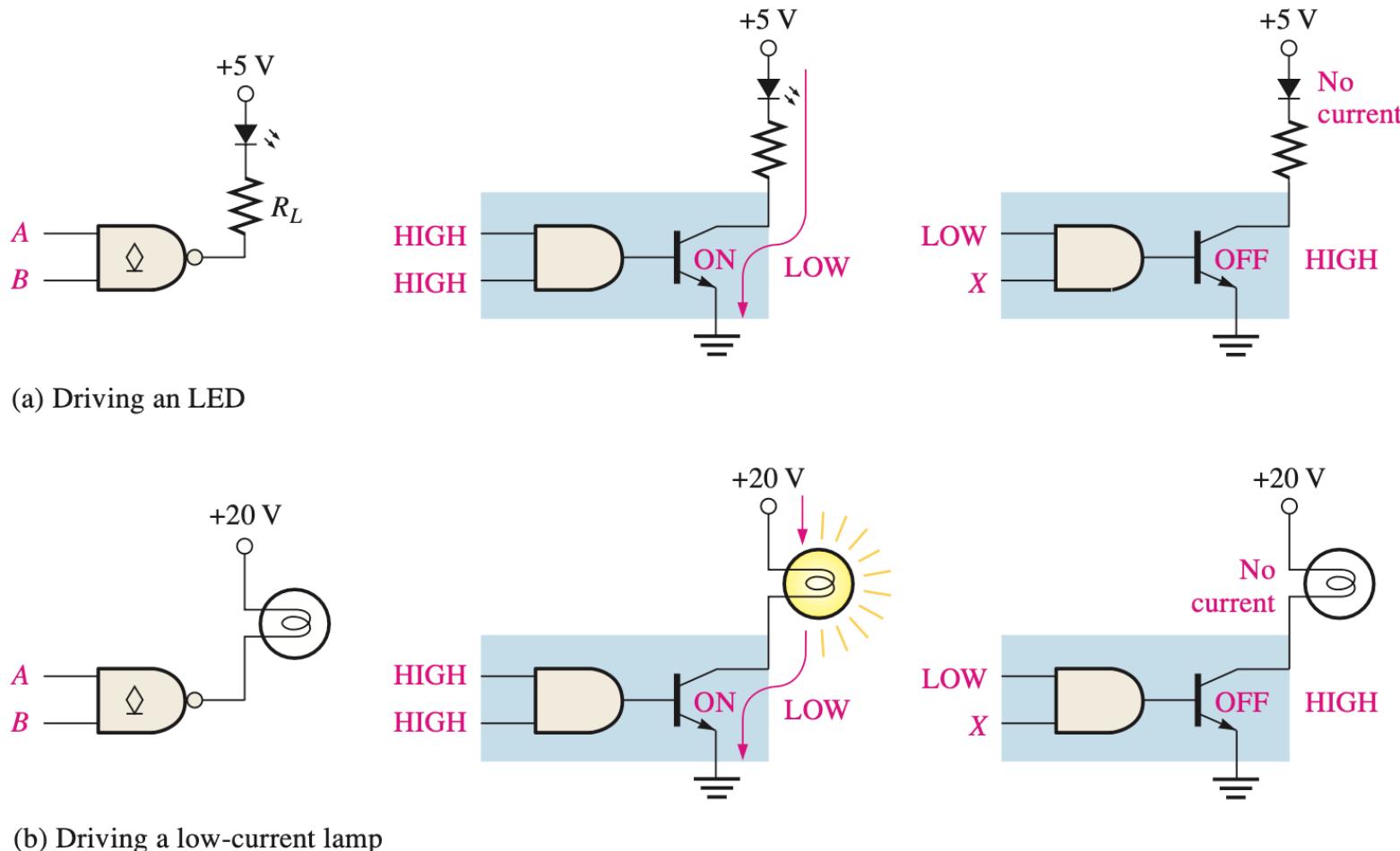


FIGURE 15–41 Totem-pole outputs wired together. Such a connection may cause excessive current through Q_1 of device A and Q_2 of device B and should never be used.

Open-Collector Buffer/Drivers



EXAMPLE 15-7

Determine the value of the limiting resistor, R_L , in the open-collector circuit of Figure 15–43 if the LED current is to be 20 mA. Assume a 1.5 V drop across the LED when it is forward-biased and a LOW-state output voltage of 0.1 V at the output of the gate.

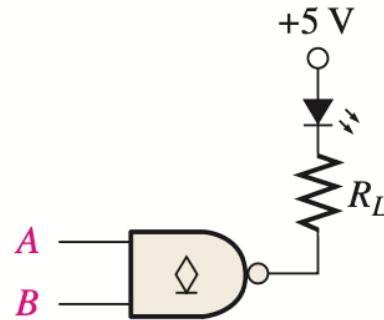


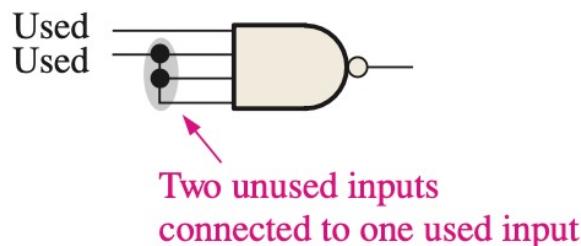
FIGURE 15–43

Solution

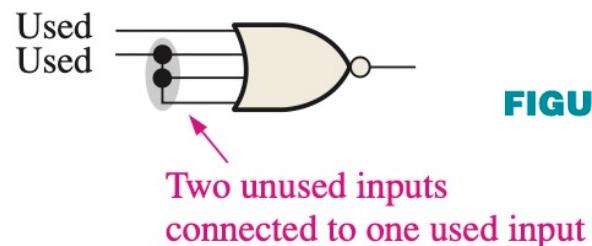
$$V_{R_L} = 5 \text{ V} - 1.5 \text{ V} - 0.1 \text{ V} = 3.4 \text{ V}$$

$$R_L = \frac{V_{R_L}}{I} = \frac{3.4 \text{ V}}{20 \text{ mA}} = 170 \Omega$$

Unused TTL Inputs

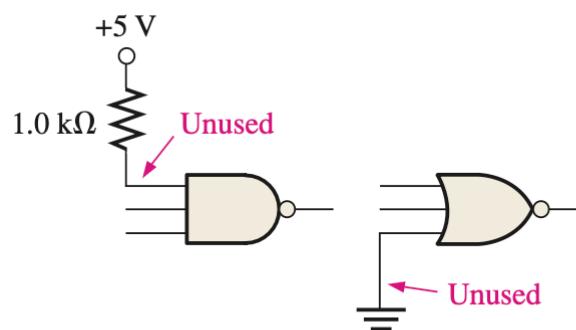


This connection counts as:
1 unit load in LOW state
3 unit loads in HIGH state



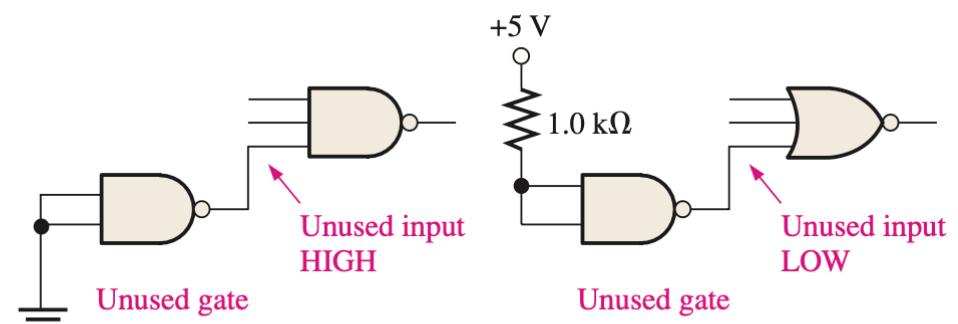
This connection counts as:
3 unit loads in LOW state
3 unit loads in HIGH state

(a) Tied-together inputs



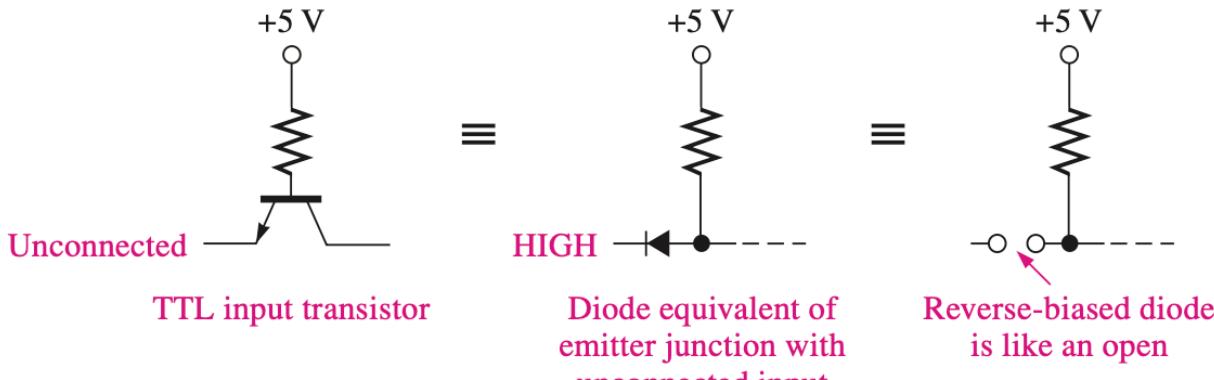
(b) Inputs to V_{CC} or ground

FIGURE 15-45 Methods for handling unused TTL inputs.



(c) Inputs to unused output

FIGURE 15-44 Comparison of an open TTL input and a HIGH-level input.



5. Comparison of CMOS and TTL Performance

TABLE 15-1

Comparison of selected performance parameters of several 74XX IC families.

	Bipolar (TTL)			BiCMOS ABT	CMOS						
					5 V			3.3 V			
	F	LS	ALS		HC	AC	AHC	LV	LVC	ALVC	
Speed											
Gate propagation delay, t_p (ns)	3.3	10	7	3.2	7	5	3.7	9	4.3	3	
FF maximum clock freq. (MHz)	145	33	45	150	50	160	170	90	100	150	
Power Dissipation Per Gate											
Bipolar: 50% dc (mW)	6	2.2	1.4								
CMOS: quiescent (μ W)				17	2.75	0.55	2.75	1.6	0.8	0.8	
Output Drive											
I_{OL} (mA)	20	8	8	64	4	24	8	12	24	24	

6. Emitter-Coupled Logic (ECL) Circuits

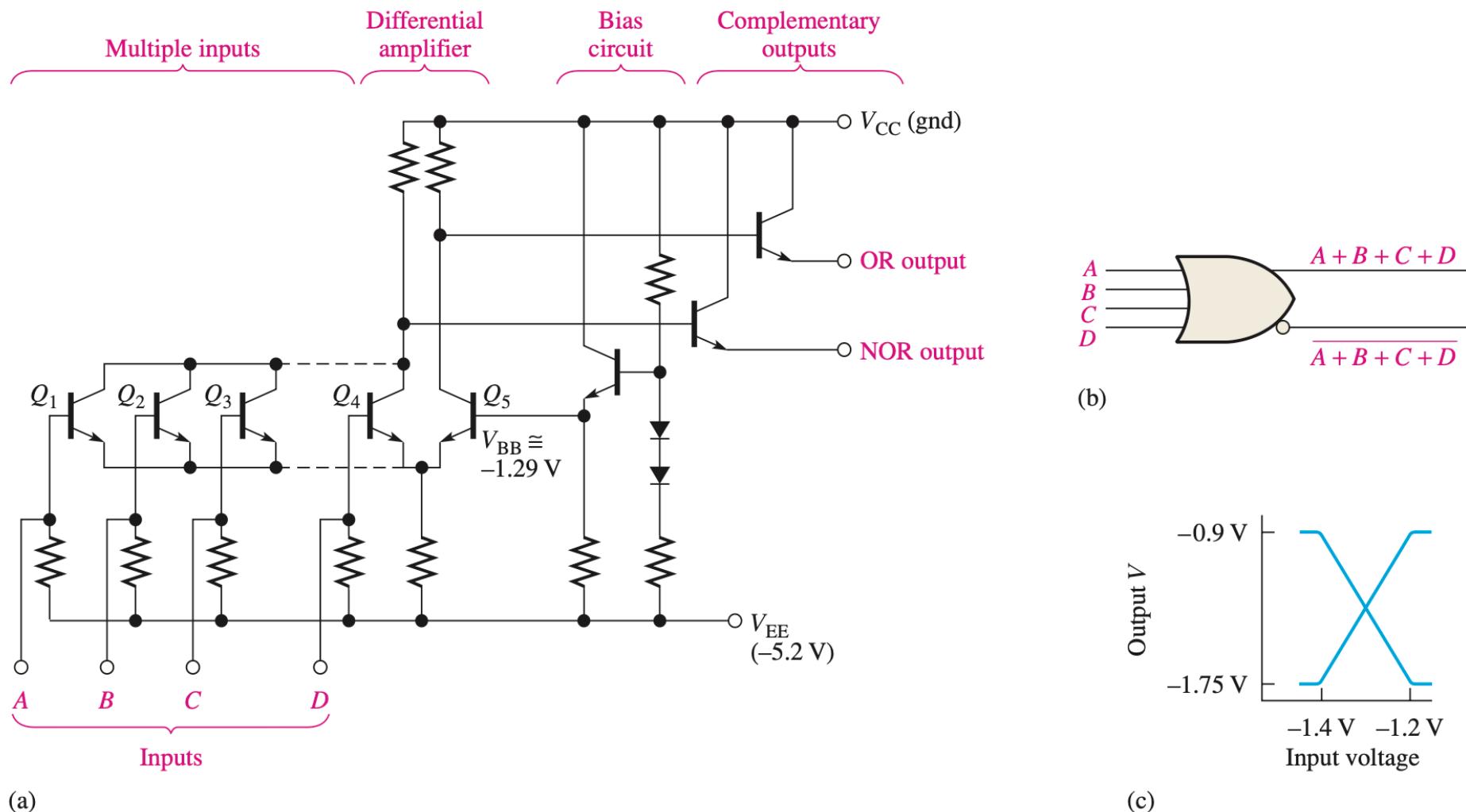


FIGURE 15-46 An ECL OR/NOR gate circuit.

Comparison of ECL with TTL and CMOS

TABLE 15-2

Comparison of ECL series performance parameters with F and AHC.

	Bipolar (TTL) F	CMOS AHC	Bipolar (ECL)
Speed			
Gate propagation delay, t_p (ns)	3.3	3.7	0.22–1
FF maximum clock freq. (MHz)	145	170	330–2800
Power Dissipation Per Gate			
Bipolar: 50% dc	6 mW		25 mW–73 mW
CMOS: quiescent		2.75 μ W	

7. PMOS, NMOS, and E²CMOS PMOS

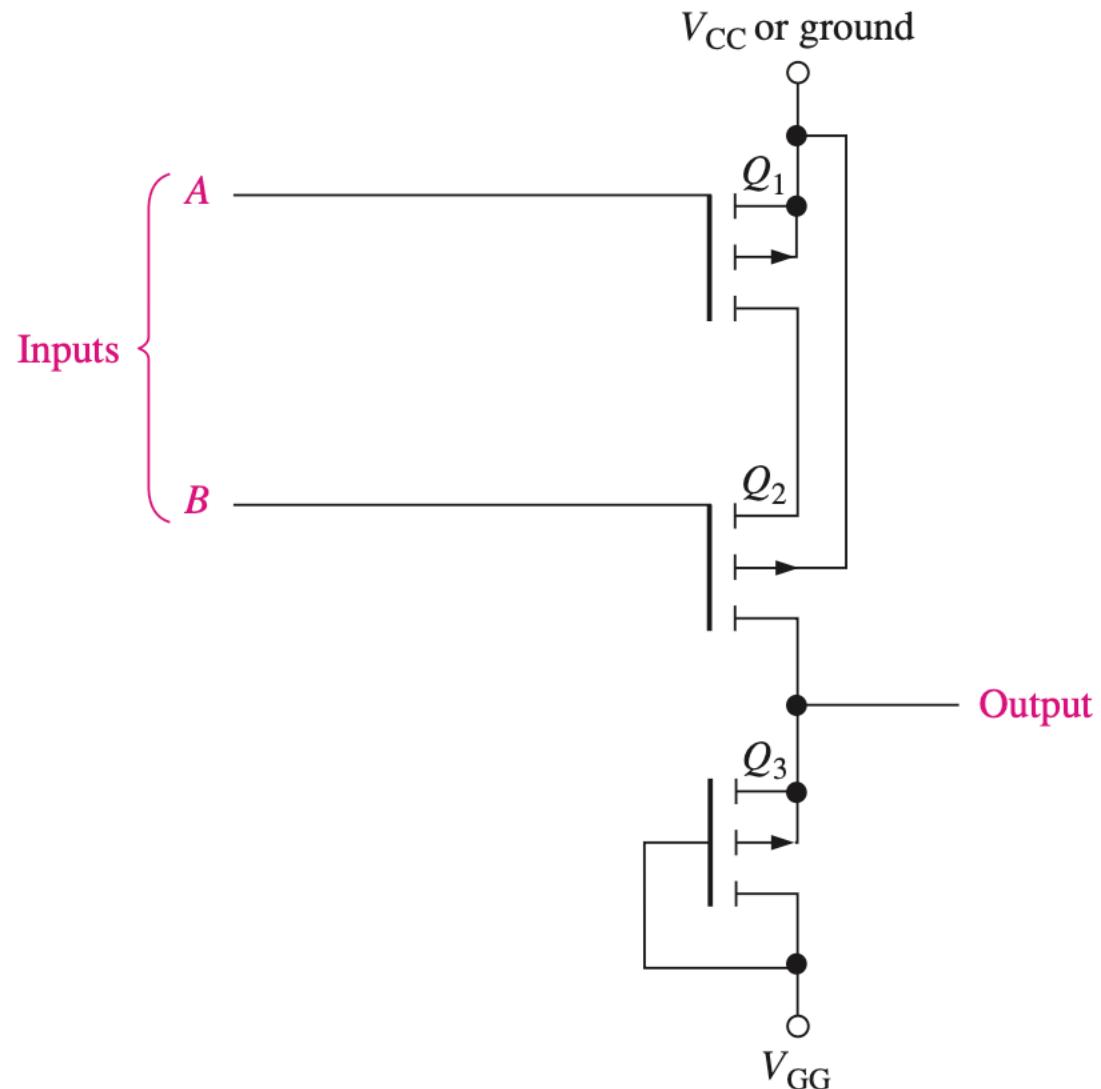


FIGURE 15–47 Basic PMOS gate.

NMOS

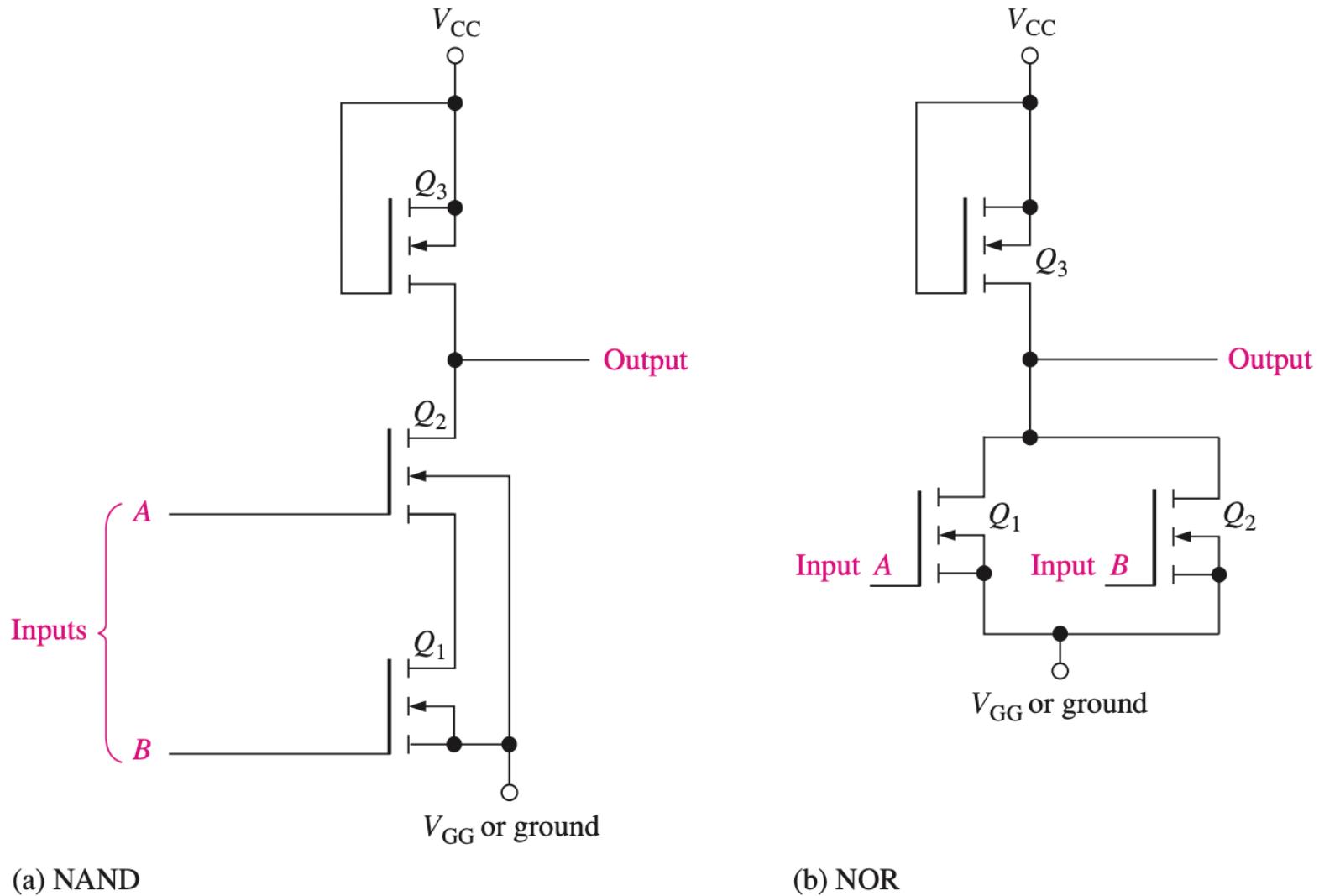


FIGURE 15–48 Two NMOS gates.

E²CMOS (electrically erasable CMOS)

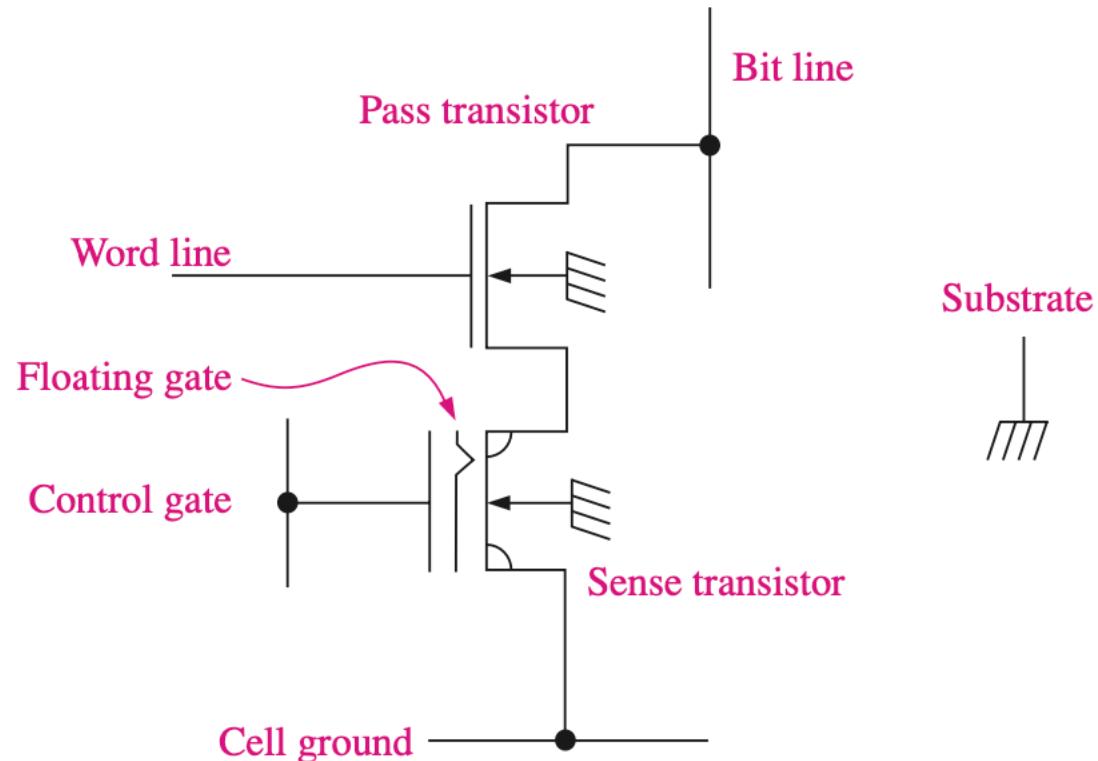
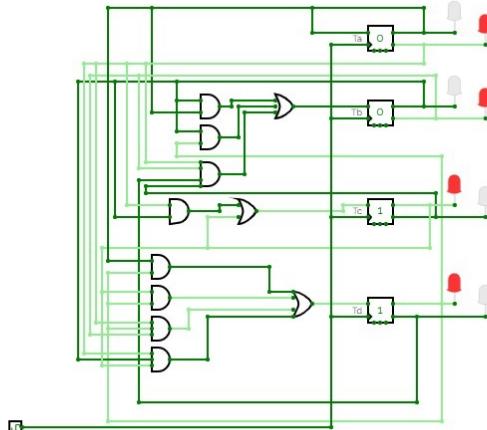


FIGURE 15–49 An E²CMOS cell.



THE END

Lecture 15: Integrated Circuit Technologies



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