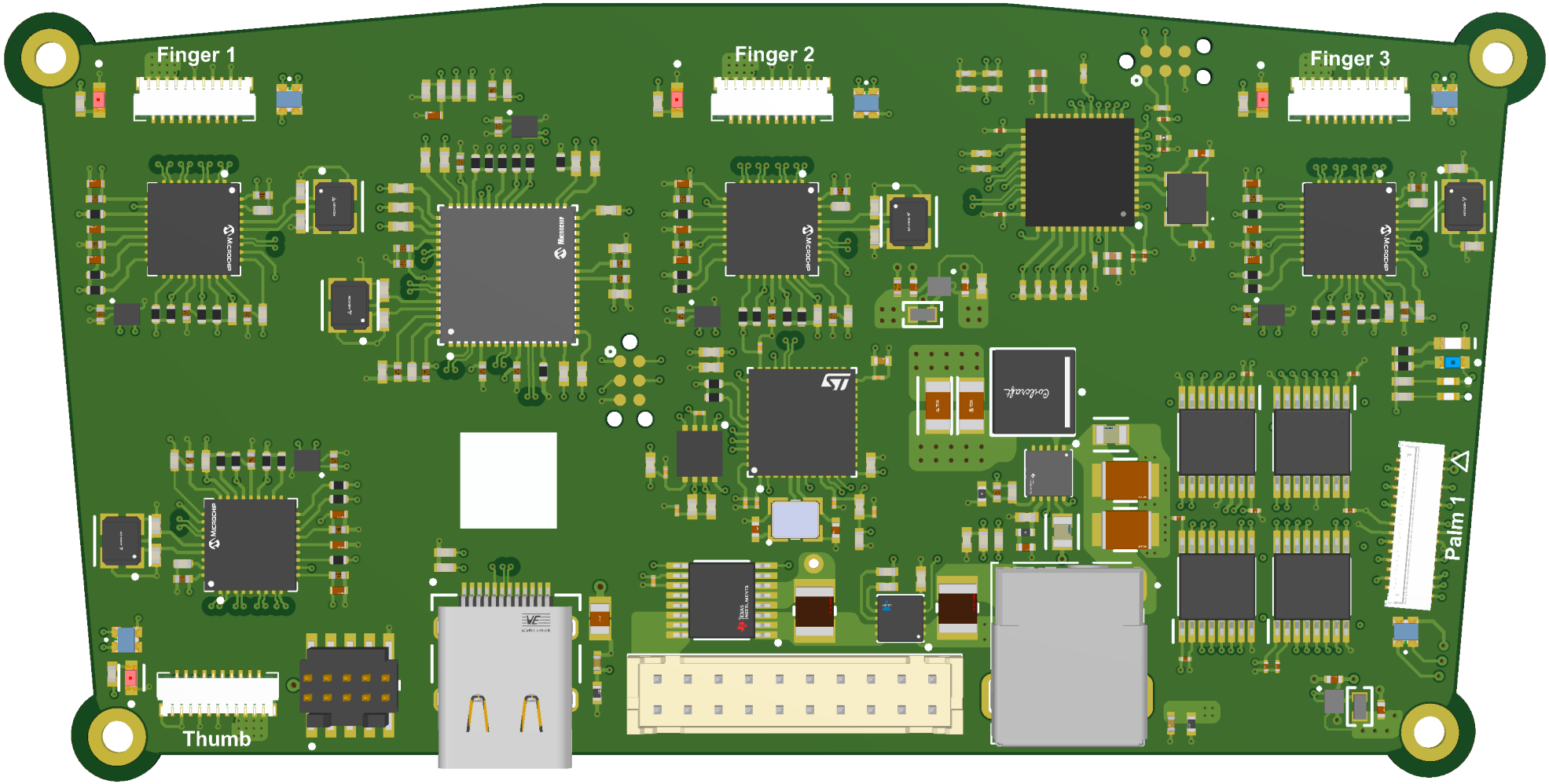
Realistic View



Plexus Hand Logic

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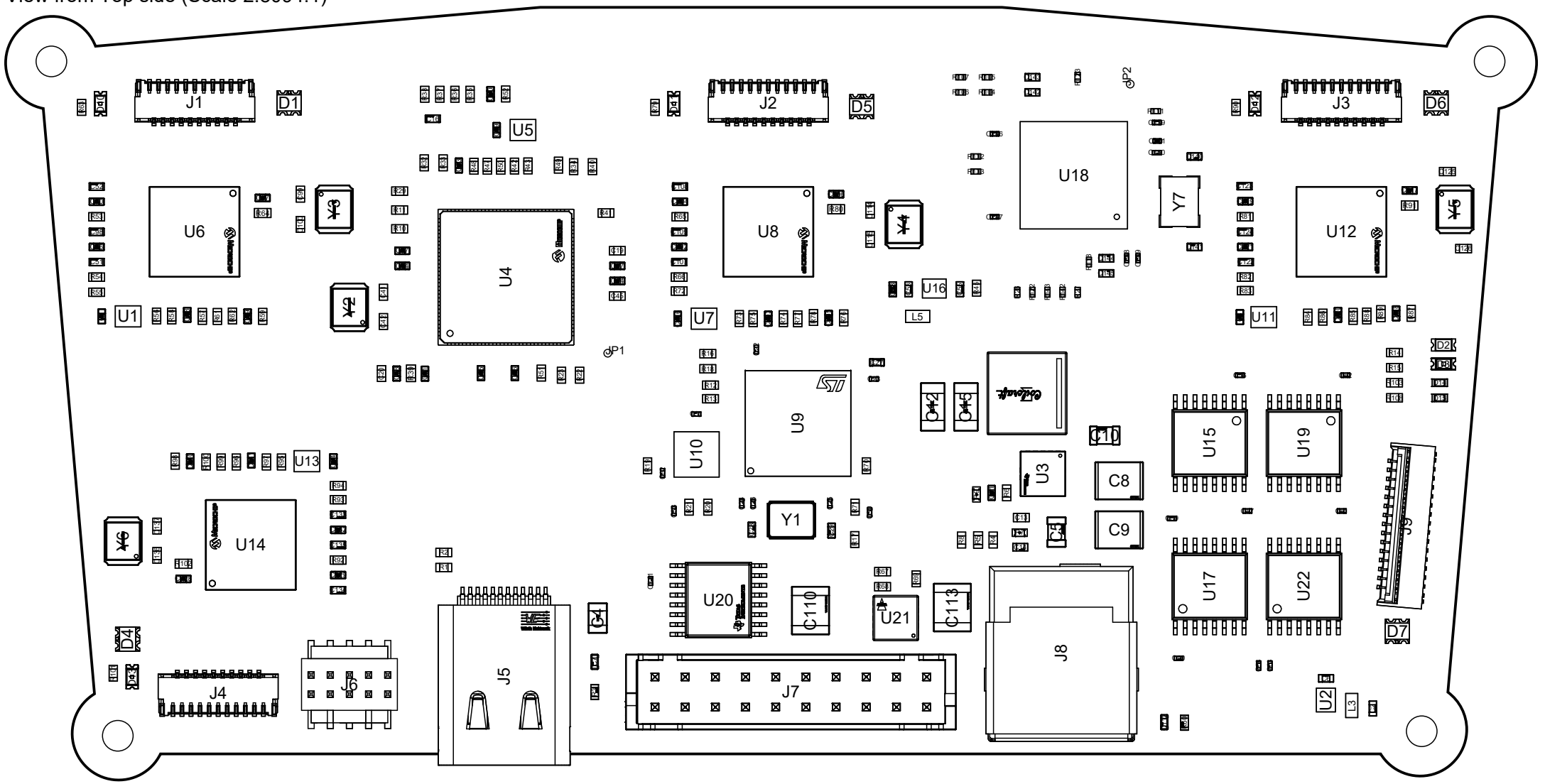
View from Top side (Scale 2.8094:1)

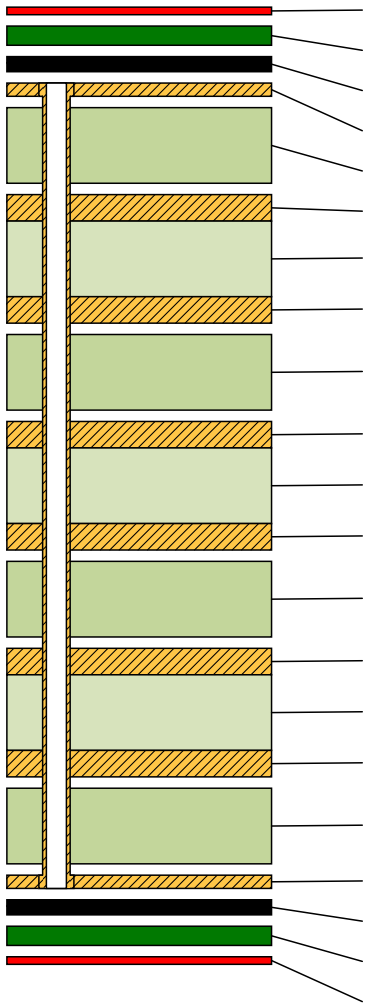


NOTES: UNITS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

1. STACKUP SUMMARY:
   A. NUMBER OF COPPER LAYERS: 8
   B. BOARD THICKNESS SHALL BE 62mil +/- 10%
   C. COPPER: See Layer Stack
   D. DEFAULT TRACE/SPACE: 5mil / 5mil
   E. CONDUCTOR WIDTH TOLERANCE = +/- 0.01mm
2. SURFACE FINISH/PLATING:
   A. BOARD SHALL BE IMMERSION GOLD PLATED (ENIG)
3. SOLDERMASK WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C, CLASS T.
   COLOR: MATTE BLACK
4. LOCATE MANUFACTURER'S IDENTIFICATION AND LOT CODE ON PRIMARY SIDE FREE FROM ALL METAL ENTITY RENDERED IN SILKSCREEN.
5. DIFFERENTIAL CONTROLLED IMPEDANCE REQUIRED ON BOARD.
   SEE TABLE : DIFFERENTIAL CONTROLLED IMPEDANCE
   SEE TABLE : SINGLE ENDED CONTROLLED IMPEDANCE
6. DETAILS NOT SPECIFIED ARE AT MANUFACTURER'S OPTION BUT FINAL APPROVAL MUST BE OBTAINED

Note: Vendor preferred

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.03mm	SM-002	Solder Mask	GTS
PbSn	Top Surface Finish	0.02mm		Surface Finish	
CF-004	**Top Layer**	**0.02mm**		**Signal**	**GTL**
Prepreg		*0.13mm*	*PP-016*	*Dielectric*	
CF-004	**Int1 (GND)**	**0.04mm**		**Signal**	**G1**
Core		*0.23mm*	*Core-027*	*Dielectric*	
CF-004	**Int2 (GND/PWR)**	**0.04mm**		**Signal**	**G2**
Prepreg		*0.20mm*	*PP-006*	*Dielectric*	
CF-004	**Int3 (SIG/PWR)**	**0.04mm**		**Signal**	**G3**
Core		*0.23mm*	*Core-027*	*Dielectric*	
CF-004	**Int4 (SIG/PWR)**	**0.04mm**		**Signal**	**G4**
Prepreg		*0.20mm*	*PP-006*	*Dielectric*	
CF-004	**Int5 (GND)/PWR)**	**0.04mm**		**Signal**	**G5**
Core		*0.23mm*	*Core-027*	*Dielectric*	
CF-004	**Int6 (GND)**	**0.04mm**		**Signal**	**G6**
Prepreg		*0.13mm*	*PP-016*	*Dielectric*	
CF-004	**Bottom Layer**	**0.02mm**		**Signal**	**GBL**
PbSn	Bottom Surface Finish	0.02mm		Surface Finish	
Surface Material	Bottom Solder	0.03mm	SM-002	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.6

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Gap	Reference layers	Clearance	Target Tolerance
1	Edge-Coupled Coated Microstrip	90	93.83	Top Layer	0.15mm	0.13mm	Int1 (GND)	0.13mm	10%
2	Edge-Coupled Coated Microstrip	90	93.83	Bottom Layer	0.15mm	0.13mm	Int6 (GND)	0.13mm	10%