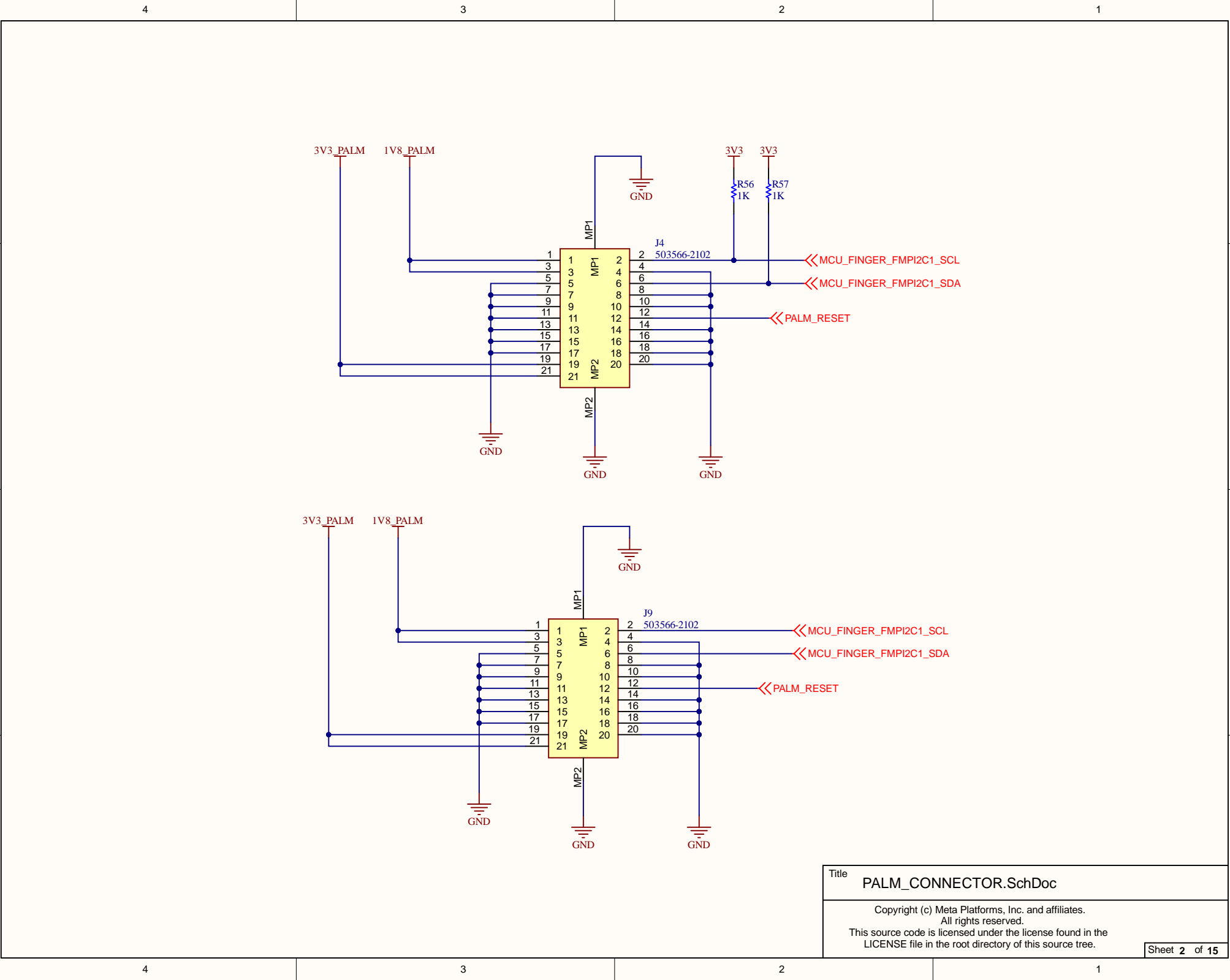
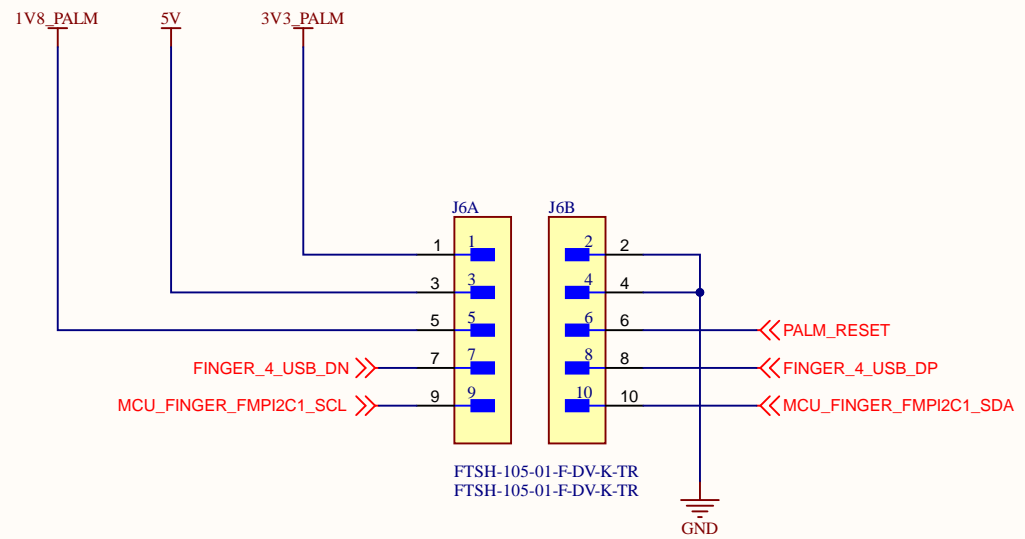
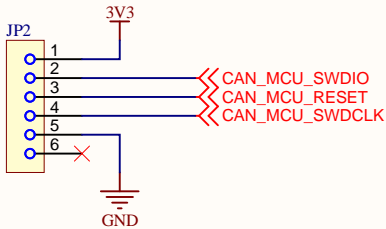
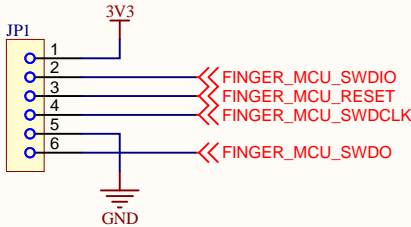


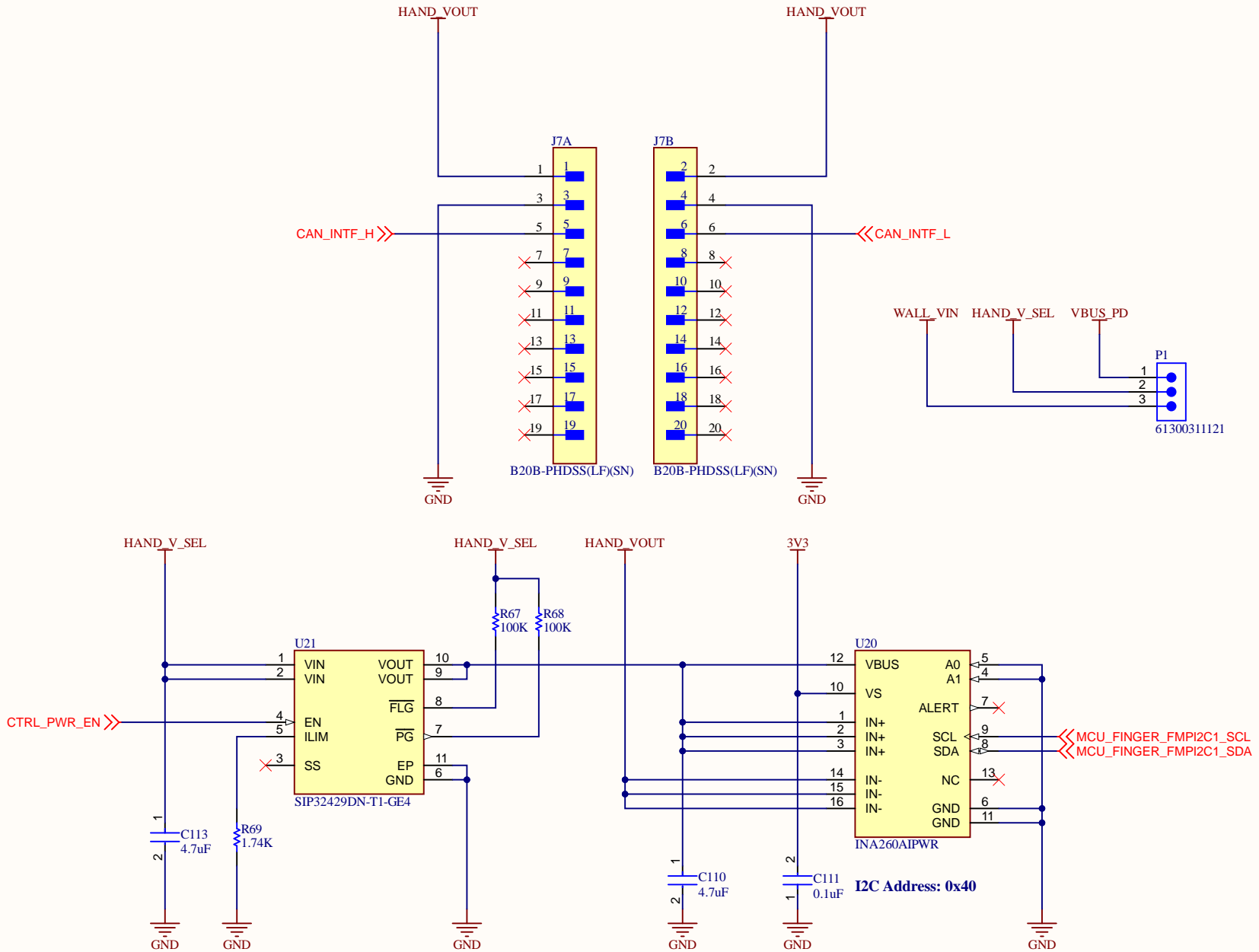
Title FINGER_CONNECTORS.SchDoc

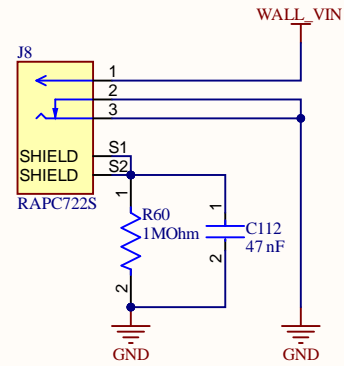
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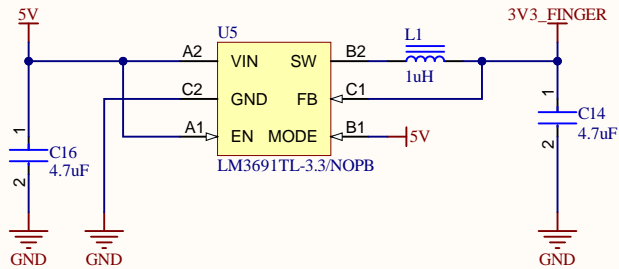




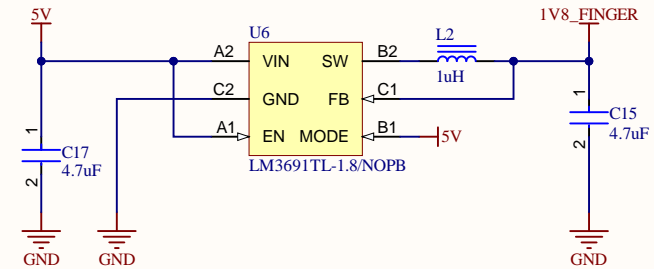




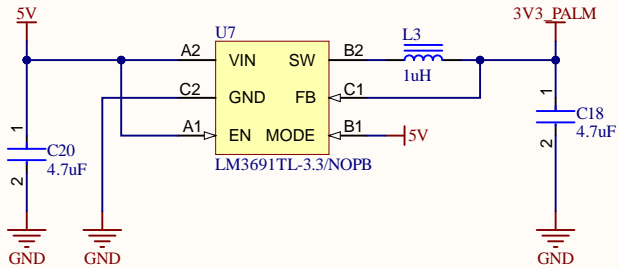
3.3V FINGER



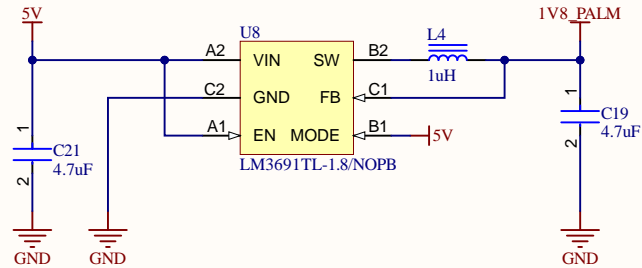
1.8V FINGER



3.3V PALM

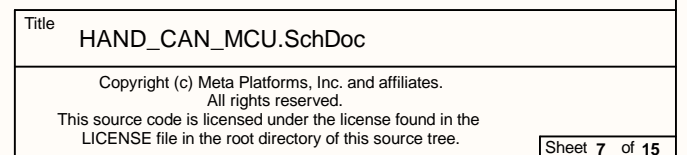


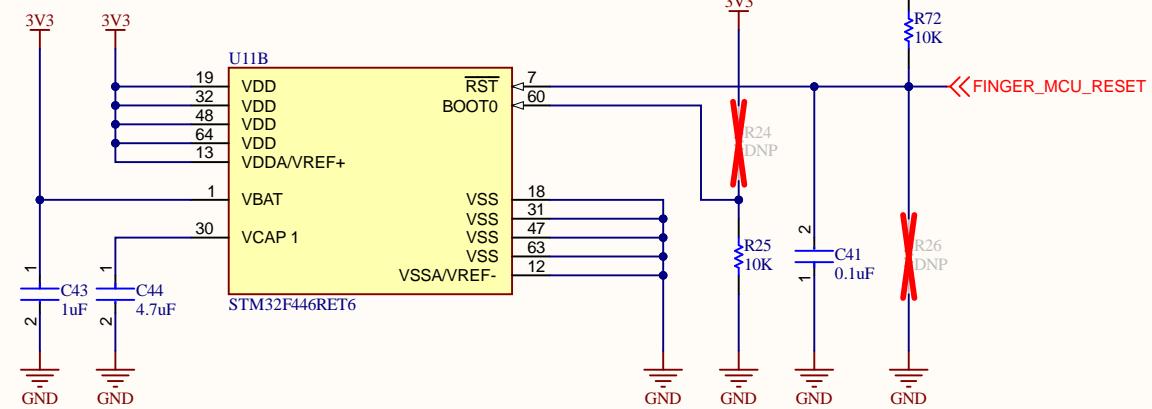
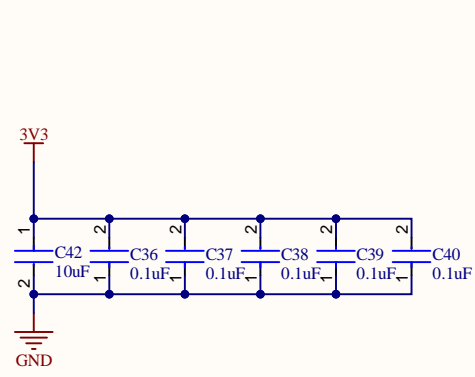
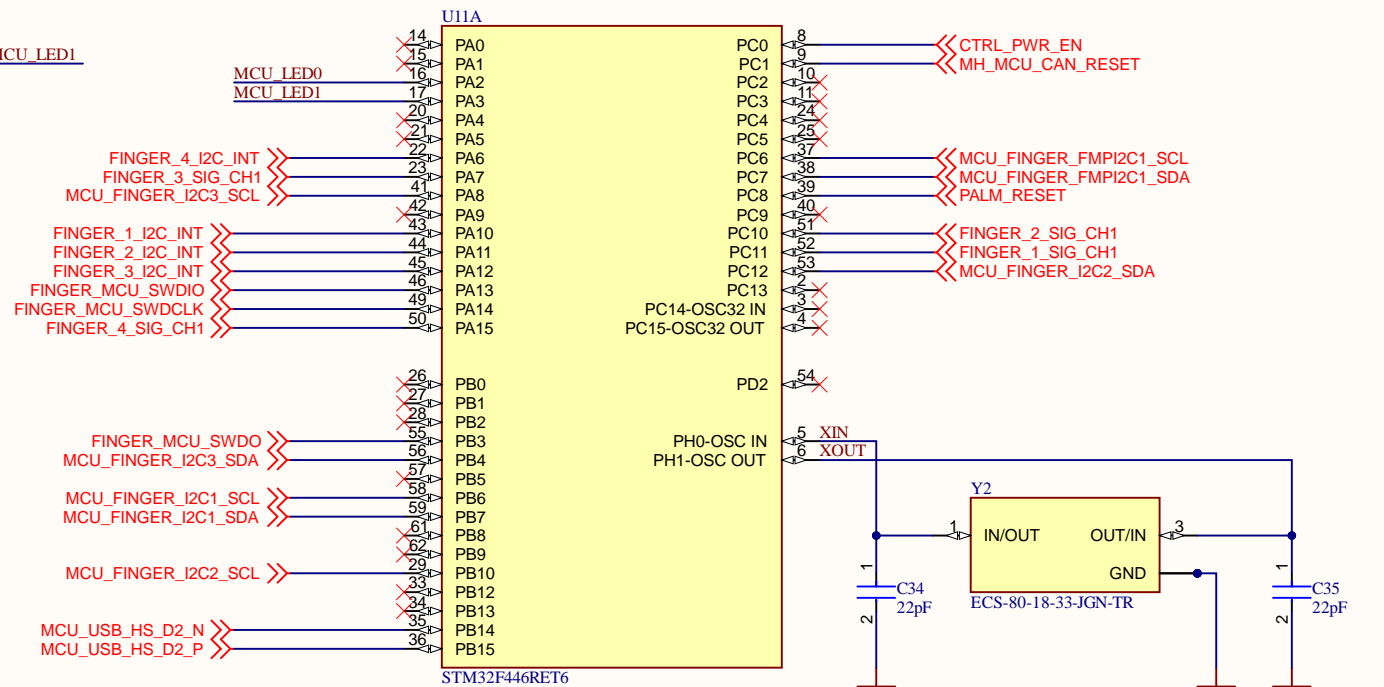
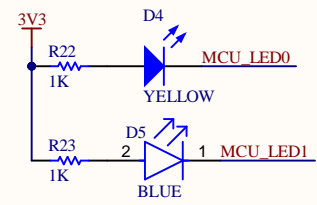
1.8V PALM

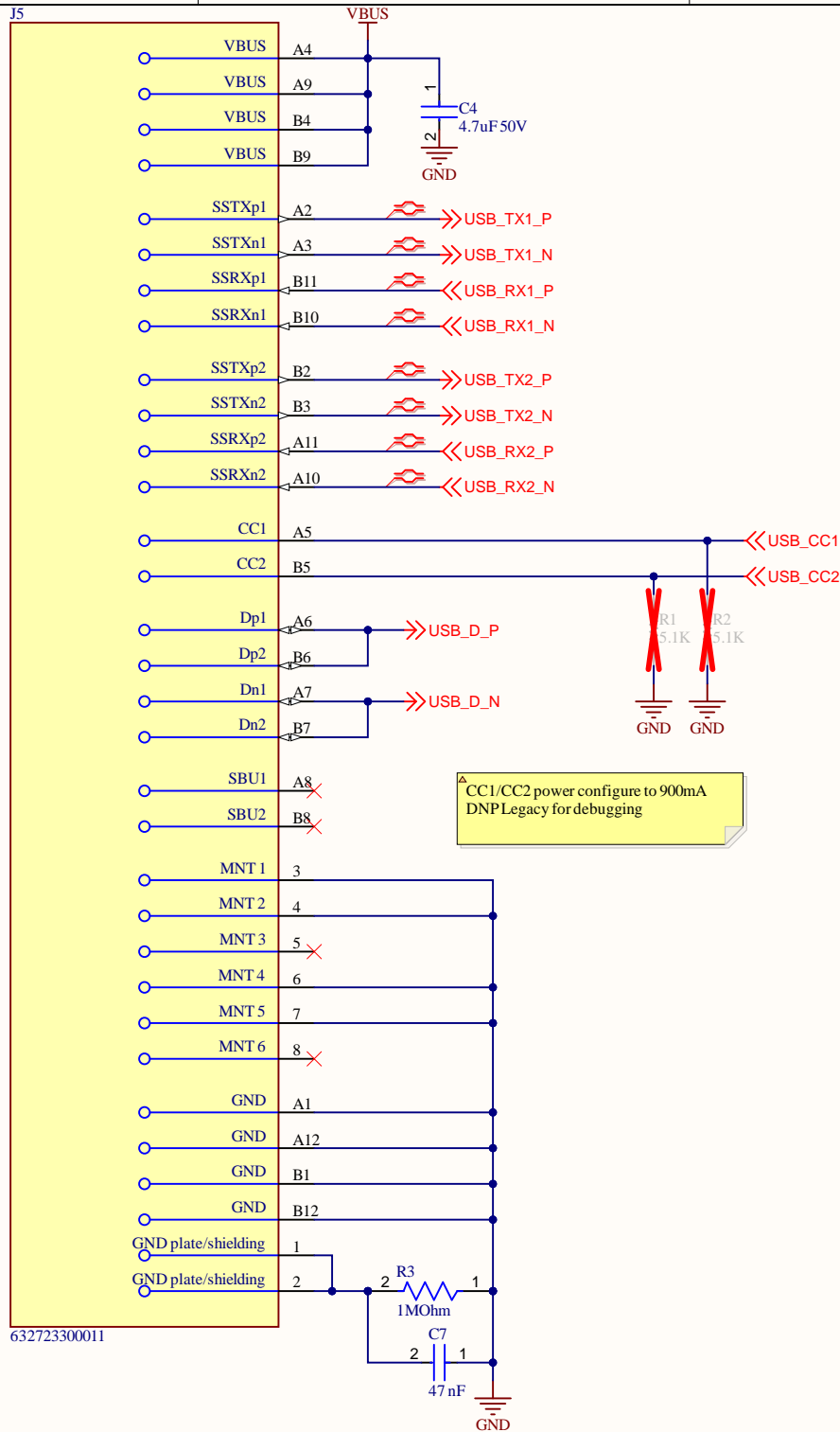


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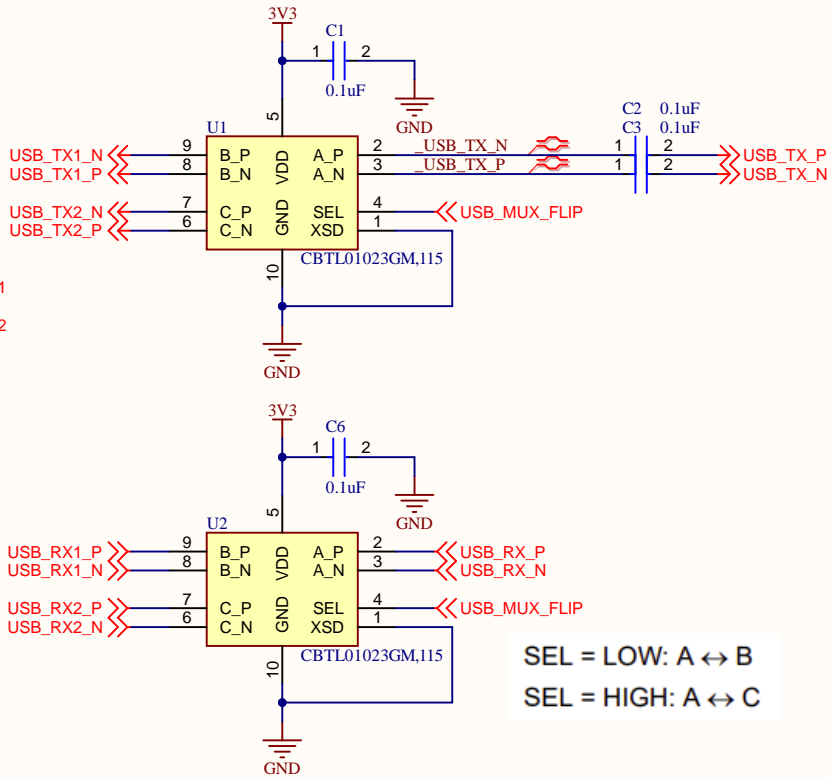




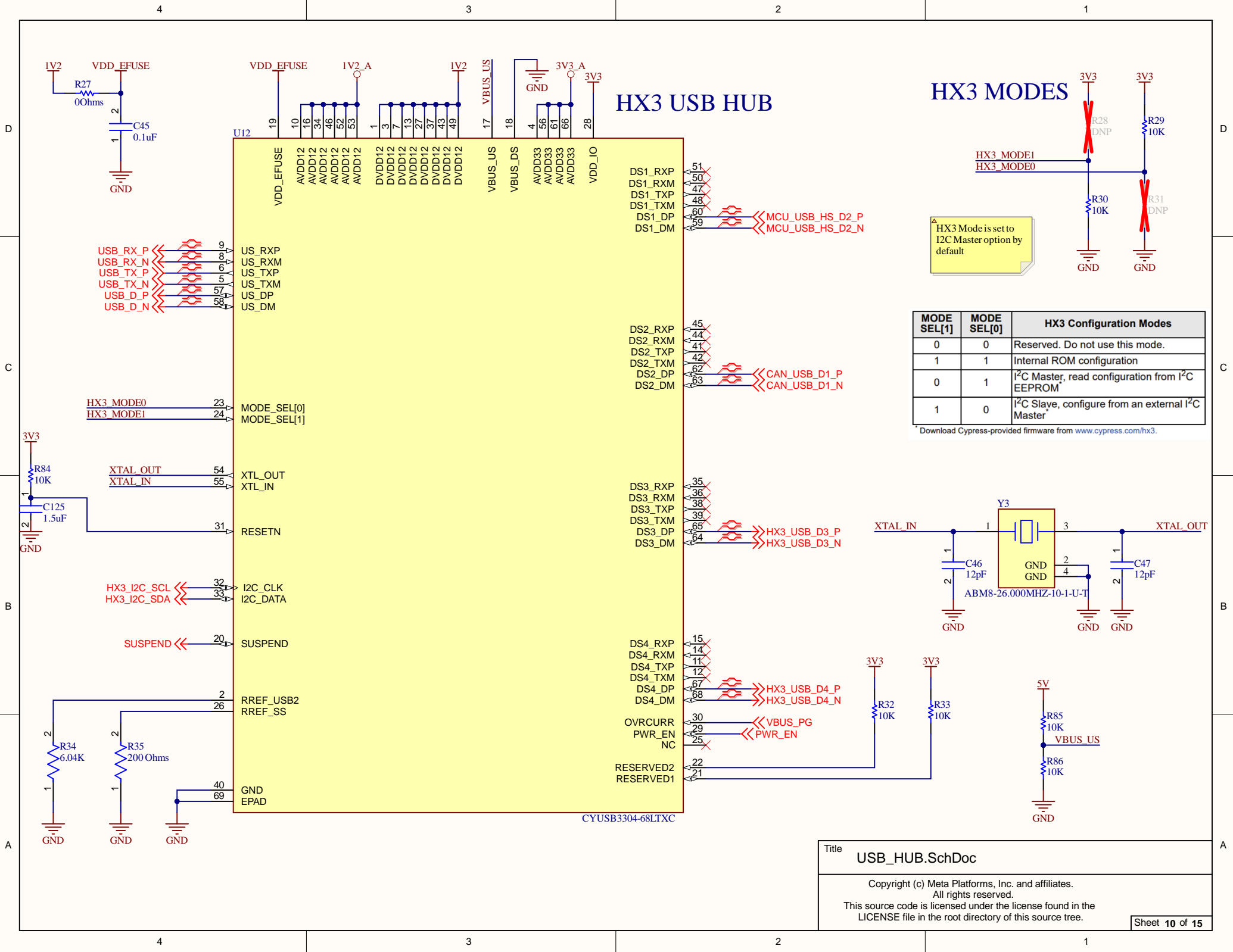


CC1/CC2 power configure to 900mA
DNP Legacy for debugging

USB C POLARITY



SEL = LOW: A ↔ B
SEL = HIGH: A ↔ C



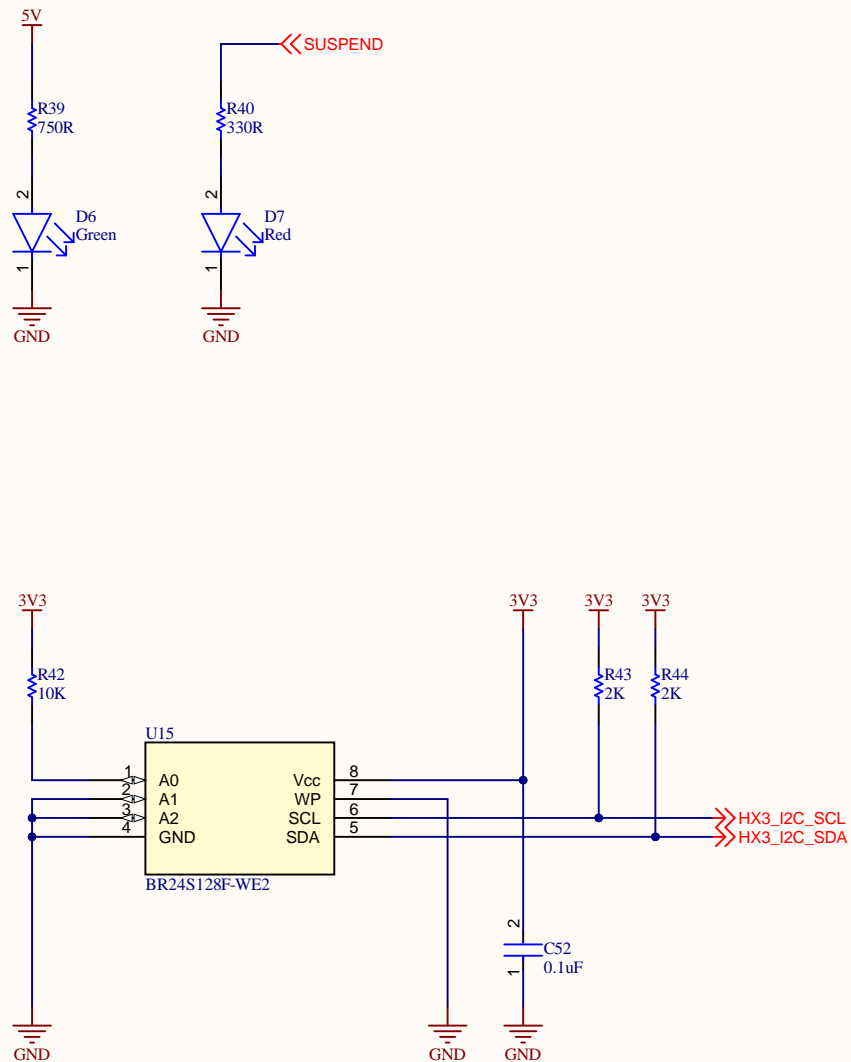
HX3 USB HUB

HX3 MODES

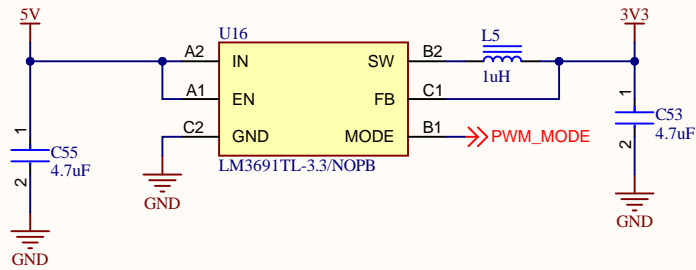
A
HX3 Mode is set to I2C Master option by default

MODE SEL[1]	MODE SEL[0]	HX3 Configuration Modes
0	0	Reserved. Do not use this mode.
1	1	Internal ROM configuration
0	1	I ² C Master, read configuration from I ² C EEPROM
1	0	I ² C Slave, configure from an external I ² C Master

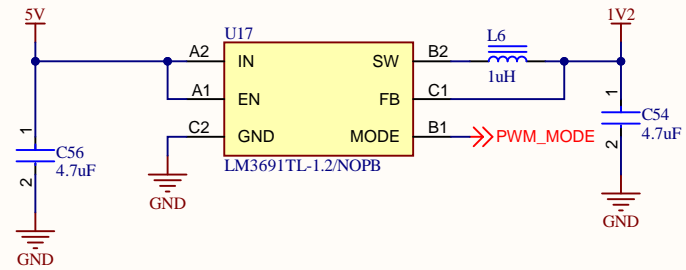
Download Cypress-provided firmware from www.cypress.com/hx3.



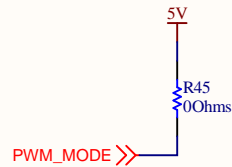
3.3V REGULATOR



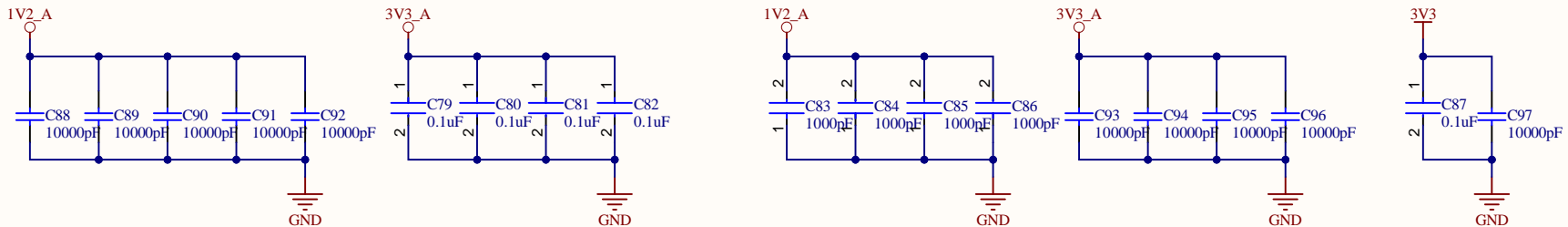
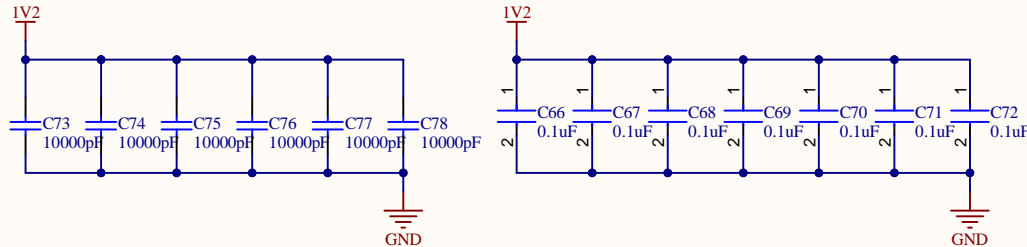
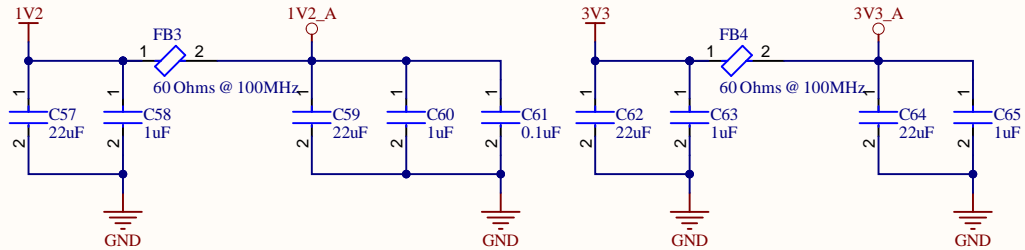
1.2V REGULATOR



POWER FILTERING



Switching regulators are set to forced PWM mode

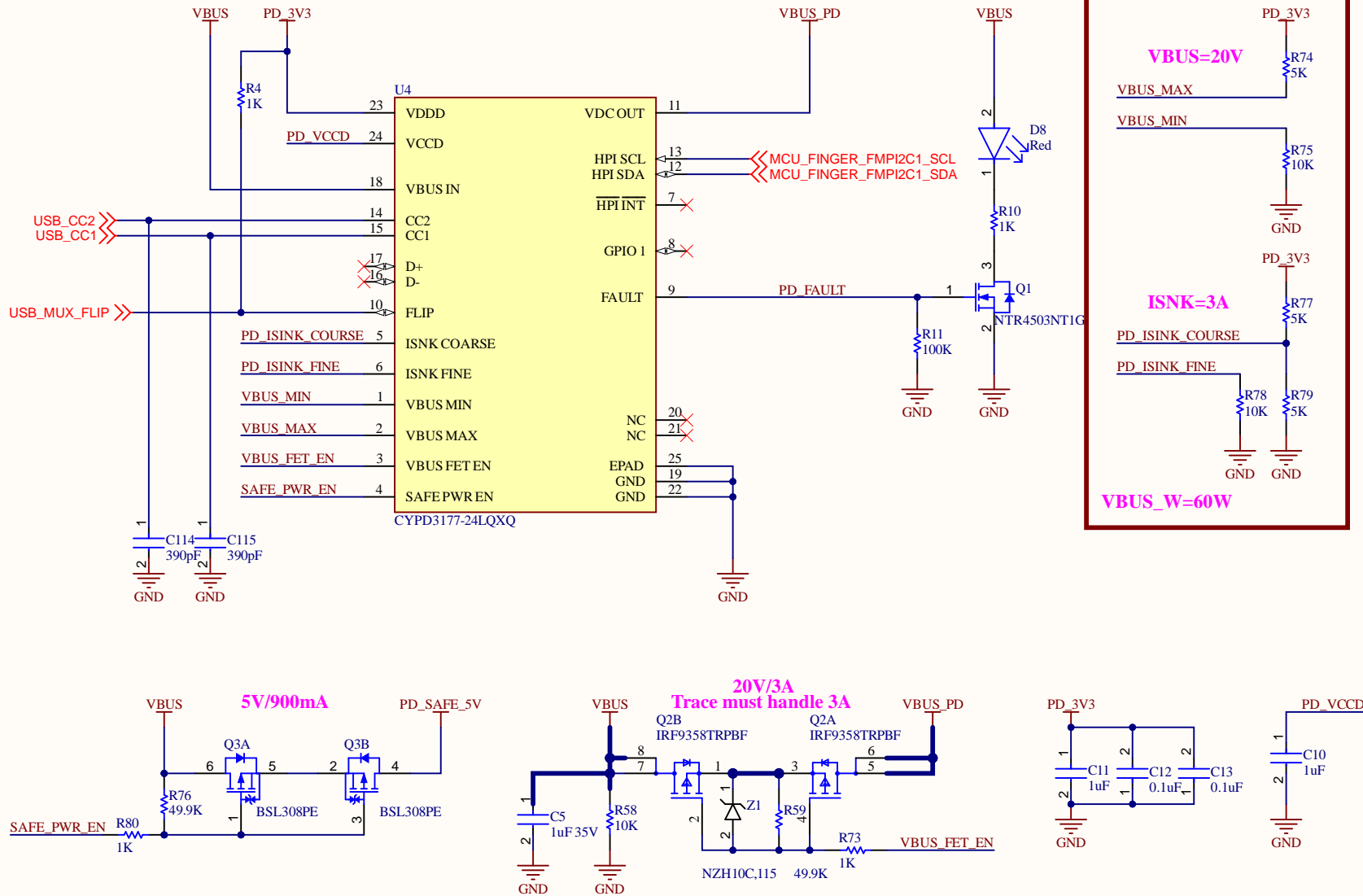


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FLIP

This is an open drain I/O that requires an external pull-up resistor. The presence or the value of the pull-up resistor connected to this pin determines the data capability reported in the UFP Vendor Data Object (VDO) by the BCR device to the Downstream Facing Port (DFP).
If there is no pull-up resistor on this pin or if its value is less than or equal to 4.7 kΩ, then the UFP VDO data capability bit is set to 1, which correlates to the port being data capable. If the value of the pull-up resistor is 50 kΩ, then the UFP VDO data capability bit is set to 0, which correlates to the port not being data capable.



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