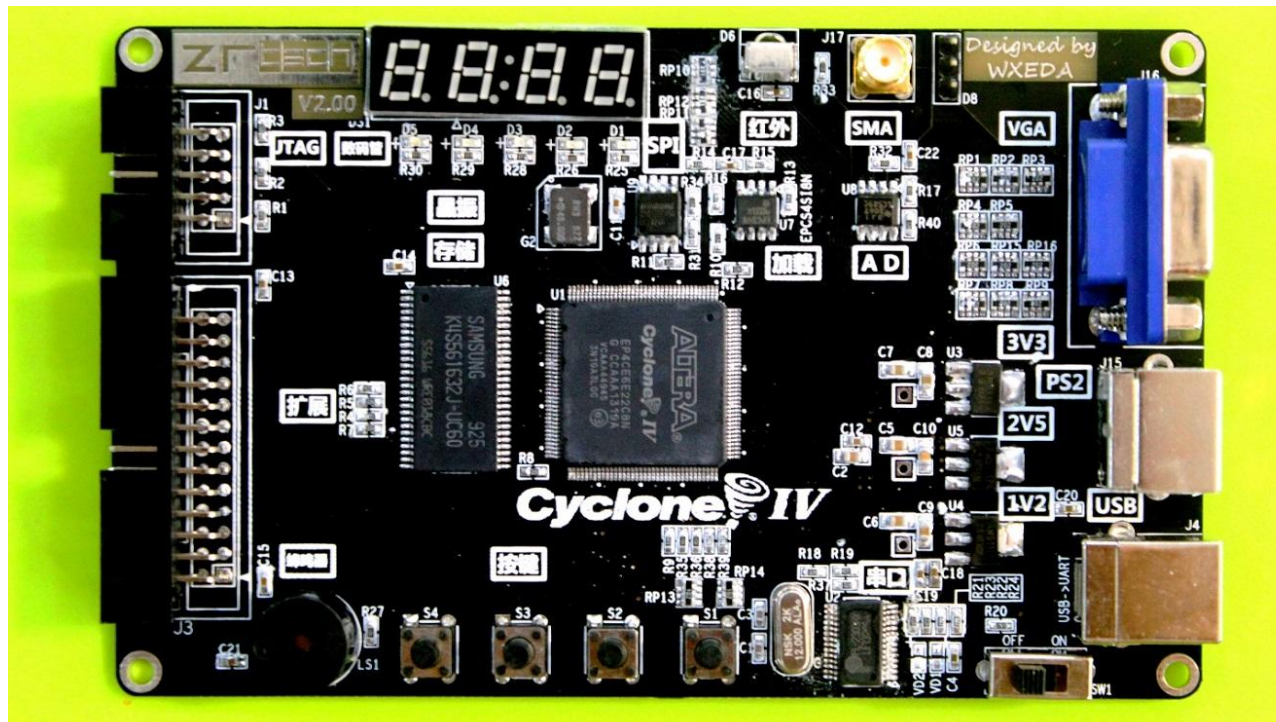


# Прошивка FPGA. Altera Quartus

# Отладочная плата

- FPGA Altera Cyclone IV EP4CE6E22C8N
- 7-сегментный индикатор
- 4 светодиода
- Питание подводится через USB
- Прошивка загружается через 10-пиновый JTAG
- 48 МГц кварцевый генератор

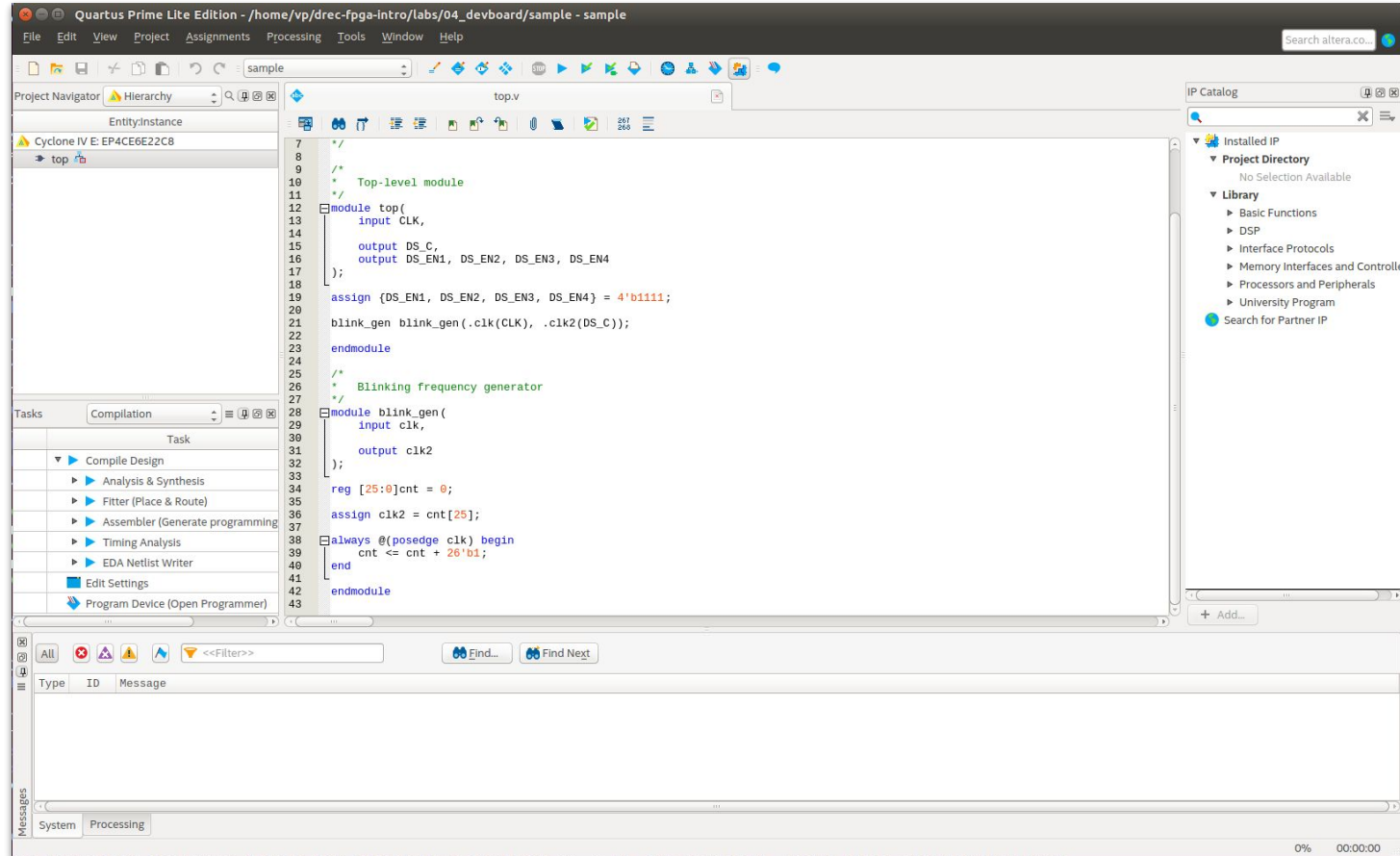


# Программатор

- USB для соединения с ПК
- 10-пиновый JTAG для соединения с отладочной платой



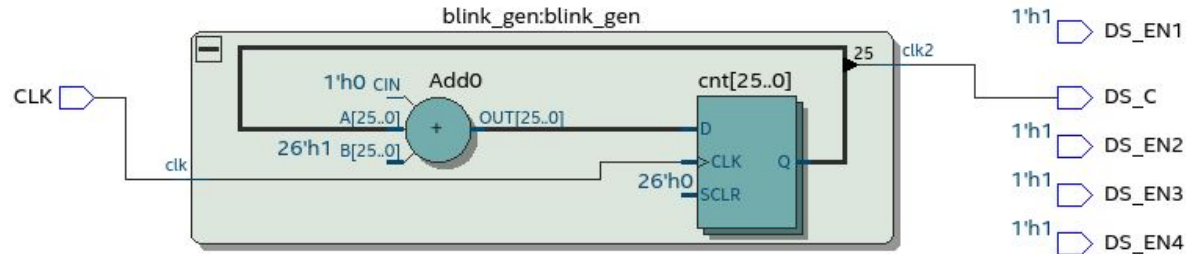
# Проект 04\_devboard в Quartus Prime Lite 18.1



# top.v

```
module top(  
    input CLK,  
  
    output DS_C,  
    output DS_EN1, DS_EN2, DS_EN3, DS_EN4  
);  
  
assign {DS_EN1, DS_EN2, DS_EN3, DS_EN4} = 4'b1111;  
  
blink_gen blink_gen(.clk(CLK), .clk2(DS_C));  
  
endmodule
```

```
module blink_gen(  
    input clk,  
  
    output clk2  
);  
  
reg [25:0] cnt = 0;  
  
assign clk2 = cnt[25];  
  
always @(posedge clk) begin  
    cnt <= cnt + 26'b1;  
end  
  
endmodule
```



# Compile Design

The screenshot displays the Quartus Prime Lite Edition interface during a compilation process. The main window is titled "Quartus Prime Lite Edition - /home/vp/drec-fpga-intro/labs/04\_devboard/sample - sample". The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The top toolbar contains various icons for file operations and compilation.

The left sidebar shows the Project Navigator with a Hierarchy view. The Entity/Instance list shows "Cyclone IV E: EP4CE6E22C8" and "top.v". The Table of Contents on the left lists various reports, with "Flow Summary" selected. The main window displays the "Flow Summary" report, which provides a detailed overview of the compilation process.

The "Flow Summary" report includes the following information:




- Flow Status: Successful - Sat Jan 19 14:01:15 2019
- Quartus Prime Version: 18.1.0 Build 625 09/12/2018 SJ Lite Edition
- Revision Name: sample
- Top-level Entity Name: top
- Family: Cyclone IV E
- Device: EP4CE6E22C8
- Timing Models: Final
- Total logic elements: 26
- Total registers: 26
- Total pins: 6
- Total virtual pins: 0
- Total memory bits: 0
- Embedded Multiplier 9-bit elements: 0
- Total PLLs: 0









The bottom status bar shows the progress of the compilation, with a progress bar indicating 5% completion. The Messages window at the bottom displays the following messages:


- 12128 Elaborating entity "blink\_gen" for hierarchy "blink\_gen:blink\_gen"
- 13024 Output pins are stuck at VCC or GND
- 280030 Timing-Driven Synthesis is running
- 16010 Generating hard\_block partition "hard\_block:auto\_generated\_inst"
- 21057 Implemented 32 device resources after synthesis - the final resource count might be different
- Quartus Prime Analysis & Synthesis was successful. 0 errors, 6 warnings

The bottom right corner of the window shows the progress bar at 25% and the time 00:00:13.

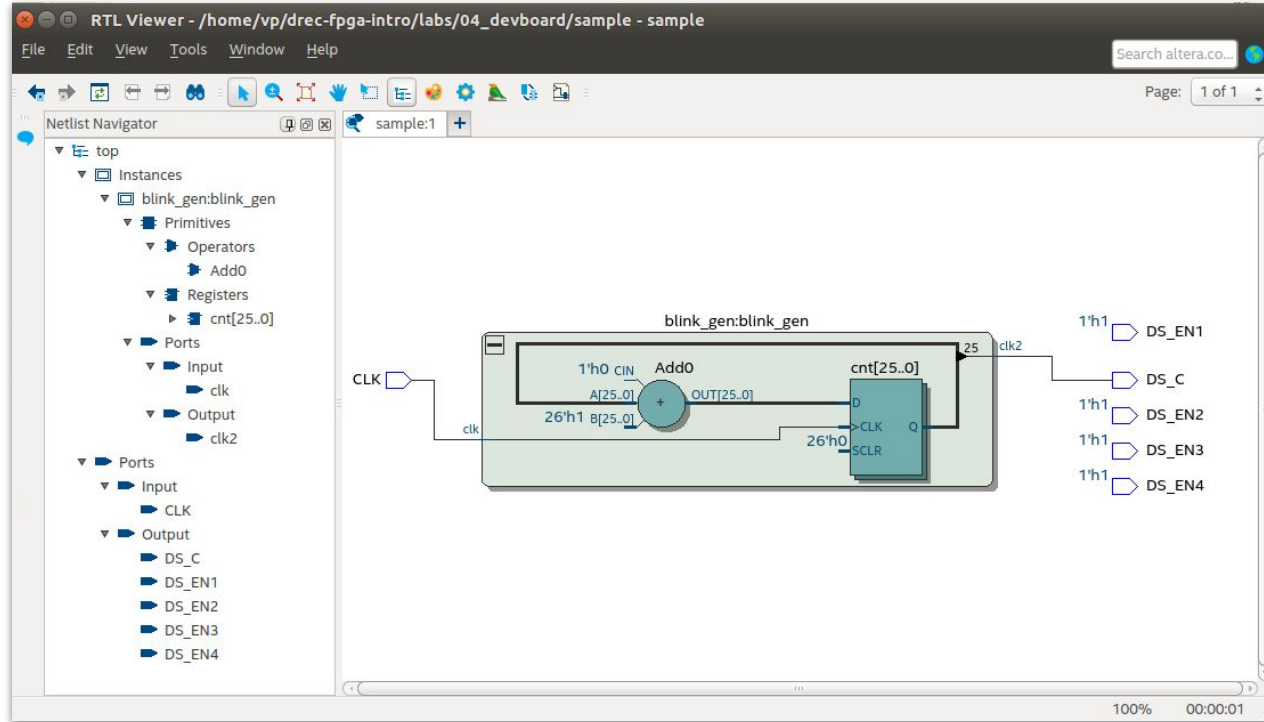
# Compilation Report

Entity:Instance	
	Cyclone IV E: EP4CE6E22C8
▼  top	
	blink_gen:blink_gen

Tasks	
	Compilation
	Task
✓	▼  Compile Design
✓	▶  Analysis & Synthesis
✓	▶  Fitter (Place & Route)
✓	▶  Assembler (Generate programming)
✓	▶  Timing Analysis
	▶  EDA Netlist Writer
	 Edit Settings
	 Program Device (Open Programmer)

Flow Summary	
 <<Filter>>	
Flow Status	Successful - Sat Jan 19 14:01:23 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	sample
Top-level Entity Name	top
Family	Cyclone IV E
Device	EP4CE6E22C8
Timing Models	Final
Total logic elements	26 / 6,272 ( < 1 % )
Total registers	26
Total pins	6 / 92 ( 7 % )
Total virtual pins	0
Total memory bits	0 / 276,480 ( 0 % )
Embedded Multiplier 9-bit elements	0 / 30 ( 0 % )
Total PLLs	0 / 2 ( 0 % )

# RTL Design Viewer



Tools > Netlist Viewers > RTL Viewer



# Pin Planner

The screenshot shows the Pin Planner application window. The main area displays a top view of the Cyclone IV E EP4CE6E22C8 device with wire bond connections. The left sidebar contains a 'Report' section (report not available), a 'Groups' section, and a 'Tasks' section with options like 'Early Pin Planning', 'Run I/O Assignment Analysis', 'Export Pin Assignments...', 'Pin Finder...', and 'Highlight Pins'. The bottom section shows a table of pin assignments.

Top View  
Wire Bond, with Exposed Pad

Cyclone IV E  
EP4CE6E22C8

Pin Legend

Symbol	Pin Type
○	User I/O
●	User assigned...
●	Fitter assigne...
○	Unbonded pad
●	Reserved pin
○	Other configu...
○	DEV_OE
○	DEV_CLR
○	DIFF_n
○	DIFF_p
○	DQ
○	DQS
○	CLK_n
○	CLK_p
○	Other PLL
○	Other dual pu...
○	MSEL0
○	MSEL1

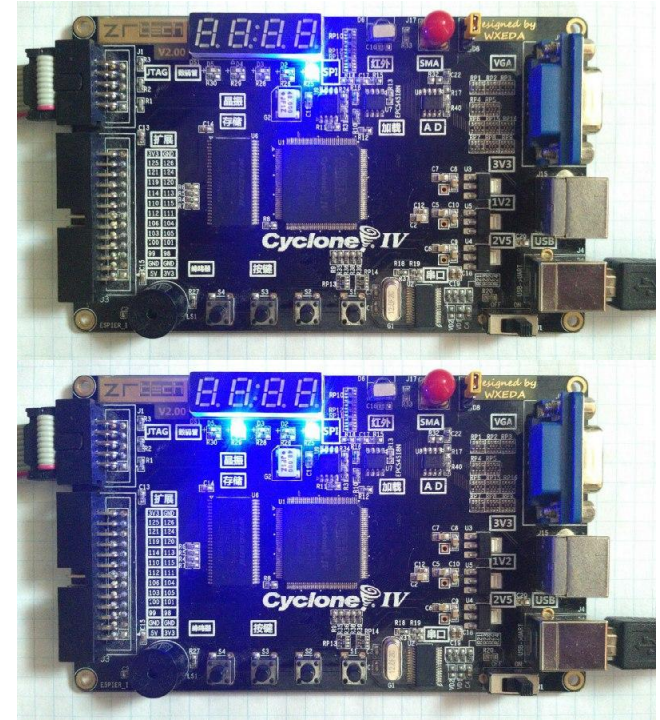
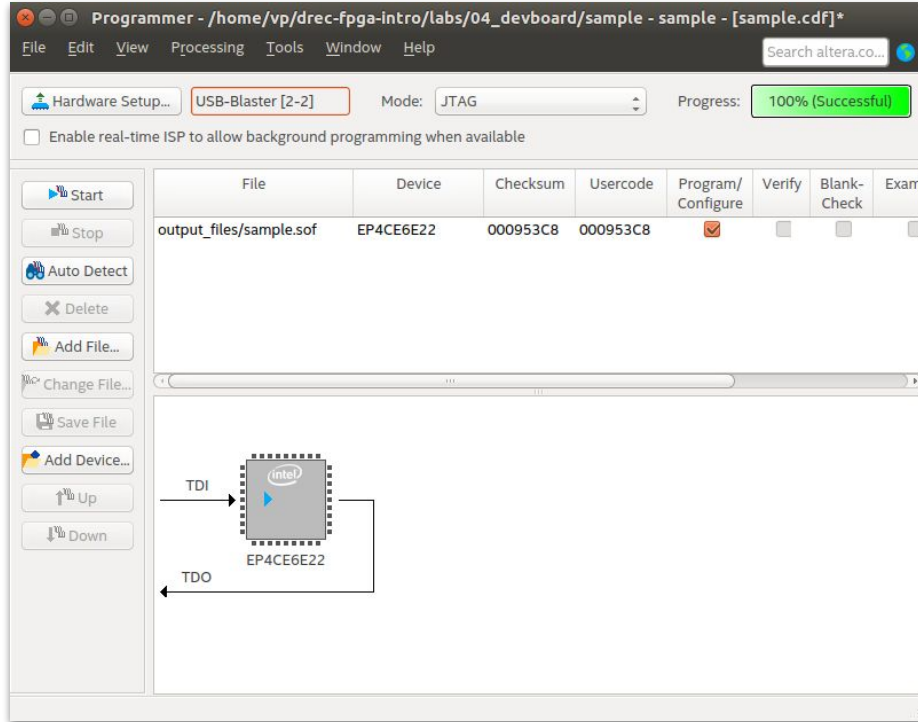
Node Name	Direction	Location	I/O Bank	VREF Group	Iter Locatio	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	trict Preservatio
DS_EN4	Output	PIN_137	8	B8_NO	PIN_137	2.5 V		8mA (default)	2 (default)		
DS_EN2	Output	PIN_136	8	B8_NO	PIN_136	2.5 V		8mA (default)	2 (default)		
DS_EN3	Output	PIN_135	8	B8_NO	PIN_135	2.5 V		8mA (default)	2 (default)		
DS_EN1	Output	PIN_133	8	B8_NO	PIN_133	2.5 V		8mA (default)	2 (default)		
CLK	Input	PIN_24	2	B2_NO	PIN_24	2.5 V		8mA (default)			
DS_C	Output	PIN_1	1	B1_NO	PIN_1	2.5 V		8mA (default)	2 (default)		
ADCLK	Unknown	PIN_127	7	B7_NO		2.5 V (default)		8mA (default)			
ADCSN	Unknown	PIN_129	8	B8_NO		2.5 V (default)		8mA (default)			
ADDAT	Unknown	PIN_128	8	B8_NO		2.5 V (default)		8mA (default)			

Filter: Pins: all

0% 00:00:00

Assignments > Pin Planner

# Programmer



Tools > Programmer

# GitHub

[github.com/viktor-prutyanov/drec-fpga-intro](https://github.com/viktor-prutyanov/drec-fpga-intro)