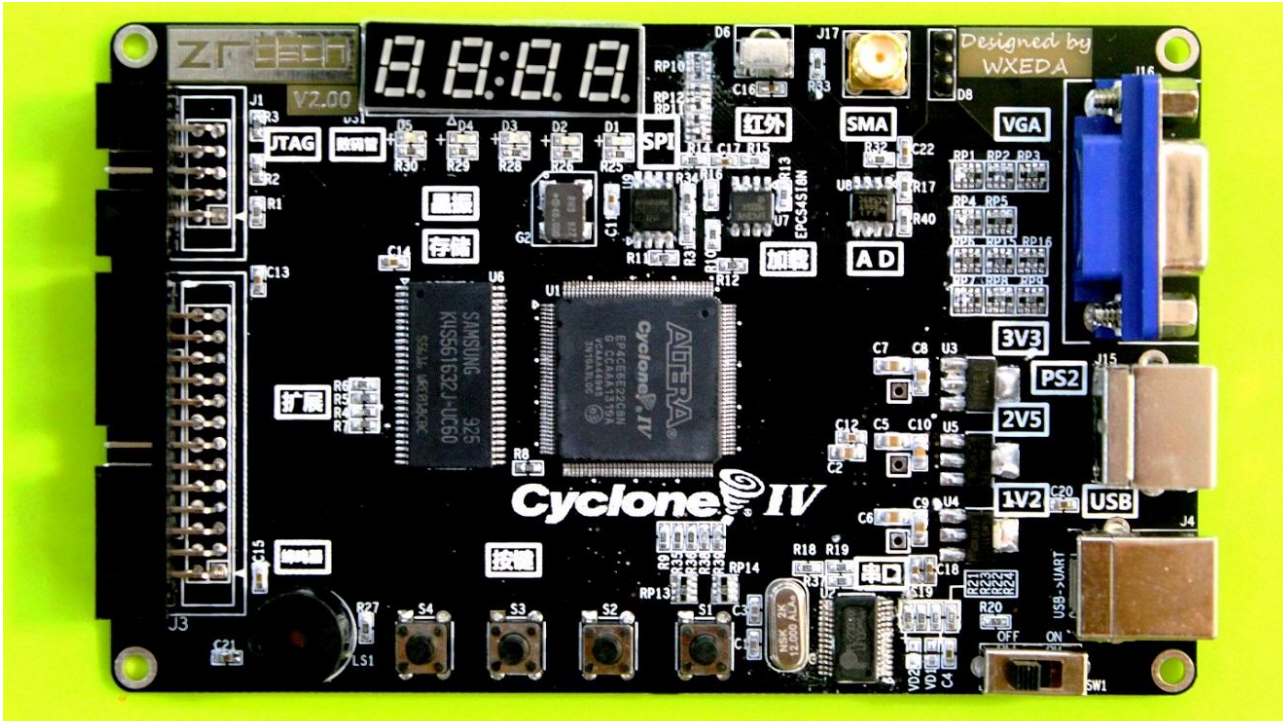
Прошивка FPGA. Altera Quartus

Отладочная плата

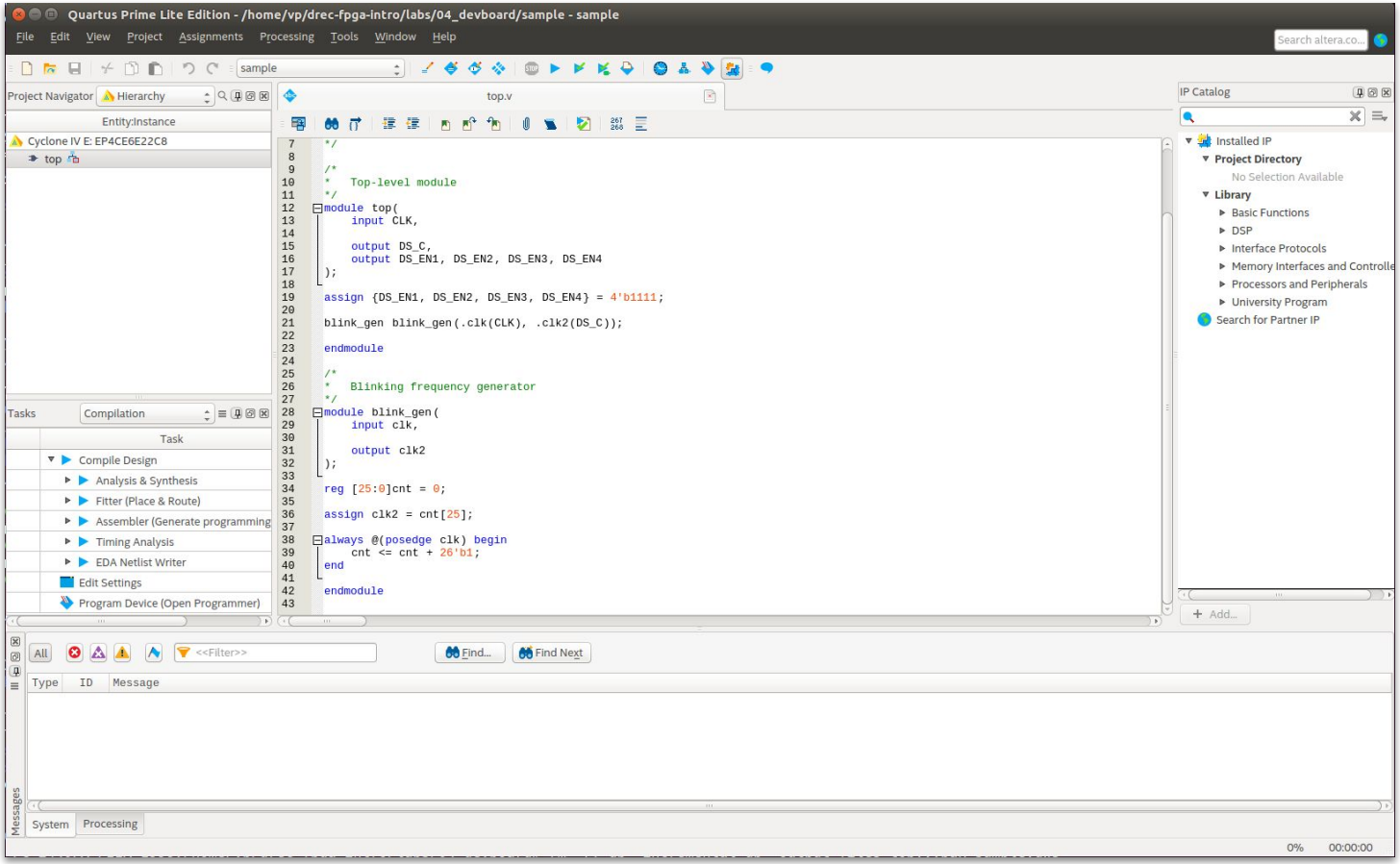
- FPGA Altera Cyclone IV EP4CE6E22C8N
- 7-сегментный индикатор
- 4 светодиода
- Питание подводится через USB
- Прошивка загружается через 10-пиновый JTAG
- 48 МГц кварцевый генератор



Программатор

- USB для соединения с ПК
- 10-пиновый JTAG для соединения с отладочной платой

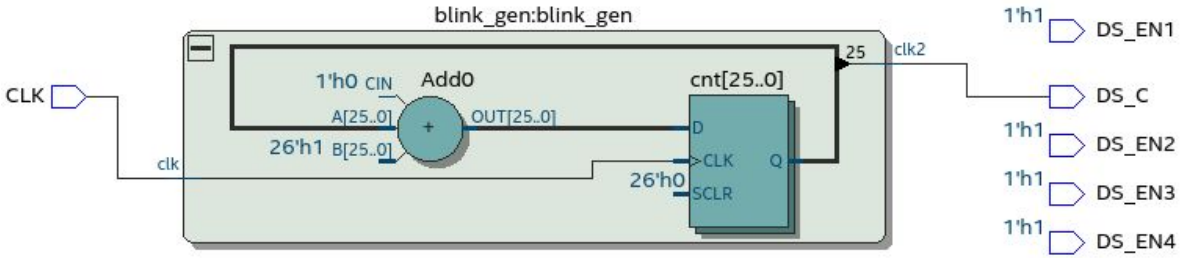
Проект 04_devboard в Quartus Prime Lite 18.1



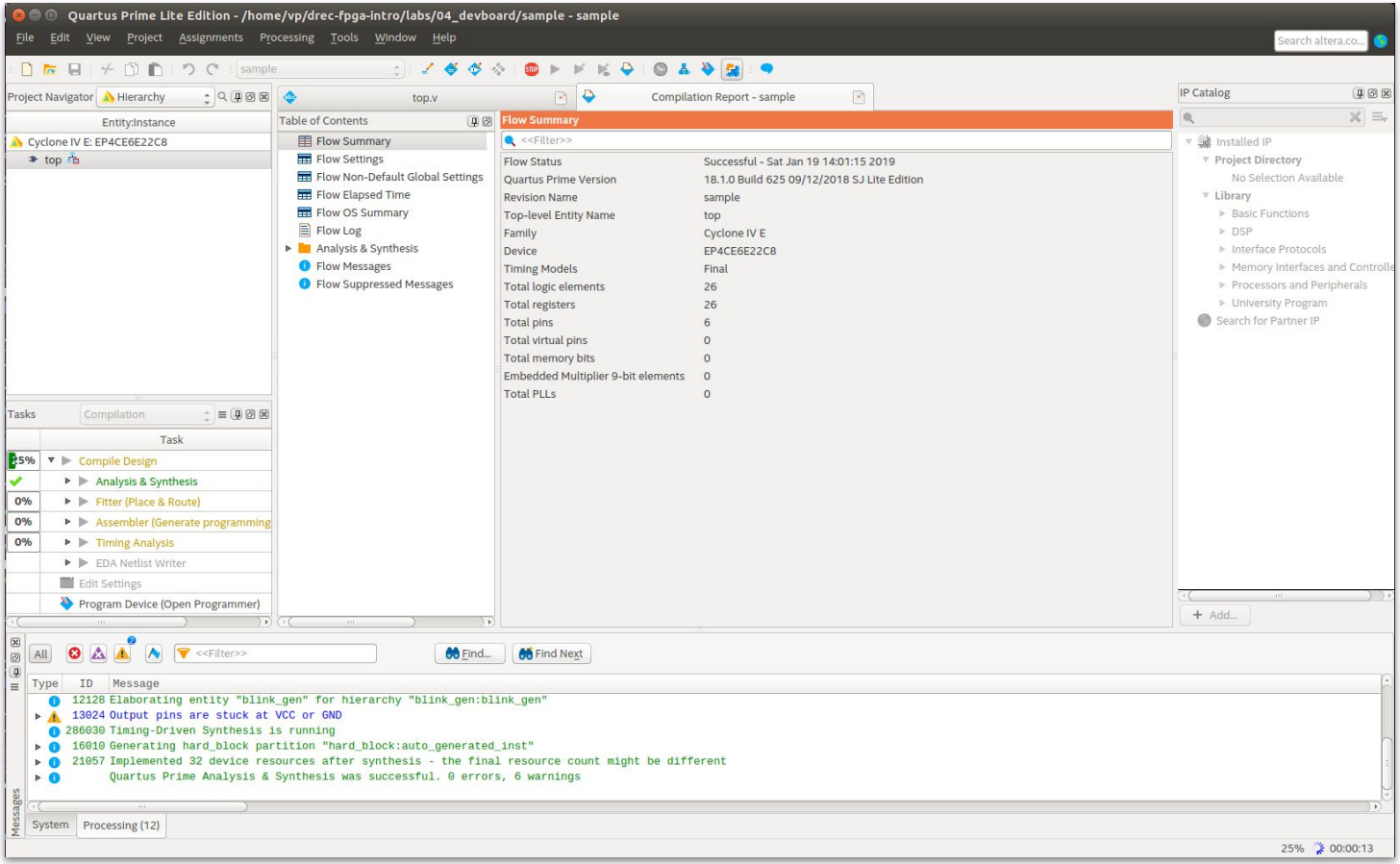
top.v

```
module top(
   input CLK,

   output DS_C,
   output DS_EN1, DS_EN2, DS_EN3, DS_EN4
);

assign {DS_EN1, DS_EN2, DS_EN3, DS_EN4} = 4'b1111;

blink_gen blink_gen(.clk(CLK), .clk2(DS_C));

endmodule
```

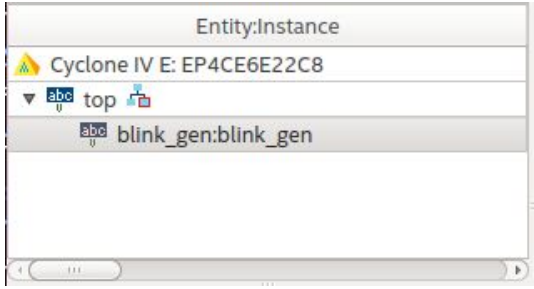
```
module blink_gen(
   input clk,

   output clk2
);

reg [25:0]cnt = 0;

assign clk2 = cnt[25];

always @(posedge clk) begin
   cnt <= cnt + 26'b1;
end

endmodule
```

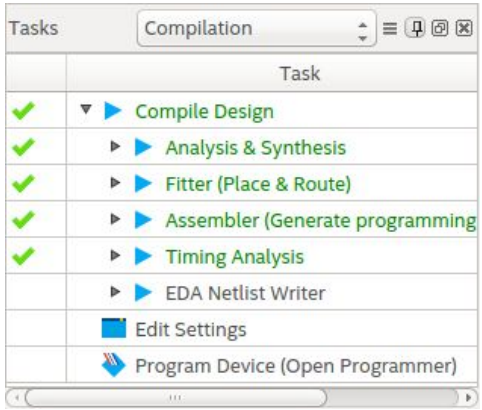


Compile Design



Compilation Report



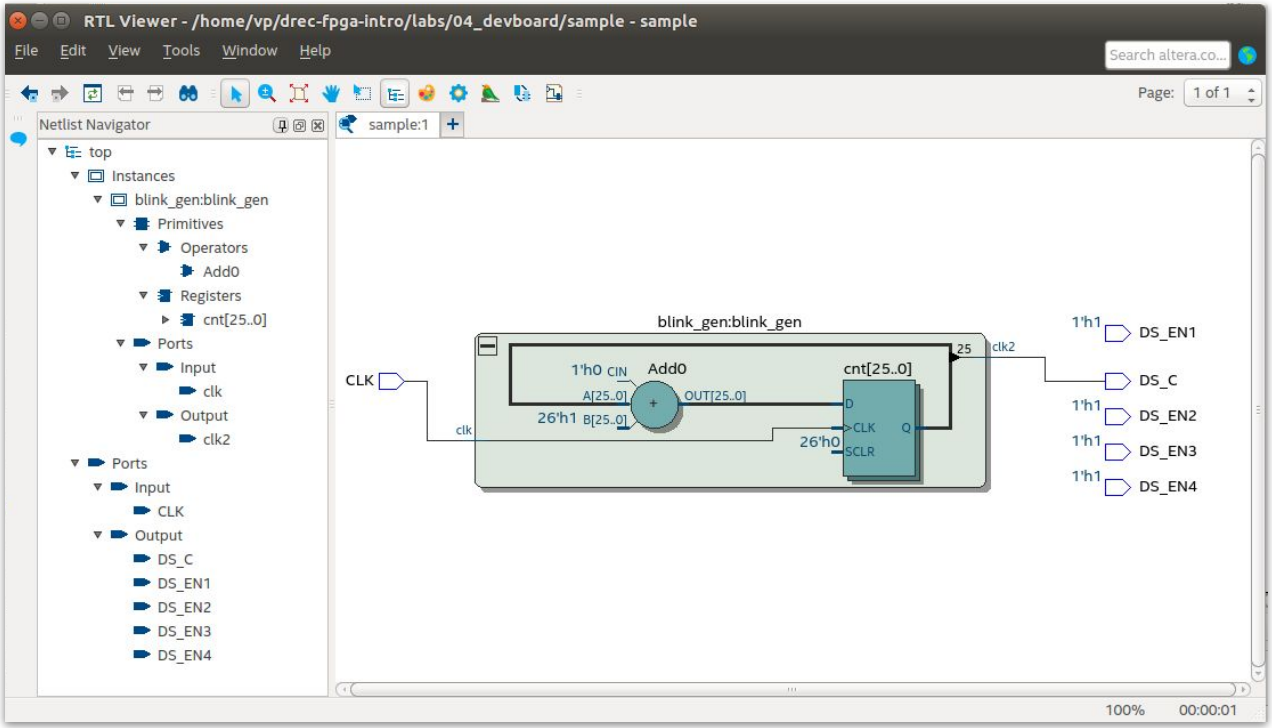


Flow Summary

<<Filter>>

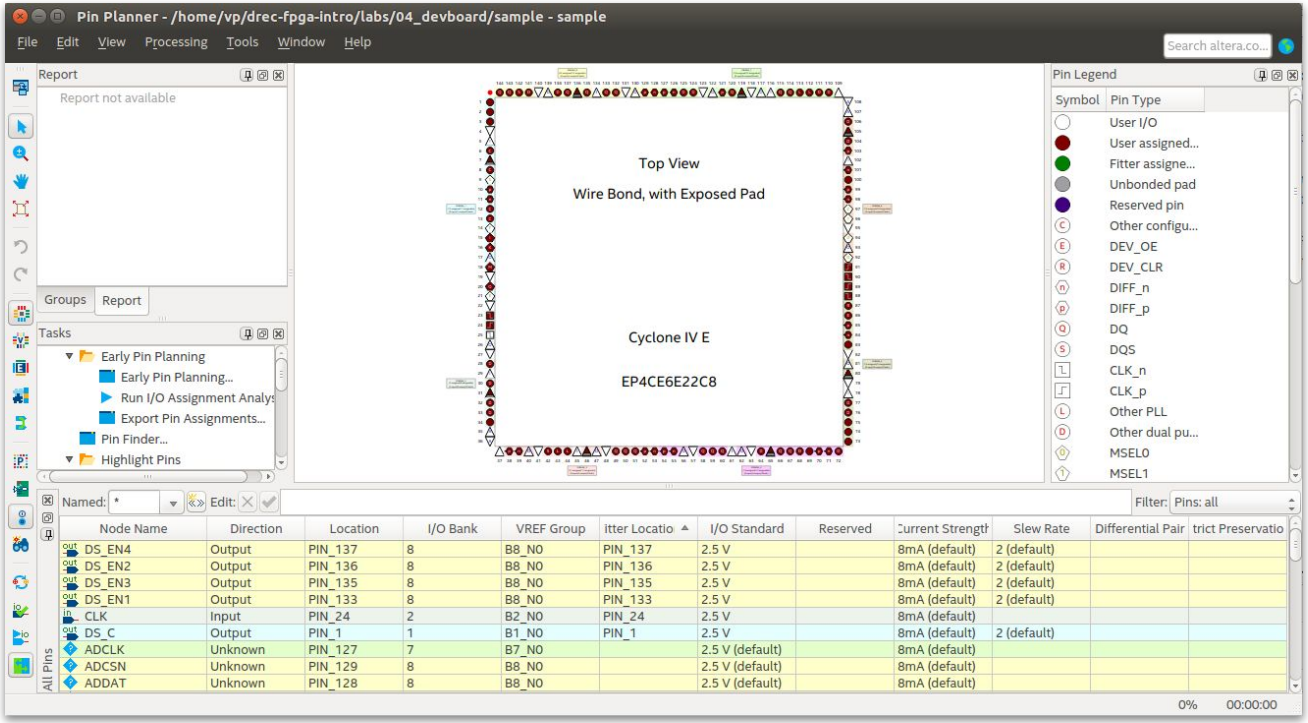
Flow Status	Successful - Sat Jan 19 14:01:23 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	sample
Top-level Entity Name	top
Family	Cyclone IV E
Device	EP4CE6E22C8
Timing Models	Final
Total logic elements	26 / 6,272 (< 1 %)
Total registers	26
Total pins	6 / 92 (7 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)

RTL Design Viewer



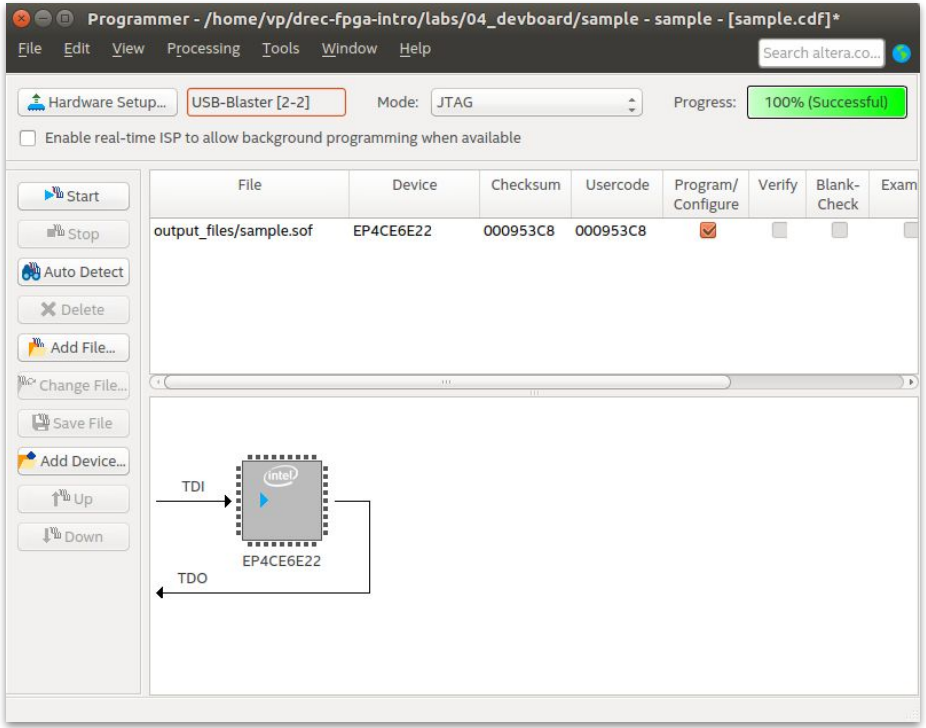
Tools > Netlist Viewers > RTL Viewer

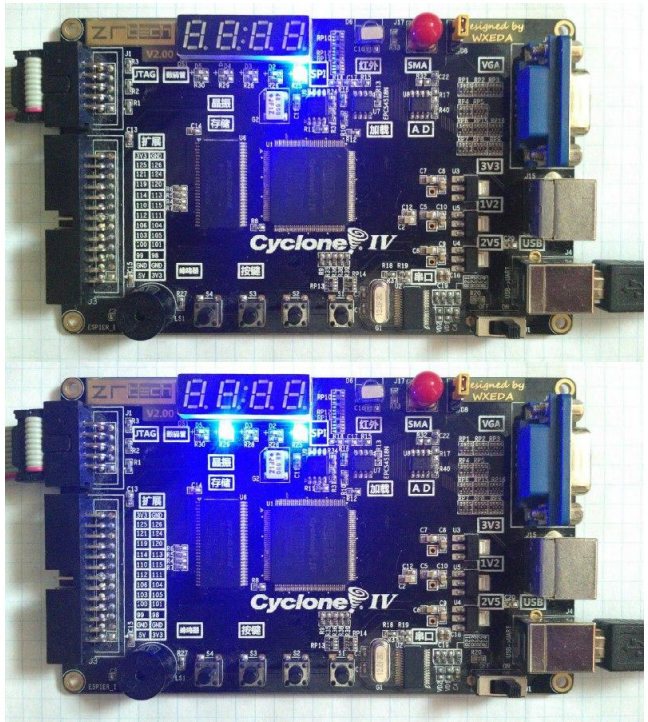
Pin Planner



Assignments > Pin Planner

Programmer





Tools > Programmer

GitHub

github.com/viktor-prutyanov/drec-fpga-intro