VHDL 101

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1 Intoduction

Things this session is intended to wet your appetite to the world of FPGAs, so that if you choose to you can start having a play in your own time. This session is:

1. A brief overview of VHDL

2. A chance to get hands on with some Hardware

3. A chance to make a 'hello world' in Hardware

Things this session is not:

1. An introduction to Digital Design

2. A comprehensive deep dive into VHDL

3. Likely to finish on time

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List of Figures

2   Why Should I Care?

FPGAs enable Low Latency processing [1], so performing a transform on data coming in and getting the result output an be much faster than in a traditional CPU based approach. They also provide far more IO configurability than the traditional approach; the IO logic, and the pin it's connected to are totally configurable in code and contstraints files. Say a rquirement changes from an 8 bit UART bus to a proprietry 11 but UART bus - this would require a whole new microcontroller in a traditional approach however with an FPGA this might only require a change to a `generic` and a recompile.

For the reasons stated above, typical uses include signal processing such as filtering [2], and High Speed IO such as devices produced by SpeedGoat [3].

3   How to use this guide

Coloured boxes for step by step instructions. Not expected to follow it step by step but just reference it to work at own pace.

3.1   Terminology

HDL Entity Module Architecture Dataflow RTL Sythesise

3.2   Toolchain

Vivade vs Quartus. Others - yosys, ghdl etc

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[1]`https://blog.esciencecenter.nl/why-use-an-fpga-instead-of-a-cpu-or-gpu-b234cd4f309c`

[2]`https://digital-library.theiet.org/content/journals/10.1049/iet-cdt.2016.0067`

[3]`https://www.speedgoat.com/products/simulink-programmable-fpgas-fpga-io-modules-io334`

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4   Important things to remember

It's not software it's hardware

5   Finally lets get to doing some VHDL

5.1   Reference Project

This will be an overview of the refernce project

5.2   How to see output from our VHDL

5.2.1   Simulation

How to interpret the waveforms

5.2.2   On the hardware itself

How to load onto the board

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