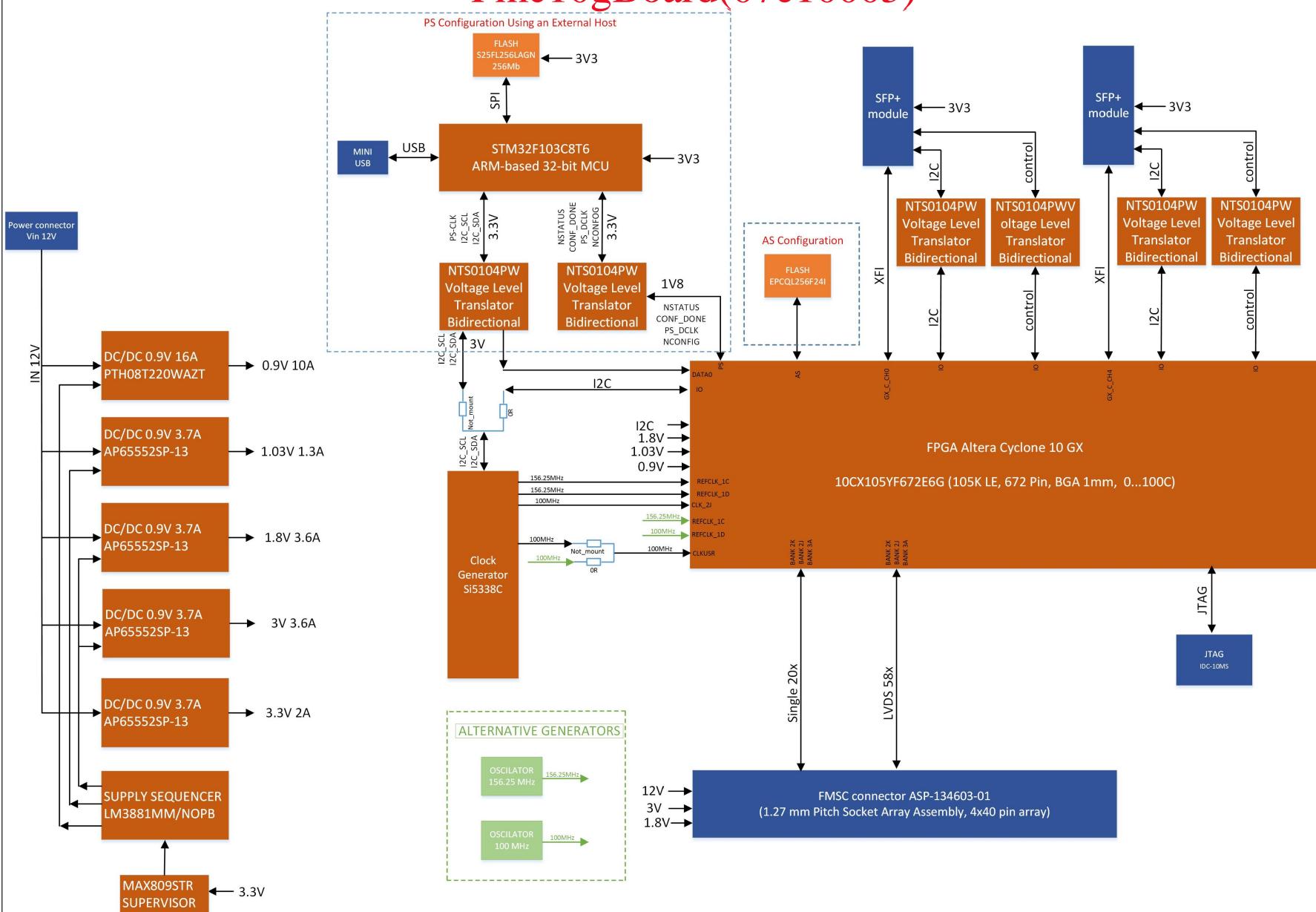
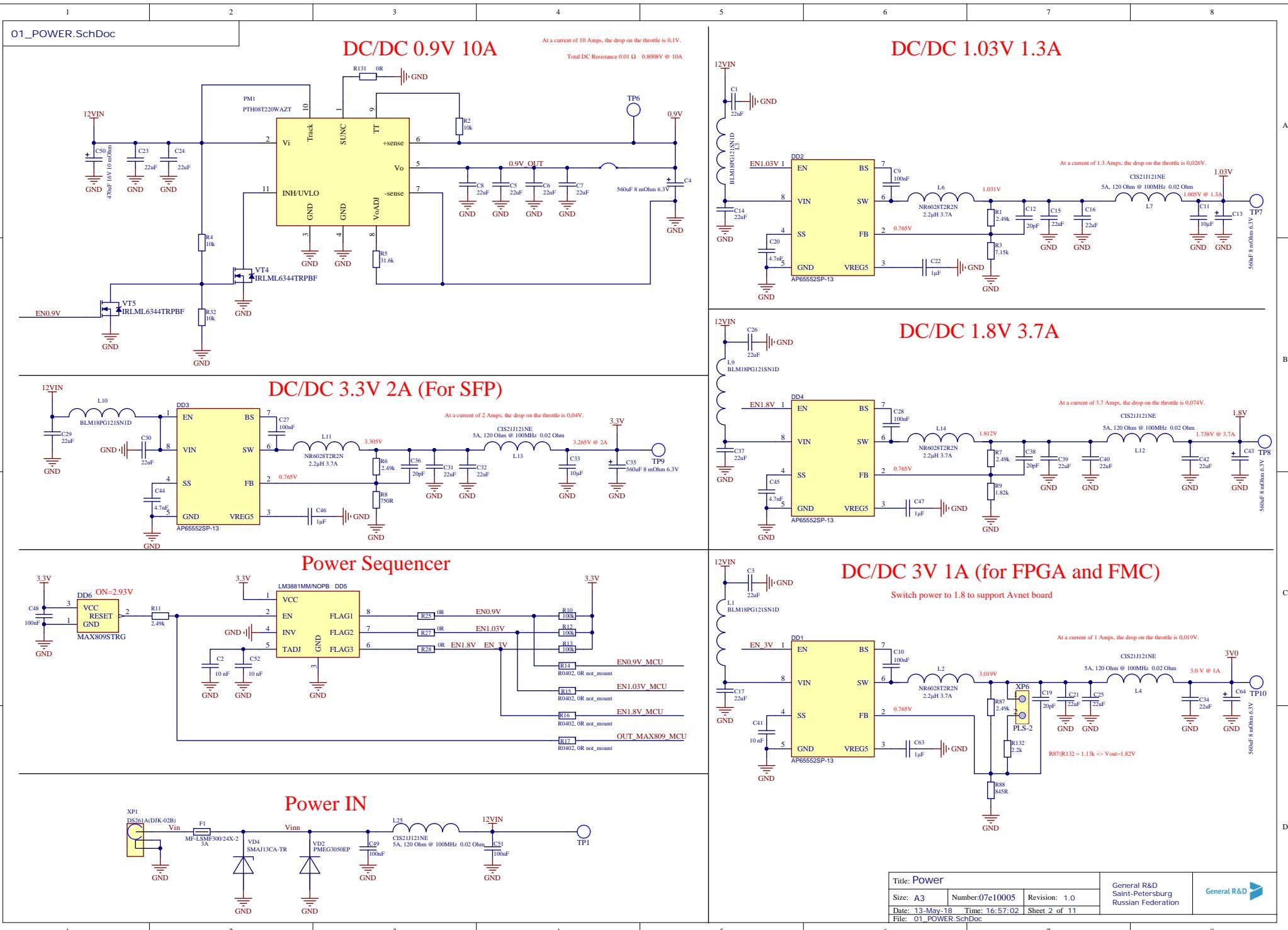
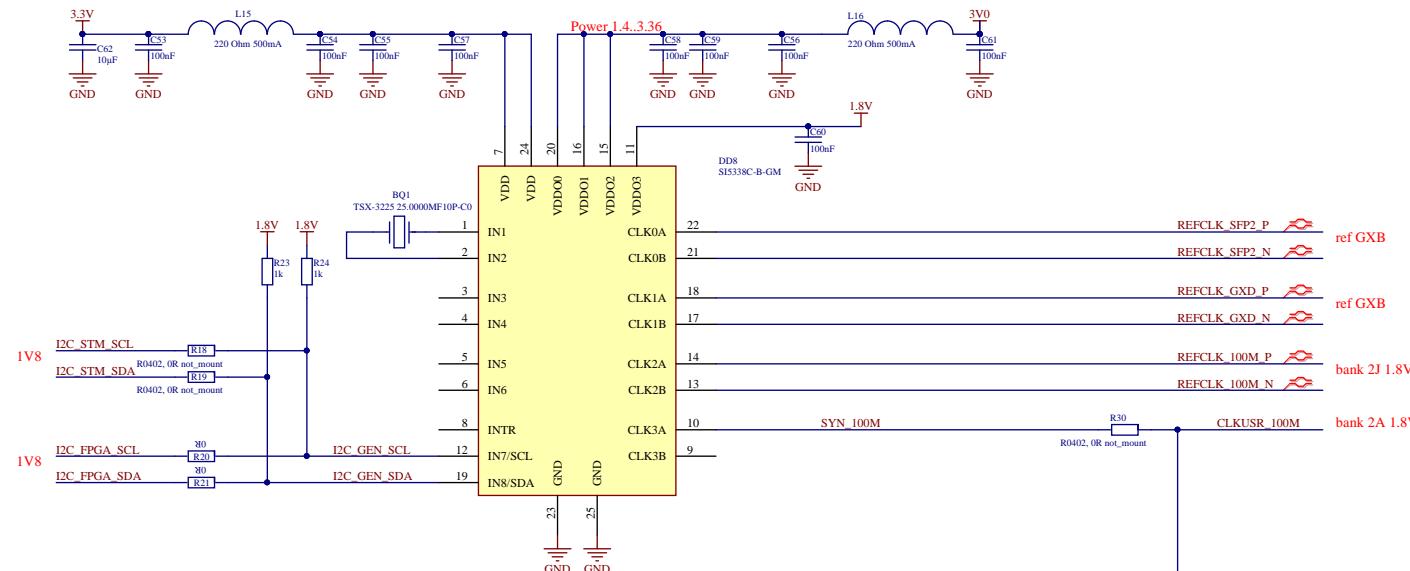


Fmc10gBoard(07e10005)

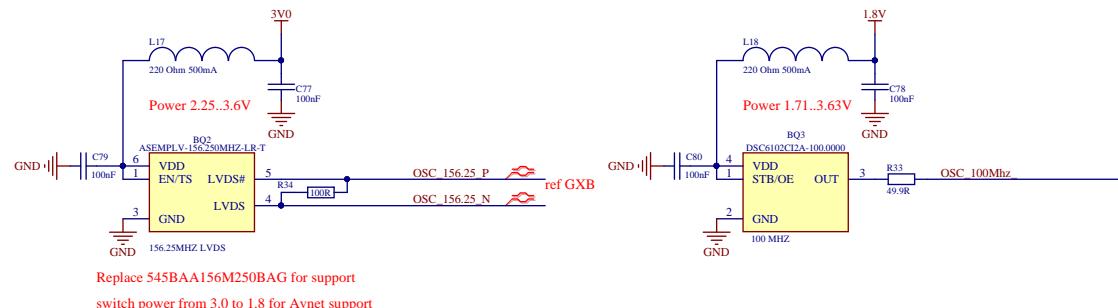




CLOCK GENERATOR AND BUFFERS



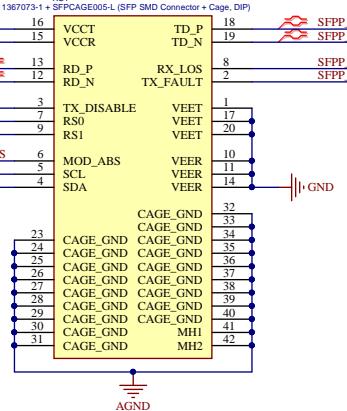
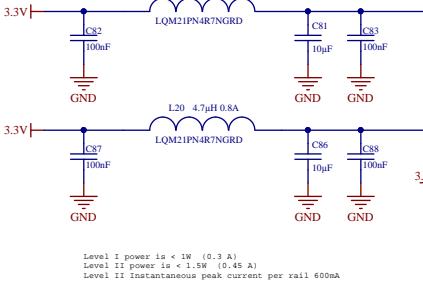
alternative generators (replacement of synthesizer SI5338)



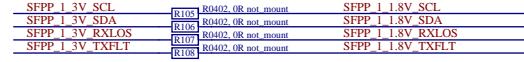
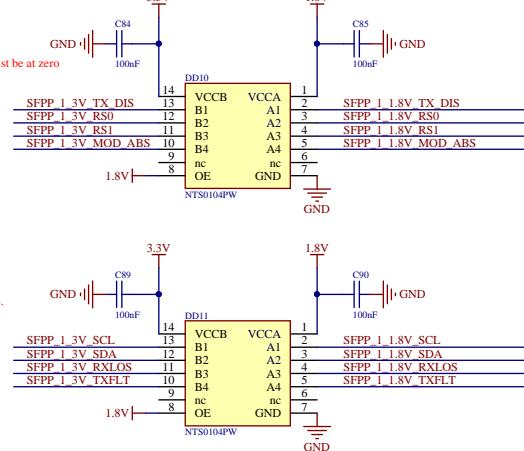
SFP+ PORTS

03_SFP+.SchDoc

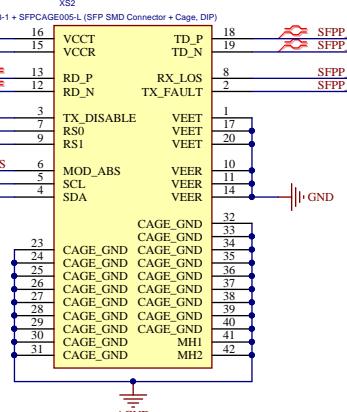
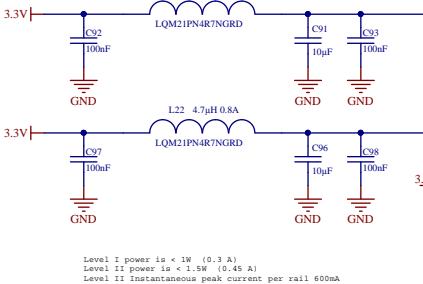
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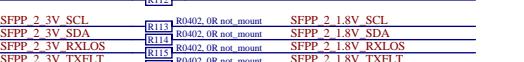
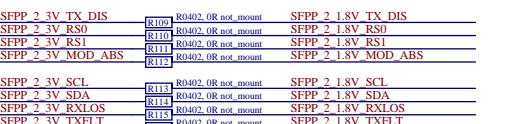
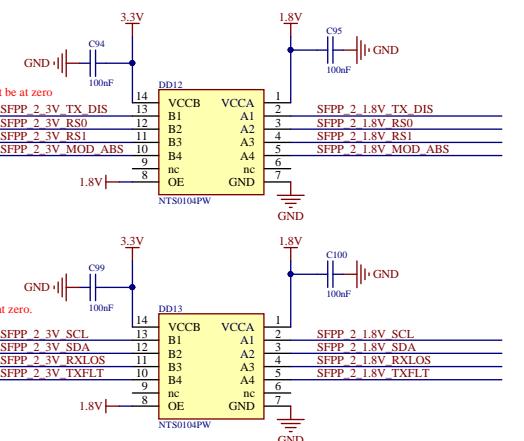
To turn on the optical transmitter, the TX_DIS signal must be at zero



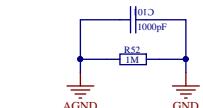
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To turn on the optical transmitter, the TX_DIS signal must be at zero



C

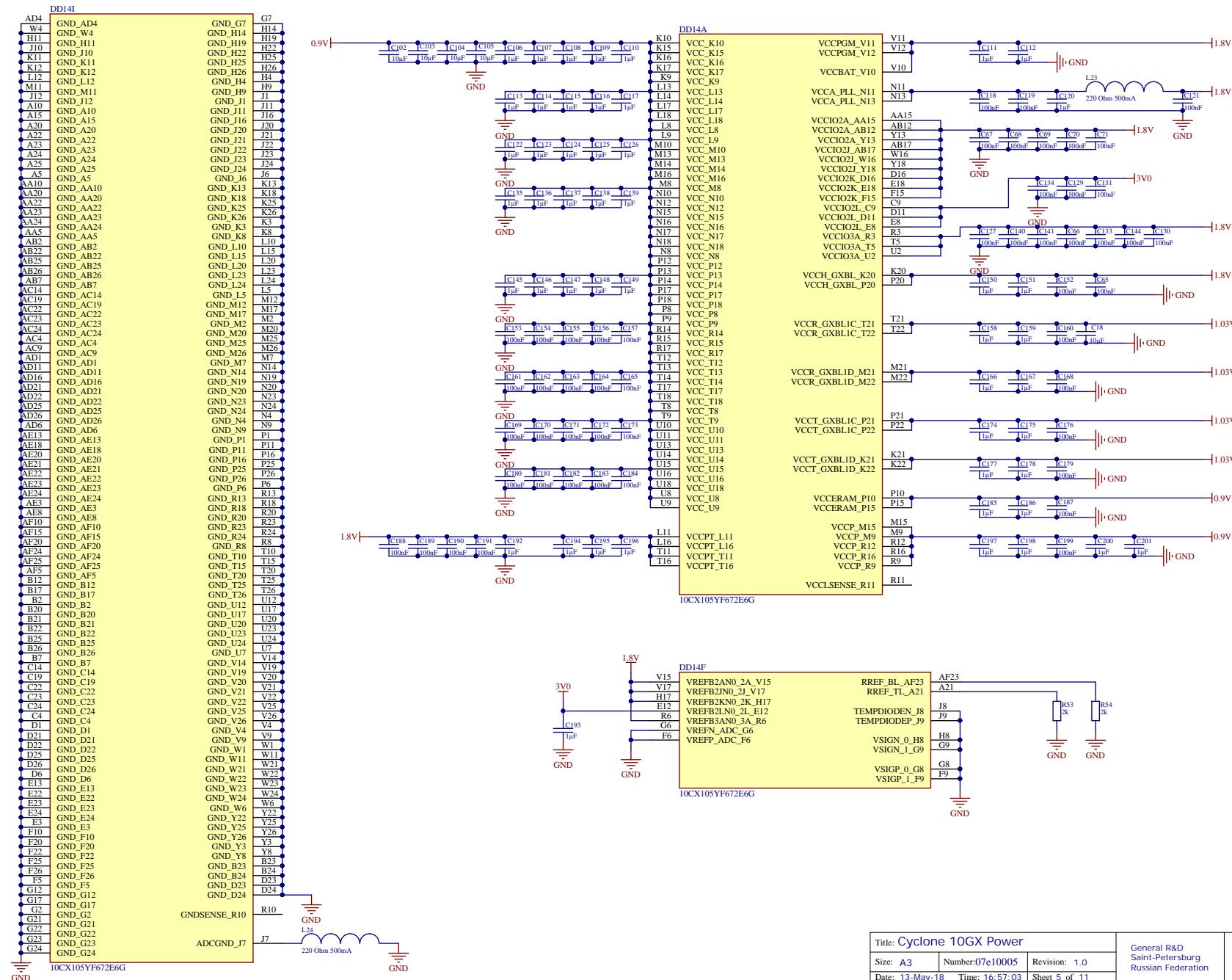


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Size: A3	Number: 07e10005	Revision: 1.0		
Date: 13-May-18	Time: 16:57:02	Sheet 4 of 11		
File: 03_SFP+.SchDoc				

D

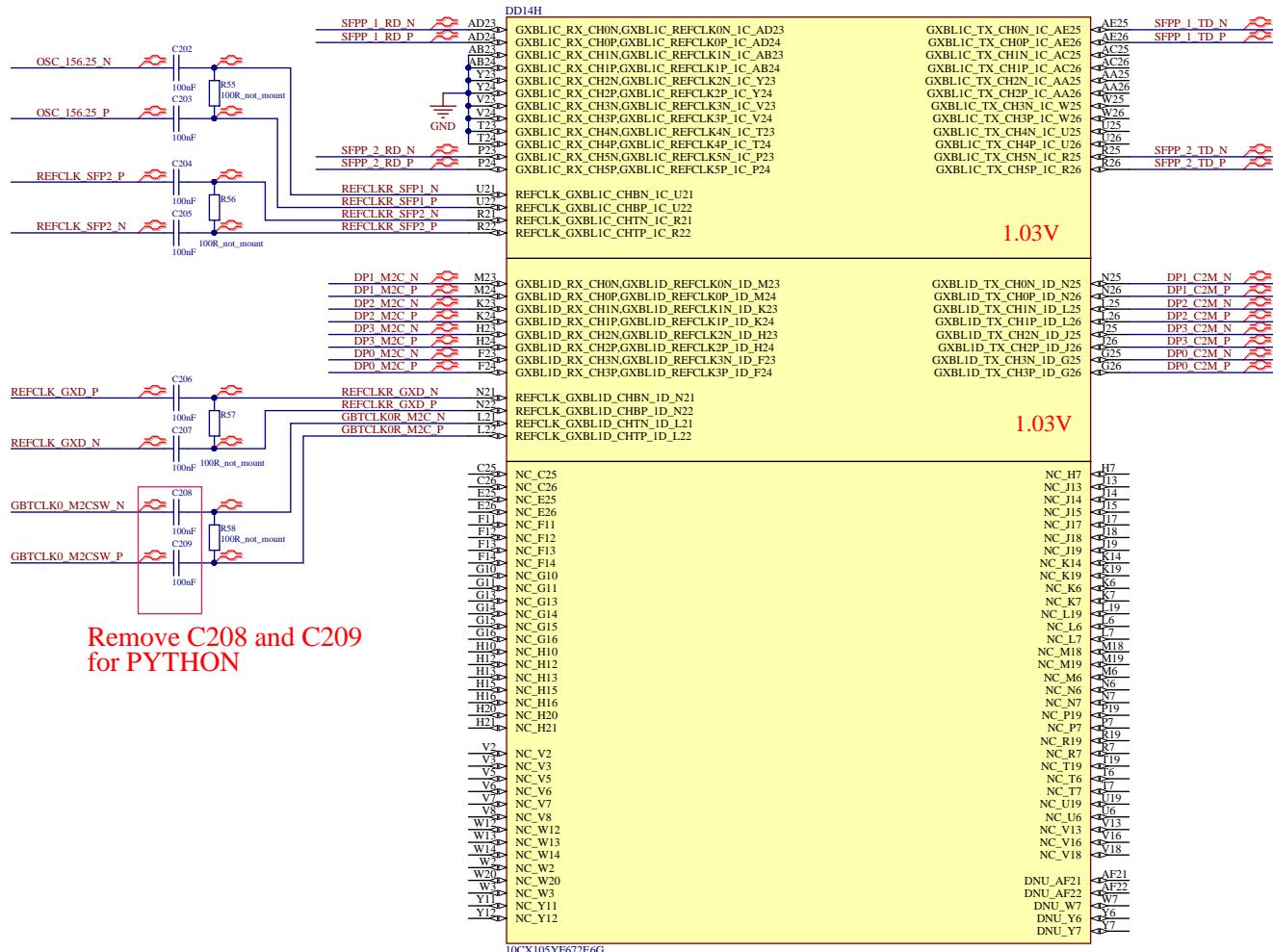
04_Cyclone 10 GX Power.SchDoc

POWER CYCLONE 10 GX



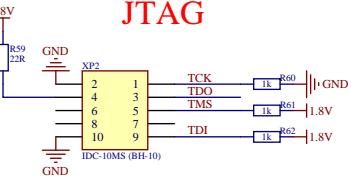
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Size: A3	Number: 07e10005	Revision: 1.0		
Date: 13-May-18	Time: 16:57:03	Sheet 5 of 11		
File: 04_Cyclone 10 GX Power.SchDoc				

Cyclone 10 GX Transceivers

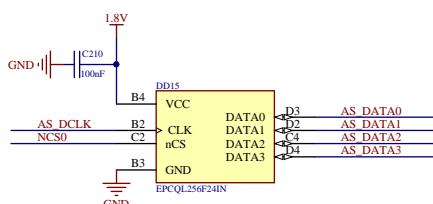


Cyclone 10 GX JTAG, MSEL, AS, PS

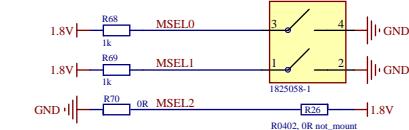
JTAG



AS Configuration with EPCQ-L Devices

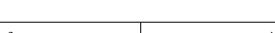
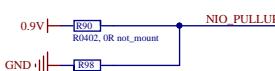
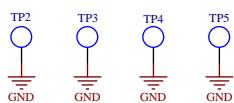
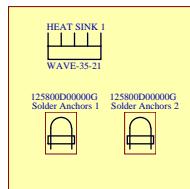


MSEL Pin Settings



MSEL [2..0]
010 - Fast AS (x1 or x4)
011 - Standart AS(x1 or x4)
000 - Fast PS
001 - Standart PS

Table 69. MSEL Pin for Configuration Scheme of Cyclone 10 GX Devices



1V8 DATA0		DD14G		1V2/1V5/1V8	
A1E	IO 2A_47, A1E5	DATA0	LVD52A_1N/DQ24		
A1F	IO 2A_46, A1E4	DATA1	LVD52A_1P/DQ24		
A1G	IO 2A_45, A1D9	DATA2	LVD52A_2N/DQ24		
A1H	IO 2A_44, A1E9	DATA3	LVD52A_2P/DQ24		
A1I	IO 2A_43, A1D7	DATA4	LVD52A_3N/DQ24		
A1J	IO 2A_42, A1E7	DATA5	LVD52A_3P/DQ24		
A1K	IO 2A_41, A1F4	DATA6	LVD52A_4N/DQ25		
A1L	IO 2A_40, A1F3	DATA7	LVD52A_4P/DQ25		
A1M	IO 2A_39, A1E6	DATA8	LVD52A_5N/DQ25		
A1N	IO 2A_38, A1F6	DATA9	LVD52A_5P/DQ25		
A1O	IO 2A_37, A1F8	DATA10	LVD52A_6N/DQ25		
A1P	IO 2A_36, A1F7	DATA11	LVD52A_6P/DQ25		
A1Q	IO 2A_35, A1C8	DATA12	LVD52A_7N/DQ26		
A1R	IO 2A_34, A1C9	DATA13	LVD52A_7P/DQ26		
A1S	IO 2A_33, A1C10	DATA14	LVD52A_8N/DQ26		
A1T	IO 2A_32, A1D10	DATA15	LVD52A_8P/DQ26		
A1U	IO 2A_31, A1B6	DATA16	LVD52A_9N/DQ26		
A1V	IO 2A_30, A1B5	DATA17	LVD52A_9P/DQ26		
A1W	IO 2A_29, A1C7	PLL	2A_CLKOUT1/PDATA18/LVD52A_10N/DQ27		
A1X	IO 2A_28, A1C6	PLL	2A_CLKOUT1/P.PLL	2A_CLKOUT1.PLL	_2A_FBI/PDATA19/LVD52A_10P/DQ27
A1Y	IO 2A_25, A1C5	PLL	2A_IN	2A_CLK2/LVD52A_12N/DQ27	
A1Z	IO 2A_24, A1D5	PLL	2A_IP	2A_CLK2/LVD52A_12P/DQ27	
A1AA	IO 2A_23, Y14 CLK	2A_0P	DATA23/LVD52A_13N/DQ28		
A1AB	IO 2A_22, AA14/CLE	2A_0P	DATA23/LVD52A_13P/DQ28		
A1AC	IO 2A_21, AD13/DATA24/LVD52A_14N/DQ28				
W1	IO 2A_19, W15 PLL	2A_CLKOUT0/N	PDATA26/LVD52A_15N/DQ28		
Y1	IO 2A_18, Y15 PLL	2A_CLKOUT0/P	PLL	2A_CLKOUT0_P	PLL
AB1	IO 2A_17, AB14	PDATA28/LVD52A_16N/DQ29			
AB2	IO 2A_16, AB15	PDATA29/LVD52A_16P/DQ29			
AB3	IO 2A_15, AB11	PDATA29/LVD52A_17N/DQ29			
AB4	IO 2A_14, AC11/DATA31/LVD52A_17P/DQ29				
AB5	IO 2A_11, AA9/LVD52A_19N/DQ30				
W2	IO 2A_9, W9/LVD52A_20N/DQ30				
W3	IO 2A_8, W8/LVD52A_20P/DQ30				
AA1	IO 2A_7, AA13/LVD52A_21N/DQ30				
AA2	IO 2A_6, AA12/LVD52A_21P/DQ30				
AA3	IO 2A_5, AA4/CV	CONF_DONE	E/LVD52A_22N/DQ31		
W4	IO 2A_4, AA7/LVD52A_22P/DQ31				
AA4	IO 2A_3, W10/INT	CONF_DONE	E/LVD52A_23N/DQ31		
AA5	IO 2A_1, AA11/CRC_ERROR	E/LVD52A_24N/DQ31			
AA6	IO 2A_0, Y10/DEV	E/LVD52A_24P/DQ31			
IV8 CLKUSR_100M					
AC13	IO 2A_13, AC13/CLKUSR	LVD52A_18N/DQ29			
AC12	IO 2A_12, AC12/LVD52A_18P/DQ29				
AB10	IO 2A_27, AB10/NCEO	LVD52A_11N/DQ27			
AB9	IO 2A_26, AB9/RZQ	2A/LVD52A_11P/DQ27			



10CX105YF672E6G

Title: Cyclone 10GX JTAG
Size: A3 Number: 07e10005 Revision: 1.0
Date: 13-May-18 Time: 16:57:03 Sheet 7 of 11
File: 06_Cyclone 10 GX JTAG.SchDoc

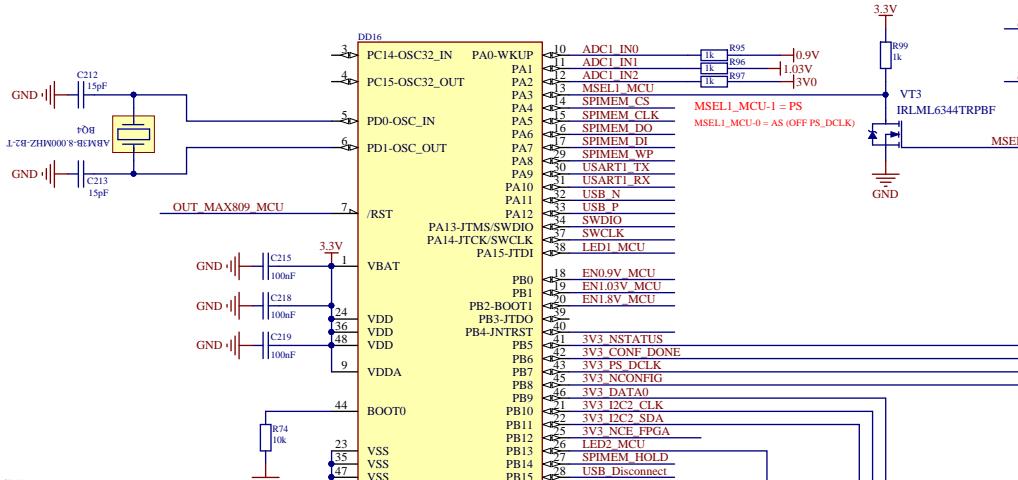
General R&D
Saint-Petersburg
Russian Federation



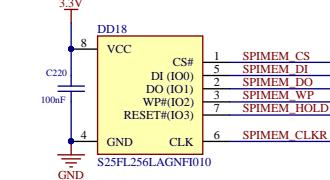
PS Configuration Using an External Host

07_PS_STM32.SchDoc

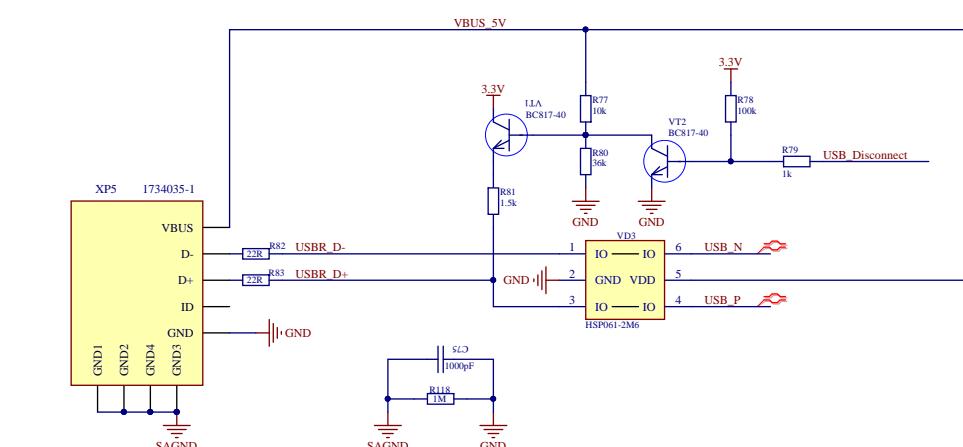
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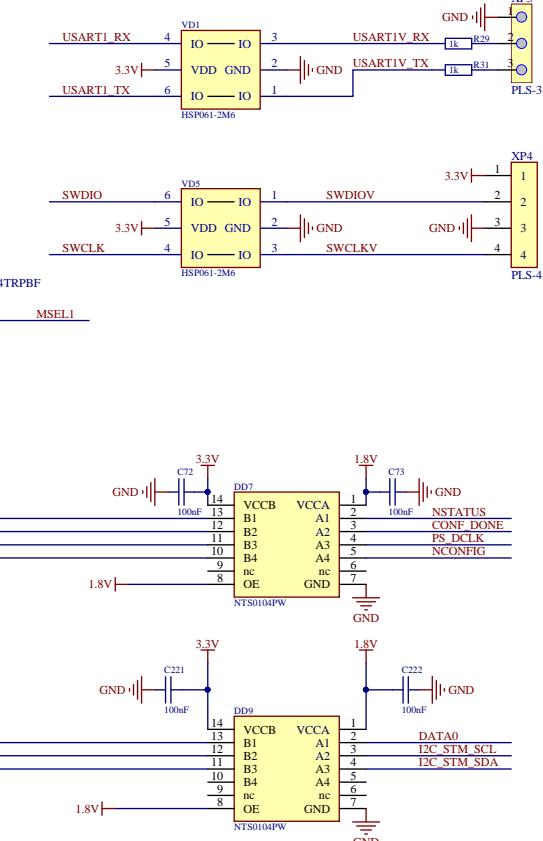
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C



D



Title: STM32

Size: A3 Number: 07e10005 Revision: 1.0

General R&D Saint-Petersburg Russian Federation

General R&D

Date: 13-May-18 Time: 16:57:03 Sheet 8 of 11

File: 07_PS_STM32.SchDoc

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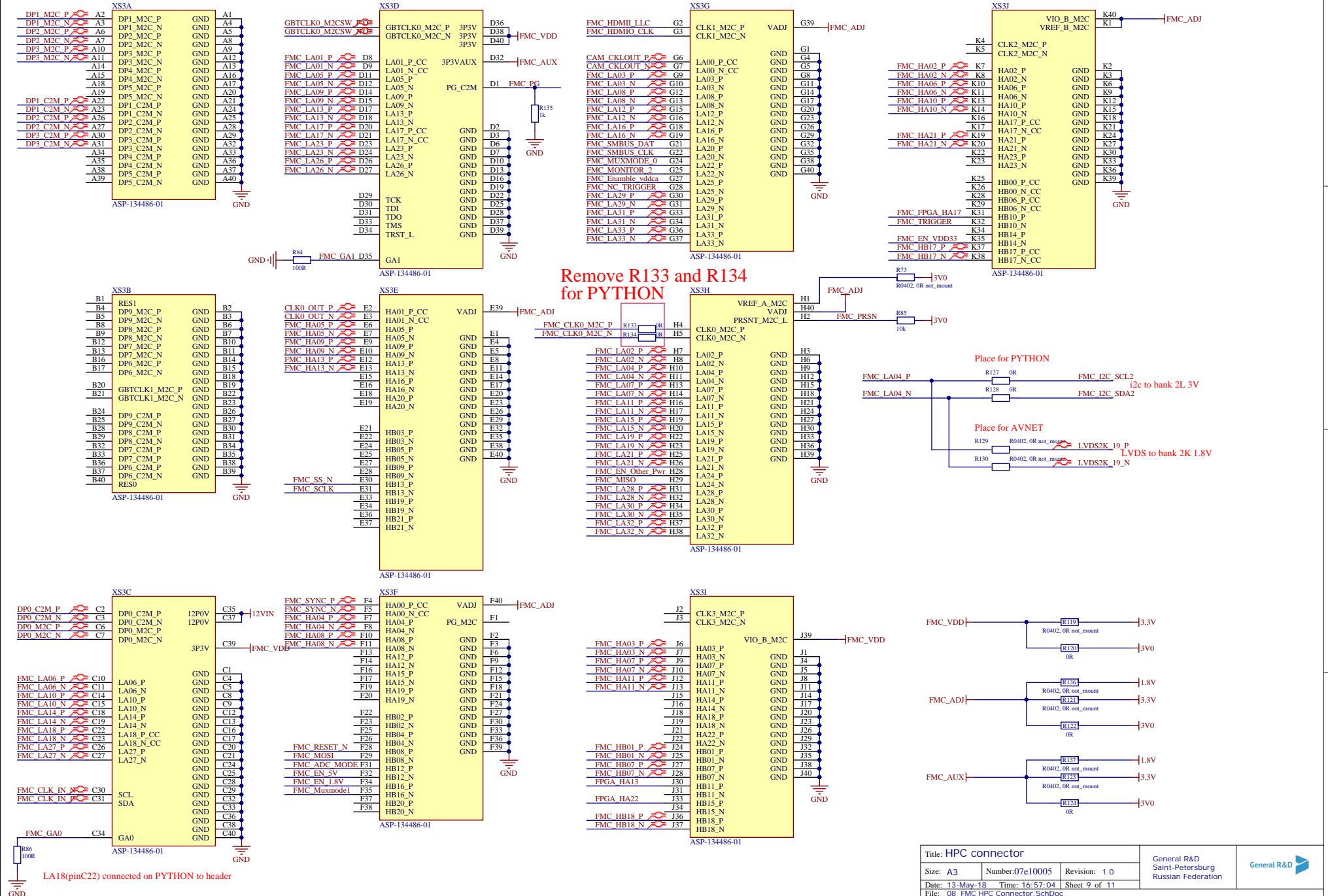
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8

FMC HPC Connector

08_FMC HPC Connector.SchDoc



FMC HPC to Cyclone 10 GX

DD14D

W18	IO_2J_47_W18_LVDS2J_1N/DQ16
Y2J	IO_2J_46_Y19_LVDS2J_1P/DQ16
I2C FPGA SDA	IO_2J_45_Y21_LVDS2J_2N/DQSN16
I2C FPGA SCL	IO_2J_43_Y21_LVDS2J_2P/DQSN16
Y19J	IO_2J_43_Y19_LVDS2J_3N/DQ16
Y20J	IO_2J_42_Y20_LVDS2J_3P/DQ16
W17J	IO_2J_41_W17_LVDS2J_4N/DQSN17
Y17J	IO_2J_40_Y17_LVDS2J_4P/DQSN17
FMC LA31_N	IO_2J_39_AA17_LVDS2J_5N/DQ17
FMC LA31_P	IO_2J_38_AB16_LVDS2J_5P/DQ17
FMC HB17_N	IO_2J_37_Y16_LVDS2J_6N/DQ17
FMC HB17_P	IO_2J_36_AA16_LVDS2J_6P/DQ17
FMC LA32_N	IO_2J_35_AB20_LVDS2J_7N/DQ18
FMC LA32_P	IO_2J_34_AB21_LVDS2J_7P/DQ18
AC20J	IO_2J_33_AC20_LVDS2J_8N/DQSN18
AC20P	IO_2J_32_AC21_LVDS2J_8P/DQSN18
AA18J	IO_2J_31_AA18_LVDS2J_9N/DQ18
AB18J	IO_2J_30_AB19_LVDS2J_9P/DQ18
AD19J	IO_2J_29_AD19_LVDS2J_11N/DQ19
AD20J	IO_2J_26_AD20_RZ0_2J_LVDS2J_11P/DQ19
FMC LA28_N	IO_2J_21_AB14_LVDS2J_14N/DQSN20
FMC LA28_P	IO_2J_20_AC15_LVDS2J_14P/DQSN20
AD17J	IO_2J_17_AD17_LVDS2J_16N/DQSN21
AE17J	IO_2J_16_AA17_LVDS2J_16P/DQSN21
FMC HB18_N	IO_2J_15_AC16_LVDS2J_17N/DQ21
FMC HB18_P	IO_2J_14_AC17_LVDS2J_17P/DQ21
FMC LA33_N	IO_2J_13_AA16_LVDS2J_18N/DQ21
FMC LA33_P	IO_2J_12_AF16_LVDS2J_18P/DQ21
AE16J	IO_2J_11_AA10_LVDS2J_19N/DQ22
FMC LA26_N	IO_2J_10_AF9_LVDS2J_19P/DQ22
FMC LA26_P	IO_2J_9_AF12_LVDS2J_20N/DQSN22
EMC LA30_N	IO_2J_8_AF11_LVDS2J_20P/DQSN22
EMC LA30_P	IO_2J_7_AA15_LVDS2J_21N/DQ22
EMC LA29_N	IO_2J_6_AA14_LVDS2J_21P/DQ22
EMC LA29_P	IO_2J_5_AD15_LVDS2J_22N/DQSN23
FMC HB07_N	IO_2J_4_AA14_LVDS2J_22P/DQSN23
FMC HB07_P	IO_2J_3_AA12_LVDS2J_23N/DQ23
AF13J	IO_2J_2_AA11_LVDS2J_23P/DQ23
AF14J	IO_2J_1_AF13_LVDS2J_24N/DQ23
AF14P	IO_2J_0_AF14_LVDS2J_24P/DQ23

1V2/1V5/1V8

DD14C

FMC HA13_N	H18	IO_2K_47_H18_LVDS2K_1N/DQ8
FMC HA13_P	G18	IO_2K_46_G18_LVDS2K_1P/DQ8
FMC LA07_N	F18	IO_2K_45_F18_LVDS2K_2N/DQSN8
FMC LA07_P	E18	IO_2K_44_E18_LVDS2K_2P/DQSN8
FMC LA01_N	F1J	IO_2K_42_F17_LVDS2K_3P/DQ8
FMC LA01_P	E1J	IO_2K_41_G19_LVDS2K_4N/DQSN9
FMC HA02_N	G20	IO_2K_40_G20_LVDS2K_4P/DQSN9
FMC HA02_P	D19	IO_2K_39_F18_LVDS2K_5N/DQ9
FMC HA09_N	F19	IO_2K_38_F19_LVDS2K_5P/DQ9
FMC HA09_P	E1A	IO_2K_37_E14_LVDS2K_6N/DQ9
FMC HA11_N	F20	IO_2K_36_E15_LVDS2K_6P/DQ9
FMC HA11_P	C20	IO_2K_35_C20_LVDS2K_7N/DQ10
FMC HA05_N	C21	IO_2K_34_C21_LVDS2K_7P/DQ10
FMC HA05_P	D21	IO_2K_33_E19_LVDS2K_8N/DQSN10
FMC LA02_N	E1B	IO_2K_32_D19_LVDS2K_8P/DQSN10
FMC LA02_P	D1B	IO_2K_31_D17_LVDS2K_9N/DQ10
FMC HA04_N	C1B	IO_2K_30_B19_LVDS2K_9P/DQ10
FMC HA04_P	B1B	IO_2K_29_A19_LVDS2K_10N/DQ11
FMC HA03_N	F2J	IO_2K_28_E2J_LVDS2K_11N/DQ11
FMC HA03_P	E2J	IO_2K_26_E2J_RZ0_2K_LVDS2K_11P/DQ11
LVDS2K_19_N	D14	IO_2K_21_D14_LVDS2K_14N/DQSN12
LVDS2K_19_P	D15	IO_2K_20_D15_LVDS2K_14P/DQSN12
FMC HA07_N	A17	IO_2K_17_A17_LVDS2K_16N/DQSN13
FMC HA07_P	A18	IO_2K_16_A18_LVDS2K_16P/DQSN13
FMC HA08_N	C15	IO_2K_15_C15_LVDS2K_17N/DQ13
FMC HA08_P	B15	IO_2K_14_B15_LVDS2K_17P/DQ13
LVDS2K_19_N	A19	IO_2K_13_B19_LVDS2K_18N/DQ13
LVDS2K_19_P	D16	IO_2K_12_A19_LVDS2K_18P/DQ13
CLK0_OUT_N	C18	IO_2K_10_D12_LVDS2K_19P/DQ14
CLK0_OUT_P	B18	IO_2K_9_C13_LVDS2K_20N/DQSN14
CAM_CLKOUT_N	C19	IO_2K_8_B13_LVDS2K_20P/DQSN14
CAM_CLKOUT_P	B19	IO_2K_7_B14_LVDS2K_21N/DQ14
FMC HA06_N	A13	IO_2K_6_A13_LVDS2K_22N/DQSN15
FMC HA06_P	A14	IO_2K_5_A13_LVDS2K_22P/DQSN15
FMC LA06_N	C13	IO_2K_3_C12_LVDS2K_23N/DQ15
FMC LA06_P	C14	IO_2K_2_C11_LVDS2K_23P/DQ15
FMC LA03_N	B11	IO_2K_1_B11_LVDS2K_24N/DQ15
FMC LA03_P	A11	IO_2K_0_A11_LVDS2K_24P/DQ15

1V2/1V5/1V8

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DD14E

FMC LA12_N	K4	IO_3A_47_K4_LVDS3A_1N/DQ56
FMC LA12_P	J4	IO_3A_46_J4_LVDS3A_1P/DQ56
FMC LA09_N	H6	IO_3A_45_H6_LVDS3A_2N/DQSN56
FMC LA09_P	H5	IO_3A_44_H5_LVDS3A_2P/DQSN56
FMC LA11_N	K7	IO_3A_43_K5_LVDS3A_3N/DQ56
FMC HA21_N	M7	IO_3A_42_J5_LVDS3A_3P/DQ56
FMC HA21_P	L7	IO_3A_41_M4_LVDS3A_4N/DQSN57
FMC LA05_N	H3	IO_3A_40_L4_LVDS3A_4P/DQSN57
FMC LA05_P	G3	IO_3A_39_H3_LVDS3A_5N/DQ57
FMC LA14_N	N5	IO_3A_38_G3_LVDS3A_5P/DQ57
FMC LA14_P	M5	IO_3A_37_N5_LVDS3A_6N/DQ57
FMC HA10_N	J3	IO_3A_36_M5_LVDS3A_6P/DQ57
FMC HA10_P	H3	IO_3A_35_N3_LVDS3A_7N/DQ58
FMC LA16_N	K3	IO_3A_34_H2_LVDS3A_7P/DQ58
FMC LA16_P	J3	IO_3A_33_K2_LVDS3A_8N/DQSN58
FMC LA08_N	H1	IO_3A_32_J2_LVDS3A_8P/DQ58
FMC LA08_P	G1	IO_3A_31_H1_LVDS3A_9N/DQ58
	M1	IO_3A_27_M1_LVDS3A_1N/DQ59
FMC HB01_N	L1	IO_3A_26_L1_RZ0_3A_LVDS3A_11P/DQ59
FMC HB01_P	L2	IO_3A_21_T3_LVDS3A_14N/DQSN60
FMC LA17_N	N3	IO_3A_20_U3_LVDS3A_14P/DQ56
FMC LA17_P	N4	IO_3A_17_N3_LVDS3A_16N/DQSN61
	U5	IO_3A_16_N2_LVDS3A_16P/DQ56
	U6	IO_3A_15_U5_LVDS3A_17N/DQ61
FMC LA18_N	R4	IO_3A_13_R4_LVDS3A_17P/DQ61
FMC LA18_P	T4	IO_3A_12_R4_LVDS3A_18N/DQ61
FMC LA15_N	T2	IO_3A_10_T2_LVDS3A_19N/DQ62
FMC LA15_P	T1	IO_3A_10_T1_LVDS3A_19P/DQ63
FMC LA21_N	U1	IO_3A_9_U1_LVDS3A_20N/DQSN62
FMC LA21_P	V1	IO_3A_8_V1_LVDS3A_20P/DQ56
FMC LA13_N	P2	IO_3A_7_P2_LVDS3A_21N/DQ62
FMC LA13_P	N1	IO_3A_6_N1_LVDS3A_21P/DQ62
	R2	IO_3A_5_R2_LVDS3A_22N/DQSN63
	R3	IO_3A_4_R1_LVDS3A_22P/DQ56
FMC HDMI0_CLK	M3	IO_3A_25_M3_CLK_3A_1N/LVDS3A_12N/DQ59
FMC HDMI1_LLC	P3	IO_3A_24_L3_CLK_3A_1P/LVDS3A_12P/DQ59
FMC SYNC_N	P3	IO_3A_23_P5_CLK_3A_0N/LVDS3A_13N/DQ60
FMC SYNC_P	R3	IO_3A_22_R5_CLK_3A_0P/LVDS3A_13P/DQ60
FMC LA10_N	L2	IO_3A_29_L2_PLL_3A_CLKOUTIN/LVDS3A_10N/DQSN59
FMC LA10_P	K1	IO_3A_28_K1_PLL_3A_CLKOUTP.PLL_3A_FBI/LVDS3A_10P/DQSN59
FMC LA19_N	P4	IO_3A_19_P4_PLL_3A_CLKOUTIN/LVDS3A_15N/DQ60
FMC LA19_P	P3	IO_3A_18_P3_PLL_3A_CLKOUTP.PLL_3A_CLKOUT0.PLL_3A_FBI/LVDS3A_15P/DQ60

1V2/1V5/1V8

10CX105YF672E6G

Title: Cyclone 10GX to HPC

Size: A3 Number: 07e10005 Revision: 1.0

Date: 13-May-18 Time: 16:57:04 Sheet 100f 11

File: 09_Cyclone 10 GX FMC SchDoc

General R&D
Saint-Petersburg
Russian Federation

1.8V / 3V Signals

A

A

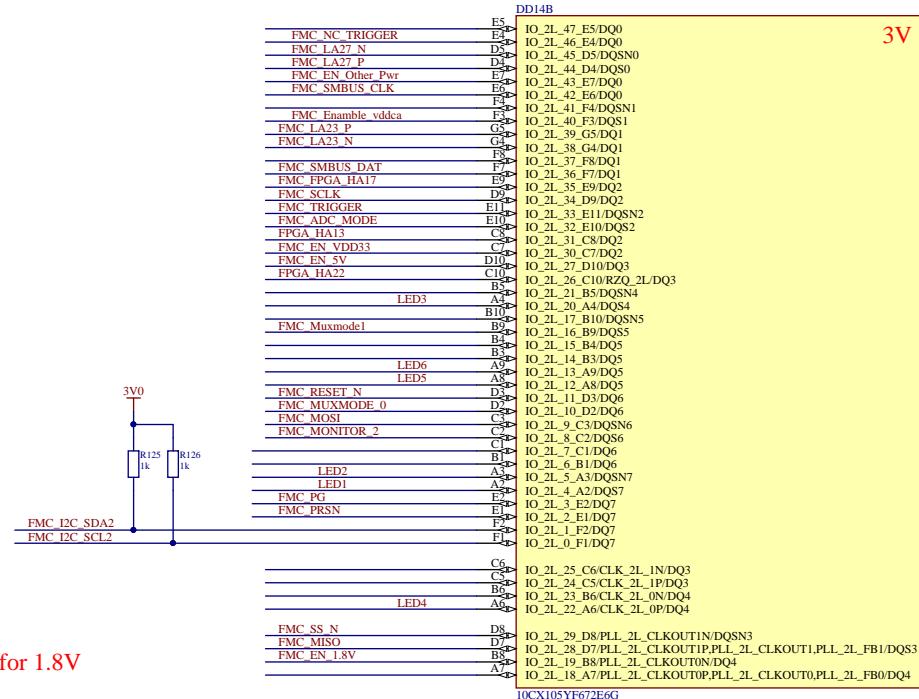
B

B

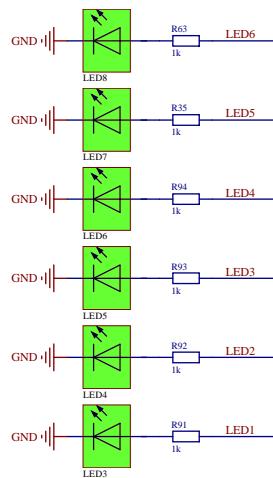
C

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Change R for 1.8V



Title: Cyclone 10GX I/O			General R&D Saint-Petersburg Russian Federation	General R&D 
Size: A3	Number: 07e10005	Revision: 1.0		
Date: 13-May-18	Time: 16:57:04	Sheet 11 of 11		
File: 10_Cyclone_10_GX_Io_LedS_SchDoc				